Open Standard Module

Hardware Specification

OPEN STANDARD MODULE ™

OSM_V1.0.docx
Dec 09, 2020

1 INTRODUCTION

1.1 Legal

1.1.1 Copyright

1.1.2 Intellectual Property

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A) Intellectual property available for licensing under reasonable and non-discriminatory terms.

- DE patent application 10 2019 115 189.9 (iesy GmbH & Co. KG)
  This patent application covers certain aspects of the Open Standard Module™ specification. iesy GmbH & Co. KG has assured SGET that it is willing to provide a non-exclusive, free license of DE patent application 10 2019 115 189.9 and all intellectual property rights evolving from this patent application to those licensees (Members and non-Members alike) desiring to implement this specification.

B) Intellectual property with undetermined licensing availability:

US patent US 9,510,461 (Samsung Electro-Mechanics Co., Ltd.), including patent family members

KR 101548799 and

CN patent CN 104241256

These patents relate to insulation of soldered joints between base boards and module boards/spacers by means of hot-melt tape, thermal bonding tape or thermosetting bonding tape The SDT believes that these patents do not directly impact the Open Standard Module™ specification which does not define such insulation. They might, however, be relevant for implementations, which seek to use additional insulation.

1.2 Disclaimers

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Compliance with this specification does not absolve manufacturers of Open Standard Module™ equipment from the requirements of safety and regulatory agencies (EN, UL, CSA, FCC, IEC, etc.).
All content and information within this document are subject to change without prior notice.

1.3 Revision History

Rev	Date	Originator	Notes
1.0	Nov 09, 2020	M. Unverdorben	Initial Release of OSM specification

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1.7 General Introduction

The idea of all Open Standard Modules™ is to create a new, future proof and versatile standard for small-size, low-cost embedded computer modules, combining the following key characteristics:

Completely machine processible during soldering, assembly and testing

Pre-tinned LGA package for direct PCB soldering without connector

Pre-defined soft- and hardware interfaces

Open-Source in soft- and hardware

The Open Standard Module™ specification allows developing, producing and distributing embedded modules for the most popular MCU32, ARM and x86 architectures. For a growing number of IoT applications this standard helps to combine the advantages of modular embedded computing with increasing requirements regarding costs, space and interfaces.

1.8 Purpose of This Document

This document defines the Module mechanical, electrical, signal and thermal parameters at a level of detail sufficient to provide a framework for OSM Module and Carrier Board designs.

1.9 Document and Standards References

- ***BT.656*** ("Recommendation ITU-R BT.656-5 Interface for digital component video signals in 525-line and 625-line television systems operating at the 4:2:2 level of Recommendation ITU-R BT.601"), International Telecommunications Union, December 2007 (**www.itu.int**)
- ***CAN*** ("Controller Area Network") Bus Standards – ISO 11898, ISO 11992, SAE J2411
- ***CSI-2*** (Camera Serial Interface version 2) The CSI-2 standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (**www.mipi.org**)
- ***CSI-3*** (Camera Serial Interface version 3) The CSI-2 standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (**www.mipi.org**)
- ***COM Express*** – the formal title for the COM Express specification is "PICMG® COM.0 COM Express Module Base Specification", Revision 2.0, August 8, 2010. This standard is owned and maintained by the PICMG ("PCI Industrial Computer Manufacturer's Group") (**www.picmg.org**)
- ***DisplayPort and Embedded DisplayPort*** These standards are owned and maintained by VESA ("Video Electronics Standards Association") (**www.vesa.org**)
- ***D-PHY CSI-2 physical layer standard*** – owned and maintained by the MIPI Alliance (**www.mipi.org**)
- ***DSI*** (Display Serial Interface) The DSI standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (**www.mipi.org**)
- ***eMMC*** ("Embedded Multi-Media Card") The eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (**www.jedec.org**)
- ***eSPI*** ("Enhanced Serial Peripheral Interface") The eSPI Interface Base Specification is defined by Intel (**https://downloadcenter.intel.com/de/download/22112**)
- ***Fieldbus*** - this term refers to a number of network protocols used for real – time industrial control. Refer to the following web sites: **www.profibus.com/downloads** and **www.canopen.org**
- ***GBE MDI*** ("Gigabit Ethernet Medium Dependent Interface") This is defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (**www.ieee.org**)
- ***I2C Specification***, Version 2.1, January 2000, Philips Semiconductor (now NXP) (**www.nxp.com**)
- ***I2S Bus Specification***, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) ()
- ***IEEE1588 - 2008***. IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems (***http://standards.ieee.org/findstds/standard/1588-2008.html***)

- ***JTAG*** ("Joint Test Action Group") This is defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (www.ieee.org)
- ***MXM3*** Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.0, Revision 1.1, © 2009 NVidia Corporation (**www.mxm-sig.org**)
- ***PICMG® EEEP*** Embedded EEPROM Specification, Rev. 1.0, August 2010 (**www.picmg.org**)
- ***PCI Express*** Specifications (**www.pci-sig.org**)
- ***Serial ATA*** Revision 3.1, July 18, 2011, Gold Revision, © Serial ATA International Organization (**www.sata-io.org**)
- ***SD Specifications*** Part 1 Physical Layer Simplified Specification, Version 3.01, ***May*** 18, 2010, © 2010 SD Group and SD Card Association ("Secure Digital") (**www.sdcard.org**)
- ***SPI Bus*** – "Serial Peripheral Interface" – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (**http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus**)
- ***USB*** Specifications (**www.usb.org**)

2 TECHNICAL SPECIFICATON

2.1 General Module Features

2.1.1 Module Size Overview

The Open Standard Module™ is made up of four different sizes that build upon each other:

- **Size-0 – "Zero"**: 30 mm x 15 mm / with **188 contacts** → shown below with red outlines
- **Size-S – "Small"**: 30 mm x 30 mm / with **332 contacts** → shown below with blue outlines
- **Size-M – "Medium"**: 30 mm x 45 mm / with **476 contacts** → shown below with orange outlines
- **Size-L – "Large"**: 45 mm x 45 mm / with **662 contacts** → shown below with green outlines

2.1.2 Module Outline Overview

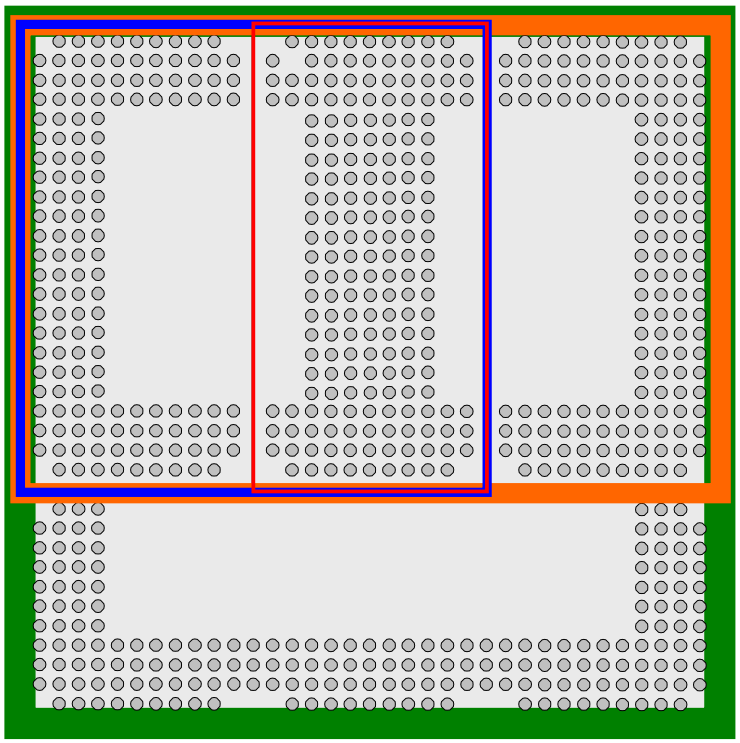


Figure 1: Overview (view from top, through the module)

2.1.3 Outline Dimensions

The Open Standard Module™ is made up of four different sizes that build upon each other:

- Size-0 – “Zero”: 30 mm x 15 mm
- Size-S – “Small”: 30 mm x 30 mm
- Size-M – “Medium”: 30 mm x 45 mm
- Size-L – “Large”: 45 mm x 45 mm

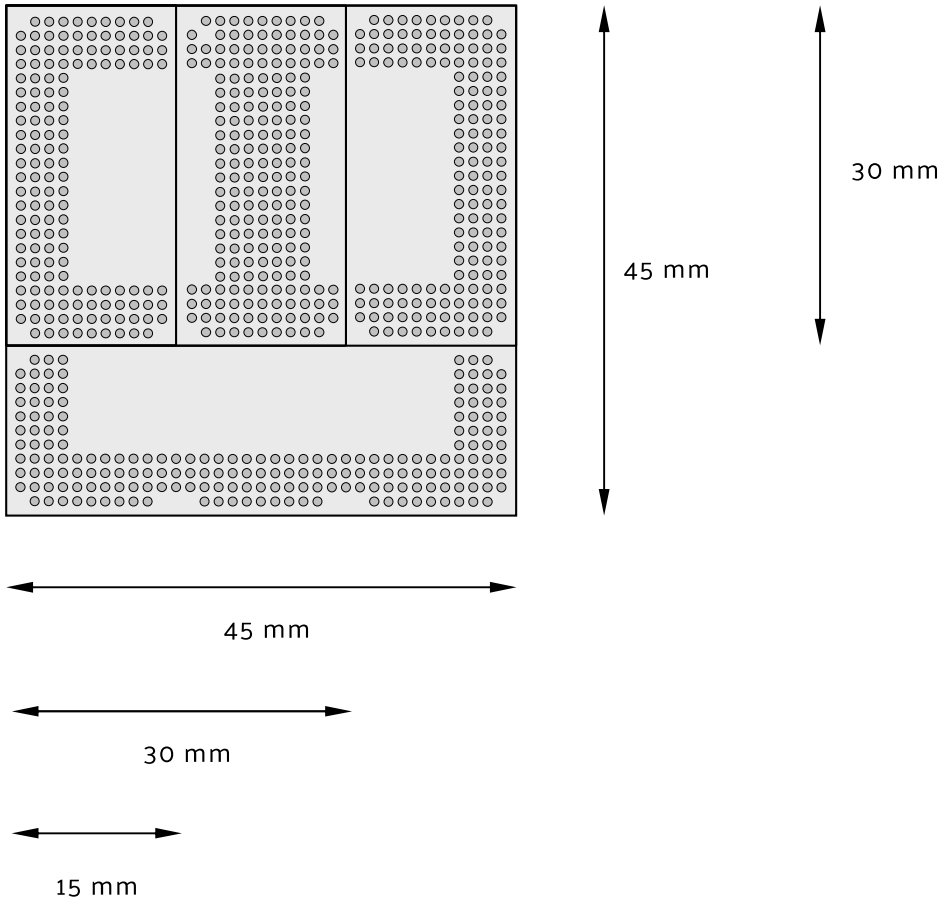


Figure 2: Sizes (view from top, through the module)

2.1.3.1 Size-0

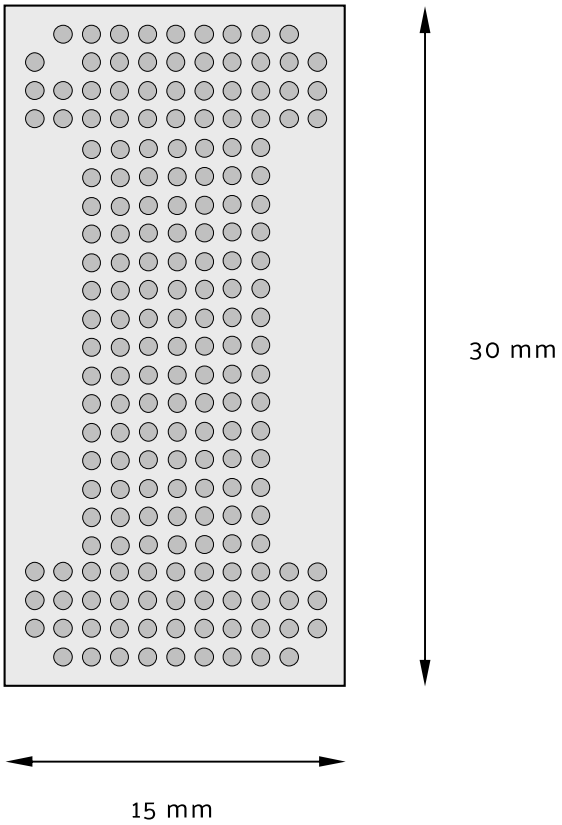


Figure 3: Size-0 Dimension and Footprint (view from top, through the module)

2.1.3.2 Size-S

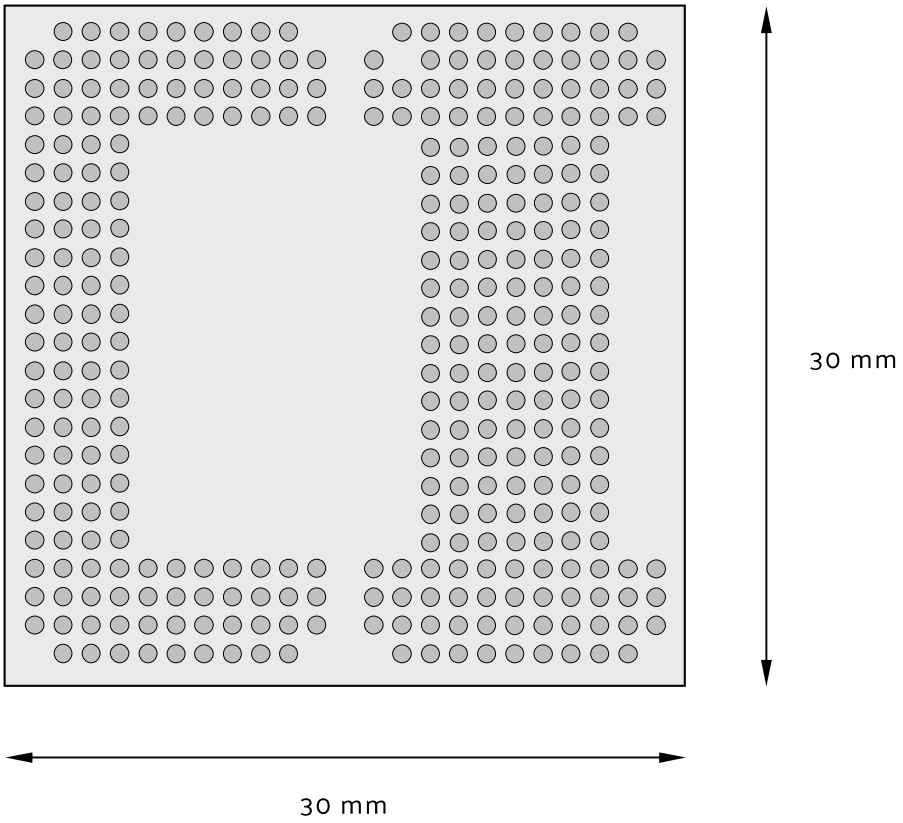


Figure 4: Size-S Dimension and Footprint (view from top, through the module)

2.1.3.3 Size-M

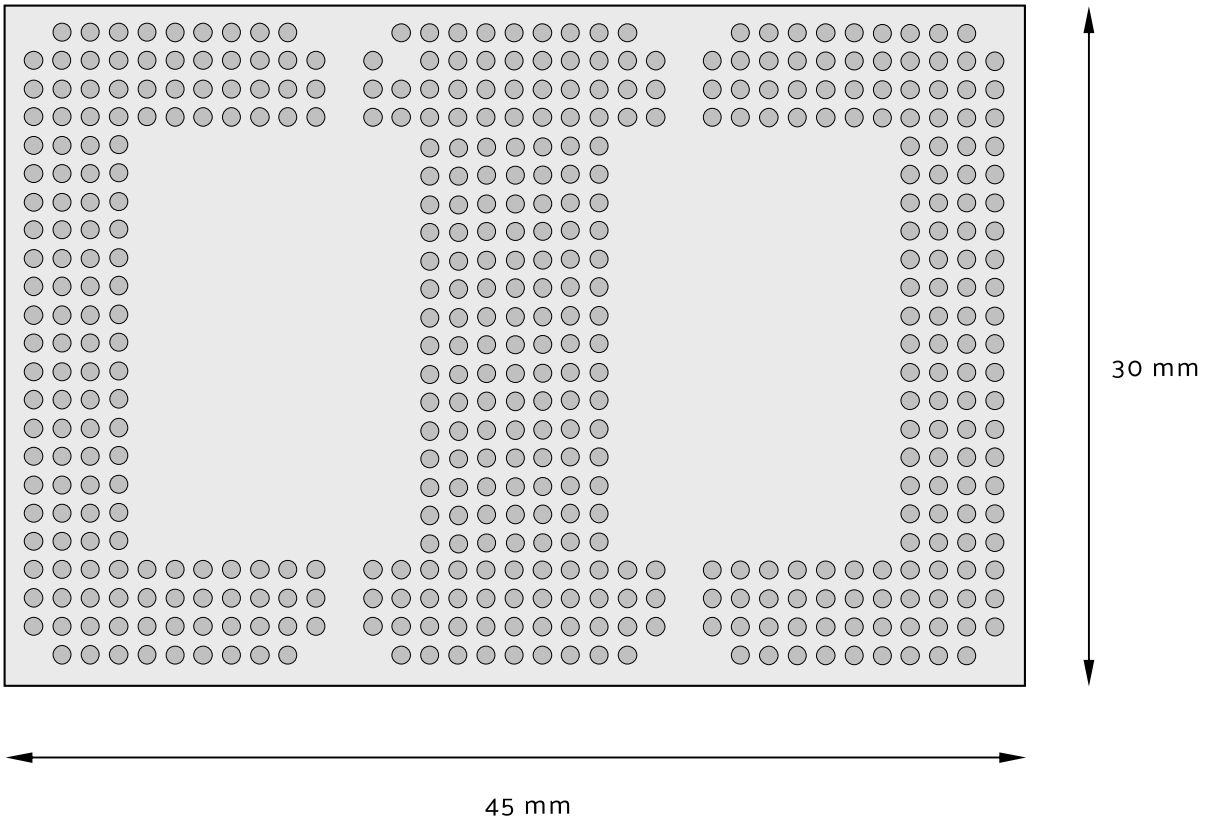


Figure 5: Size-M Dimension and Footprint (view from top, through the module)

2.1.3.4 Size-L

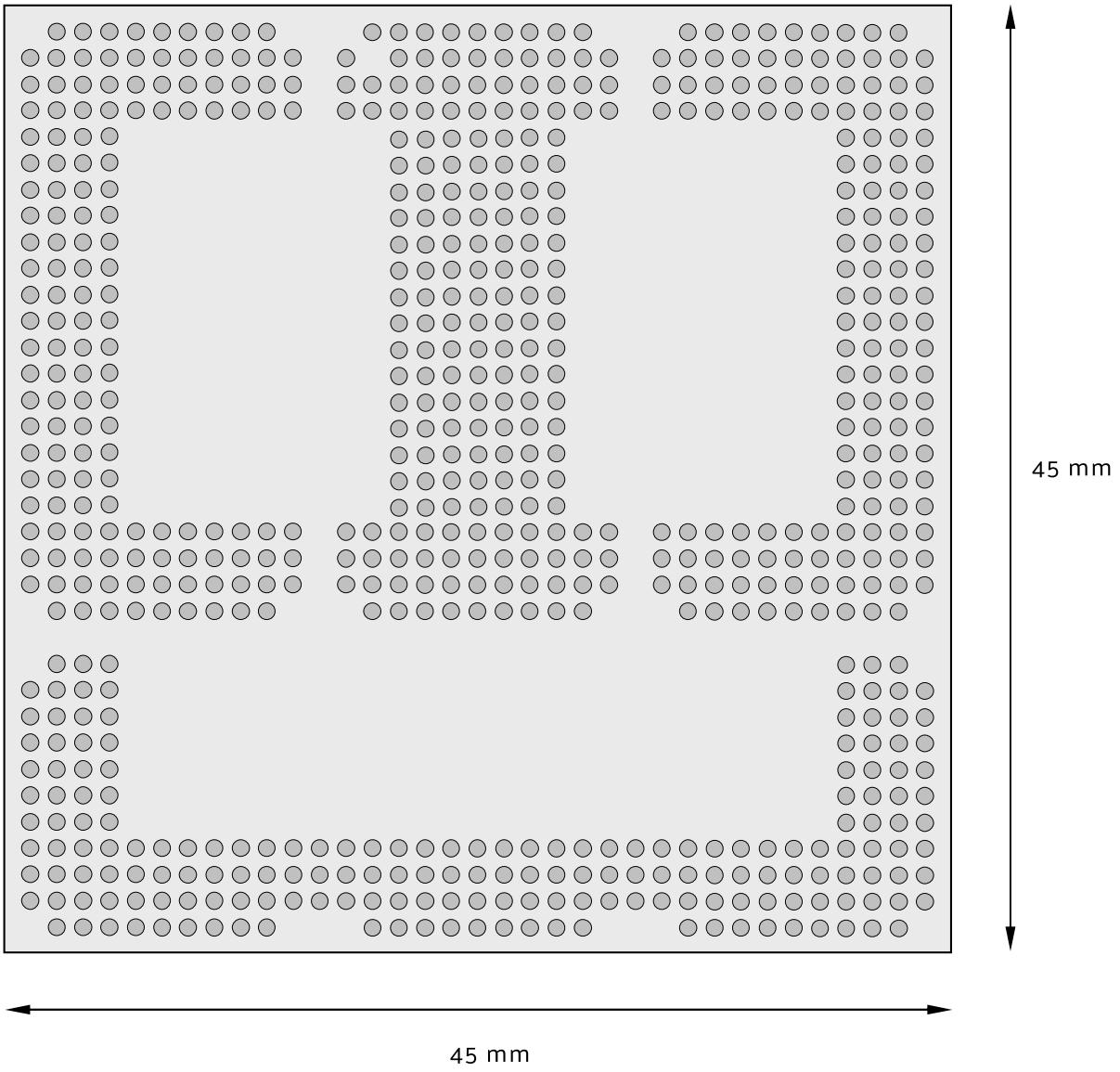


Figure 6: Size-L Dimension and Footprint (view from top, through the module)

2.1.4 Interface Overview

Feature	Sub Feature	Size-0	Size-S	Size-M	Size-L
01	Ethernet / LAN (Q)(S)(R)(G)MII	0 … 1	0 … 2	0 … 3	0 … 5
02	USB 2.0	0 … 2	1 … 3	1 … 4	1 … 4
03	USB 3.0 (w/o USB 2.0)	-	0 … 1	0 … 2	0 … 2
04	UART Console	1	1	1	1
05	UART (Rx/Tx only, 2 x with RTS/CTS)	0 … 4	0 … 4	0 … 4	0 … 4
06	- Communication Area - Wireless (Antenna Signals) - Wired (Fieldbus Signals)	0 … 1	0 … 1	0 … 1	0 … 1
07	GPIO contacts	0 … 15	0 … 23	0 … 31	0 … 39
08	SPI (1 x Quad SPI optional)	0 … 2	0 … 2	0 … 3	0 … 3
09	I2C (general purpose, besides Display, etc.)	0 … 2	0 … 2	0 … 2	0 … 2
10	I2S / PDM	0 … 1	0 … 1	0 … 1	0 … 1
11	SDIO (with 4 lane + 8 lane interface)	0 … 2	0 … 2	0 … 2	0 … 2
12	UFS	0 ... 1	0 … 1	0 … 1	0 … 1
13	CAN	0 … 2	0 … 2	0 … 2	0 … 2
14	JTAG	0 … 1	0 … 1	0 … 1	0 … 1
15	Analog Input contacts	0 … 2	0 … 2	0 … 2	0 … 2
16	PWM signals	0 … 6	0 … 6	0 … 6	0 … 6
17	Power Supply via 3.3V contacts	0 … 1	0 … 1	0 … 1	0 … 1
18	Power Supply via 5V contacts	0 … 1	5	9	17
19	Vendor Defined Contacts (up to)	3	7	13	19
20	Reserved Contacts (up to)	9	11	27	58
21	Parallel Display Interface (RGB with 18 bit)	-	0 … 1	0 … 1	0 … 1
22	Display Serial Interface (DSI with 4 channels)	-	0 … 1	0 … 1	0 … 1
23	Camera Serial Interface (CSI with 4 channels)	-	0 … 1	0 … 1	0 … 1
24	PCIe x1	-	0 … 1	0 … 2	0 … 2
25	PCIe x4 (configurable as PCIe x1 / PCIe x2)	-	-	-	0 … 2
26	Embedded DisplayPort (eDP/eDP++)	-	-	0 … 2	0 … 2
27	LVDS Display Interface	-	-	-	0 … 1

Table 2: Interface Overview for each size*

* The numbers show the total amount of each size.

2.1.5 Required and Optional Feature Table

Required and optional features for an OSM are summarized in the table below.

“Shall”	indicates a mandatory requirement
“Should”	indicates a recommended but not mandatory requirement
“May”	indicates a lesser used optional interface
“NA”	indicates an optional interface, which is not allowed to be implement
“-”	indicates an interface, that is not available in this size

Feature	Sub Feature	Size 0	Size S	Size M	Size L
Ethernet					
	Ethernet A (Q)(S)(R)(G)MII	Should	Shall	Shall	Shall
	Ethernet B (Q)(S)(R)(G)MII	-	May	May	May
	Ethernet C (Q)(S)(R)(G)MII	-	-	May	May
	Ethernet D (Q)(S)(R)(G)MII	-	-	-	May
	Ethernet E (Q)(S)(R)(G)MII	-	-	-	May
USB					
	USB A	Should	Shall	Shall	Shall
	USB A as Dual Role	Should	Should	Should	Should
	USB A as host	Should	Should	Should	Should
	USB B as host	Should	Should	Should	Should
	USB C as USB 2.0 host	-	May	May	May
	USB C as USB 3.0 host	-	May	May	May
	USB C as USB 2.0 Dual Role	-	NA	NA	NA
	USB C as USB 3.0 Dual Role	-	May	May	May
	USB D as USB 2.0 host	-	-	May	May
	USB D as USB 3.0 host	-	-	May	May
	USB D as USB 2.0 Dual Role	-	-	NA	NA
	USB D as USB 3.0 Dual Role	-	-	NA	NA
Serial Ports					
	UART Console	Shall	Shall	Shall	Shall
	UART A	Should	Should	Should	Should
	UART A Handshake Support	May	May	May	May

	UART B	May	May	May	May
	UART B Handshake Support	May	May	May	May
	UART C	May	May	May	May
	UART D	May	May	May	May
Communication Area		May	May	May	May
	Wireless Mode	May	May	May	May
	Fieldbus Mode	May	May	May	May
GPIO					
	GPIO[0:15]	Should	Should	Should	Should
	GPIO[0:15] interrupt capability	May	May	May	May
	GPIO[16:23]	-	May	May	May
	GPIO[16:23] interrupt capability	-	May	May	May
	GPIO[24:31]	-	-	May	May
	GPIO[24:31] interrupt capability	-	-	May	May
SPI					
	SPI A	Should	Should	Should	Should
	SPI B	May	May	May	May
	SPI C	-	May	May	May
I2C					
	I2C A	Should	Shall	Shall	Shall
	I2C B	May	Should	Should	Should
Audio					
	I2S A	May	May	May	May
	I2S B	May	May	May	May
RTC		Shall	Shall	Shall	Shall
JTAG		Should	Should	Should	Should
UFS		-	-	May	May
CAN					
	CAN A	May	May	May	May
	CAN B	May	May	May	May

PWM	PWM[0:5]	May	May	May	May
Power					
	VCC supply via 3.3V	Should	May	May	May
	VCC supply via 5V	May	Shall	Shall	Shall
	Flexible IO voltage (controlled by module)	May	NA	NA	NA
Display Interfaces					
	Parallel Display Interface (RGB with 18 bit)	-	May	May	May
	Display Serial Interface (DSI with 4 channels)	-	May	May	May
	Embedded DisplayPort (eDP)	-	-	May	May
	LVDS Display Interface	-	-	-	May
Camera Interface					
	CSI – 2 lane support	-	May	May	May
	CSI – 4 lane support	-	May	May	May
PCIe					
	PCIe A	-	May	May	May
	PCIe B	-	-	May	May
	PCIe C 4 x x1 lanes	-	-	-	May
	PCIe C 2 x x2 lanes	-	-	-	May
	PCIe C 1 x x4 lanes	-	-	-	May
	PCIe D 4 x x1 lanes	-	-	-	May
	PCIe D 2 x x2 lanes	-	-	-	May
	PCIe D 1 x x4 lanes	-	-	-	May

Table 3: Required and Optional Features

2.1.6 Footprint Grid

The Contact Grid for the Open Standard Module™ Specification is symmetrically and defines the following dimensions:

- Contact Diameter: 0.8 mm
- Contact Grid: 1.25 mm
- Contact-to-Contact: 0.45 mm
- Contact-to-Edge: 0.85 mm

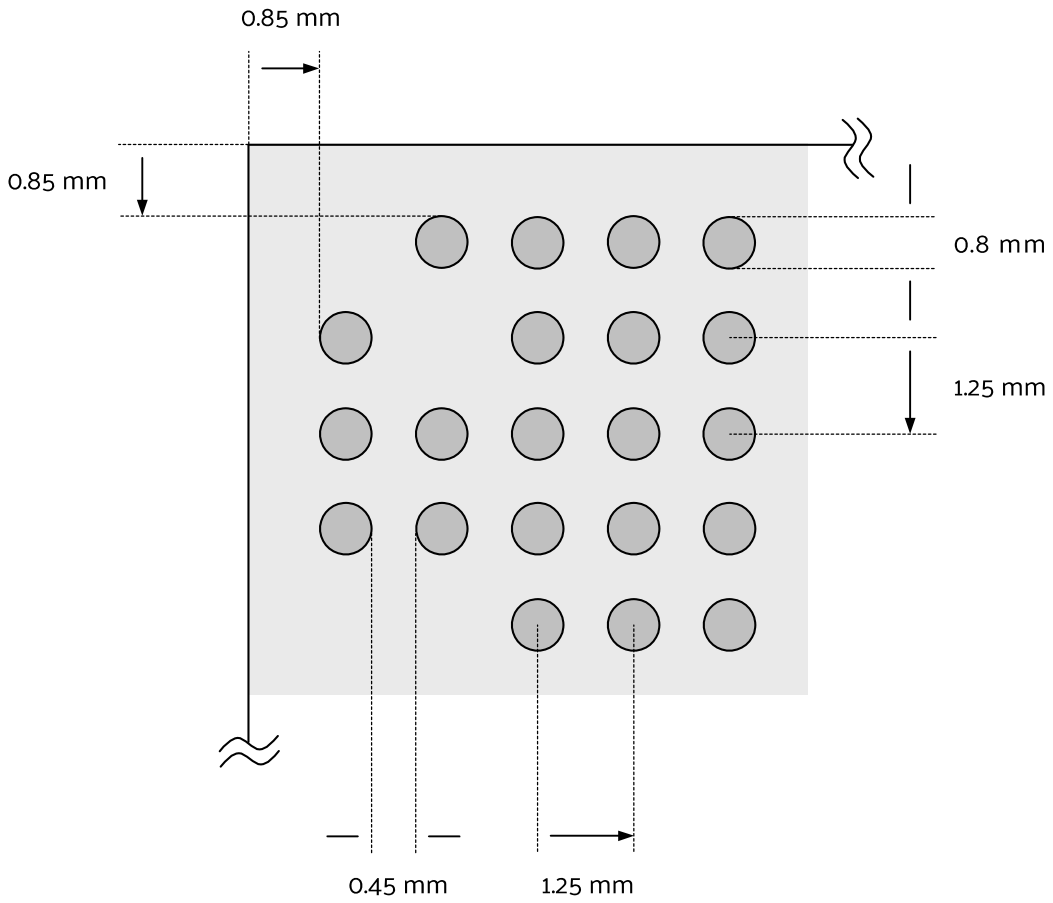


Figure 7: Footprint Grid Dimensions, Size-S upper left corner (view from top, through the module)

2.1.7 Contacts Characteristics

All Open Standard Modules™ use a symmetric LGA package for connecting the module PCB to the baseboard PCB. The manufacturer may decide and specify the use of one the following, recommended contact technologies:

- **Fused Tin Grid Array (FTGA)**: see Figure 8: Fused Tin Grid Array bottom view below
- **ENIG LGA**: see Figure 9: ENIG LGA package (bottom side) below
- **BGA**: see Figure 10: BGA package (bottom side) below

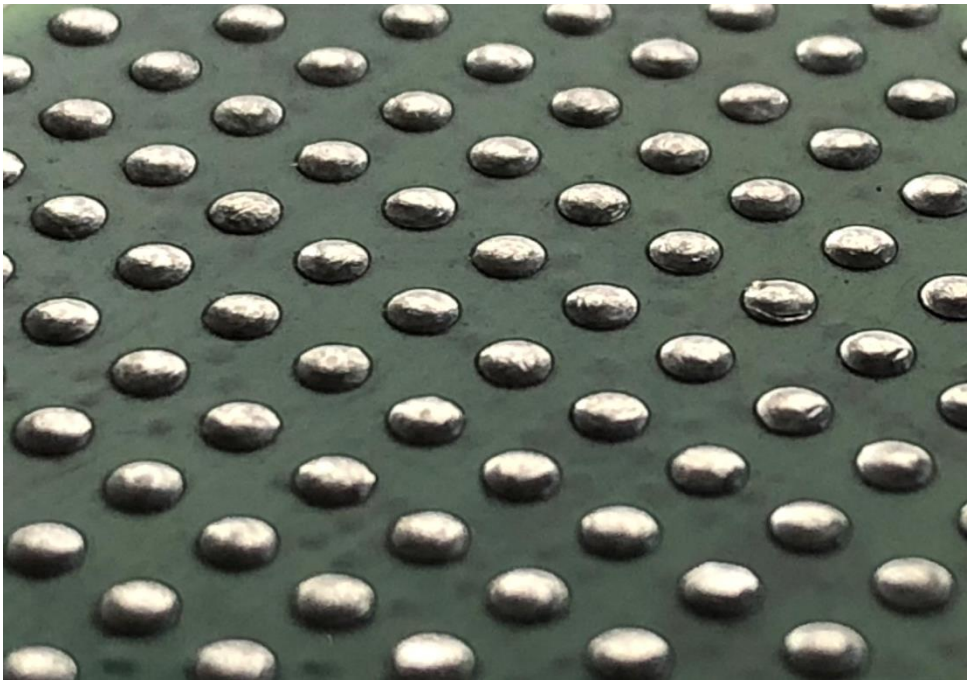


Figure 8: Fused Tin Grid Array bottom view

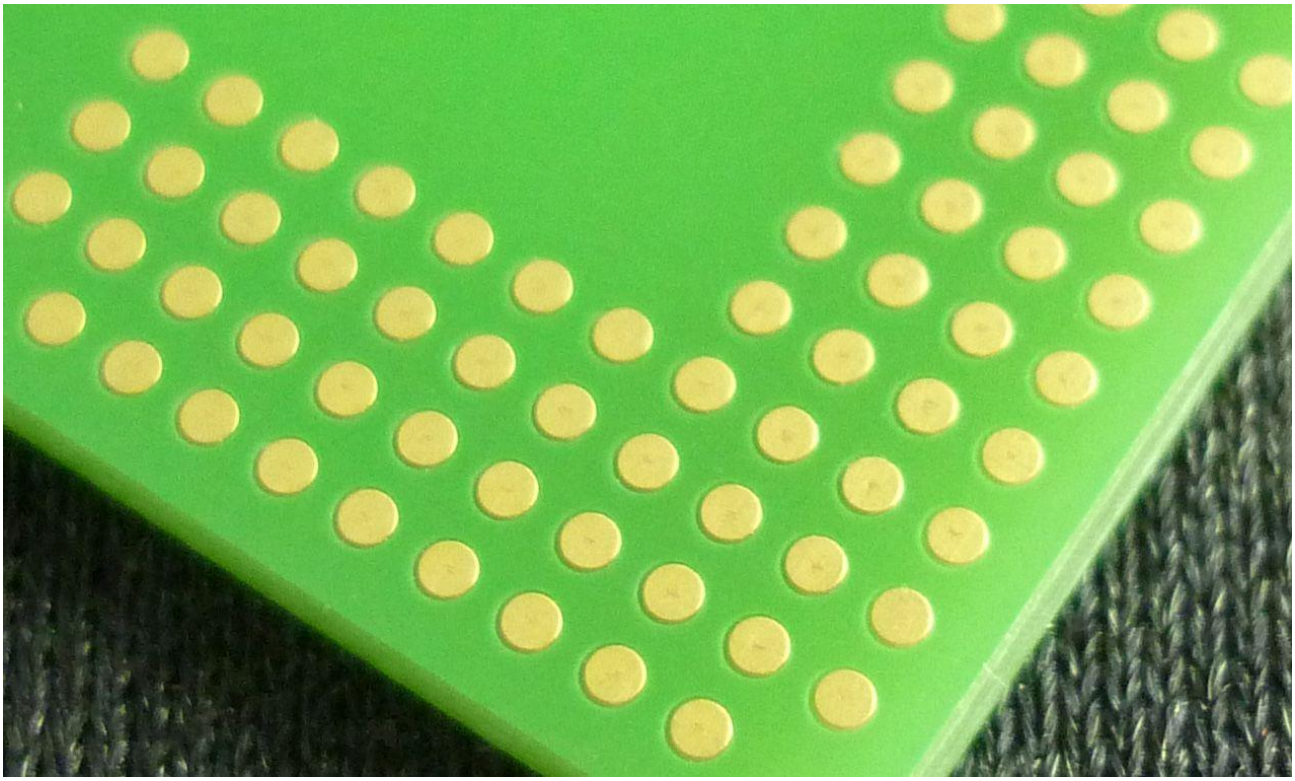


Figure 9: ENIG LGA package (bottom side)

Figure 10: BGA package (bottom side)

2.2 Module Height Specification

The Open Standard Module™ Specification allows different heights to adopt the module to different technical requirements:

- **Standard Height F – "Flat:"** The Module PCB height is NOT extended via a "PCB Spacer" and has to be soldered directly on the Open Standard Module™ Carrier Board
- **Extended Height E – "Extended":** The Module PCB height is extended via a "PCB Spacer". The "PCB Spacer" extends the total height of the Open Standard Module™ and is pre-soldered on the bottom side of the Open Standard Module™.

2.2.1 Standard Height F

Standard Height Open Standard Modules™ will be directly soldered on the PCB base board.

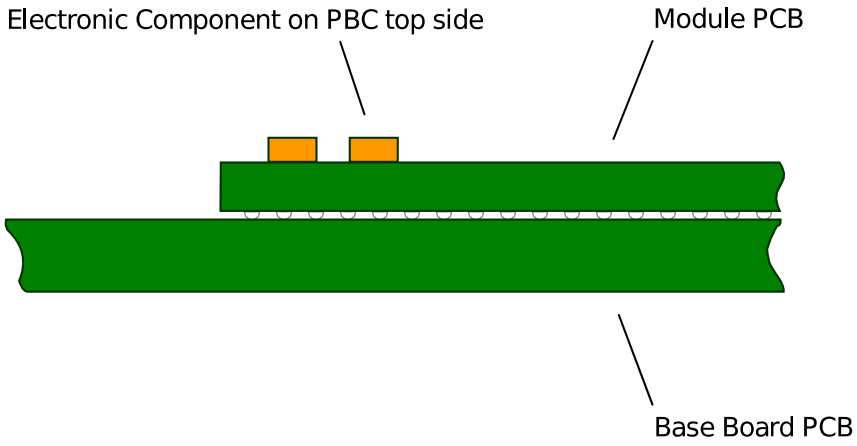


Figure 11: Sectional view on Standard Height F ("Flat" module)

2.2.2 Extended Height E

Extended Height Open Standard Modules™ have an increased module height from additional “Spacer PCB Layers” between module and base board PCB. The “Spacer PCB Layers” need to be pressed or grouted directly on the bottom of the module PCB - most likely before the electronic components have been populated or assembled. The “Spacer PCB Layer” might help to facilitate the placement of components on the bottom of the Open Standard Module™

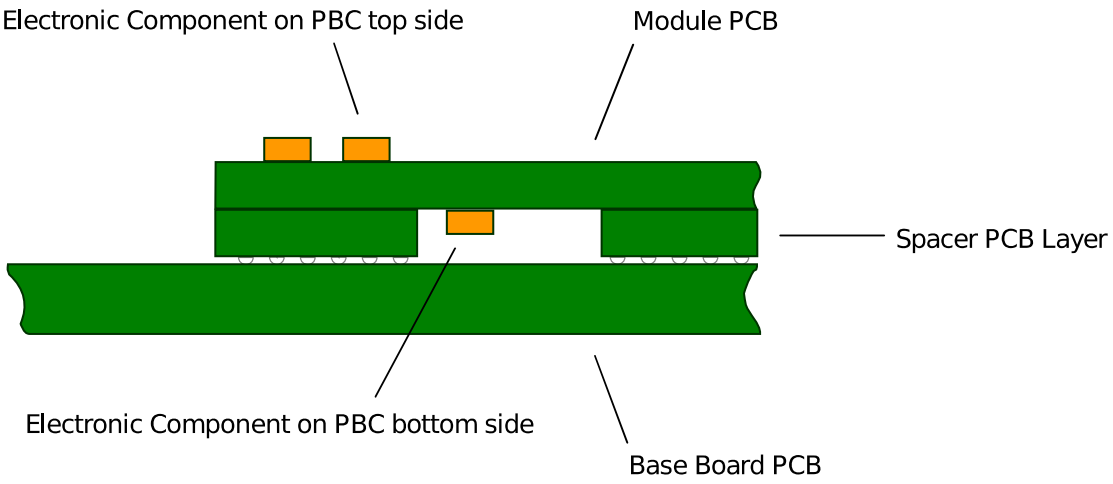


Figure 12: Sectional view on Standard Height E ("Extended" module)

2.2.2.1 Schematic Illustration

The following illustration shows the structure and assembly of an exemplary Open Standard Module™ with Spacer PCB and Size “Small” and Height “Extended”.

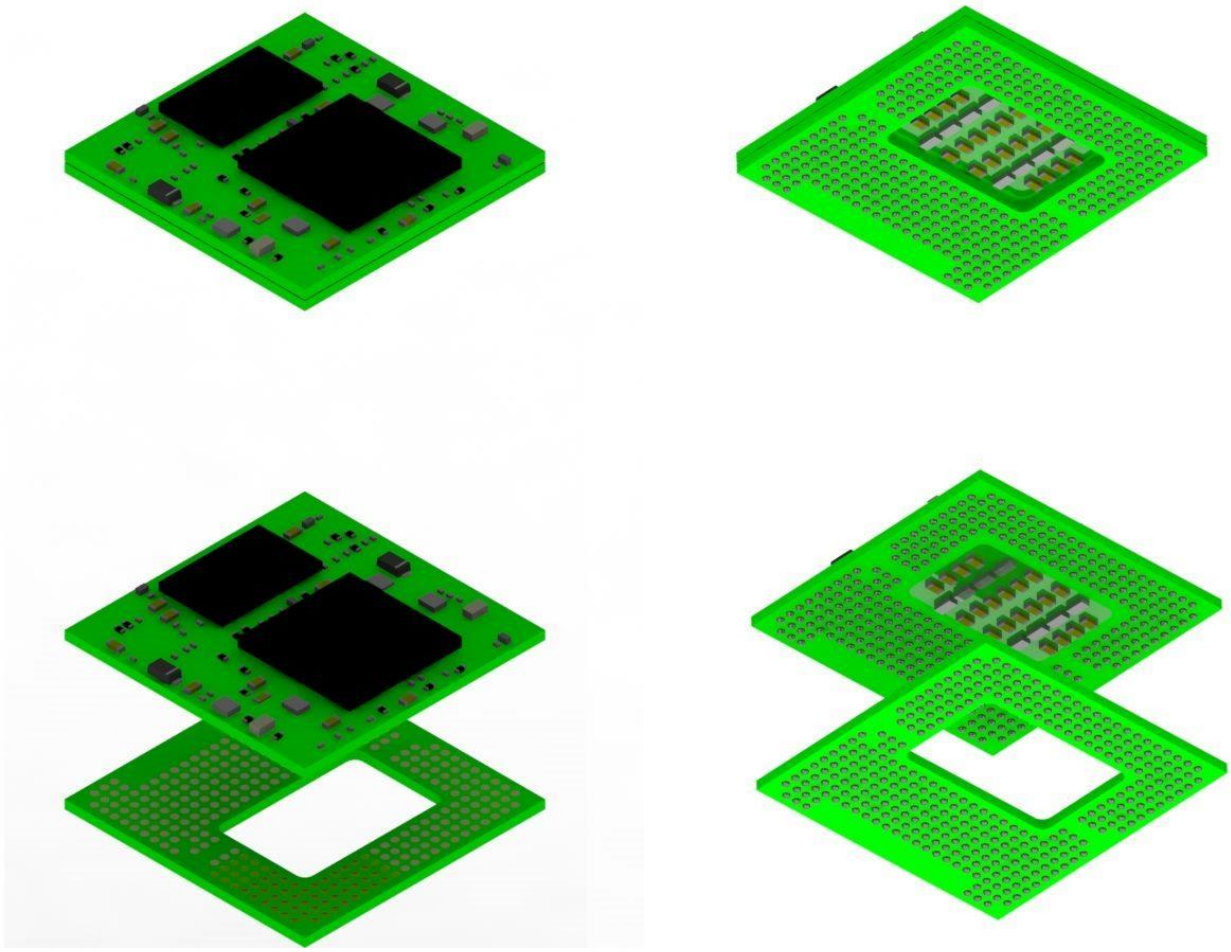


Figure 13: Schematic illustration of the Spacer PCB for Extended Height E (Size-S)

2.2.2.2 Possible Cut-out and Placement Areas (bottom side)

All modules adhering to the Open Standard Module™ Specification are meant to be soldering modules. Therefore, the definition of placement areas on bottom side of the module is necessary to allow placement of electronic components on the opposite of some main components like CPU,
RAM, etc. Predefined placement areas will need to be taken into account for baseboard designs for recesses or cut-out areas. Otherwise, the module PCB itself could be increased with a Spacer PCB layer considering the placement areas on module bottom side.

- Optional Placement Area #1: 10.25 mm width x 16.5 mm height
- Optional Placement Area #2: 10.25 mm width x 16.5 mm height
- Optional Placement Area #3: 31.5 mm width x 7.75 mm height

Additionally, to the placement area, also the area for the cut-out either on the spacer PCB or the carrier board needs to be defined.

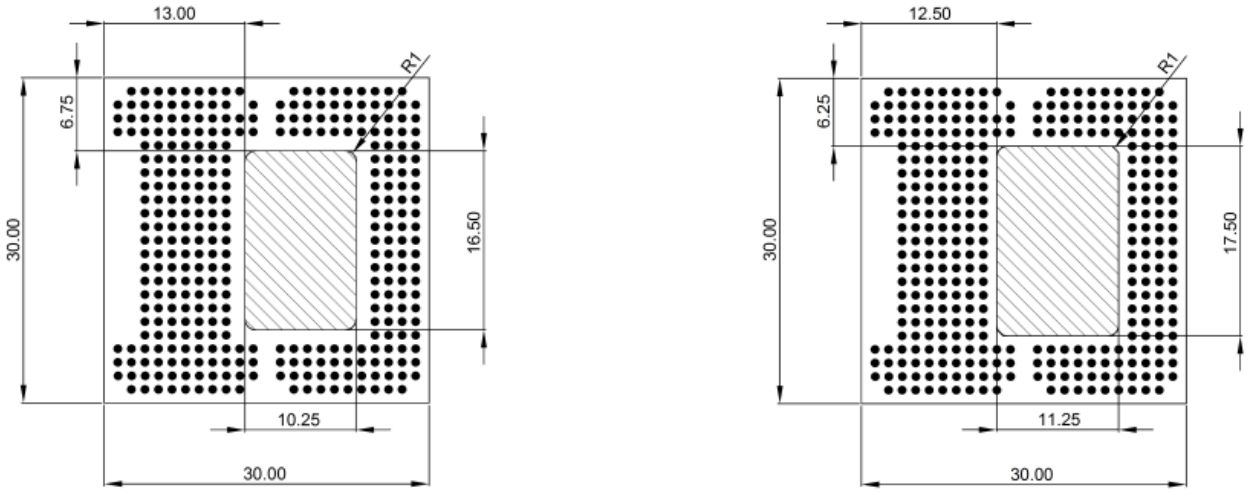


Figure 14: Placement Area (left) and Cut-Out Area (right) - Size S (view from bottom)

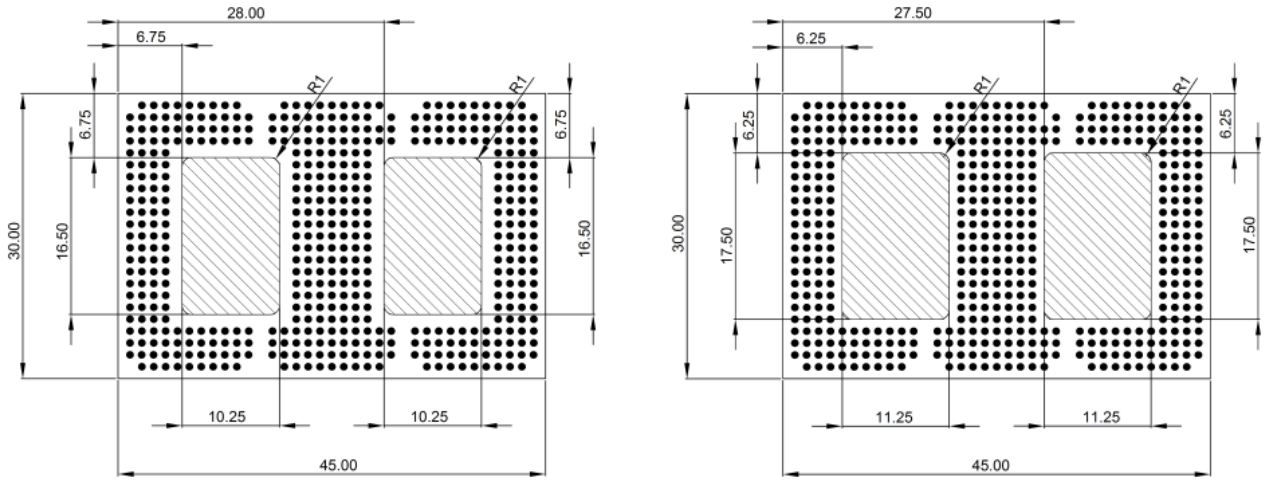


Figure 15: Placement Area (left) and Cut-Out Area (right) - Size M (view from bottom)

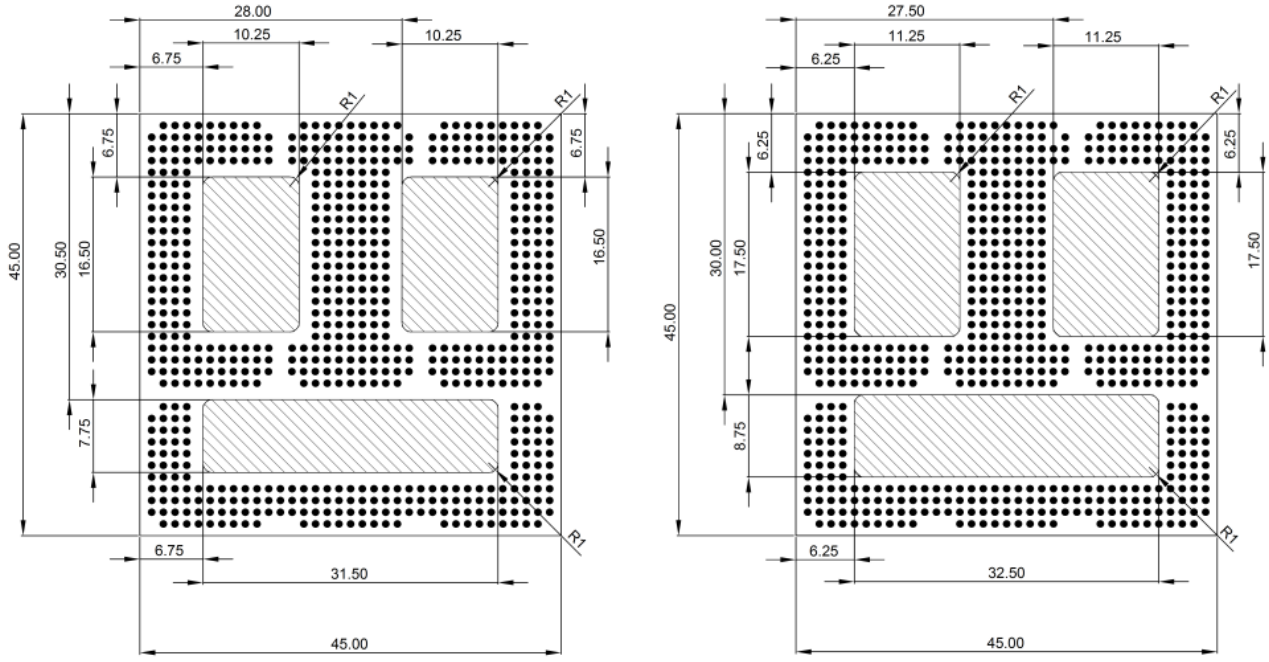


Figure 16: Placement Area (left) and Cut-Out Area (right) - Size L (view from bottom)

2.2.3 RF Antenna Connector Area

All modules adhering to the Open Standard Module™ Specification **may** provide one specific areas for potential RF antenna connectors. This area might be used for other electrical components as well, no matter if RF antenna connectors are provided or not.

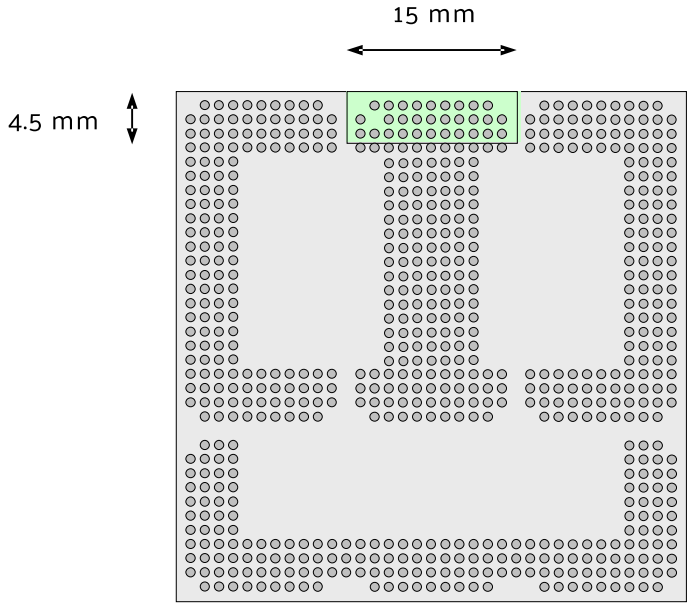


Figure 17: RF Antenna Connector Area (all sizes) (view from top, through the module)

2.2.4 Standard Metal Shielding

All modules adhering to the Open Standard Module™ Specification **may** be able to carry a standardized RF Metal Shielding. This shielding helps to improve the EMC characteristics and reduce EMC emissions.

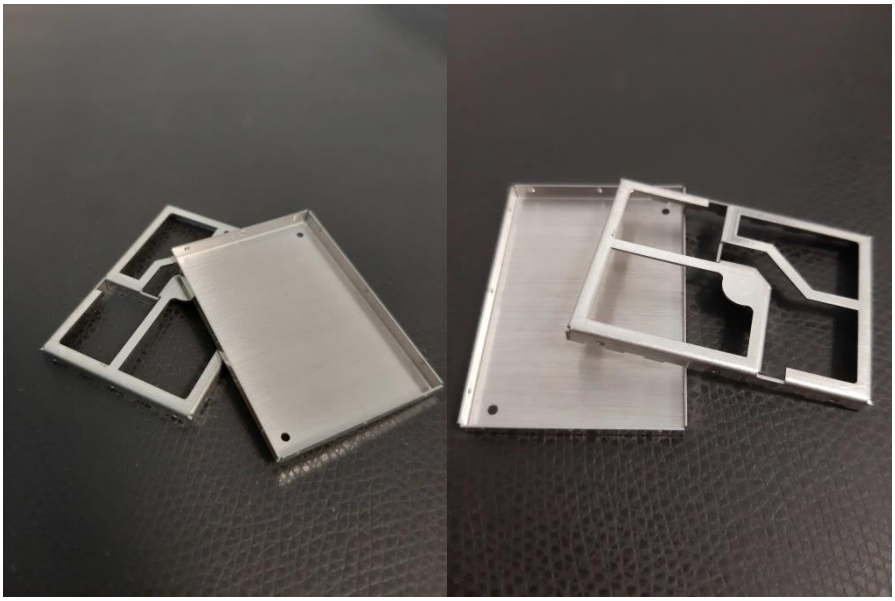


Figure 18: PCB RF Metal shielding (example)

2.2.5 Breakout Area and Tolerances

All modules adhering to the Open Standard Module™ Specification **may** have predefined panel breakout areas. Within these breakout areas the outline and texture of the module PCB might vary.
The definition of breakout areas might facilitate the production of the modules as well as testing equipment and shall reduce potential mechanical intolerances and conflicts on the baseboard.
Therefore, the red areas (below) border the maximum tolerances to be considered during production and assembly. The usage of those breakout areas is not a mandatory requirement.

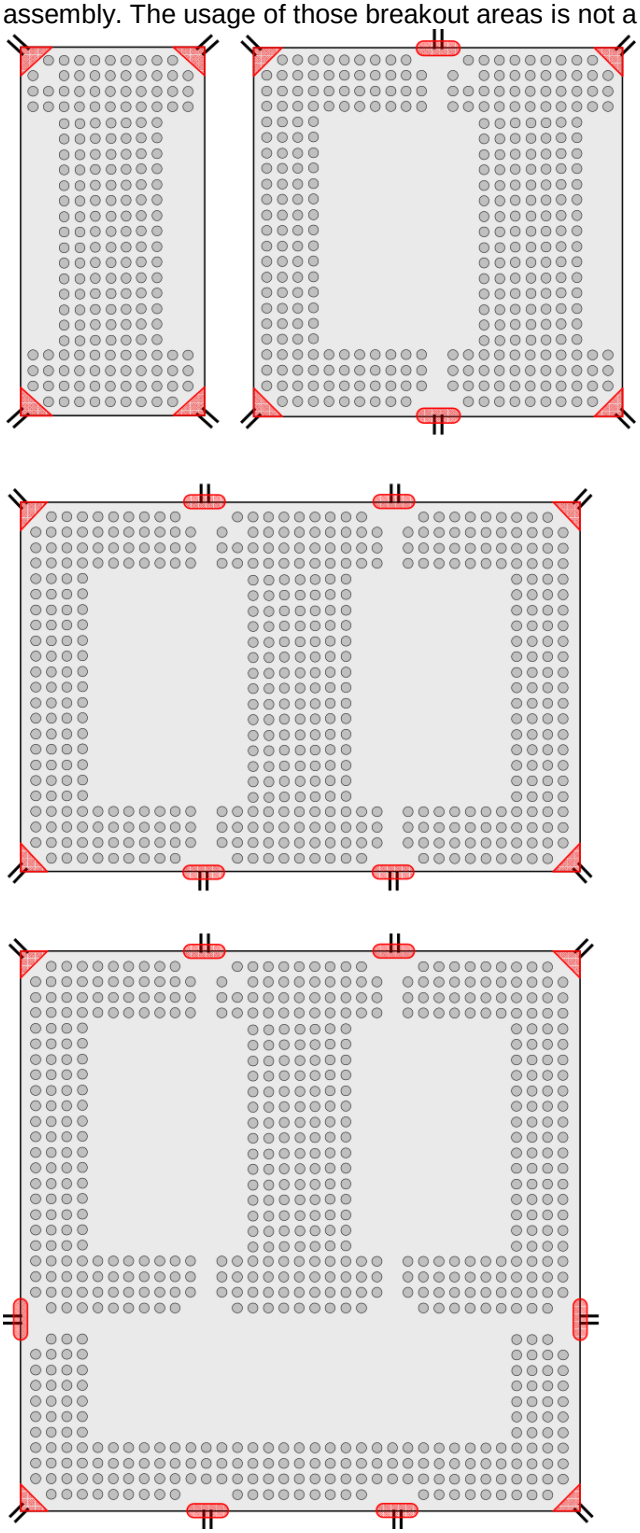


Figure 19: Breakout Areas (all sizes) (view from top, through the module)

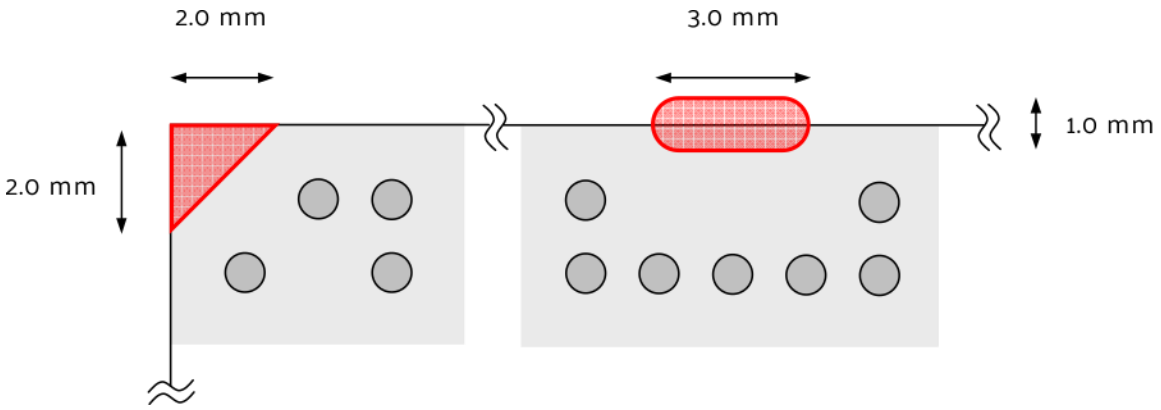


Figure 20: Tolerances Breakout Areas (all sizes)

2.3 Electrical Interfaces

2.3.1 Contact Grid

Modules adhering to the Open Standard Module™ Specification **shall** use the following contact grid and the regarding designation:

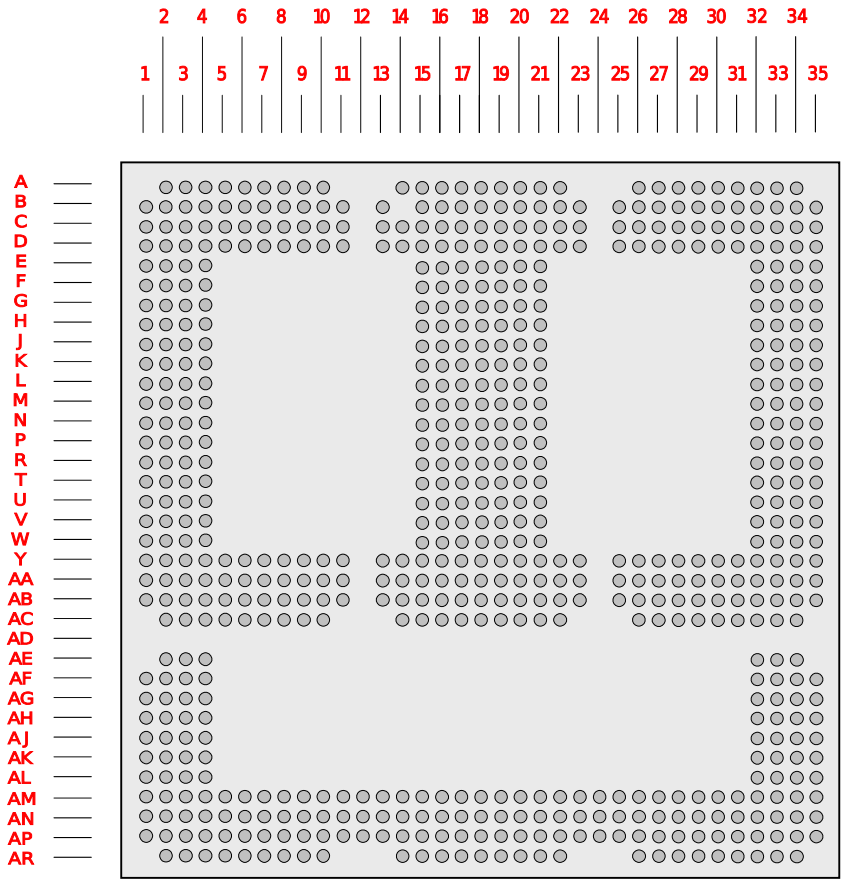


Figure 21: Contact Grid (all sizes) (view from top, through the module)

2.3.2 Contact Overview

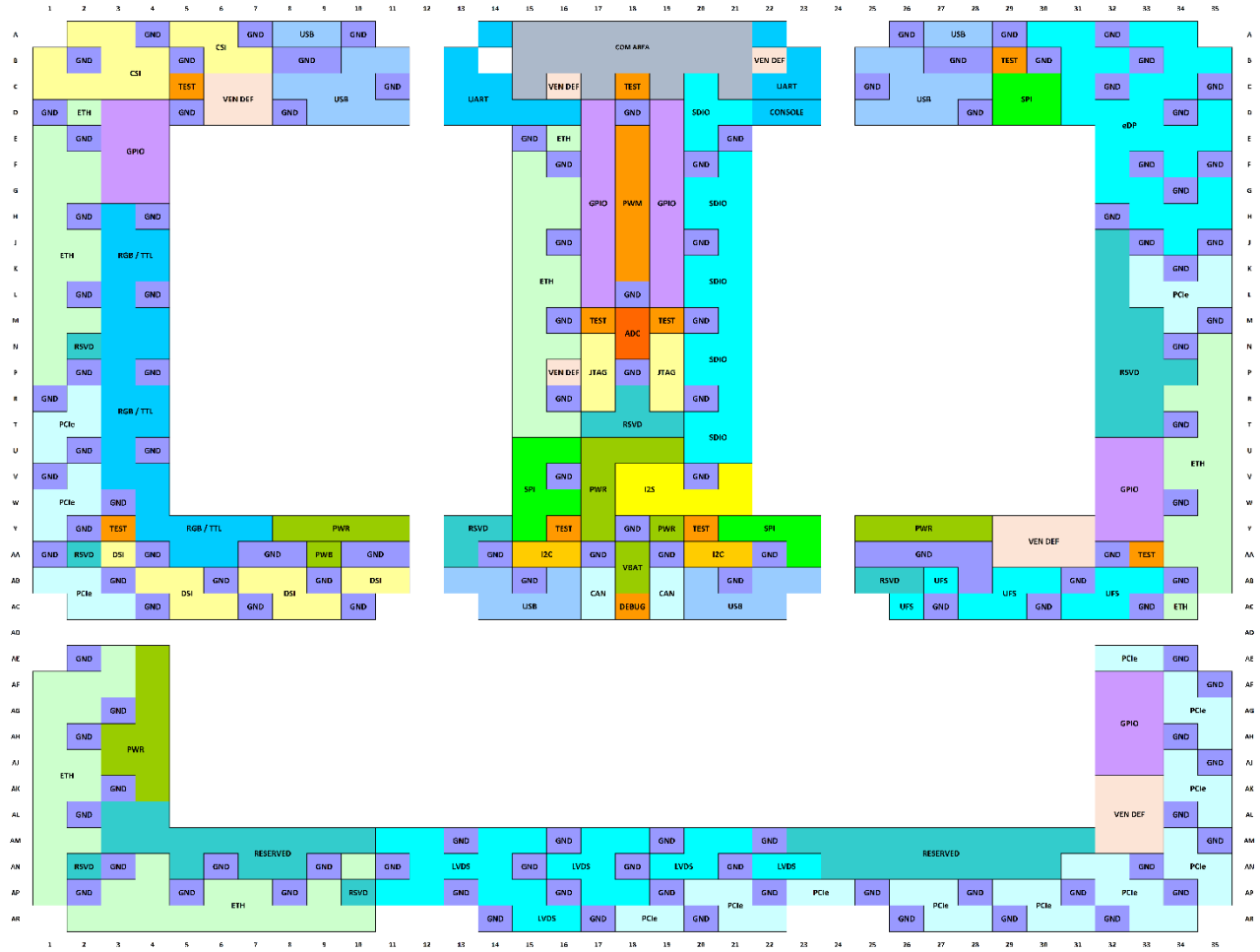


Figure 22: Contact Overview (all sizes)

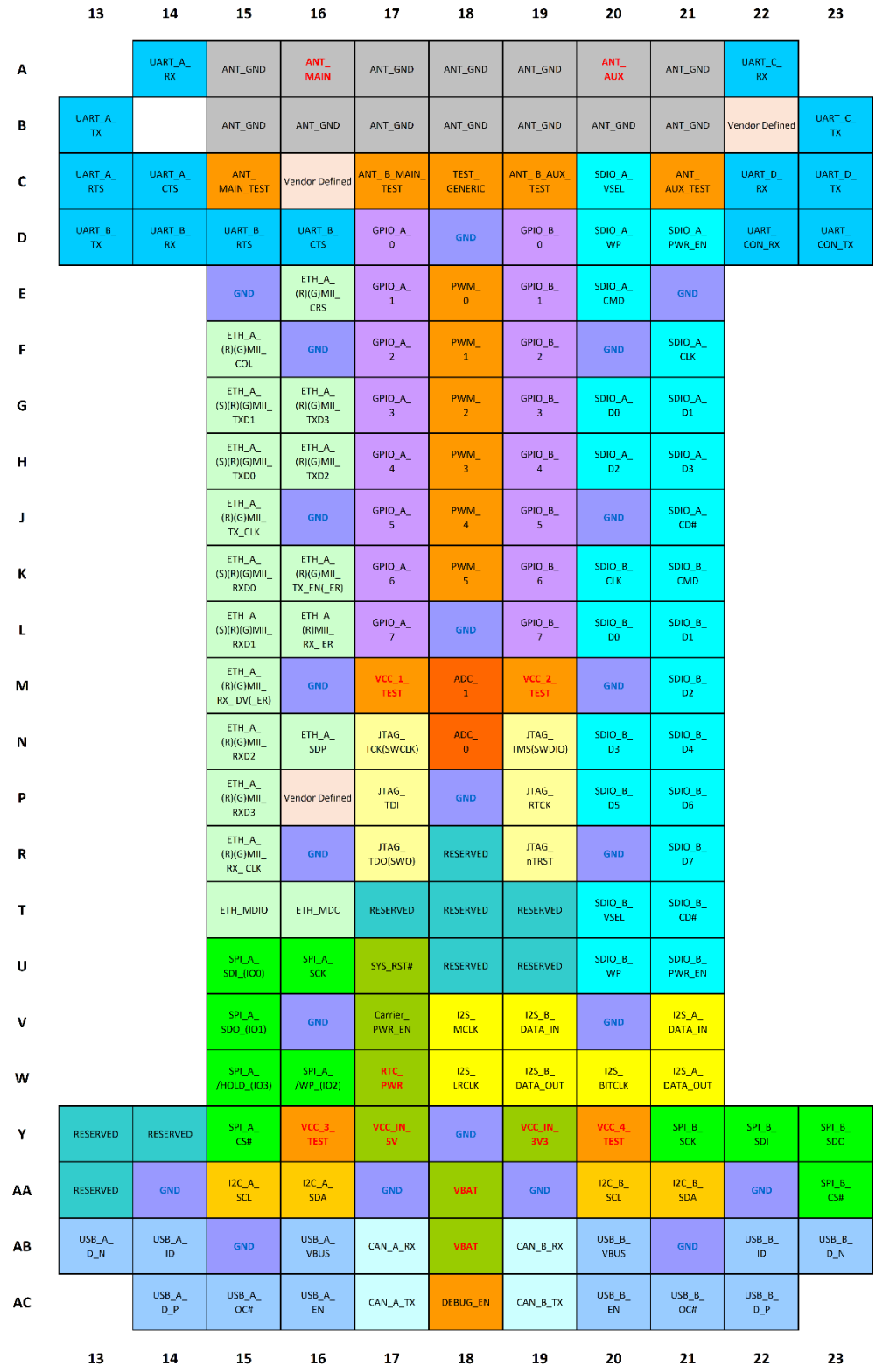
2.3.3 Size-0 – Basic Functions

2.3.3.1 Size-0 – Function Table

Functionality	Description	Quantity of Interfaces	No. of Contacts	Mandatory Interface	Color Code
Ethernet / LAN	(Q)(S)(R)(G)MII, 100/1000 Mbit	0 … 1	18	No	
USB	USB 2.0	0 … 2	12	No	
UART Console	Rx, Tx only	1 … 2	2	Yes	
UART	Rx, Tx, 2xRTS, 2xCTS	0 … 4	12	No	
Power Supply	5 / 3.3 V-DC, Battery, System Reset, Control signals	1	8	Yes	
Ground	Main Power GND	1	22	Yes	
JTAG		1	6	Yes	
GPIO	General Purpose Input Output	0 … 16	16	No	
Testing	VCC_Test_0 … 3, SWIM, etc.	0 … 6	6	No	
Vendor Defined	Defined by module manufacturer	0 … 3	3	No	
Reserved	TBD / for future use	0 … 8	8	No	
Communication Area	Either in Wireless Mode or in Fieldbus Mode	0 … 1	18	No	
SPI	Host or Slave, 1 x Quad SPI optional	0 … 2	10	No	
I2C		0 … 2	4	No	
I2S / PDM	one channel	0 … 2	7	No	
SDIO	4 Lanes + 8 Lanes	0 … 2	24	No	
CAN		0 … 2	4	No	
Analog Input		0 … 2	2	No	
PWM	PWM_0 …5	0 … 6	6	No	
Amount of Contacts			188		

Table 4: Size-0 – Function Table

2.3.3.2 Size-0 – Detailed Contact Overview



	13	14	15	16	17	18	19	20	21	22	23
A		UART_A_RX	ANT_GND	ANT_MAIN	ANT_GND	ANT_GND	ANT_GND	ANT_AUX	ANT_GND	UART_C_RX	
B	UART_A_TX		ANT_GND	ANT_GND	ANT_GND	ANT_GND	ANT_GND	ANT_GND	ANT_GND	Vendor Defined	UART_C_TX
C	UART_A_RTS	UART_A_CTS	ANT_MAIN_TEST	Vendor Defined	ANT_B_MAIN_TEST	TEST_GENERIC	ANT_B_AUX_TEST	SDIO_A_VSEL	ANT_AUX_TEST	UART_D_RX	UART_D_TX
D	UART_B_TX	UART_B_RX	UART_B_RTS	UART_B_CTS	GPIO_A_0	GND	GPIO_B_0	SDIO_A_WP	SDIO_A_PWR_EN	UART_CON_RX	UART_CON_TX
E			GND	ETH_A_(R)(G)MII_CRS	GPIO_A_1	PWM_0	GPIO_B_1	SDIO_A_CMD	GND		
F			ETH_A_(R)(G)MII_COL	GND	GPIO_A_2	PWM_1	GPIO_B_2	GND	SDIO_A_CLK		
G			ETH_A_(S)(R)(G)MII_TXD1	ETH_A_(R)(G)MII_TXD3	GPIO_A_3	PWM_2	GPIO_B_3	SDIO_A_D0	SDIO_A_D1		
H			ETH_A_(S)(R)(G)MII_TXD0	ETH_A_(R)(G)MII_TXD2	GPIO_A_4	PWM_3	GPIO_B_4	SDIO_A_D2	SDIO_A_D3		
J			ETH_A_(R)(G)MII_TX_CLK	GND	GPIO_A_5	PWM_4	GPIO_B_5	GND	SDIO_A_CD#		
K			ETH_A_(S)(R)(G)MII_RXD0	ETH_A_(R)(G)MII_TX_EN(_ER)	GPIO_A_6	PWM_5	GPIO_B_6	SDIO_B_CLK	SDIO_B_CMD		
L			ETH_A_(S)(R)(G)MII_RXD1	ETH_A_(R)MII_RX_ER	GPIO_A_7	GND	GPIO_B_7	SDIO_B_D0	SDIO_B_D1		
M			ETH_A_(R)(G)MII_RX_DV(_ER)	GND	VCC_1_TEST	ADC_1	VCC_2_TEST	GND	SDIO_B_D2		
N			ETH_A_(R)(G)MII_RXD2	ETH_A_SDP	JTAG_TCK(SWCLK)	ADC_0	JTAG_TMS(SWDIO)	SDIO_B_D3	SDIO_B_D4		
P			ETH_A_(R)(G)MII_RXD3	Vendor Defined	JTAG_TDI	GND	JTAG_RTCK	SDIO_B_D5	SDIO_B_D6		
R			ETH_A_(R)(G)MII_RX_CLK	GND	JTAG_TDO(SWO)	RESERVED	JTAG_nTRST	GND	SDIO_B_D7		
T			ETH_MDIO	ETH_MDC	RESERVED	RESERVED	RESERVED	SDIO_B_VSEL	SDIO_B_CD#		
U			SPI_A_SDI_(IO0)	SPI_A_SCK	SYS_RST#	RESERVED	RESERVED	SDIO_B_WP	SDIO_B_PWR_EN		
V			SPI_A_SDO_(IO1)	GND	Carrier_PWR_EN	I2S_MCLK	I2S_B_DATA_IN	GND	I2S_A_DATA_IN		
W			SPI_A_/HOLD_(IO3)	SPI_A_/WP_(IO2)	RTC_PWR	I2S_LRCLK	I2S_B_DATA_OUT	I2S_BITCLK	I2S_A_DATA_OUT		
Y	RESERVED	RESERVED	SPI_A_CS#	VCC_3_TEST	VCC_IN_5V	GND	VCC_IN_3V3	VCC_4_TEST	SPI_B_SCK	SPI_B_SDI	SPI_B_SDO
AA	RESERVED	GND	I2C_A_SCL	I2C_A_SDA	GND	VBAT	GND	I2C_B_SCL	I2C_B_SDA	GND	SPI_B_CS#
AB	USB_A_D_N	USB_A_ID	GND	USB_A_VBUS	CAN_A_RX	VBAT	CAN_B_RX	USB_B_VBUS	GND	USB_B_ID	USB_B_D_N
AC		USB_A_D_P	USB_A_OC#	USB_A_EN	CAN_A_TX	DEBUG_EN	CAN_B_TX	USB_B_EN	USB_B_OC#	USB_B_D_P	

Figure 23: Size-0 - detailed contact overview

2.3.4 Size-S – ADDITIONAL Functions

2.3.4.1 Size-S – Function Table

Size-S's functionality on column 13 to 23 is identical to Size-0. There is only one change in the necessity of USB interfaces according to following table:

Functionality	Description	Quantity of Interfaces	No. of Contacts	Mandatory Interface
USB	USB 2.0	1 … 2	12	**1x Yes**
I2C	I2C	1 … 2	4	**1x Yes**

Table 5: Size-S Changes to Size-0

The following table describes the additional functions on column 1 to 11.

Functionality	Description	Quantity of additional Interfaces	No. of additional Contacts	Mandatory Interface	Color code
Power Supply	5 V-DC, Power Button	1	5	Yes	
Ground	Main Power GND	1	36	Yes	
GPIO	General Purpose Input Output	0 … 8	8	No	
Reserved	TBD / for future use	0 … 2	2	No	
Vendor Defined	Defined by module manufacturer	0 … 4	4	No	
Ethernet / LAN	(Q)(S)(R)(G)MII, 100/1000 Mbit	0 … 1	16	No	
USB	USB 2.0 with 3.0 option, with Dual Role option	0 … 1	10	No	
MIPI Interfaces	DSI, CSI	0 … 3	24	No	
RGB	Parallel Display	0 … 1	25	No	
Testing	VCC_Test_5 … 6	0 … 2	2	No	
PCIe x1	With WAKE and SMBus signal	0 … 1	12	No	
Amount of Contacts			144		

Table 6: Size-S Additional Functionality / Interfaces

2.3.4.2 Size-S – Detailed Contact Overview

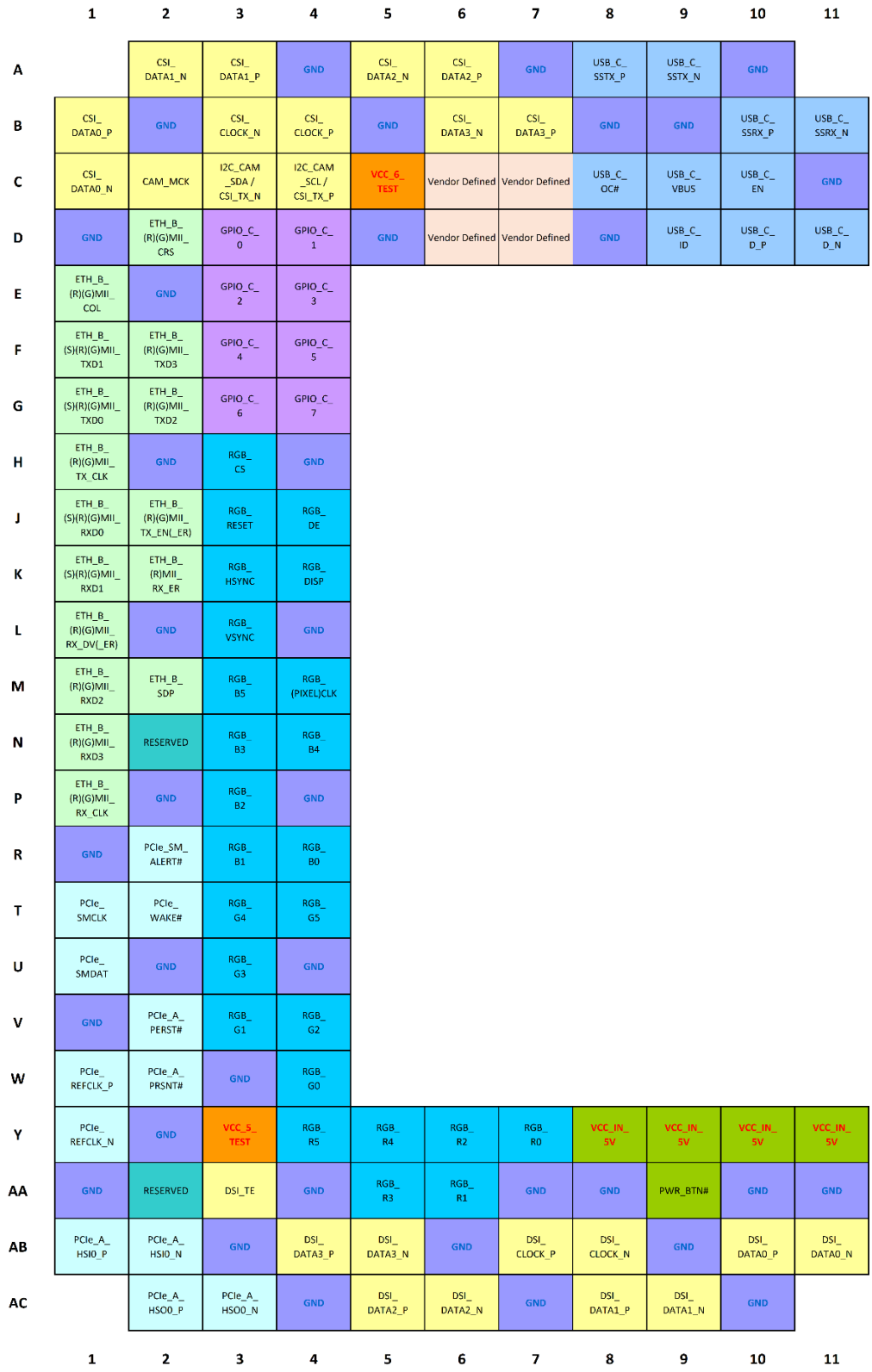


Figure 24: Size-S detailed Contact Overview

2.3.5 Size-M – ADDITIONAL Functions

2.3.5.1 Size-M – Function Table

Size-M's functionality on column 13 to 23 is identical to Size-0. There is only one change in the necessity of USB interfaces according to following table:

Functionality	Description	Quantity of Interfaces	No. of Contacts	Mandatory Interface
USB	USB 2.0	1 … 2	12	**1x Yes**
I2C	I2C	1 … 2	4	**1x Yes**

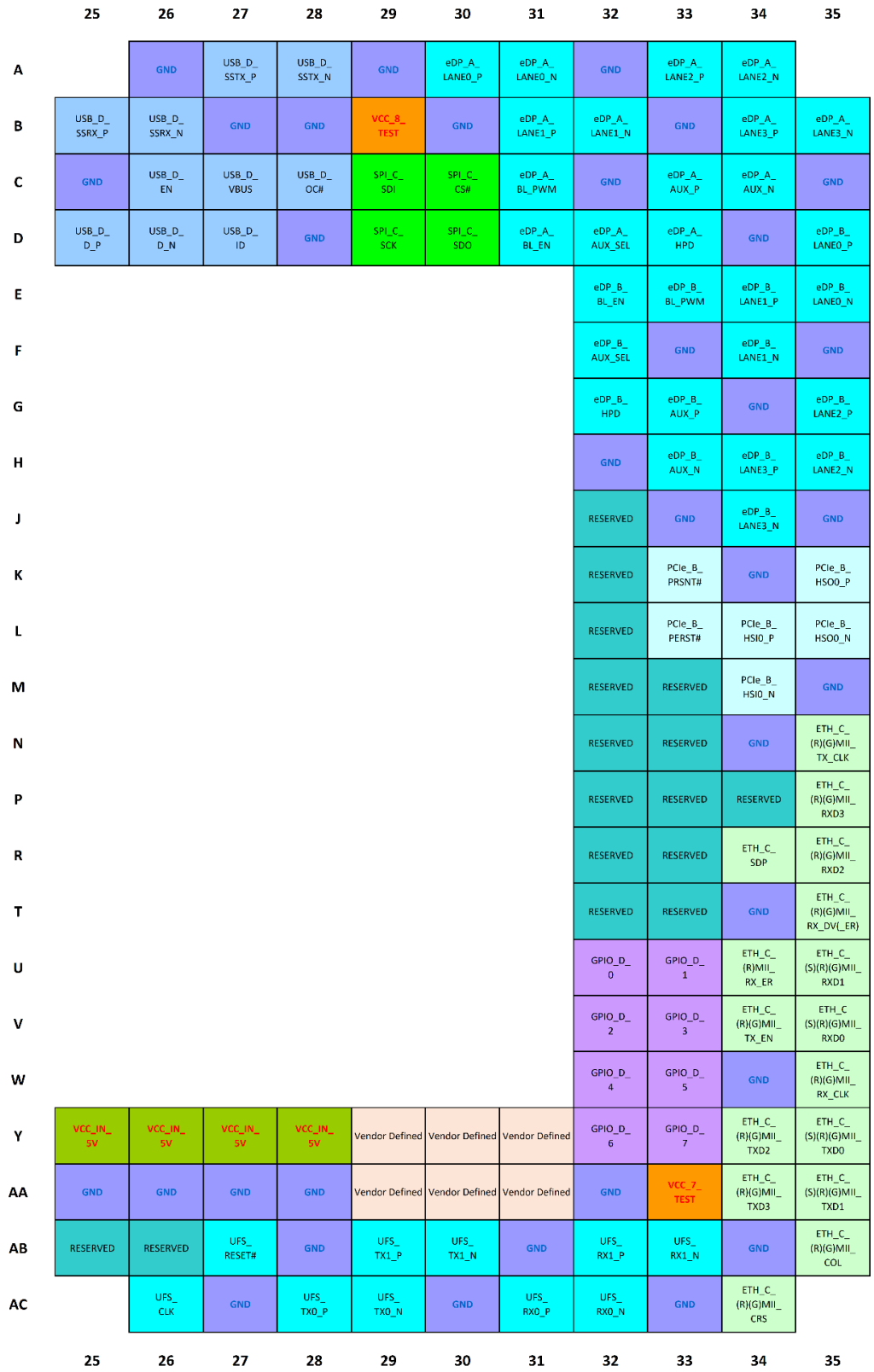
Table 7: Size-M Changes to Size-0

The following table describes the additional functions on column 24 to 35.

Functionality	Description	Quantity of additional Interfaces	No. of additional Contacts	Mandatory Interface	Color code
Power Supply	5 V-DC	1	4	Yes	
Ground	Main Power GND	1	34	Yes	
GPIO	General Purpose Input Output	0 … 8	8	No	
Reserved	TBD / for future use	0 … 16	16	No	
Vendor Defined	Defined by module manufacturer	0 … 6	6	No	
Ethernet / LAN	(Q)(S)(R)(G)MII, 100/1000 Mbit	0 … 1	16	No	
USB	USB 2.0 with 3.0 option	0 … 1	10	No	
Display Interface	eDP_A, eDP_B	0 … 2	28	No	
PCIe x1		0 … 1	6	No	
Testing	VCC_Test_5 … 6	0 … 2	2	No	
UFS		0 … 1	10	No	
SPI	Host or Slave	0 … 1	4	No	
Amount of Contacts			144		

Table 8: Size-M Additional Functionality / Interfaces

2.3.5.2 Size-M – Detailed Contact Overview



	25	26	27	28	29	30	31	32	33	34	35
A		GND	USB_D_ SSTX_P	USB_D_ SSTX_N	GND	eDP_A_ LANE0_P	eDP_A_ LANE0_N	GND	eDP_A_ LANE2_P	eDP_A_ LANE2_N	
B	USB_D_ SSRX_P	USB_D_ SSRX_N	GND	GND	VCC_8_ TEST	GND	eDP_A_ LANE1_P	eDP_A_ LANE1_N	GND	eDP_A_ LANE3_P	eDP_A_ LANE3_N
C	GND	USB_D_ EN	USB_D_ VBUS	USB_D_ OC#	SPI_C_ SDI	SPI_C_ CS#	eDP_A_ BL_PWM	GND	eDP_A_ AUX_P	eDP_A_ AUX_N	GND
D	USB_D_ D_P	USB_D_ D_N	USB_D_ ID	GND	SPI_C_ SCK	SPI_C_ SDO	eDP_A_ BL_EN	eDP_A_ AUX_SEL	eDP_A_ HPD	GND	eDP_B_ LANE0_P
E								eDP_B_ BL_EN	eDP_B_ BL_PWM	eDP_B_ LANE1_P	eDP_B_ LANE0_N
F								eDP_B_ AUX_SEL	GND	eDP_B_ LANE1_N	GND
G								eDP_B_ HPD	eDP_B_ AUX_P	GND	eDP_B_ LANE2_P
H								GND	eDP_B_ AUX_N	eDP_B_ LANE3_P	eDP_B_ LANE2_N
J								RESERVED	GND	eDP_B_ LANE3_N	GND
K								RESERVED	PCIe_B_ PRSNT#	GND	PCIe_B_ HSO0_P
L								RESERVED	PCIe_B_ PERST#	PCIe_B_ HSI0_P	PCIe_B_ HSO0_N
M								RESERVED	RESERVED	PCIe_B_ HSI0_N	GND
N								RESERVED	RESERVED	GND	ETH_C_ (R)(G)MII_ TX_CLK
P								RESERVED	RESERVED	RESERVED	ETH_C_ (R)(G)MII_ RXD3
R								RESERVED	RESERVED	ETH_C_ SDP	ETH_C_ (R)(G)MII_ RXD2
T								RESERVED	RESERVED	GND	ETH_C_ (R)(G)MII_ RX_DV(_ER)
U								GPIO_D_ 0	GPIO_D_ 1	ETH_C_ (R)MII_ RX_ER	ETH_C_ (S)(R)(G)MII_ RXD1
V								GPIO_D_ 2	GPIO_D_ 3	ETH_C_ (R)(G)MII_ TX_EN	ETH_C (S)(R)(G)MII_ RXD0
W								GPIO_D_ 4	GPIO_D_ 5	GND	ETH_C_ (R)(G)MII_ RX_CLK
Y	VCC_IN_ 5V	VCC_IN_ 5V	VCC_IN_ 5V	VCC_IN_ 5V	Vendor Defined	Vendor Defined	Vendor Defined	GPIO_D_ 6	GPIO_D_ 7	ETH_C_ (R)(G)MII_ TXD2	ETH_C_ (S)(R)(G)MII_ TXD0
AA	GND	GND	GND	GND	Vendor Defined	Vendor Defined	Vendor Defined	GND	VCC_7_ TEST	ETH_C_ (R)(G)MII_ TXD3	ETH_C_ (S)(R)(G)MII_ TXD1
AB	RESERVED	RESERVED	UFS_ RESET#	GND	UFS_ TX1_P	UFS_ TX1_N	GND	UFS_ RX1_P	UFS_ RX1_N	GND	ETH_C_ (R)(G)MII_ COL
AC		UFS_ CLK	GND	UFS_ TX0_P	UFS_ TX0_N	GND	UFS_ RX0_P	UFS_ RX0_N	GND	ETH_C_ (R)(G)MII_ CRS	

Figure 25: Size-M detailed Contact Overview

2.3.6 Size-L – ADDITIONAL Functions

2.3.6.1 Size-L – Function Table

Size-L's functionality on column 13 to 23 is identical to Size-0. There is only one change in the necessity of USB interfaces according to following table:

Functionality	Description	Quantity of Interfaces	No. of Contacts	Mandatory Interface
USB	USB 2.0	1 … 2	12	**1x Yes**
I2C	I2C	1 … 2	4	**1x Yes**

Table 9: Size-L Changes to Size-0

The following table describes the additional functions on line AE to AP

Functionality	Description	Quantity of additional Interfaces	No. of additional Contacts	Mandatory Interface	Color Code
Power Supply	5 V-DC	1	8	Yes	
Ground	Main Power GND	1	40	Yes	
GPIO	General Purpose Input Output	0 … 8	8	No	
Reserved	TBD / for future use	0 … 37	31	No	
Vendor Defined	Defined by module manufacturer	0 … 6	6	No	
Ethernet / LAN	(Q)(S)(R)(G)MII, 100/1000 Mbit	0 … 2	32	No	
Display Interface	LVDS	0 … 1	25	No	
PCIe x4	x1 option	0 … 2	36	No	
Amount of Contacts			186		

Table 10: Size-L Additional Functionality / Interfaces

2.3.6.2 Size-L – Detailed Contact Overview

	1	2	3	4	5	6	7	8	9	10	11	12
AE		GND	ETH_D_ (R)(G)MII_ CRS	VCC_IN_ 5V								
AF	ETH_D_ (S)(R)(G)MII_ TXD0	ETH_D_ (R)(G)MII_ TXD3	ETH_D_ (R)(G)MII_ COL	VCC_IN_ 5V								
AG	ETH_D_ (S)(R)(G)MII_ TXD1	ETH_D_ (R)(G)MII_ TXD2	GND	VCC_IN_ 5V								
AH	ETH_D_ (R)(G)MII_ TX_CLK	GND	VCC_IN_ 5V	VCC_IN_ 5V								
AJ	ETH_D_ (S)(R)(G)MII_ RXD0	ETH_D_ (R)(G)MII_ TX_EN(_ER)	VCC_IN_ 5V	VCC_IN_ 5V								
AK	ETH_D_ (S)(R)(G)MII_ RXD1	ETH_D_ (R)MII_ RX_ER	GND	VCC_IN_ 5V								
AL	ETH_D_ (R)(G)MII_ RX_DV(_ER)	GND	RESERVED	RESERVED								
AM	ETH_D_ (R)(G)MII_ RXD2	ETH_B_ SDP	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LVDS_ I2C_CLK	LVDS_ I2C_DAT
AN	ETH_D_ (R)(G)MII_ RXD3	RESERVED	GND	ETH_E_ (R)(G)MII_ CRS	RESERVED	GND	RESERVED	RESERVED	GND	ETH_E_ (R)(G)MII_ RX_CLK	GND	LVDS_A_ CLK_N
AP	ETH_D_ (R)(G)MII_ RX_CLK	GND	ETH_E_ (R)(G)MII_ TXD2	ETH_E_ (R)(G)MII_ TXD3	GND	ETH_E_ (R)(G)MII_ TX_EN(_EN)	ETH_E_ (R)MII_ RX_ER	GND	ETH_E_ SDP	RESERVED	LVDS_A_ LANE3_N	LVDS_A_ LANE3_P
AR		ETH_E_ (R)(G)MII_ COL	ETH_E_ (S)(R)(G)MII_ TXD0	ETH_E_ (S)(R)(G)MII_ TXD1	ETH_E_ (R)(G)MII_ TX_CLK	ETH_E_ (S)(R)(G)MII_ RXD0	ETH_E_ (S)(R)(G)MII_ RXD1	ETH_E_ (R)(G)MII_ RX_DV(_ER)	ETH_E_ (R)(G)MII_ RXD2	ETH_E_ (R)(G)MII_ RXD3		
	1	2	3	4	5	6	7	8	9	10	11	12

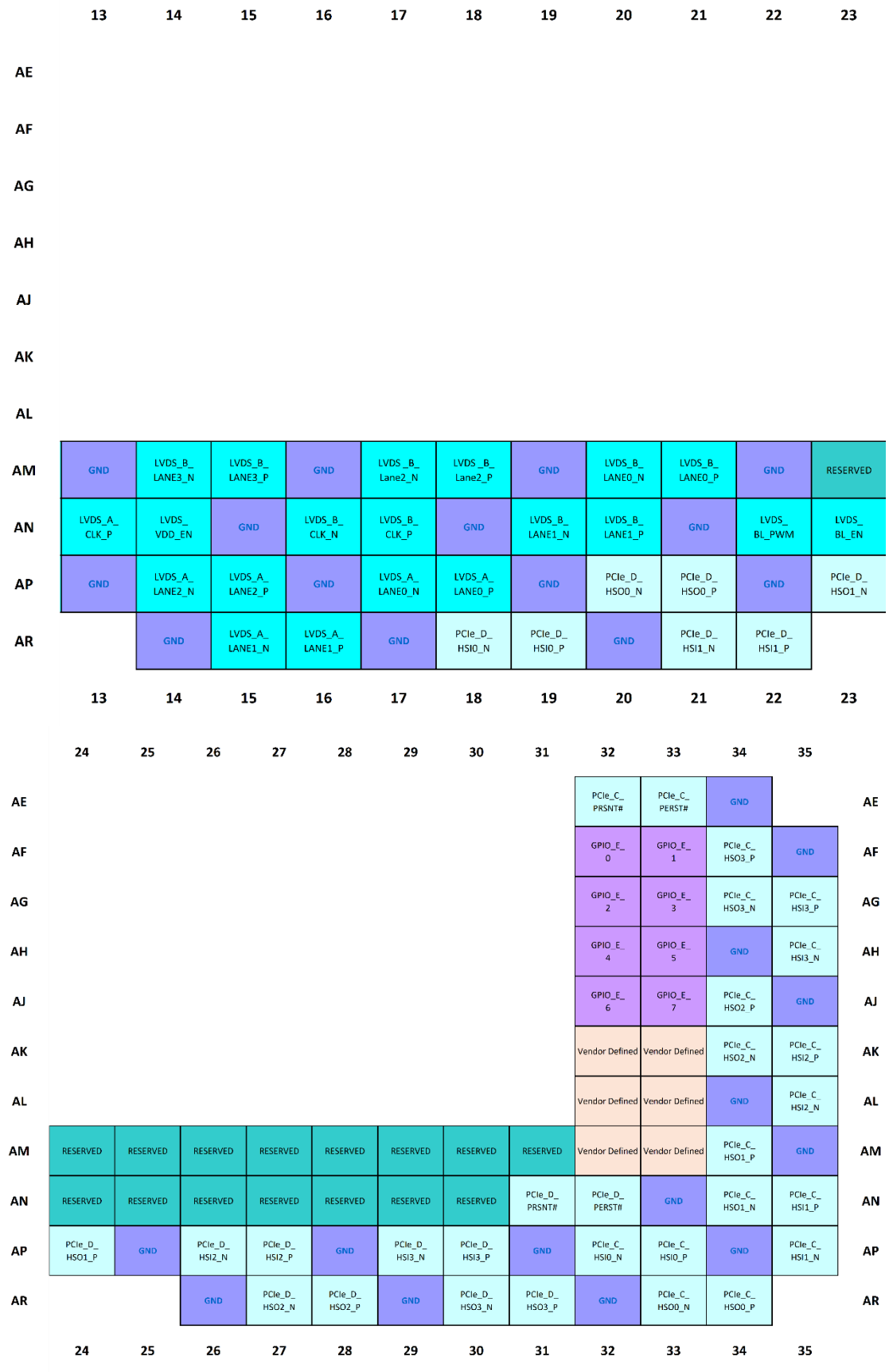


Figure 26: Size-L Detailed Contact Overview

2.4 Contact Tables

All data in the contacts tables refer to the associated module, i.e. any mentioned PU/PD should be placed on the module, not on the carrier.

2.4.1 Signal Descriptions

2.4.1.1 Signal Naming Convention

Active-low signals are indicated by a trailing '#' sign: REQ#

Differential pairs are indicated by trailing '_P' and '_N' signs: TX_P, TX_N

2.4.1.2 I/O Types

The I/O Type defines Contact Type and Buffer Type according following Tables

Contact Type	Description	Comments
I	Input to the Module	
O	Output from the Module	
I/O	Bi-directional Input / Output signal	
OD	Open Drain Output	
I OD	Input to the module, where an OD output on the carrier is expected	

Table 11: Contact Types

Buffer Type	Description	Comments
P	Power to the module or Power source from the module	
Analog	Analog signal between defined voltage	
CMOS	Logic input or output.	Please check the noise margins for your logic levels.
USB	USB compatible differential signal. Please refer to the USB Specification for details.	
USB SS	USB SuperSpeed signal. Please refer to the USB 3.x specification for details.	
MDI	Media Dependent Interface, differential signal.	
LVDS D-PHY	MIPI-DSI/CSI differential signal. Please refer to the MIPI D-PHY specification	
LVDS M-PHY	MIPI-DSI/CSI differential signal. Please refer to the MIPI M-PHY specification	
LVDS PCIE	PCI Express compatible differential signal. Please refer to the PCI Express Specification for details.	
LVDS UFS	UFS compatible differential signal. Please refer to the UFS specification by JEDEC.	
LVDS DP	DisplayPort compatible differential signal. Please refer to the DisplayPort specification for details.	
LVDS LCD	Low Voltage Differential signals for connecting an LCD. Please refer to the LDI/OLDI specification for details.	

Table 12: Buffer Types

2.4.2 Size-0 Basic Functionality

2.4.2.1 Power Supply + Ground

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
VCC_1_TEST	M17	Module power voltage testpoint	P			
VCC_2_TEST	M19	Module power voltage testpoint	P			
VCC_3_TEST	Y16	Module power voltage testpoint	P			
VCC_4_TEST	Y20	Module power voltage testpoint	P			
VCC_IN_5V	Y17	Module power input voltage of 5V – Primary voltage rail for size S, M and L modules	P			
VCC_IN_3V3	Y19	Module power input voltage of 3.3V – Primary voltage rail for 0 size modules	P			
V_BAT	AA18,AB18	Module power input battery voltage	P			
GND	D18, E15, E21, F16, F20, J16, J20, L18, M16, M20, P18, R16, R20, V16, V20, Y18, AA14, AA17, AA19, AA22, AB15, AB21	Module Signal and power return and GND reference	P			
SYS_RST#	U17	Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise.	I OD CMOS	1.8V	PU 10K	
CARRIER_PWR_EN	V17	Carrier board circuits should not be powered up until the module asserts the CARRIER_PWR_EN signal	O CMOS	1.8V		

VCC_OUT_IO	U18	Can provide IO voltage level for several interfaces to connect	P	1.8V/3.3V		Only applicable in size 0 – minimum current: 100mA; All other sizes or feature not used: NC
RTC_PWR	W17	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based Lithium cell or Super Cap.	P			
BOOT_SEL#	U19	If low on carrier board it has to boot from carrier boot medium (SD/USB/SPI)	I OD CMOS	1.8V	PU 10k	The boot medium is the choice of the module vendor.

Table 13: Size-0 Power

2.4.2.2 JTAG

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level (Size-0 only, optional)	I/O Level (>Size-0)	PU / PD	Comments
JTAG_TCK(SWCLK)	N17	Test Clock	I CMOS	V_OUT_IO	1.8V		
JTAG_TMS(SWDIO)	N19	Test Mode Select	I CMOS	V_OUT_IO	1.8V		
JTAG_TDI	P17	Test Data Input	I CMOS	V_OUT_IO	1.8V		
JTAG_RTCK	P19	Returned Test Clock	O CMOS	V_OUT_IO	1.8V		
JTAG_TDO(SWO)	R17	Test Data Output	O CMOS	V_OUT_IO	1.8V		
JTAG_nTRST	R19	Test Reset, Active Low	I CMOS	V_OUT_IO	1.8V		
DEBUG_EN	AC18	Enables JTAG function	I CMOS	V_OUT_IO	1.8V		
TEST_GENERIC	C18	General purpose for testing	O CMOS	V_OUT_IO	1.8V		

Table 14: Size-0 JTAG

2.4.2.3 UART

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level (Size-0 only, optional)	I/O Level (>Size-0)	PU / PD	Comments
UART_A_RX	A14	Asynchronous serial data input port A	I CMOS	V_OUT_IO	1.8V		
UART_A_TX	B13	Asynchronous serial data output port A	O CMOS	V_OUT_IO	1.8V		
UART_A_RTS	C13	"Request to Send" handshake line for port A	O CMOS	V_OUT_IO	1.8V		
UART_A_CTS	C14	"Clear to Send" handshake line for port A	I CMOS	V_OUT_IO	1.8V		
UART_B_RX	D14	Asynchronous serial data input port B	I CMOS	V_OUT_IO	1.8V		
UART_B_TX	D13	Asynchronous serial data output port B	O CMOS	V_OUT_IO	1.8V		
UART_B_RTS	D15	"Request to Send" handshake line for port B	O CMOS	V_OUT_IO	1.8V		
UART_B_CTS	D16	"Clear to Send" handshake line for port B	I CMOS	V_OUT_IO	1.8V		
UART_C_RX	A22	Asynchronous serial data input port C	I CMOS	V_OUT_IO	1.8V		
UART_C_TX	B23	Asynchronous serial data output port C	O CMOS	V_OUT_IO	1.8V		
UART_D_RX	C22	Asynchronous serial data input port D	I CMOS	V_OUT_IO	1.8V		
UART_D_TX	C23	Asynchronous serial data output port D	O CMOS	V_OUT_IO	1.8V		

Table 15: Size-0 UART

2.4.2.4 UART Console

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level (Size-0 only, optional)	I/O Level (>Size-0)	PU / PD	Comments
UART_CON_RX	D22	Asynchronous serial data input port console	I CMOS	V_OUT_IO	1.8V		
UART_CON_TX	D23	Asynchronous serial data output port console	O CMOS	V_OUT_IO	1.8V		

Table 16: Size-0 UART Console

2.4.2.5 Ethernet

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
ETH_A_(R)(G)MII_CRS	E16	Carrier Sense port A	I CMOS	1.8V/2.5V/3.3V		
ETH_A_(R)(G)MII_COL	F15	Collision detect (half speed only) port A	I CMOS	1.8V/2.5V/3.3V		
ETH_A_(S)(R)(G)MII_TXD0	H15	Transmit data bit 0 (transmitted first) port A	O CMOS	1.8V/2.5V/3.3V		_P when used as differential
ETH_A_(S)(R)(G)MII_TXD1	G15	Transmit data bit 1 port A	O CMOS	1.8V/2.5V/3.3V		_N when used as differential
ETH_A_(R)(G)MII_TXD2	H16	Transmit data bit 2 port A	O CMOS	1.8V/2.5V/3.3V		
ETH_A_(R)(G)MII_TXD3	G16	Transmit data bit 3 port A	O CMOS	1.8V/2.5V/3.3V		
ETH_A_(R)(G)MII_TX_EN(_ER)	K16	Transmit enable (Error) port A	O CMOS	1.8V/2.5V/3.3V		
ETH_A_(R)(G)MII_TX_CLK	J15	Transmit clock port A	I/O CMOS	1.8V/2.5V/3.3V		
ETH_A_(S)(R)(G)MII_RXD0	K15	Receive data bit 0 (received first) port A	I CMOS	1.8V/2.5V/3.3V		_P when used as differential
ETH_A_(S)(R)(G)MII_RXD1	L15	Receive data bit 1 port A	I CMOS	1.8V/2.5V/3.3V		_N when used as differential
ETH_A_(R)(G)MII_RXD2	N15	Receive data bit 2 port A	I CMOS	1.8V/2.5V/3.3V		
ETH_A_(R)(G)MII_RXD3	P15	Receive data bit 3 port A	I CMOS	1.8V/2.5V/3.3V		
ETH_A_(R)(G)MII_RX_ER	L16	Receive error port A	I CMOS	1.8V/2.5V/3.3V		
ETH_A_(R)(G)MII_RX_DV(_ER)	M15	Receive data valid port A	I CMOS	1.8V/2.5V/3.3V		
ETH_A_(R)(G)MII_RX_CLK	R15	Receive clock port A	I/O CMOS	1.8V/2.5V/3.3V		
ETH_A_SDP	N16	Ethernet port A System Defined Contact	O CMOS	1.8V/2.5V/3.3V		

ETH_MDIO	T15	Management data	I/O CMOS	1.8V/2.5V/3.3V		
ETH_MDC	T16	Management data clock	O CMOS	1.8V/2.5V/3.3V		

Table 17: Size-0 Ethernet

2.4.2.6 GPIO

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level (Size-0 only, optional)	I/O Level (>Size-0)	PU / PD	Comments
GPIO_A_0	D17	General purpose I/O Contact A0	I/O CMOS	V_OUT_IO	1.8V		
GPIO_A_1	E17	General purpose I/O Contact A1	I/O CMOS	V_OUT_IO	1.8V		
GPIO_A_2	F17	General purpose I/O Contact A2	I/O CMOS	V_OUT_IO	1.8V		
GPIO_A_3	G17	General purpose I/O Contact A3	I/O CMOS	V_OUT_IO	1.8V		
GPIO_A_4	H17	General purpose I/O Contact A4	I/O CMOS	V_OUT_IO	1.8V		
GPIO_A_5	J17	General purpose I/O Contact A5	I/O CMOS	V_OUT_IO	1.8V		
GPIO_A_6	K17	General purpose I/O Contact A6	I/O CMOS	V_OUT_IO	1.8V		
GPIO_A_7	L17	General purpose I/O Contact A7	I/O CMOS	V_OUT_IO	1.8V		
GPIO_B_0	D19	General purpose I/O Contact B0	I/O CMOS	V_OUT_IO	1.8V		
GPIO_B_1	E19	General purpose I/O Contact B1	I/O CMOS	V_OUT_IO	1.8V		
GPIO_B_2	F19	General purpose I/O Contact B2	I/O CMOS	V_OUT_IO	1.8V		
GPIO_B_3	G19	General purpose I/O Contact B3	I/O CMOS	V_OUT_IO	1.8V		
GPIO_B_4	H19	General purpose I/O Contact B4	I/O CMOS	V_OUT_IO	1.8V		
GPIO_B_5	J19	General purpose I/O Contact B5	I/O CMOS	V_OUT_IO	1.8V		
GPIO_B_6	K19	General purpose I/O Contact B6	I/O CMOS	V_OUT_IO	1.8V		
GPIO_B_7	L19	General purpose I/O Contact B7	I/O CMOS	V_OUT_IO	1.8V		

Table 18: Size-0 GPIO

2.4.2.7 SDIO

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
SDIO_A_CMD	E20	SDIO A Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O CMOS	1.8V or 3.3V		
SDIO_A_CLK	F21	SDIO A Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	O CMOS	1.8V or 3.3V		
SDIO_A_D0	G20	SDIO A Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V		
SDIO_A_D1	G21	SDIO A Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V		
SDIO_A_D2	H20	SDIO A Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V		
SDIO_A_D3	H21	SDIO A Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V		
SDIO_A_CD#	J21	SDIO A Card Detect. This signal indicates when a SDIO/MMC card is present.	I OD CMOS	1.8V or 3.3V	PU 10k	
SDIO_A_WP	D20	SDIO A Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I OD CMOS	1.8V or 3.3V	PU 10k	Tie to GND on carrier, if not used
SDIO_A_PWR_EN	D21	SDIO A Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	O CMOS	1.8V or 3.3V		
SDIO_A_IOPWR	C20	SDIO A Voltage. It is used to provide the IO Voltage Level	P	1.8V or 3.3V		Minimum current: 100mA
SDIO_B_CLK	K20	SDIO B Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	O CMOS	1.8V or 3.3V		
SDIO_B_CMD	K21	SDIO B Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O CMOS	1.8V or 3.3V		

SDIO_B_D0	L20	SDIO B Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V		
SDIO_B_D1	L21	SDIO B Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V		
SDIO_B_D2	M21	SDIO B Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V		
SDIO_B_D3	N20	SDIO B Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V		
SDIO_B_D4	N21	SDIO B Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V		
SDIO_B_D5	P20	SDIO B Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V		
SDIO_B_D6	P21	SDIO B Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V		
SDIO_B_D7	R21	SDIO B Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V		
SDIO_B_CD#	T21	SDIO B Card Detect. This signal indicates when a SDIO/MMC card is present.	I OD CMOS	1.8V or 3.3V	PU 10k	
SDIO_B_WP	U20	SDIO B Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I OD CMOS	1.8V or 3.3V	PU 10k	Tie to GND on carrier, if not used
SDIO_B_PWR_EN	U21	SDIO B Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	O CMOS	1.8V or 3.3V		
SDIO_B_IOPWR	T20	SDIO B Voltage. It is used to provide the IO Voltage Level	P	1.8V or 3.3V		Minimum current: 100mA

Table 19: Size-0 SDIO

2.4.2.8 PWM

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level (Size-0 only, optional)	I/O Level (>Size-0)	PU / PD	Comments
PWM_0	E18	Pulse width modulation 0	O CMOS	V_OUT_IO	1.8V		
PWM_1	F18	Pulse width modulation 1	O CMOS	V_OUT_IO	1.8V		
PWM_2	G18	Pulse width modulation 2	O CMOS	V_OUT_IO	1.8V		
PWM_3	H18	Pulse width modulation 3	O CMOS	V_OUT_IO	1.8V		
PWM_4	J18	Pulse width modulation 4	O CMOS	V_OUT_IO	1.8V		
PWM_5	K18	Pulse width modulation 5	O CMOS	V_OUT_IO	1.8V		

Table 20: Size-0 PWM

2.4.2.9 Analog Signals

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
ADC_0	M18	Analog Digital Converter 0	Analog	0V – 1.8V		
ADC_1	N18	Analog Digital Converter 1	Analog	0V – 1.8V		

Table 21: Size-0 Analog Signals

2.4.2.10 SPI

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level (Size-0 only, optional)	I/O Level (>Size-0)	PU / PD	Comments
SPI_A_SDI_(IO0)	U15	SPI A Serial Data Input	IO CMOS	V_OUT_IO	1.8V		Alternate use: QuadSPI IO0
SPI_A_SDO_(IO1)	V15	SPI A Serial Data Output	IO CMOS	V_OUT_IO	1.8V		Alternate use: QuadSPI IO1
SPI_A_/WP_(IO2)	W16	SPI A Write Protect	IO CMOS	V_OUT_IO	1.8V		Alternate use: QuadSPI IO2
SPI_A_/HOLD_(IO3)	W15	SPI A Suspends Serial Input	IO CMOS	V_OUT_IO	1.8V		Alternate use: QuadSPI IO3
SPI_A_CS#	Y15	SPI A Master Chip Select	O CMOS	V_OUT_IO	1.8V		
SPI_A_SCK	U16	SPI A Serial Data Clock	O CMOS	V_OUT_IO	1.8V		
SPI_B_SDI	Y22	SPI B Serial Data Input	I CMOS	V_OUT_IO	1.8V		
SPI_B_SDO	Y23	SPI B Serial Data Output	O CMOS	V_OUT_IO	1.8V		
SPI_B_CS#	AA23	SPI B Master Chip Select	O CMOS	V_OUT_IO	1.8V		
SPI_B_SCK	Y21	SPI B Serial Data Clock	O CMOS	V_OUT_IO	1.8V		

Table 22: Size-0 SPI

2.4.2.11 I2S

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level (Size-0 only, optional)	I/O Level (>Size-0)	PU / PD	Comments
I2S_A_DATA_IN	V21	I2S A Digital audio Input	I/O CMOS	V_OUT_IO	1.8V		
I2S_A_DATA_OUT	W21	I2S A Digital audio Output	I/O CMOS	V_OUT_IO	1.8V		
I2S_B_DATA_IN	V19	I2S B Digital audio Input	I/O CMOS	V_OUT_IO	1.8V		
I2S_B_DATA_OUT	W19	I2S B Digital audio Output	I/O CMOS	V_OUT_IO	1.8V		
I2S_MCLK	V18	Master clock output to I2S codec(s)	I/O CMOS	V_OUT_IO	1.8V		
I2S_LRCLK	W18	I2S Left & Right synchronization clock	I/O CMOS	V_OUT_IO	1.8V		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
I2S_BITCLK	W20	I2S Digital audio clock	I/O CMOS	V_OUT_IO	1.8V		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode

Table 23: Size-0 I2S

2.4.2.12 CAN

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level (Size-0 only, optional)	I/O Level (>Size-0)	PU / PD	Comments
CAN_A_TX	AC17	CAN port A Transmit output	O CMOS	V_OUT_IO	1.8V		
CAN_A_RX	AB17	CAN port A Receive input	I CMOS	V_OUT_IO	1.8V		
CAN_B_TX	AC19	CAN port B Transmit output	O CMOS	V_OUT_IO	1.8V		
CAN_B_RX	AB19	CAN port B Receive input	I CMOS	V_OUT_IO	1.8V		

Table 24: Size-0 CAN

2.4.2.13 USB

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
USB_A_D_N	AB13	USB differential data pairs for port A	I/O USB	USB		
USB_A_D_P	AC14	USB differential data pairs for port A	I/O USB	USB		
USB_A_ID	AB14	Input Contact to announce OTG device insertion on USB 2.0 port	I CMOS	3.3V		
USB_A_OC#	AC15	USB over-current for port A	I OD CMOS	3.3V	PU 10k	
USB_A_VBUS	AB16	USB port 0 port power detection	I USB VBUS 5V	USB VBUS 5V		
USB_A_EN	AC16	Power enable for usb VBUS voltage	O CMOS	3.3V		
USB_B_D_N	AB23	USB differential data pairs for port B	I/O USB	USB		
USB_B_D_P	AC22	USB differential data pairs for port B	I/O USB	USB		
USB_B_ID	AB22	Input Contact to announce OTG device insertion on USB 2.0 port	I CMOS	3.3V		
USB_B_OC#	AC21	USB over-current for port B	I OD CMOS	3.3V	PU 10k	
USB_B_VBUS	AB20	USB port 0 port power detection	I USB VBUS 5V	USB VBUS 5V		
USB_B_EN	AC20	Power enable for usb VBUS voltage	O CMOS	3.3V		

Table 25: Size-0 USB

2.4.2.14 I2C

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level (Size-0 only, optional)	I/O Level (>Size-0)	PU / PD	Comments
I2C_A_SCL	AA15	I2C Port A Clock Signal	I/O OD CMOS	V_OUT_IO	1.8V	PU 2k2	
I2C_A_SDA	AA16	I2C Port A Data Signal	I/O OD CMOS	V_OUT_IO	1.8V	PU 2k2	
I2C_B_SCL	AA20	I2C Port B Clock Signal	I/O OD CMOS	V_OUT_IO	1.8V	PU 2k2	
I2C_B_SDA	AA21	I2C Port B Data Signal	I/O OD CMOS	V_OUT_IO	1.8V	PU 2k2	

Table 26: I2C

2.4.2.15 Communication Area

The Communication Area can have two different modes, which can be used exclusively either/or and are defined by the module manufacturer.

2.4.2.15.1 Communication Area in Wireless Mode

Contact Name	Contact Name in Wireless Mode	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
COM_AREA_01	ANT_GND	A15	Antenna Ground				
COM_AREA_02	ANT_MAIN	A16	Main Antenna				
COM_AREA_03	ANT_GND	A17	Antenna Ground				
COM_AREA_04	ANT_GND	A18	Antenna Ground				
COM_AREA_05	ANT_GND	A19	Antenna Ground				
COM_AREA_06	ANT_AUX	A20	Antenna Auxiliary Signal				
COM_AREA_07	ANT_GND	A21	Antenna Ground				
COM_AREA_08	ANT_GND	B15	Antenna Ground				
COM_AREA_09	ANT_GND	B16	Antenna Ground				
COM_AREA_10	ANT_GND	B17	Antenna Ground				
COM_AREA_11	ANT_GND	B18	Antenna Ground				
COM_AREA_12	ANT_GND	B19	Antenna Ground				
COM_AREA_13	ANT_GND	B20	Antenna Ground				
COM_AREA_14	ANT_GND	B21	Antenna Ground				

COM_AREA_15	ANT_MAIN_TEST	C15	Main antenna test point				
COM_AREA_16	ANT_B_MAIN_TEST	C17	Main antenna test point				
COM_AREA_17	ANT_B_AUX_TEST	C19	Auxiliary antenna test point				
COM_AREA_18	ANT_AUX_TEST	C21	Auxiliary antenna test point				

Table 27: Size-0 Communication Area - Wireless Mode

2.4.2.15.2 Communication Area in Fieldbus Mode

Contact Name	Contact Name in Fieldbus Mode	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
COM_AREA_01	CH1_RX_N	A15	MDI Channel 1	I MDI			Auto-MDIX capable
COM_AREA_02	CH1_LINK	A16	LINK LED Channel 0	O OD CMOS	3.3V		
COM_AREA_03	CH1_TX_N	A17	MDI Channel 1	O MDI			Auto-MDIX capable
COM_AREA_04	CH0_SYNC_TRIGGER	A18	SYNC Trigger Signal Channel 0	O CMOS	3.3V		
COM_AREA_05	CH0_RX_N	A19	MDI Channel 0	I MDI			Auto-MDIX capable
COM_AREA_06	CH0_LINK	A20	LINK LED Channel 0	O OD CMOS	3.3V		
COM_AREA_07	CH0_TX_N	A21	MDI Channel 0	O MDI			Auto-MDIX capable
COM_AREA_08	CH1_RX_P	B15	MDI Channel 1	I MDI			Auto-MDIX capable
COM_AREA_09	CH1_ACT	B16	ACT LED Channel 1	O OD CMOS	3.3V		
COM_AREA_10	CH1_TX_P	B17	MDI Channel 1	O MDI			Auto-MDIX capable
COM_AREA_11	CH1_SYNC_TRIGGER	B18	SYNC Trigger Signal Channel 1	O CMOS	3.3V		
COM_AREA_12	CH0_RX_P	B19	MDI Channel 0	I MDI			Auto-MDIX capable
COM_AREA_13	CH0_ACT	B20	ACT LED Channel 0	O OD CMOS	3.3V		
COM_AREA_14	CH0_TX_P	B21	MDI Channel 0	O MDI			Auto-MDIX capable
COM_AREA_15	CH1_RXC	C15	MDI Channel 1	Analog	0 to 3.3V		
COM_AREA_16	CH1_TXC	C17	MDI Channel 1	Analog	0 to 3.3V		
COM_AREA_17	CH0_RXC	C19	MDI Channel 0	Analog	0 to 3.3V		

COM_AREA_18	CH0_TXC	C21	MDI Channel 0	Analog	0 to 3.3V		

Table 28: Size-0 Communication Area - Fieldbus Mode

2.4.2.16 Reserved

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
RESERVED	R18, T17, T18, T19, Y13, Y14, AA13	Reserved for future use				

Table 29: Size-0 Reserved Contacts

2.4.2.17 Vendor Defined Contacts

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
Vendor Defined	B22, C16, P16	Defined by module manufacturer				

2.4.3 Size-S – Additional Functionality

2.4.3.1 Power Supply + Ground

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
VCC_5_TEST	Y3	Module power voltage test point	P			
VCC_6_TEST	C5	Module power voltage test point	P			
VCC_IN_5V	Y8, Y9, Y10, Y11	Module power input voltage of 5V	P			
GND	A4, A7, A10, B2, B5, B8, B9, C11, D1, D5, D8, E2, H2, H4, L2, L4, P2, P4, R1, U2, U4, V1, W3, Y2, AA1, AA4, AA7, AA8, AA10, AA11, AB3, AB6, AB9, AC4, AC7, AC10	Module Signal and power return and GND reference	P			
PWR_BTN#	AA9	Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module.	I OD CMOS	1.8 to 5V	PU 10K	

Table 30: Size-S Power + Ground

2.4.3.2 Ethernet / LAN

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
ETH_B_(R)(G)MII_CRS	D2	Carrier Sense port B	I CMOS	1.8V/2.5V/3.3V		
ETH_B_(R)(G)MII_COL	E1	Collision detect (half speed only) port B	I CMOS	1.8V/2.5V/3.3V		
ETH_B_(S)(R)(G)MII_TXD0	G1	Transmit data bit 0 (transmitted first) port B	O CMOS	1.8V/2.5V/3.3V		_P when used as differential
ETH_B_(S)(R)(G)MII_TXD1	F1	Transmit data bit 1 port B	O CMOS	1.8V/2.5V/3.3V		_N when used as differential
ETH_B_(R)(G)MII_TXD2	G2	Transmit data bit 2 port B	O CMOS	1.8V/2.5V/3.3V		
ETH_B_(R)(G)MII_TXD3	F2	Transmit data bit 3 port B	O CMOS	1.8V/2.5V/3.3V		
ETH_B_(R)(G)MII_TX_EN(_ER)	J2	Transmit enable (Error) port B	O CMOS	1.8V/2.5V/3.3V		
ETH_B_(R)(G)MII_TX_CLK	H1	Transmit clock port B	I/O CMOS	1.8V/2.5V/3.3V		
ETH_B_(S)(R)(G)MII_RXD0	J1	Receive data bit 0 (received first) port B	I CMOS	1.8V/2.5V/3.3V		_P when used as differential
ETH_B_(S)(R)(G)MII_RXD1	K1	Receive data bit 1 port B	I CMOS	1.8V/2.5V/3.3V		_N when used as differential
ETH_B_(R)(G)MII_RXD2	M1	Receive data bit 2 port B	I CMOS	1.8V/2.5V/3.3V		
ETH_B_(R)(G)MII_RXD3	N1	Receive data bit 3 port B	I CMOS	1.8V/2.5V/3.3V		
ETH_B_(R)(G)MII_RX_ER	K2	Receive error port B	I CMOS	1.8V/2.5V/3.3V		
ETH_B_(R)(G)MII_RX_DV(_ER)	L1	Receive data valid (Error) port B	I CMOS	1.8V/2.5V/3.3V		
ETH_B_(R)(G)MII_RX_CLK	P1	Receive clock port B	I/O CMOS	1.8V/2.5V/3.3V		
ETH_B_SDP	M2	Ethernet port B System Defined Contact	O CMOS	1.8V/2.5V/3.3V		

Table 31 Size-S: Ethernet

2.4.3.3 GPIO

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
GPIO_C_0	D3	General purpose I/O Contact C0	I/O CMOS	1.8V		
GPIO_C_1	D4	General purpose I/O Contact C1	I/O CMOS	1.8V		
GPIO_C_2	E3	General purpose I/O Contact C2	I/O CMOS	1.8V		
GPIO_C_3	E4	General purpose I/O Contact C3	I/O CMOS	1.8V		
GPIO_C_4	F3	General purpose I/O Contact C4	I/O CMOS	1.8V		
GPIO_C_5	F4	General purpose I/O Contact C5	I/O CMOS	1.8V		
GPIO_C_6	G3	General purpose I/O Contact C6	I/O CMOS	1.8V		Dual function: CAM_PWR
GPIO_C_7	G4	General purpose I/O Contact C7	I/O CMOS	1.8V		Dual function: CAM_RST#

Table 32: Size-S GPIO

2.4.3.4 MIPI DSI

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
DSI_DATA0_N	AB11	DSI differential output (point to point)	O LVDS D-PHY			
DSI_DATA0_P	AB10	DSI differential output (point to point)	O LVDS D-PHY			
DSI_DATA1_N	AC9	DSI differential output (point to point)	O LVDS D-PHY			
DSI_DATA1_P	AC8	DSI differential output (point to point)	O LVDS D-PHY			
DSI_DATA2_N	AC6	DSI differential output (point to point)	O LVDS D-PHY			
DSI_DATA2_P	AC5	DSI differential output (point to point)	O LVDS D-PHY			
DSI_DATA3_N	AB5	DSI differential output (point to point)	O LVDS D-PHY			
DSI_DATA3_P	AB4	DSI differential output (point to point)	O LVDS D-PHY			
DSI_CLOCK_N	AB8	DSI differential clock output (point to point)	O LVDS D-PHY			
DSI_CLOCK_P	AB7	DSI differential clock output (point to point)	O LVDS D-PHY			
DSI_TE	AA3	DSI panel tearing effect signal	I CMOS	1.8V		

Table 33: Size-S MIPI DSI

2.4.3.5 MIPI CSI

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
CSI_DATA0_N	C1	CSI differential input (point to point)	I LVDS D-PHY/ I LVDS M-PHY			
CSI_DATA0_P	B1	CSI differential input (point to point)	I LVDS D-PHY / I LVDS M-PHY			
CSI_DATA1_N	A2	CSI differential input (point to point)	I LVDS D-PHY / I LVDS M-PHY			
CSI_DATA1_P	A3	CSI differential input (point to point)	I LVDS D-PHY / I LVDS M-PHY			
CSI_DATA2_N	A5	CSI differential input (point to point)	I LVDS D-PHY / I LVDS M-PHY			
CSI_DATA2_P	A6	CSI differential input (point to point)	I LVDS D-PHY / I LVDS M-PHY			
CSI_DATA3_N	B6	CSI differential input (point to point)	I LVDS D-PHY / I LVDS M-PHY			
CSI_DATA3_P	B7	CSI differential input (point to point)	I LVDS D-PHY / I LVDS M-PHY			
CSI_CLOCK_N	B3	CSI differential clock input (point to point)	I LVDS D-PHY			
CSI_CLOCK_P	B4	CSI differential clock input (point to point)	I LVDS D-PHY			
CAM_MCK	C2	Master clock output	O CMOS	1.8V		
I2C_CAM_SDA / CSI_TX_N	C3	I2C data for serial camera data support link or differential data lane	I/O OD CMOS / O LVDS M-PHY	1.8V	PU 2.2K	MIPI-CSI 2.0 mode uses I2C_CAM_SDA MIPI-CSI 3.0 mode uses CSI_TX_N
I2C_CAM_SCL / CSI_TX_P	C4	I2C clock for serial camera data support link or differential data lane	I/O OD CMOS / O LVDS M-PHY	1.8V	PU 2.2K	MIPI-CSI 2.0 mode uses I2C_CAM_SCL MIPI-CSI 3.0 mode uses CSI_TX_P
CAM_PWR / GPIO_C_6	G3	Camera 0 Power Enable, active high output.	O CMOS	1.8V		

CAM_RST# / GPIO_C_7	G4	Camera 0 reset, active low output	O CMOS	1.8V		

Table 34: Size-S MIPI CSI

2.4.3.6 Parallel RGB Display

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
RGB_R0	Y7	Red data bit 0	O CMOS	3.3V		
RGB_R1	AA6	Red data bit 1	O CMOS	3.3V		
RGB_R2	Y6	Red data bit 2	O CMOS	3.3V		
RGB_R3	AA5	Red data bit 3	O CMOS	3.3V		
RGB_R4	Y5	Red data bit 4	O CMOS	3.3V		
RGB_R5	Y4	Red data bit 5	O CMOS	3.3V		
RGB_G0	W4	Green data bit 0	O CMOS	3.3V		
RGB_G1	V3	Green data bit 1	O CMOS	3.3V		
RGB_G2	V4	Green data bit 2	O CMOS	3.3V		
RGB_G3	U3	Green data bit 3	O CMOS	3.3V		
RGB_G4	T3	Green data bit 4	O CMOS	3.3V		
RGB_G5	T4	Green data bit 5	O CMOS	3.3V		
RGB_B0	R4	Blue data bit 0	O CMOS	3.3V		
RGB_B1	R3	Blue data bit 1	O CMOS	3.3V		
RGB_B2	P3	Blue data bit 2	O CMOS	3.3V		
RGB_B3	N3	Blue data bit 3	O CMOS	3.3V		
RGB_B4	N4	Blue data bit 4	O CMOS	3.3V		
RGB_B5	M3	Blue data bit 5	O CMOS	3.3V		

RGB_(PIXEL)CLK	M4	Pixel clock signal	O CMOS	3.3V		
RGB_VSYNC	L3	Vertical synch	O CMOS	3.3V		
RGB_HSYNC	K3	horizontal synch	O CMOS	3.3V		
RGB_DISP	K4	Display ON/OFF	O CMOS	3.3V		
RGB_DE	J4	Data Enable	O CMOS	3.3V		
RGB_RESET#	J3	Global Reset	O CMOS	3.3V		
RGB_CS#	H3	Chip select	O CMOS	3.3V		

Table 35: Size-S Parallel RGB Display

2.4.3.7 USB

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
USB_C_D_N	D11	USB differential data pairs for port C	I/O USB	USB		
USB_C_D_P	D10	USB differential data pairs for port C	I/O USB	USB		
USB_C_ID	D9	Input Contact to announce OTG device insertion on USB 2.0 port	I CMOS	3.3V		
USB_C_OC#	C8	USB over-current for port C	I OD CMOS	3.3V	PU 10k	
USB_C_VBUS	C9	USB port 0 port power detection	I USB VBUS 5V	USB VBUS 5V		
USB_C_EN	C10	Power enable for usb VBUS voltage	O CMOS	3.3V		
USB_C_SSTX_N	A9	Transmit signal differential pairs for SuperSpeed on port C	O USB SS	USB SS		AC coupled off module
USB_C_SSTX_P	A8	Transmit signal differential pairs for SuperSpeed on port C	O USB SS	USB SS		AC coupled off module
USB_C_SSRX_N	B11	Receive signal differential pairs for SuperSpeed on port C	I USB SS	USB SS		AC coupled off module
USB_C_SSRX_P	B10	Receive signal differential pairs for SuperSpeed on port C	I USB SS	USB SS		AC coupled off module

Table 36: Size-S UFS

2.4.3.8 PCIe

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
PCIe_A_HSI0_P	AB1	Differential PCIe link A receive data pair	I LVDS PCIE			AC coupled off module
PCIe_A_HSI0_N	AB2	Differential PCIe link A receive data pair	I LVDS PCIE			AC coupled off module
PCIe_A_HSO0_P	AC2	Differential PCIe link A transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_A_HSO0_N	AC3	Differential PCIe link A transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_A_PRSNT#	W2	PCIe Port A present input	I OD CMOS	3.3V	PU 10k	
PCIe_A_PERST#	V2	PCIe Port A reset output	O CMOS	3.3V		
PCIe_REFCLK_P	W1	Differential PCIe reference clock output	O LVDS PCIE			
PCIe_REFCLK_N	Y1	Differential PCIe reference clock output	O LVDS PCIE			
PCIe_WAKE#	T2	PCIe wake up interrupt to host – common to PCIe links A, B, C, D	I OD CMOS	3.3V	PU 10k	
PCIe_SMDAT	U1	System management I2C bus DATA	I/O OD CMOS	1.8V	PU 2k2	
PCIe_SMCLK	T1	System management I2C bus CLK	O OD CMOS	1.8V	PU 2k2	
PCIe_SM_ALERT#	R2	SMBus Alert# (interrupt) signal	I OD CMOS	1.8V	PU 2k2	

Table 37: Size-S PCIe

2.4.3.9 Reserved

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
RESERVED	N2, AA2	Reserved for future use				

Table 38: Size-S Reserved Contacts

2.4.3.10 Vendor Defined Contacts

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
Vendor Defined	C6, C7, D6, D7	Defined by module manufacturer				

Table 39: Size-S Vendor Defined Contacts

2.4.4 Size-M – Additional Functionality

2.4.4.1 Power Supply + Ground

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
VCC_7_TEST	AA33	Module power voltage testpoint	P			
VCC_8_TEST	B29	Module power voltage testpoint	P			
VCC_IN_5V	Y25, Y26, Y27, Y28	Module power input voltage of 5V	P			
GND	A26, A29, A32, B27, B28, B30, B33, C25, C32, C35, D28, D34, F33, F35, G34, H32, J33, J35, K34, M35, N34, T34, W34, AA25, AA26, AA27, AA28, AA32, AB28, AB31, AB34, AC27, AC30, AC33	Module Signal and power return and GND reference	P			

Table 40: Size-M Power + Ground

2.4.4.2 Ethernet / LAN

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
ETH_C_(R)(G)MII_CRS	AC34	Carrier Sense port C	I CMOS	1.8V/2.5V/3.3V		
ETH_C_(R)(G)MII_COL	AB35	Collision detect (half speed only) port C	I CMOS	1.8V/2.5V/3.3V		
ETH_C_(S)(R)(G)MII_TXD0	Y35	Transmit data bit 0 (transmitted first) port C	O CMOS	1.8V/2.5V/3.3V		_P when used as differential
ETH_C_(S)(R)(G)MII_TXD1	AA35	Transmit data bit 1 port C	O CMOS	1.8V/2.5V/3.3V		_N when used as differential
ETH_C_(R)(G)MII_TXD2	Y34	Transmit data bit 2 port C	O CMOS	1.8V/2.5V/3.3V		
ETH_C_(R)(G)MII_TXD3	AA34	Transmit data bit 3 port C	O CMOS	1.8V/2.5V/3.3V		
ETH_C_(R)(G)MII_TX_EN(_ER)	V34	Transmit enable (Error) port C	O CMOS	1.8V/2.5V/3.3V		
ETH_C_(R)(G)MII_TX_CLK	N35	Transmit clock port C	I/O CMOS	1.8V/2.5V/3.3V		
ETH_C_(S)(R)(G)MII_RXD0	V35	Receive data bit 0 (received first) port C	I CMOS	1.8V/2.5V/3.3V		_P when used as differential
ETH_C_(S)(R)(G)MII_RXD1	U35	Receive data bit 1 port C	I CMOS	1.8V/2.5V/3.3V		_N when used as differential
ETH_C_(R)(G)MII_RXD2	R35	Receive data bit 2 port C	I CMOS	1.8V/2.5V/3.3V		
ETH_C_(R)(G)MII_RXD3	P35	Receive data bit 3 port C	I CMOS	1.8V/2.5V/3.3V		
ETH_C_(R)(G)MII_RX_ER	U34	Receive error port C	I CMOS	1.8V/2.5V/3.3V		
ETH_C_(R)(G)MII_RX_DV(_ER)	T35	Receive data valid (Error) port C	I CMOS	1.8V/2.5V/3.3V		
ETH_C_(R)(G)MII_RX_CLK	W35	Receive clock port C	I/O CMOS	1.8V/2.5V/3.3V		
ETH_C_SDP	R34	Ethernet port C System Defined Contact	O CMOS	1.8V/2.5V/3.3V		

Table 41: Size-M Ethernet

2.4.4.3 GPIO

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
GPIO_D_0	U32	General purpose I/O Contact D0	I/O CMOS	1.8V		
GPIO_D_1	U33	General purpose I/O Contact D1	I/O CMOS	1.8V		
GPIO_D_2	V32	General purpose I/O Contact D2	I/O CMOS	1.8V		
GPIO_D_3	V33	General purpose I/O Contact D3	I/O CMOS	1.8V		
GPIO_D_4	W32	General purpose I/O Contact D4	I/O CMOS	1.8V		
GPIO_D_5	W33	General purpose I/O Contact D5	I/O CMOS	1.8V		
GPIO_D_6	Y32	General purpose I/O Contact D6	I/O CMOS	1.8V		
GPIO_D_7	Y33	General purpose I/O Contact D7	I/O CMOS	1.8V		

Table 42: Size-M GPIO

2.4.4.4 SPI

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
SPI_C_SDI	C29	SPI C Serial Data Input	I CMOS	1.8V		
SPI_C_SDO	D30	SPI C Serial Data Output	O CMOS	1.8V		
SPI_C_CS#	C30	SPI C Master Chip Select	O CMOS	1.8V		
SPI_C_SCK	D29	SPI C Serial Data Clock	O CMOS	1.8V		

Table 43: Size-M SPI

2.4.4.5 UFS

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
UFS_TX0_N	AC29	UFS differential output (point to point)	O LVDS UFS			
UFS_TX0_P	AC28	UFS differential output (point to point)	O LVDS UFS			
UFS_RX0_N	AC32	UFS differential input (point to point)	I LVDS UFS			
UFS_RX0_P	AC31	UFS differential input (point to point)	I LVDS UFS			
UFS_TX1_N	AB30	UFS differential output (point to point)	O LVDS UFS			
UFS_TX1_P	AB29	UFS differential output (point to point)	O LVDS UFS			
UFS_RX1_N	AB33	UFS differential input (point to point)	I LVDS UFS			
UFS_RX1_P	AB32	UFS differential input (point to point)	I LVDS UFS			
UFS_RESET#	AB27	UFS reset output	O CMOS	1.8V / 1.2V		USF 3.0 need 1.2V I/O level
UFS_CLK	AC26	UFS reference clock output	O CMOS	1.8V / 1.2 V		USF 3.0 need 1.2V I/O level

Table 44: Size-M UFS

2.4.4.6 USB

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
USB_D_D_N	D26	USB differential data pairs for port D	I/O USB	USB		
USB_D_D_P	D25	USB differential data pairs for port D	I/O USB	USB		
USB_D_ID	D27	Input Contact to announce OTG device insertion on USB 2.0 port	I CMOS	3.3V		
USB_D_OC#	C28	USB over-current for port D	I OD CMOS	3.3V	PU 10k	
USB_D_VBUS	C27	USB port 0 port power detection	I USB VBUS 5V	USB VBUS 5V		
USB_D_EN	C26	Power enable for usb VBUS voltage	O CMOS	3.3V		
USB_D_SSTX_N	A28	Transmit signal differential pairs for SuperSpeed on port D	O USB SS	USB SS		AC coupled off module
USB_D_SSTX_P	A27	Transmit signal differential pairs for SuperSpeed on port D	O USB SS	USB SS		AC coupled off module
USB_D_SSRX_N	B26	Receive signal differential pairs for SuperSpeed on port D	I USB SS	USB SS		AC coupled off module
USB_D_SSRX_P	B25	Receive signal differential pairs for SuperSpeed on port D	I USB SS	USB SS		AC coupled off module

Table 45: Size-M USB

2.4.4.7 PCIe

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
PCIe_B_HSI0_P	L34	Differential PCIe link B receive data pair	I LVDS PCIE			AC coupled off module
PCIe_B_HSI0_N	M34	Differential PCIe link B receive data pair	I LVDS PCIE			AC coupled off module
PCIe_B_HSO0_P	K35	Differential PCIe link B transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_B_HSO0_N	L35	Differential PCIe link B transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_B_PRSNT#	K33	PCIe Port B present input	I OD CMOS	3.3V	PU 10k	
PCIe_B_PERST#	L33	PCIe Port B reset output	O CMOS	3.3V		

Table 46: Size-M PCIe

2.4.4.8 eDP/eDP++

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
eDP_A_LANE0_P	A30	Primary 4-lane eDP differential pair data lines	O LVDS DP			AC coupled off module
eDP_A_LANE0_N	A31	Primary 4-lane eDP differential pair data lines	O LVDS DP			AC coupled off module
eDP_A_LANE1_P	B31	Primary 4-lane eDP differential pair data lines	O LVDS DP			AC coupled off module
eDP_A_LANE1_N	B32	Primary 4-lane eDP differential pair data lines	O LVDS DP			AC coupled off module
eDP_A_LANE2_P	A33	Primary 4-lane eDP differential pair data lines	O LVDS DP			AC coupled off module
eDP_A_LANE2_N	A34	Primary 4-lane eDP differential pair data lines	O LVDS DP			AC coupled off module
eDP_A_LANE3_P	B34	Primary 4-lane eDP differential pair data lines	O LVDS DP			AC coupled off module
eDP_A_LANE3_N	B35	Primary 4-lane eDP differential pair data lines	O LVDS DP			AC coupled off module
eDP_A_AUX_P	C33	Primary bidirectional channel used for link management and device control	I/O LVDS DP		PD 100k	AC coupled off module
eDP_A_AUX_N	C34	Primary bidirectional channel used for link management and device control	I/O LVDS DP		PD 100k	AC coupled off module
eDP_A_AUX_SEL	D32	Strapping signal to enable either HDMI or DP output	I CMOS	1.8V	PD 1M	Pulled to GND on Carrier for DP operation in Dual Mode (DP++) implementations. Driven to 1.8V on carrier for HDMI mode Module must tolerate high level in stand-by mode
eDP_A_BL_HPD	D33	Detection of Hot Plug / Unplug of primary eDP display and notification of the link layer.	I CMOS	1.8V	PD 1M	Module must tolerate high level in stand-by mode
eDP_A_BL_EN	D31	Primary panel backlight enable, active high	O CMOS	1.8V		

eDP_A_BL_PWM	C31	Primary panel brightness control through pulse width modulation	O CMOS	1.8V		
eDP_B_LANE0_P	D35	Secondary 4-lane eDP differential pair data lines	O LVDS DP			AC coupled off module
eDP_B_LANE0_N	E35	Secondary 4-lane eDP differential pair data lines	O LVDS DP			AC coupled off module
eDP_B_LANE1_P	E34	Secondary 4-lane eDP differential pair data lines	O LVDS DP			AC coupled off module
eDP_B_LANE1_N	F34	Secondary 4-lane eDP differential pair data lines	O LVDS DP			AC coupled off module
eDP_B_LANE2_P	G35	Secondary 4-lane eDP differential pair data lines	O LVDS DP			AC coupled off module
eDP_B_LANE2_N	H35	Secondary 4-lane eDP differential pair data lines	O LVDS DP			AC coupled off module
eDP_B_LANE3_P	H34	Secondary 4-lane eDP differential pair data lines	O LVDS DP			AC coupled off module
eDP_B_LANE3_N	J34	Secondary 4-lane eDP differential pair data lines	O LVDS DP			AC coupled off module
eDP_B_AUX_P	G33	Secondary bidirectional channel used for link management and device control	I/O LVDS DP		PD 100k	AC coupled off module
eDP_B_AUX_N	H33	Secondary bidirectional channel used for link management and device control	I/O LVDS DP		PD 100k	AC coupled off module
eDP_B_AUX_SEL	F32	Auxilary Selection	I CMOS	1.8V	PD 1M	Pulled to GND on Carrier for DP operation in Dual Mode (DP++) implementations. Driven to 1.8V on carrier for HDMI mode Module must tolerate high level in stand-by mode
eDP_B_BL_HPD	G32	Detection of Hot Plug / Unplug of secondary eDP display and notification of the link layer.	I CMOS	1.8V	PD 1M	Module must tolerate high level in stand-by mode
eDP_B_BL_EN	E32	Secondary panel backlight enable, active high	O CMOS	1.8V		

eDP_B_BL_PWM	E33	Secondary panel brightness control through pulse width modulation	O CMOS	1.8V		

Table 47: Size-M eDP

2.4.4.9 Reserved

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
RESERVED	J32, K32, L32, M32, M33, N32, N33, P32, P33, P34, R32, R33, T32, T33, AB25, AB26	Reserved for future use				

Table 48: Size-M Reserved Contacts

2.4.4.10 Vendor Defined Contacts

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
Vendor Defined	Y29, Y30, Y31, AA29, AA30, AA31	Defined by module manufacturer				

Table 49: Size-M Vendor Defined Contacts

2.4.5 Size-L – Additional Functionality

2.4.5.1 Power Supply + Ground

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
VCC_IN_5V	AE4, AF4, AG4, AH3, AH4, AJ3, AJ4, AK4	Module power input voltage of 5V	P			
GND	AE2, AE34, AF35, AG3, AH2, AH34, AJ35, AK3, AL2, AL34, AM13, AM16, AM19, AM22, AM35, AN3, AN6, AN9, AN11, AN15, AN18, AN21, AN33, AP2, AP5, AP8, AP13, AP16, AP19, AP22, AP25, AP28, AP31, AP34, AR14, AR17, AR20, AR26, AR29, AR32	Module Signal and power return and GND reference	P			

Table 50: Size-L Power + Ground

2.4.5.2 Ethernet / LAN

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
ETH_D_(R)(G)MII_CRS	AE3	Carrier Sense port D	I CMOS	1.8V/2.5V/3.3V		
ETH_D_(R)(G)MII_COL	AF3	Collision detect (half speed only) port D	I CMOS	1.8V/2.5V/3.3V		
ETH_D_(S)(R)(G)MII_TXD0	AF1	Transmit data bit 0 (transmitted first) port D	O CMOS	1.8V/2.5V/3.3V		_P when used as differential
ETH_D_(S)(R)(G)MII_TXD1	AG1	Transmit data bit 1 port D	O CMOS	1.8V/2.5V/3.3V		_N when used as differential
ETH_D_(R)(G)MII_TXD2	AG2	Transmit data bit 2 port D	O CMOS	1.8V/2.5V/3.3V		
ETH_D_(R)(G)MII_TXD3	AF2	Transmit data bit 3 port D	O CMOS	1.8V/2.5V/3.3V		
ETH_D_(R)(G)MII_TX_EN(_ER)	AJ2	Transmit enable (Error) port D	O CMOS	1.8V/2.5V/3.3V		
ETH_D_(R)(G)MII_TX_CLK	AH1	Transmit clock port D	I/O CMOS	1.8V/2.5V/3.3V		
ETH_D_(S)(R)(G)MII_RXD0	AJ1	Receive data bit 0 (received first) port D	I CMOS	1.8V/2.5V/3.3V		_P when used as differential
ETH_D_(S)(R)(G)MII_RXD1	AK1	Receive data bit 1 port D	I CMOS	1.8V/2.5V/3.3V		_N when used as differential
ETH_D_(R)(G)MII_RXD2	AM1	Receive data bit 2 port D	I CMOS	1.8V/2.5V/3.3V		
ETH_D_(R)(G)MII_RXD3	AN1	Receive data bit 3 port D	I CMOS	1.8V/2.5V/3.3V		
ETH_D_(R)(G)MII_RX_ER	AK2	Receive error port D	I CMOS	1.8V/2.5V/3.3V		
ETH_D_(R)(G)MII_RX_DV(_ER)	AL1	Receive data valid (Error) port D	I CMOS	1.8V/2.5V/3.3V		
ETH_D_(R)(G)MII_RX_CLK	AP1	Receive clock port D	I/O CMOS	1.8V/2.5V/3.3V		
ETH_D_SDP	AM2	Ethernet port D System Defined Contact	O CMOS	1.8V/2.5V/3.3V		
ETH_E_(R)(G)MII_CRS	AN4	Carrier Sense port E	I CMOS	1.8V/2.5V/3.3V		

ETH_E_(R)(G)MII_COL	AR2	Collision detect (half speed only) port E	I CMOS	1.8V/2.5V/3.3V		
ETH_E_(S)(R)(G)MII_TXD0	AR3	Transmit data bit 0 (transmitted first) port E	O CMOS	1.8V/2.5V/3.3V		_P when used as differential
ETH_E_(S)(R)(G)MII_TXD1	AR4	Transmit data bit 1 port E	O CMOS	1.8V/2.5V/3.3V		_N when used as differential
ETH_E_(R)(G)MII_TXD2	AP3	Transmit data bit 2 port E	O CMOS	1.8V/2.5V/3.3V		
ETH_E_(R)(G)MII_TXD3	AP4	Transmit data bit 3 port E	O CMOS	1.8V/2.5V/3.3V		
ETH_E_(R)(G)MII_TX_EN(_ER)	AP6	Transmit enable (Error) port E	O CMOS	1.8V/2.5V/3.3V		
ETH_E_(R)(G)MII_TX_CLK	AR5	Transmit clock port E	I/O CMOS	1.8V/2.5V/3.3V		
ETH_E_(S)(R)(G)MII_RXD0	AR6	Receive data bit 0 (received first) port E	I CMOS	1.8V/2.5V/3.3V		_P when used as differential
ETH_E_(S)(R)(G)MII_RXD1	AR7	Receive data bit 1 port E	I CMOS	1.8V/2.5V/3.3V		_N when used as differential
ETH_E_(R)(G)MII_RXD2	AR9	Receive data bit 2 port E	I CMOS	1.8V/2.5V/3.3V		
ETH_E_(R)(G)MII_RXD3	AR10	Receive data bit 3 port E	I CMOS	1.8V/2.5V/3.3V		
ETH_E_(R)(G)MII_RX_ER	AP7	Receive error port E	I CMOS	1.8V/2.5V/3.3V		
ETH_E_(R)(G)MII_RX_DV(_ER)	AR8	Receive data valid (Error) port E	I CMOS	1.8V/2.5V/3.3V		
ETH_E_(R)(G)MII_RX_CLK	AN10	Receive clock port E	I/O CMOS	1.8V/2.5V/3.3V		
ETH_E_SDP	AP9	Ethernet port E System Defined Contact	O CMOS	1.8V/2.5V/3.3V		

Table 51: Size-L Ethernet

2.4.5.3 GPIO

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
GPIO_E_0	AF32	General purpose I/O Contact E0	I/O CMOS	1.8V		
GPIO_E_1	AF33	General purpose I/O Contact E1	I/O CMOS	1.8V		
GPIO_E_2	AG32	General purpose I/O Contact E2	I/O CMOS	1.8V		
GPIO_E_3	AG33	General purpose I/O Contact E3	I/O CMOS	1.8V		
GPIO_E_4	AH32	General purpose I/O Contact E4	I/O CMOS	1.8V		
GPIO_E_5	AH33	General purpose I/O Contact E5	I/O CMOS	1.8V		
GPIO_E_6	AJ32	General purpose I/O Contact E6	I/O CMOS	1.8V		
GPIO_E_7	AJ33	General purpose I/O Contact E7	I/O CMOS	1.8V		

Table 52: Size-L GPIO

2.4.5.4 LVDS – Display Interface

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
LVDS_I2C_CLK	AM11	DDC clock line used for flat panel detection and control	O OD CMOS	1.8V	PU 2k2	
LVDS_I2C_DAT	AM12	DDC data line used for flat panel detection and control	I/O OD CMOS	1.8V	PU 2k2	
LVDS_VDD_EN	AN14	LVDS channel power enable, active high	O CMOS	1.8V		
LVDS_BL_PWM	AN22	LVDS channel brightness control through pulse width modulation	O CMOS	1.8V		
LVDS_BL_EN	AN23	LVDS channel backlight enable, active high	O CMOS	1.8V		
LVDS_A_CLK_P	AN13	LVDS channel A differential pair clock lines	O LVDS LCD			
LVDS_A_CLK_N	AN12	LVDS channel A differential pair clock lines	O LVDS LCD			
LVDS_A_LANE0_P	AP18	LVDS channel A differential pair data lines	O LVDS LCD			
LVDS_A_LANE0_N	AP17	LVDS channel A differential pair data lines	O LVDS LCD			
LVDS_A_LANE1_P	AR16	LVDS channel A differential pair data lines	O LVDS LCD			
LVDS_A_LANE1_N	AR15	LVDS channel A differential pair data lines	O LVDS LCD			
LVDS_A_LANE2_P	AP15	LVDS channel A differential pair data lines	O LVDS LCD			
LVDS_A_LANE2_N	AP14	LVDS channel A differential pair data lines	O LVDS LCD			
LVDS_A_LANE3_P	AP12	LVDS channel A differential pair data lines	O LVDS LCD			
LVDS_A_LANE3_N	AP11	LVDS channel A differential pair data lines	O LVDS LCD			
LVDS_B_CLK_P	AN17	LVDS channel B differential pair clock lines	O LVDS LCD			
LVDS_B_CLK_N	AN16	LVDS channel B differential pair clock lines	O LVDS LCD			

LVDS_B_LANE0_P	AM21	LVDS channel B differential pair data lines	O LVDS LCD			
LVDS_B_LANE0_N	AM20	LVDS channel B differential pair data lines	O LVDS LCD			
LVDS_B_LANE1_P	AN20	LVDS channel B differential pair data lines	O LVDS LCD			
LVDS_B_LANE1_N	AN19	LVDS channel B differential pair data lines	O LVDS LCD			
LVDS_B_LANE2_P	AM18	LVDS channel B differential pair data lines	O LVDS LCD			
LVDS_B_LANE2_N	AM17	LVDS channel B differential pair data lines	O LVDS LCD			
LVDS_B_LANE3_P	AM15	LVDS channel B differential pair data lines	O LVDS LCD			
LVDS_B_LANE3_N	AM14	LVDS channel B differential pair data lines	O LVDS LCD			

Table 53: Size-L LVDS

2.4.5.5 PCIe x4

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
PCIe_C_HSI0_P	AP33	Differential PCIe link C receive data pair	I LVDS PCIE			AC coupled off module
PCIe_C_HSI0_N	AP32	Differential PCIe link C receive data pair	I LVDS PCIE			AC coupled off module
PCIe_C_HSO0_P	AR34	Differential PCIe link C transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_C_HSO0_N	AR33	Differential PCIe link C transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_C_HSI1_P	AN35	Differential PCIe link C receive data pair	I LVDS PCIE			AC coupled off module
PCIe_C_HSI1_N	AP35	Differential PCIe link C receive data pair	I LVDS PCIE			AC coupled off module
PCIe_C_HSO1_P	AM34	Differential PCIe link C transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_C_HSO1_N	AN34	Differential PCIe link C transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_C_HSI2_P	AK35	Differential PCIe link C receive data pair	I LVDS PCIE			AC coupled off module
PCIe_C_HSI2_N	AL35	Differential PCIe link C receive data pair	I LVDS PCIE			AC coupled off module
PCIe_C_HSO2_P	AJ34	Differential PCIe link C transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_C_HSO2_N	AK34	Differential PCIe link C transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_C_HSI3_P	AG35	Differential PCIe link C receive data pair	I LVDS PCIE			AC coupled off module
PCIe_C_HSI3_N	AH35	Differential PCIe link C receive data pair	I LVDS PCIE			AC coupled off module
PCIe_C_HSO3_P	AF34	Differential PCIe link C transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_C_HSO3_N	AG34	Differential PCIe link C transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_C_PRSNT#	AE32	PCIe Port C present input	I OD CMOS	3.3V	PU 10k	

PCIe_C_PERST#	AE33	PCIe Port C reset output	O CMOS	3.3V		
PCIe_D_HSI0_P	AR19	Differential PCIe link D receive data pair	I LVDS PCIE			AC coupled off module
PCIe_D_HSI0_N	AR18	Differential PCIe link D receive data pair	I LVDS PCIE			AC coupled off module
PCIe_D_HSO0_P	AP21	Differential PCIe link D transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_D_HSO0_N	AP20	Differential PCIe link D transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_D_HSI1_P	AR22	Differential PCIe link D receive data pair	I LVDS PCIE			AC coupled off module
PCIe_D_HSI1_N	AR21	Differential PCIe link D receive data pair	I LVDS PCIE			AC coupled off module
PCIe_D_HSO1_P	AP24	Differential PCIe link D transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_D_HSO1_N	AP23	Differential PCIe link D transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_D_HSI2_P	AP27	Differential PCIe link D receive data pair	I LVDS PCIE			AC coupled off module
PCIe_D_HSI2_N	AP26	Differential PCIe link D receive data pair	I LVDS PCIE			AC coupled off module
PCIe_D_HSO2_P	AR28	Differential PCIe link D transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_D_HSO2_N	AR27	Differential PCIe link D transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_D_HSI3_P	AP30	Differential PCIe link D receive data pair	I LVDS PCIE			AC coupled off module
PCIe_D_HSI3_N	AP29	Differential PCIe link D receive data pair	I LVDS PCIE			AC coupled off module
PCIe_D_HSO3_P	AR31	Differential PCIe link D transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_D_HSO3_N	AR30	Differential PCIe link D transmit data pair	O LVDS PCIE			AC coupled off module
PCIe_D_PRSNT#	AN31	PCIe Port D present input	I OD CMOS	3.3V	PU 10k	
PCIe_D_PERST#	AN32	PCIe Port D reset output	O CMOS	3.3V		

Table 54: Size-L PCIe x4

2.4.5.6 Reserved

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
RESERVED	AL3, AL4, AM3, AM4, AM5, AM6, AM7, AM8, AM9, AM10, AM23, AM24, AM25, AM26,AM27, AM28, AM29, AM30, AM31, AN2, AN5, AN7, AN8, AN24, AN25, AN26, AN27, AN28, AN29, AN30, AP10	Reserved for future use				

Table 55: Size-L Reserved Contacts

2.4.5.7 Vendor Defined Contacts

Contact Name	Contact Acronym	Functional Description	I/O Type	I/O Level	PU / PD	Comments
Vendor Defined	AK32, AK33, AL32, AL33, AM32, AM33	Defined by module manufacturer				

Table 56: Vendor Defined Contacts

2.5 Module Designation

All modules adhering to the Open Standard Module™ Specification **shall** use a consistent and unique designator describing size and height of the Module. This designator **shall** be used together with the vendor's and module name of the Open Standard Module™.

The Open Standard Module™ designator consists of the prefix "OSM-" combined with two further letters/characters describing size and height of the module.

[vendor's name] [module name] **OSM-[module size][module height]**

The following examples illustrate the designator for Open Standard Modules™:

- **OSM-0F**: OSM™ module with Size-0 "Zero" and Height "Flat"
- **OSM-SE**: OSM™ module with Size-S "Small" and Height "Extended"
- **OSM-LE**: OSM™ module with Size-L "Large" and Height "Extended"

2.6 Packing and Production Technologies

2.6.1 Packing Method

All modules adhering to the Open Standard Module™ Specification **should** be packed and stored in a pre-defined SMD tape / reel or JEDEC tray, as shown for example below:

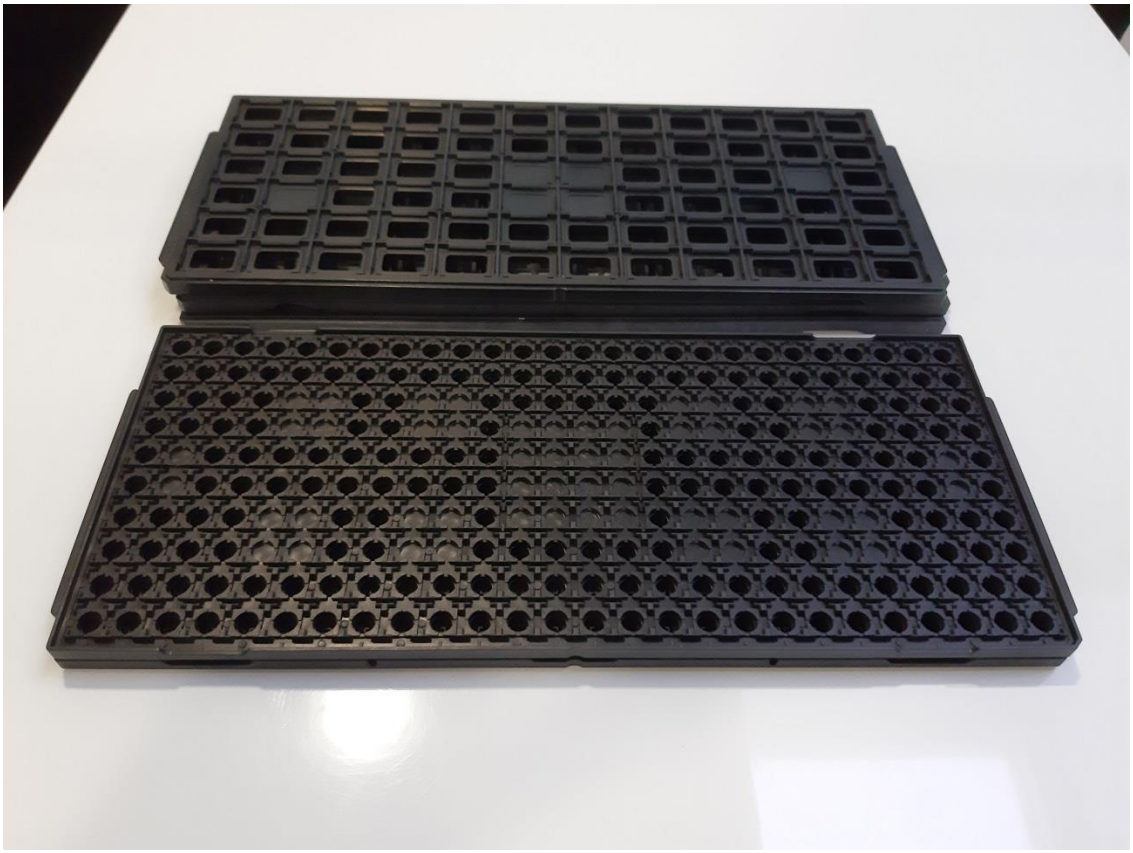


Figure 27: JEDEC Tray

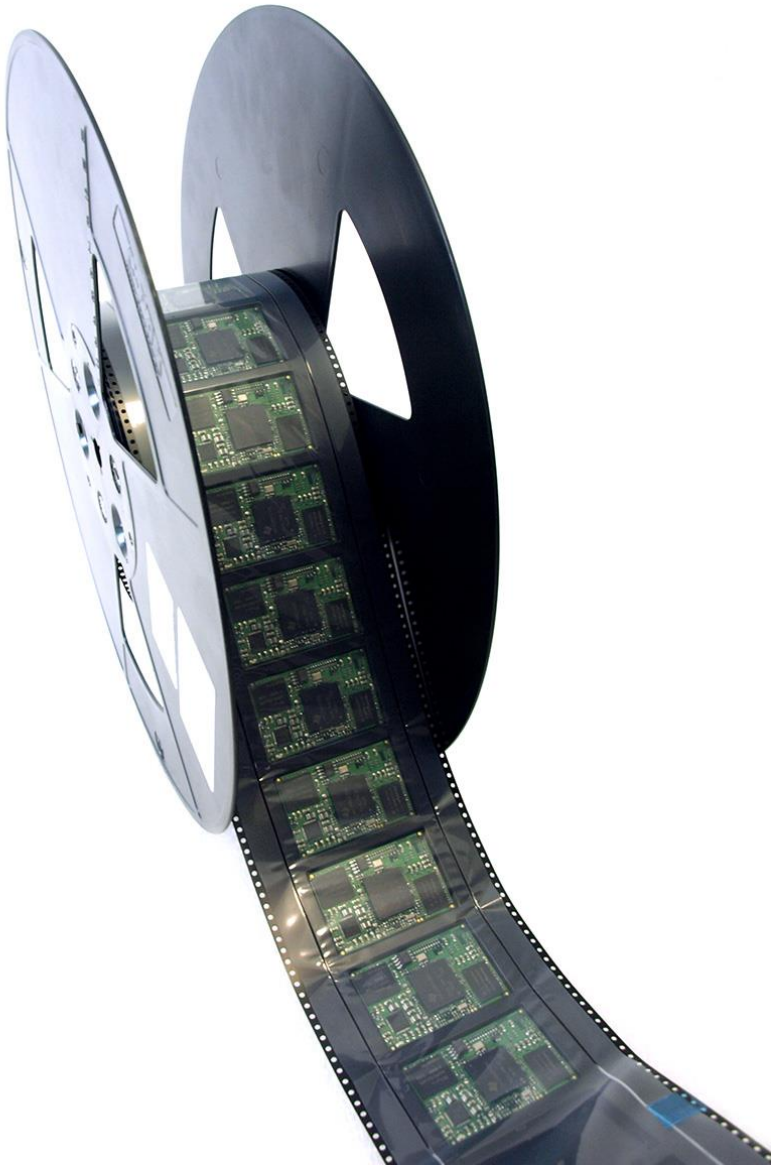


Figure 28: Reel

2.6.2 Handling Instruction

For all modules adhering to the Open Standard Module™ Specification the vendor **shall** provide a detailed set of information regarding the subsequent handling process, such as

- Carrier board pad design
- Processing
- Packaging Notes

It is recommended to use following draft for the module's documentation

Subject

In the following processing recommendations for the xxxxx[1] are given.

Design

Carrier board pad design

The terminal pad size should be Ø xx mm, like the pad size of the Module. The pitch is xx mm.

(detailed drawing)

Stencil layout for paste print

The paste should be printed with a stencil thickness of xx µm.

The breakthroughs have to be square (xx mm edge length, xx µm corner radius).

It is recommended to use the solder paste as on the pre-soldered contact pads of the Module: Type of Solder past

Processing

Storage

The Module is sensitive to humidity

The Module are delivered in suitable packaging including dry bag.

The storage time of the Module is limited to xx hours at max. +xx °C and max. xx % relative humidity, when the package is opened.

It is not recommended to repeat drying procedures.

Assembly

The xxxxxx are assembled from the carrier tape (see packaging notes).

The Module has to be picked up eccentrically in the middle of component xxx

(drawing of pick and place pattern)

The pickup tool has to be selected according to the following table:

Dimensions	Outer diameter (mm)
Minimum	xx.x
Recommended	xx.x
Maximum	xx.x

[1] All marked "x", are for reference only and should be replaced appropriately

Reflow soldering

The reflow profile shown as follows corresponds to the measurement at the soldering balls in the middle of the.

Drawing of an reflow profile

The Module may only be soldered using a reflow process as described above.

Packaging notes

The modules are delivered in a carrier tape with a packaging unit of xxxx pieces.

The following illustration shows the carrier tape specification.

(drawing of tape or tray)

3 SOFTWARE

Key to success is a breadth of software support, ranging from Bootloader to Operating Systems and API support as well as for security. One of the goals of Open Standard Module™ Specification is to attract market-leaders as well as rising stars who deliver feel-good software-solutions for a broad range of applications and scopes.

All modules adhering to the Open Standard Module™ specification **shall** provide at least one opensource software environment including the following components:

- Bootloader
- Operating System
- APIs
- Others

The complete open-source software environment **shall** be published in a joint/common open Git repository (i.e. github.com).

4 ACCESSORIES

4.1 Evaluation Carrier Board

All modules adhering to the Open Standard Module™ Specification **shall** utilize a standardized OSM™ Evaluation Carrier Board, providing access to all predefined features for the predefined sizes.
Ideally this Evaluation Carrier Board is designed and produced by one member of the SGET Standardization group.

4.2 Cooling solution

All modules adhering to the Open Standard Module™ Specification **may** utilize a standardized cooling interface and concept.

There will be a recommendation of a mounting hole pattern in the upcoming Design Guide.

5 CERTIFICATION / COMPLIANCE

All modules adhering to the Open Standard Module™ Specification **shall** fulfill the regional required Conformity Declarations.

6 APPENDIX

6.1 Abbreviations

Abbreviation	Description
SGET	Standardization Group for Embedded Technologies e.V.
OSB	Open Standard Module
PCB	Printed Circuit Board
LAN	Local Area Network
LVDS	Low Voltage Differential Signaling
USB	Universal Serial Bus
I2C	Inter Integrated Circuit Interface
I2S	Inter-IC Sound Interface
PDM	Pulse Density Modulation
PWM	Pulse Width Modulation
CAN	Controller Area Network
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter
PCIe	Peripheral Component Interconnect Express
GPIO	General Purpose Input Output
eDP	Embedded DisplayPort

Table 57: Abbreviations