



# **PCI/104-Express™ & PCIe/104™ Specification**

**Including Adoption on  
104™, EPIC™ and EBX™ Form Factors**

**Version 1.0**

**March 24, 2008**

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## Glossary of Terms

| Terms         | Definitions                                                                                                                                                                                                                                       |
|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ATX           | Advanced Technology Extended<br>A specification for PC motherboards, power supplies, and system chassis. One of its most notable features is support for “Standby” and “Soft-Off” power savings modes.                                            |
| Device        | A logical device attached to a PCIe Link. Generally an add-in card.                                                                                                                                                                               |
| DMA           | Direct Memory Access<br>A method for peripherals to efficiently access system memory without CPU intervention.                                                                                                                                    |
| EBX           | Form factor for SBC’s                                                                                                                                                                                                                             |
| Host          | The central connection of a PCIe system, typically a CPU module. This is called the “Root Complex” by the PCIe specification.                                                                                                                     |
| ISA Bus       | Industry Standard Architecture<br>A legacy bus used on earlier PCs. It has been phased out of desktop PCs, but is still common in embedded systems.                                                                                               |
| Lane          | Fundamental unit of a PCI Express connection. A set of differential signal pairs, one pair for transmission, and one pair for reception. Multiple lanes may be combined to increase bandwidth (up to x16). A “by-N Link” is comprised of N Lanes. |
| Link          | The collection of one or more PCI Express Lanes, plus an additional differential pair for a clock, which make up a standard PCI Express interconnect. According to PCI Express Specification 1.1 a Link can be comprised of 1, 4, 8, or 16 Lanes. |
| Packet Switch | A device used to attach multiple PCIe devices to a single link on the HOST. The PCIe Specification refers to this simply as a “Switch.” In this document, the term “Packet Switch” is used to differentiate from a “Signal Switch.”               |
| PCIe          | PCI Express                                                                                                                                                                                                                                       |
| PEG           | PCI Express Graphics                                                                                                                                                                                                                              |
| SBC           | Single Board Computer                                                                                                                                                                                                                             |
| SDVO          | Serial Digital Video Output used from Intel 915/945/965 chipsets                                                                                                                                                                                  |
| Signal Switch | An analog switch used to select between multiple PCIe devices to attach to a single PCIe link, or multiple links to attach to a single device. Also called a “Channel Switch.”                                                                    |

## 1. INTRODUCTION

### 1.1. Purpose

This document defines the addition of PCI Express, the next generation serial interconnect bus, to the stackable 104, EPIC, and EBX form factors. PCI Express was chosen because of its performance, scalability, wide market acceptance, and growing silicon availability worldwide. The PCI Express architecture uses familiar software and configuration interfaces of the conventional PCI bus architecture, but provides a new high-performance physical interface while retaining software compatibility with the existing conventional PCI infrastructure.

PCI Express is a high performance I/O architecture used in both desktop and mobile applications. This hierarchical, point-to-point interconnect works well with on-board and slot oriented architectures. The purpose of this Specification is to adapt PCI Express to the stacked architecture employed with 104, EPIC and EBX form factors.

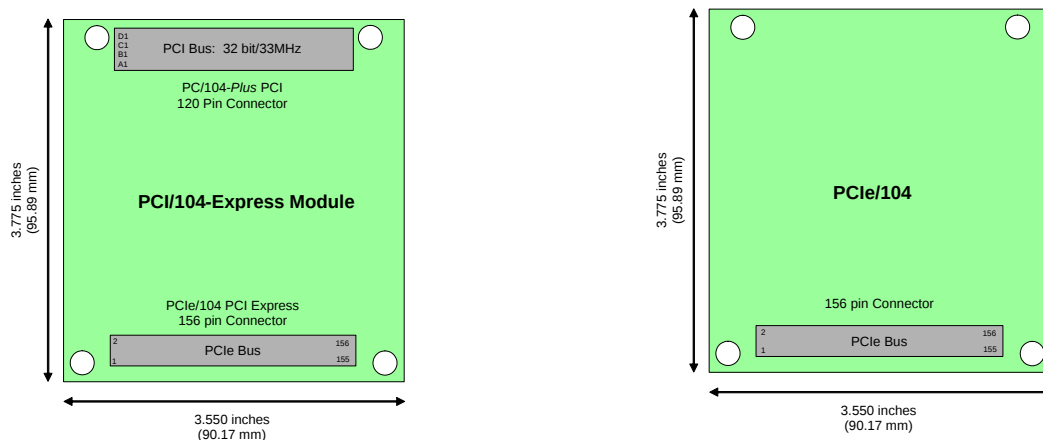
### 1.2. Standard Identification

A PCI-104 board with the addition of PCI Express becomes PCI/104-Express. A board with only the PCI Express connector is called PCIe/104. Each of these configurations can be applied to EPIC and EBX as shown in Appendix B and C. This allows full interchangeability with add-in Devices.

### 1.3. Description

As computer technology continues to develop, the PC/104 community must expand to the new, widely accepted technologies of today. Currently we are seeing the introduction of PCI Express (PCIe) into the mainstream computer market. Therefore, the PC/104 platform must be promoted with a connector architecture that provides a high-speed interface, maintains the ability to develop low-cost modules, and is sustainable for the foreseeable future.

PCI/104-Express meets these needs with a stackable PCIe connector for both up and down stacking, and retains the stackable PCI connector for backward compatibility to PCI-104, PC/104-Plus, and PC/104 peripheral modules. Figure 1-1 shows a basic view of the PCI/104-Express and PCIe/104 layouts.



**Figure 1-1: PCI/104-Express and PCIe/104 Board Layouts on 104 Form Factor**

ISA bus backward compatibility can naturally and easily be achieved with the use of a PCI-to-ISA bridge peripheral module (see Appendix A).

PCI/104-Express has the following features:

Connector A: PCI Express Bus

- Four x1 PCIe Links
- One x16 PCIe Link, or optionally two x8 Links, two x4 PCIe Links, or two SDVO
- ATX power and control signals: +5V Standby, Power supply on, Power OK
- Power: +3.3V, +5V, +12V
- SMBus

Connector B: PCI Bus:

- PCI Bus: 32 bit, 33 MHz, Four Bus Master capable (same as on PC/104-*Plus* and & PCI-104)
- +5V Standby, Power supply on, and power management event signals for ATX power supply
- Power: +3.3V, +5V, +12V, -12V

PCIe/104 has the following features:

Connector A: PCI Express Bus

- Four x1 PCIe Links
- One x16 PCIe Link, or optionally two x8 Links, two x4 PCIe Links, or two SDVO
- ATX power and control signals: +5V Standby, Power supply on, Power OK
- Power: +3.3V, +5V, +12V
- SMBus

## **1.4. Bus and Signal Group Descriptions**

### **1.4.1 PCI Express Expansion Bus**

PCI/104-Express and PCIe/104 incorporate four x1 PCI Express Links and options for either a single x16 Link, or two x8 Links, or two x4 PCIe Links to allow connections to standard PCI Express device chips. The x16 Link option allows maximum flexibility, configurability, and expandability for current and future designs. Some examples of x16 Link application are next generation graphics chips, gigabit Ethernet chips, or use with a PCI Express Switch which can then branch the high throughput out into any number of various size Links including multiple x16 Link graphics engines. The only limitation is the bandwidth requirement for each of the branched links.

PCI Express is a high performance, general purpose I/O interconnect defined for a wide variety of future computing and communication platforms. Key PCI attributes, such as its usage model, load-store architecture, and software interfaces, are maintained, whereas its parallel bus implementation is replaced by a highly scalable, fully serial interface. PCI Express takes advantage of recent advances in point-to-point interconnects, Switch-based technology, and packet-protocol to deliver new levels of performance and features. Power Management, Quality of Service (QoS), Hot-Plug/Hot-Swap support, Data Integrity, and Error Handling are among some of the advanced features supported by PCI Express.

#### **1.4.1.1 PEG Link**

PEG (PCI Express for Graphics) is a graphic interface with 16 differential lanes to connect a high performance video controller. Most of today's chipsets support the PEG bus. In such chipsets with internal graphics, the PEG bus is used as an alternative to connect an external video controller. The internal chip controller is disabled in this case. The PEG-Bus configuration must be enabled from the Device by connecting the PEG-ENA# signal to ground. For SDVO-applications, the PEG-ENA# remains open.

### **1.4.2 SDVO Links**

Serial Digital Video Output is the interface for up to two LVDS/DVI controllers on a chipset with internal graphics controller. This bus is normally provided as an alternative to the PEG-Bus. SDVO-Links needs up to 7 differential signal pairs per interface.

### **1.4.3 PCI Expansion Bus**

The PCI Expansion Bus is the same 32 bit, 33 MHz PCI bus found on the PC/104-*Plus* and PCI-104 Specifications with the addition of +5V\_SB, PSON#, and PME#.

### **1.4.4 System Management Bus**

The optional System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate with each other and with the rest of the system. It is based on the principles of operation of I2C. SMBus provides a control bus for system- and power-management related tasks. A system may use SMBus to pass messages to and from devices instead of tripping individual control lines. Removing the individual control lines reduces pin count. Accepting messages ensures future expandability. With SMBus, a device can provide manufacturer information, tell the system what its model/part number is, save its state for a suspended event, report different types of errors, accept control parameters, and return its status. SMBus is described in System Management Bus (SMBus) Specification, Version 2.0. Refer to this specification for DC characteristics and all AC timings. If the system board or add-in card supports SMBus, it must adhere to additional requirements that may be found in Chapter 8 of the PCI Local Bus Specification, Revision. 3.0.

An address resolution protocol (ARP) is defined in the SMBus 2.0 Specification that is used to assign slave addresses to SMBus devices. Although optional in the SMBus 2.0 Specification, it is required that systems that connect the SMBus to PCI slots implement ARP for assignment of SMBus slave addresses to SMBus interface devices on PCI add-in cards. The system must execute ARP on a logical SMBus whenever any PCI bus segment associated with the logical SMBus exits the B3 state or a device in an individual slot associated with the logical

SMBus exits the D3cold state. Prior to executing ARP, the system must insure that all ARP-capable SMBus interface devices are returned to their default address state.

The system board provides pull-ups to the +3.3Vaux rail per the above specification and the components attached to these signals need to have a 3.3V signaling tolerance (5V signaling must not be used). Also, the SMBus is used during all power states, so all components attached to the SMBus must remain powered during standby, or ensure that the bus is not pulled down when not powered.

The SMBus interface is based upon the System Management Bus Specification (SMBus 2.0 Specification). This two-wire serial interface has low power and low software overhead characteristics that make it well suited for low-bandwidth system management functions.

The capabilities enabled by the SMBus interface include, but are not limited to, the following:

- Support for client management technologies.
- Support for server management technologies.
- Support for thermal sensors and other instrumentation devices on add-in cards.
- Add-in card identification when the bus is in the B3 state or when the PCI device is in the D3hot or D3cold states as defined in the PCI Power Management Interface Specification.

#### **1.4.5 ATX and Power Management**

PCI/104-Express and PCIe/104 incorporate all of the necessary control and signal lines for ATX and power management functionalities. These signals include PWR\_OK, PSON#, +5V\_SB, and PME#. The inclusion of these signals allows maximum power savings.

PWR\_OK is a “power good” signal. It should be asserted high by the power supply to indicate that the +12 VDC, +5 VDC, and +3.3 VDC outputs are above the under-voltage thresholds and that sufficient main energy is stored by the converter to guarantee continuous power operation within specifications. Conversely, PWR\_OK should be de-asserted to a low state when any of the +12 VDC, +5 VDC, or +3.3 VDC output voltages falls below its under-voltage threshold, or when main-power has been removed for a sufficiently long enough time that the power supply operation cannot be guaranteed beyond the power-down warning time.

PSON# is an active-low, TTL-compatible signal that allows a motherboard to remotely control the power supply in conjunction with features such as soft on/off, Wake-on-LAN, or wake-on-modem. When PSON# is pulled to TTL low, the power supply should turn on the five main DC output rails: +12 VDC, +5 VDC, +3.3 VDC, -5 VDC, and -12 VDC. When PSON# is pulled to TTL high or open-circuited, the DC output rails should not deliver current and should be held at zero potential with respect to ground. PSON# has no effect on the +5 VSB output, which is always enabled whenever AC power is present.

+5V\_SB is a standby supply output that is active whenever AC power is present. It provides a power source for circuits that must remain operational when the five main DC output rails are in a disabled state. Example uses include soft power control, Wake-on-LAN, wake-on-modem, intrusion detection, or suspend state activities.

### **1.5. References**

The following documents should be used as reference for a detailed understanding of the overall system requirements. For latest revisions of the above specifications contact the respective organizations.

|                                             |                                   |                                                    |
|---------------------------------------------|-----------------------------------|----------------------------------------------------|
| PC/104 Specification                        | <b>PC/104 Embedded Consortium</b> | <a href="http://www.pc104.org">www.pc104.org</a>   |
| PC/104-Plus Specification                   | <b>PC/104 Embedded Consortium</b> | <a href="http://www.pc104.org">www.pc104.org</a>   |
| PCI-104 Specification                       | <b>PC/104 Embedded Consortium</b> | <a href="http://www.pc104.org">www.pc104.org</a>   |
| PCI Local Bus Specification Revision 2.2    | <b>PCI Special Interest Group</b> | <a href="http://www.pcisig.com">www.pcisig.com</a> |
| PCI Express Base Specification Revision 1.1 | <b>PCI Special Interest Group</b> | <a href="http://www.pcisig.com">www.pcisig.com</a> |

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|                                                                  |                               |                                                          |
|------------------------------------------------------------------|-------------------------------|----------------------------------------------------------|
| ATX Specification Version 2.2                                    | <b>Intel Corporation</b>      | <a href="http://www.intel.com">www.intel.com</a>         |
| System Management Bus (SMBus)<br>Specification Version 2.0       | <b>SBS Implementers Forum</b> | <a href="http://www.sbs-forum.org">www.sbs-forum.org</a> |
| INTEL description of PEG and SDVO in the<br>915/945/965 chipsets | <b>Intel</b>                  | <a href="http://www.intel.com">www.intel.com</a>         |

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## 2. EXPANSION CONNECTOR A

### 2.1. Functions

- Four x1 PCI Express Links
- One x16 PCI Express Link, can be configured as two x8 PCI Express Links, two x4 PCI Express Links, or two SDVO
- ATX power and control signals
- Power: +3.3V, +5 Volts, +12 Volts, +5 Volts Standby
- System Management Bus (SMBus)

Because not all chipsets support all PCI Express link configurations, it is up the Host manufacturer to determine the type and number of PCI Express Links to include in their expansion connector. However, the placement of these PCI Express Links must comply with the pin out described below for Connector A. This will ensure that any x1 or x4 or x8 or x16 PCI Express Device will work on any Host that has an x1, or x4 or x8, or x16, respectively.

### 2.2. Signal Descriptions

**Table 2-1 Connector A Signals: PCI Express and Others**

| Group                              | Pins | Signal Name      | Host Direction | Description                                                                                                                   |
|------------------------------------|------|------------------|----------------|-------------------------------------------------------------------------------------------------------------------------------|
| x1<br>PCIe Links                   | 4    | PEx1 [0:3]Tp     | Output         | <b>Transmit Differential Upper Line</b> for x1 Links 0, 1, 2, 3. Shifted when used.                                           |
|                                    | 4    | PEx1 [0:3]Tn     | Output         | <b>Transmit Differential Lower Line</b> for x1 Links 0, 1, 2, 3. Shifted when used.                                           |
|                                    | 4    | PEx1 [0:3]Rp     | Input          | <b>Receive Differential Upper Line</b> for x1 Links 0, 1, 2, 3. Shifted when used.                                            |
|                                    | 4    | PEx1 [0:3]Rn     | Input          | <b>Receive Differential Lower Line</b> for x1 Links 0, 1, 2, 3. Shifted when used.                                            |
|                                    | 4    | PEx1 [0:3]CLKp   | Output         | <b>Clock Differential Upper Line</b> for x1 Links 0, 1, 2, 3. Shifted when used.                                              |
|                                    | 4    | PEx1 [0:3]CLKn   | Output         | <b>Clock Differential Lower Line</b> for x1 Links 0, 1, 2, 3. Shifted when used.                                              |
| x16, x8, or x4<br>PCIe Links       | 16   | PEx16_0T(#p)     | Output         | <b>Transmit Differential Upper Lines</b> for the x16, x8 or the x4 Links.<br>The x4 and x8 Links should be shifted when used. |
|                                    | 16   | PEx8 [0:1]T(#p)  |                |                                                                                                                               |
|                                    | 8    | PEx4 [0:1]T(#p)  |                |                                                                                                                               |
|                                    | 16   | PEx16_0T(#n)     | Output         | <b>Transmit Differential Lower Lines</b> for x16, x8 or the x4 Links.<br>The x4 and x8 Links should be shifted when used.     |
|                                    | 16   | PEx8 [0:1]T(#n)  |                |                                                                                                                               |
|                                    | 8    | PEx4 [0:1]T(#n)  |                |                                                                                                                               |
|                                    | 16   | PEx16_0R(#p)     | Input          | <b>Receive Differential Upper Lines</b> for the x16, x8, or the x4 Links.<br>The x4 and x8 Links should be shifted when used. |
|                                    | 16   | PEx8 [0:1]R(#p)  |                |                                                                                                                               |
|                                    | 8    | PEx4 [0:1]R(#p)  |                |                                                                                                                               |
|                                    | 16   | PEx16_0R(#n)     | Input          | <b>Receive Differential Lower Lines</b> for the x16, x8, or the x4 Links.<br>The x4 and x8 Links should be shifted when used. |
|                                    | 16   | PEx8 [0:1]R(#n)  |                |                                                                                                                               |
|                                    | 8    | PEx4 [0:1]R(#n)  |                |                                                                                                                               |
| Misc.                              | 1    | PEx16_x8_x4_CLKp | Output         | <b>Clock Differential Upper Line</b> for x16 or first x8 or x4 Link. Re-driven when used                                      |
|                                    | 1    | PEx16_x8_x4_CLKn | Output         | <b>Clock Differential Lower Line</b> for x16 or first x8 or x4 Link. Re-driven when used                                      |
| Misc.                              | 1    | DIR              | Output         | <b>Direction</b> indicates to the Device if it is installed above or below the Host                                           |
| PCIe                               | 1    | PERST#           | Output         | <b>Reset</b> for PCI Express Bus                                                                                              |
| PCIe                               | 1    | Reserved WAKE#   | Input          | <b>Reserved</b> for Wake on Lan                                                                                               |
| ATX<br>Power<br>Supply             | 1    | PSON#            | Output         | <b>Power Supply On</b> brings the ATX power supply out of sleep mode.                                                         |
|                                    | 1    | PWRGD            | Input          | <b>Power Good</b> from the power supply indicates power is good                                                               |
|                                    | 2    | +5V_SB           | Power          | <b>Standby Power</b> for advanced power saving modes. Always on                                                               |
|                                    | 2    | +5V              | Power          | +5V central power planes                                                                                                      |
|                                    | 2    | +3.3V            | Power          | +3.3V power                                                                                                                   |
|                                    | 1    | +12V             | Power          | +12V central power plane                                                                                                      |
|                                    | 46   | GND              | Power          | <b>GND</b> pins                                                                                                               |
| SMB                                | 1    | SMB_Clk          | Output         | <b>Clock for SMBus</b>                                                                                                        |
|                                    | 1    | SMB_Data         | Bidirectional  | <b>Data for SMBus</b>                                                                                                         |
|                                    | 1    | SMB_Alert#       | Input          | <b>Alert for SMBus</b>                                                                                                        |
| Reserved                           | 4    | Reserved HS+/-   |                | <b>Reserved</b> for 2 high speed differential pairs                                                                           |
|                                    | 1    | Reserved GPIO0   |                | <b>Reserved</b> for general purpose I/O                                                                                       |
| # indicates the lane within a link |      |                  |                |                                                                                                                               |
| [0:3] indicates link 0, 1, 2, or 3 |      |                  |                |                                                                                                                               |
| [0:1] indicates link 0 or 1        |      |                  |                |                                                                                                                               |

Table 2-1 shows only the required pins, arranged in functional groups, for the various buses housed in Connector A. This version of the stackable PCIe is as defined in the *PCIe Base Specification Revision 1.1* with the exception that Hot plug present detect, Hot plug detect, and JTAG are not supported.

## **2.3. Signal Naming Convention**

The PCI Express signals on Connector A are named so that signal groupings are obvious. The fields in a signal name go from general to specific. The PCI Express signals start with the characters “PE,” followed by the width of the Link (“x1”, “x4”, “x8”, or “x16”), followed by an underscore “\_”. Next is the Link number if there is more than one Link of that width. Then is either “T”, “R”, or “Clk” for Transmit, Receive, or Clock respectively. Next is the lane number in the link in parenthesis, for the links that have more than one lane. Last is “p” or “n” for the positive and negative signal in the differential pair.

For example, PEx4\_OT(2)p is the positive signal in lane number 2 of the first x4 Link.

A signal on the connector is designated “transmit” or “receive” in a Host-centric manner. The “transmit” pin on the Host connects to the “T” (transmit) pin of the connector. From there, the signal connects to “receive” pin of the Device.

In a PCIe system the transmit pins of the chip are always connected to the receive pins of the other chip in the link, and vice-versa. For example, for a specific link, transmit on the Host chip is connected to receive on the Device chip, and receive on the Host is connected to transmit on the Device.

Other non-PCIe signals follow a similar convention.

## **2.4. Pin Assignment**

On both of these connectors, the odd-numbered pins are located towards the inside of the board, and the even numbered pins are located towards the edge of the board. Signals were assigned to pins to simplify breakout and reduce trace lengths of the PCI Express signals around Connector A. See Table 2-2.

Table 2-2 Connector A Pin assignments

| Top View Signal Assignment |                  |                  |     | Bottom View Signal Assignment |                  |                  |     |
|----------------------------|------------------|------------------|-----|-------------------------------|------------------|------------------|-----|
| 1                          | Reserved (GPIO0) | PE_RST#          | 2   | 2                             | PE_RST#          | Reserved (GPIO0) | 1   |
| 3                          | 3.3V             | 3.3V             | 4   | 4                             | 3.3V             | 3.3V             | 3   |
| 5                          | Reserved (HS1+)  | Reserved (HS0+)  | 6   | 6                             | Reserved (HS0+)  | Reserved (HS1+)  | 5   |
| 7                          | Reserved (HS1-)  | Reserved (HS0-)  | 8   | 8                             | Reserved (HS0-)  | Reserved (HS1-)  | 7   |
| 9                          | GND              | GND              | 10  | 10                            | GND              | GND              | 9   |
| 11                         | PEx1_1Tp         | PEx1_0Tp         | 12  | 12                            | PEx1_0Tp         | PEx1_1Tp         | 11  |
| 13                         | PEx1_1Tn         | PEx1_0Tn         | 14  | 14                            | PEx1_0Tn         | PEx1_1Tn         | 13  |
| 15                         | GND              | GND              | 16  | 16                            | GND              | GND              | 15  |
| 17                         | PEx1_2Tp         | PEx1_3Tp         | 18  | 18                            | PEx1_3Tp         | PEx1_2Tp         | 17  |
| 19                         | PEx1_2Tn         | PEx1_3Tn         | 20  | 20                            | PEx1_3Tn         | PEx1_2Tn         | 19  |
| 21                         | GND              | GND              | 22  | 22                            | GND              | GND              | 21  |
| 23                         | PEx1_1Rp         | PEx1_0Rp         | 24  | 24                            | PEx1_0Rp         | PEx1_1Rp         | 23  |
| 25                         | PEx1_1Rn         | PEx1_0Rn         | 26  | 26                            | PEx1_0Rn         | PEx1_1Rn         | 25  |
| 27                         | GND              | GND              | 28  | 28                            | GND              | GND              | 27  |
| 29                         | PEx1_2Rp         | PEx1_3Rp         | 30  | 30                            | PEx1_3Rp         | PEx1_2Rp         | 29  |
| 31                         | PEx1_2Rn         | PEx1_3Rn         | 32  | 32                            | PEx1_3Rn         | PEx1_2Rn         | 31  |
| 33                         | GND              | GND              | 34  | 34                            | GND              | GND              | 33  |
| 35                         | PEx1_1Clkp       | PEx1_0Clkp       | 36  | 36                            | PEx1_0Clkp       | PEx1_1Clkp       | 35  |
| 37                         | PEx1_1Clkn       | PEx1_0Clkn       | 38  | 38                            | PEx1_0Clkn       | PEx1_1Clkn       | 37  |
| 39                         | 5V_Always        | 5V_Always        | 40  | 40                            | 5V_Always        | 5V_Always        | 39  |
| 41                         | PEx1_2Clkp       | PEx1_3Clkp       | 42  | 42                            | PEx1_3Clkp       | PEx1_2Clkp       | 41  |
| 43                         | PEx1_2Clkn       | PEx1_3Clkn       | 44  | 44                            | PEx1_3Clkn       | PEx1_2Clkn       | 43  |
| 45                         | CPU_DIR          | PWRGOOD          | 46  | 46                            | PWRGOOD          | CPU_DIR          | 45  |
| 47                         | SMB_DAT          | PEx16_x8_x4_Clkp | 48  | 48                            | PEx16_x8_x4_Clkp | SMB_DAT          | 47  |
| 49                         | SMB_CLK          | PEx16_x8_x4_Clkn | 50  | 50                            | PEx16_x8_x4_Clkn | SMB_CLK          | 49  |
| 51                         | SMB_ALERT        | PSON#            | 52  | 52                            | PSON#            | SMB_ALERT        | 51  |
| 53                         | Reserved / WAKE# | PEG_ENA#         | 54  | 54                            | PEG_ENA#         | Reserved / WAKE# | 53  |
| 55                         | GND              | GND              | 56  | 56                            | GND              | GND              | 55  |
| 57                         | PEx16_0T(8)p     | PEx16_0T(0)p     | 58  | 58                            | PEx16_0T(0)p     | PEx16_0T(8)p     | 57  |
| 59                         | PEx16_0T(8)n     | PEx16_0T(0)n     | 60  | 60                            | PEx16_0T(0)n     | PEx16_0T(8)n     | 59  |
| 61                         | GND              | GND              | 62  | 62                            | GND              | GND              | 61  |
| 63                         | PEx16_0T(9)p     | PEx16_0T(1)p     | 64  | 64                            | PEx16_0T(1)p     | PEx16_0T(9)p     | 63  |
| 65                         | PEx16_0T(9)n     | PEx16_0T(1)n     | 66  | 66                            | PEx16_0T(1)n     | PEx16_0T(9)n     | 65  |
| 67                         | GND              | GND              | 68  | 68                            | GND              | GND              | 67  |
| 69                         | PEx16_0T(10)p    | PEx16_0T(2)p     | 70  | 70                            | PEx16_0T(2)p     | PEx16_0T(10)p    | 69  |
| 71                         | PEx16_0T(10)n    | PEx16_0T(2)n     | 72  | 72                            | PEx16_0T(2)n     | PEx16_0T(10)n    | 71  |
| 73                         | GND              | GND              | 74  | 74                            | GND              | GND              | 73  |
| 75                         | PEx16_0T(11)p    | PEx16_0T(3)p     | 76  | 76                            | PEx16_0T(3)p     | PEx16_0T(11)p    | 75  |
| 77                         | PEx16_0T(11)n    | PEx16_0T(3)n     | 78  | 78                            | PEx16_0T(3)n     | PEx16_0T(11)n    | 77  |
| 79                         | GND              | GND              | 80  | 80                            | GND              | GND              | 79  |
| 81                         | PEx16_0T(12)p    | PEx16_0T(4)p     | 82  | 82                            | PEx16_0T(4)p     | PEx16_0T(12)p    | 81  |
| 83                         | PEx16_0T(12)n    | PEx16_0T(4)n     | 84  | 84                            | PEx16_0T(4)n     | PEx16_0T(12)n    | 83  |
| 85                         | GND              | GND              | 86  | 86                            | GND              | GND              | 85  |
| 87                         | PEx16_0T(13)p    | PEx16_0T(5)p     | 88  | 88                            | PEx16_0T(5)p     | PEx16_0T(13)p    | 87  |
| 89                         | PEx16_0T(13)n    | PEx16_0T(5)n     | 90  | 90                            | PEx16_0T(5)n     | PEx16_0T(13)n    | 89  |
| 91                         | GND              | GND              | 92  | 92                            | GND              | GND              | 91  |
| 93                         | PEx16_0T(14)p    | PEx16_0T(6)p     | 94  | 94                            | PEx16_0T(6)p     | PEx16_0T(14)p    | 93  |
| 95                         | PEx16_0T(14)n    | PEx16_0T(6)n     | 96  | 96                            | PEx16_0T(6)n     | PEx16_0T(14)n    | 95  |
| 97                         | GND              | GND              | 98  | 98                            | GND              | GND              | 97  |
| 99                         | PEx16_0T(15)p    | PEx16_0T(7)p     | 100 | 100                           | PEx16_0T(7)p     | PEx16_0T(15)p    | 99  |
| 101                        | PEx16_0T(15)n    | PEx16_0T(7)n     | 102 | 102                           | PEx16_0T(7)n     | PEx16_0T(15)n    | 101 |
| 103                        | GND              | GND              | 104 | 104                           | GND              | GND              | 103 |
| 105                        | SDVO_DAT (PENA#) | SDVO_CLK         | 106 | 106                           | SDVO_CLK         | SDVO_DAT (PENA#) | 105 |
| 107                        | GND              | GND              | 108 | 108                           | GND              | GND              | 107 |
| 109                        | PEx16_0R(8)p     | PEx16_0R(0)p     | 110 | 110                           | PEx16_0R(0)p     | PEx16_0R(8)p     | 109 |
| 111                        | PEx16_0R(8)n     | PEx16_0R(0)n     | 112 | 112                           | PEx16_0R(0)n     | PEx16_0R(8)n     | 111 |
| 113                        | GND              | GND              | 114 | 114                           | GND              | GND              | 113 |
| 115                        | PEx16_0R(9)p     | PEx16_0R(1)p     | 116 | 116                           | PEx16_0R(1)p     | PEx16_0R(9)p     | 115 |
| 117                        | PEx16_0R(9)n     | PEx16_0R(1)n     | 118 | 118                           | PEx16_0R(1)n     | PEx16_0R(9)n     | 117 |
| 119                        | GND              | GND              | 120 | 120                           | GND              | GND              | 119 |
| 121                        | PEx16_0R(10)p    | PEx16_0R(2)p     | 122 | 122                           | PEx16_0R(2)p     | PEx16_0R(10)p    | 121 |
| 123                        | PEx16_0R(10)n    | PEx16_0R(2)n     | 124 | 124                           | PEx16_0R(2)n     | PEx16_0R(10)n    | 123 |
| 125                        | GND              | GND              | 126 | 126                           | GND              | GND              | 125 |
| 127                        | PEx16_0R(11)p    | PEx16_0R(3)p     | 128 | 128                           | PEx16_0R(3)p     | PEx16_0R(11)p    | 127 |
| 129                        | PEx16_0R(11)n    | PEx16_0R(3)n     | 130 | 130                           | PEx16_0R(3)n     | PEx16_0R(11)n    | 129 |
| 131                        | GND              | GND              | 132 | 132                           | GND              | GND              | 131 |
| 133                        | PEx16_0R(12)p    | PEx16_0R(4)p     | 134 | 134                           | PEx16_0R(4)p     | PEx16_0R(12)p    | 133 |
| 135                        | PEx16_0R(12)n    | PEx16_0R(4)n     | 136 | 136                           | PEx16_0R(4)n     | PEx16_0R(12)n    | 135 |
| 137                        | GND              | GND              | 138 | 138                           | GND              | GND              | 137 |
| 139                        | PEx16_0R(13)p    | PEx16_0R(5)p     | 140 | 140                           | PEx16_0R(5)p     | PEx16_0R(13)p    | 139 |
| 141                        | PEx16_0R(13)n    | PEx16_0R(5)n     | 142 | 142                           | PEx16_0R(5)n     | PEx16_0R(13)n    | 141 |
| 143                        | GND              | GND              | 144 | 144                           | GND              | GND              | 143 |
| 145                        | PEx16_0R(14)p    | PEx16_0R(6)p     | 146 | 146                           | PEx16_0R(6)p     | PEx16_0R(14)p    | 145 |
| 147                        | PEx16_0R(14)n    | PEx16_0R(6)n     | 148 | 148                           | PEx16_0R(6)n     | PEx16_0R(14)n    | 147 |
| 149                        | GND              | GND              | 150 | 150                           | GND              | GND              | 149 |
| 151                        | PEx16_0R(15)p    | PEx16_0R(7)p     | 152 | 152                           | PEx16_0R(7)p     | PEx16_0R(15)p    | 151 |
| 153                        | PEx16_0R(15)n    | PEx16_0R(7)n     | 154 | 154                           | PEx16_0R(7)n     | PEx16_0R(15)n    | 153 |
| 155                        | GND              | GND              | 156 | 156                           | GND              | GND              | 155 |

## 2.4.1 x16 Link Alternate Uses

The x16 Link is also able to be configured for alternate uses. These uses include two x8 Links, two x4 Links, or two SDVO. Support for these alternate modes is Host and Device dependant. A Host that supports an x16 Link is not required to support SDVO, two x8, or two x4 Links. Also, a Device that supports operation at x16 is not required to support operation at x8 or x4.

### 2.4.1.1 x8 and x4 Links

Two x8 Links can be provided on the x16 Link. When a Device uses one of the Links, the other Link is shifted according to the same rules as the x1 Links. Each x8 Link may also be used as an x4 Link.

Because there is only one clock provided for the x16 Link and potentially two devices when operating as x8 or x4, any Device that operates at x8 or x4 must re-drive the clock. The clock must not incur more than 10ns of phase delay when it is re-driven.

The pin assignments for the x8 and x4 Links are shown in Table 2-3 below.

**Table 2-3: x16 Link as Two x8 or Two x4 Links**

| Host Transmit Signals |            |            | Host Receive Signals |            |            |
|-----------------------|------------|------------|----------------------|------------|------------|
| x16 Signal            | x8 Signal  | x4 Signal  | x16 Signal           | x8 Signal  | x4 Signal  |
| PEx16_0T(0)           | PEx8_0T(0) | PEx4_0T(0) | PEx16_0R(0)          | PEx8_0R(0) | PEx4_0R(0) |
| PEx16_0T(1)           | PEx8_0T(1) | PEx4_0T(1) | PEx16_0R(1)          | PEx8_0R(1) | PEx4_0R(1) |
| PEx16_0T(2)           | PEx8_0T(2) | PEx4_0T(2) | PEx16_0R(2)          | PEx8_0R(2) | PEx4_0R(2) |
| PEx16_0T(3)           | PEx8_0T(3) | PEx4_0T(3) | PEx16_0R(3)          | PEx8_0R(3) | PEx4_0R(3) |
| PEx16_0T(4)           | PEx8_0T(4) |            | PEx16_0R(4)          | PEx8_0R(4) |            |
| PEx16_0T(5)           | PEx8_0T(5) |            | PEx16_0R(5)          | PEx8_0R(5) |            |
| PEx16_0T(6)           | PEx8_0T(6) |            | PEx16_0R(6)          | PEx8_0R(6) |            |
| PEx16_0T(7)           | PEx8_0T(7) |            | PEx16_0R(7)          | PEx8_0R(7) |            |
| PEx16_0T(8)           | PEx8_1T(0) | PEx4_1T(0) | PEx16_0R(8)          | PEx8_1R(0) | PEx4_1R(0) |
| PEx16_0T(9)           | PEx8_1T(1) | PEx4_1T(1) | PEx16_0R(9)          | PEx8_1R(1) | PEx4_1R(1) |
| PEx16_0T(10)          | PEx8_1T(2) | PEx4_1T(2) | PEx16_0R(10)         | PEx8_1R(2) | PEx4_1R(2) |
| PEx16_0T(11)          | PEx8_1T(3) | PEx4_1T(3) | PEx16_0R(11)         | PEx8_1R(3) | PEx4_1R(3) |
| PEx16_0T(12)          | PEx8_1T(4) |            | PEx16_0R(12)         | PEx8_1R(4) |            |
| PEx16_0T(13)          | PEx8_1T(5) |            | PEx16_0R(13)         | PEx8_1R(5) |            |
| PEx16_0T(14)          | PEx8_1T(6) |            | PEx16_0R(14)         | PEx8_1R(6) |            |
| PEx16_0T(15)          | PEx8_1T(7) |            | PEx16_0R(15)         | PEx8_1R(7) |            |

### 2.4.1.2 SDVO

The x16 Link can also be re-configured as an SDVO connections as shown in Table 2-4. The exact implementation of this is chipset specific. Table 2-4 below shows the configuration when using an Intel® 915/945/965 chipset. When using the x16 Link as SDVO, the PEx16\_ENA signal must be left floating at the Device.

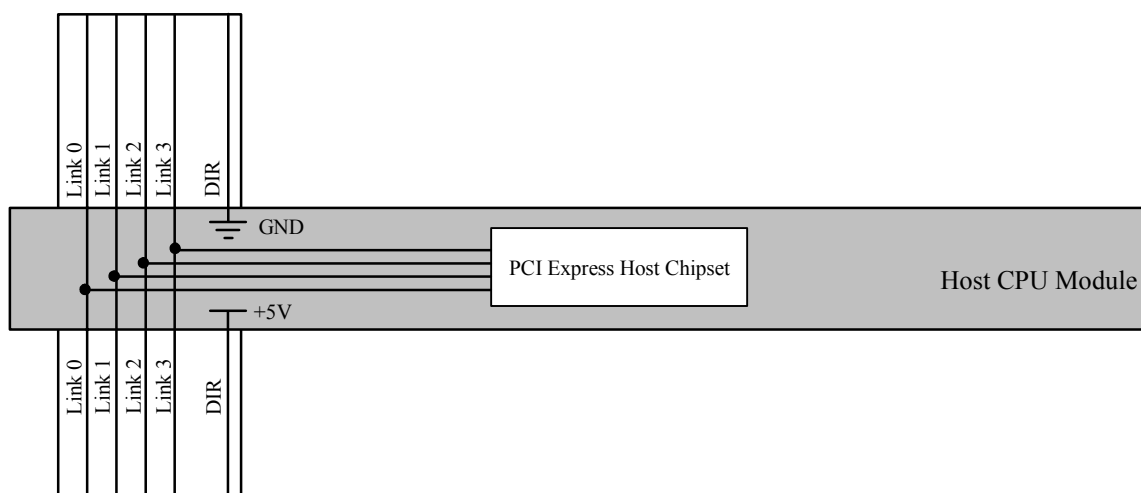
**Table 2-4: x16 Link as SDVO**

| x16 Signal Name | SDVO Signal Name | x16 Signal Name | SDVO Signal Name |
|-----------------|------------------|-----------------|------------------|
| PEx16_0T(0)     | SDVO_0RED        | PEx16_0R(0)     | SDVO_TVCLKIN     |
| PEx16_0T(1)     | SDVO_0GREEN      | PEx16_0R(1)     | SDVO_0INT        |
| PEx16_0T(2)     | SDVO_0BLUE       | PEx16_0R(2)     | SDVO_FLDSTALL    |
| PEx16_0T(3)     | SDVO_0CLK        | PEx16_0R(3)     |                  |
| PEx16_0T(4)     | SDVO_1RED        | PEx16_0R(4)     |                  |
| PEx16_0T(5)     | SDVO_1GREEN      | PEx16_0R(5)     | SDVO_1INT        |
| PEx16_0T(6)     | SDVO_1BLUE       | PEx16_0R(6)     |                  |
| PEx16_0T(7)     | SDVO_1CLK        | PEx16_0R(7)     |                  |
| PEx16_0T(8)     |                  | PEx16_0R(8)     |                  |
| PEx16_0T(9)     |                  | PEx16_0R(9)     |                  |
| PEx16_0T(10)    |                  | PEx16_0R(10)    |                  |
| PEx16_0T(11)    |                  | PEx16_0R(11)    |                  |
| PEx16_0T(12)    |                  | PEx16_0R(12)    |                  |
| PEx16_0T(13)    |                  | PEx16_0R(13)    |                  |
| PEx16_0T(14)    |                  | PEx16_0R(14)    |                  |
| PEx16_0T(15)    |                  | PEx16_0R(15)    |                  |

## 2.4.2 DIR Signal

### 2.4.2.1 DIR Line on Host

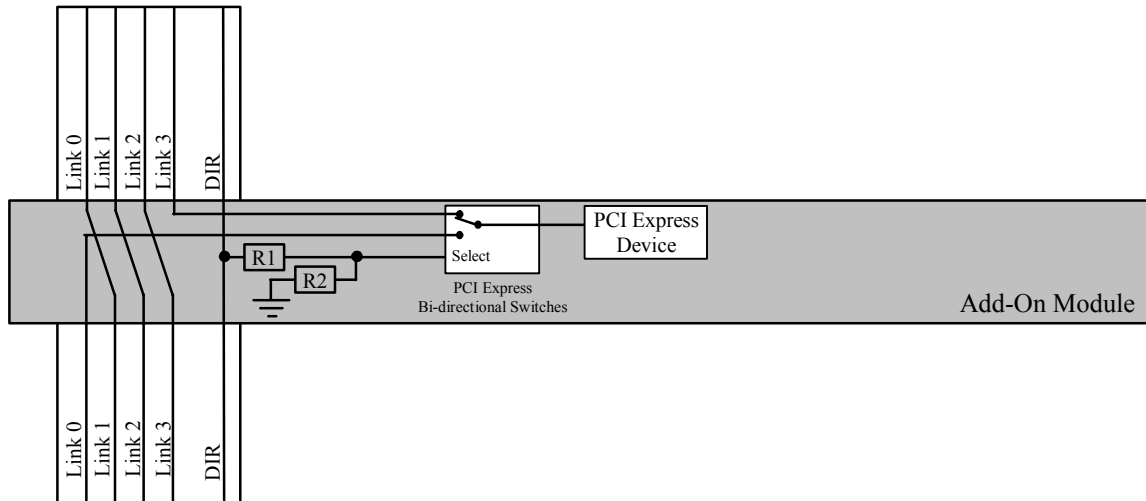
The DIR line provides a means for the Devices to select the correct Link depending if it is above or below the Host in the stack. The state of the DIR line is always determined by the Host so that the Devices can be designed without regards to the design of other Devices. On the top side connector this line must be tied to ground on the Host. On the bottom side connector the DIR line must be tied to +5V power during all implemented power saving modes except power completely off. A Host that supports suspend modes may want to use +5V\_Aux diode ORed with +5V in case the power supply does not provide +5V\_Aux. Shown in Figure 2-1 is the required PCB connection for the DIR line on the Host.



**Figure 2-1 Required Circuitry for a Host Module Configuration for Automatic Link Shifting**

### 2.4.2.2 DIR Line on Device

On the Device the DIR line is an input to the resident auto-switching multiplexers. A resistor divider is required on the DIR line on each Device to adjust the SELECT line voltage for the switches. Each Device must sink or source less than 300uA of current. Therefore, the divider resistors R1 and R2 shown in Figure 2-2 must total 15K or greater.



**Figure 2-2 Required Device Circuitry for Automatic Link Shifting**

If the Device is positioned above the Host, then the DIR signal would be grounded and the SELECT line of the multiplexers would allow Link 0 to connect to the PCI device. Links 1, 2, and 3 are then allowed to shift and pass over so that Link 1 is in the Link 0 position, Link 2 is in the Link 1 position, and Link 3 is in the Link 2 position. A left-most Link is now available for the next Device card to be stacked above the first Device.

If the Device is stacked below the module, then the DIR line would be set to +5V and the SELECT line of the multiplexers would allow Link 3 to connect to the PCI device. Links 0, 1, and 2 are then allowed to shift and pass over so that Link 2 is in the Link 3 position, Link 1 is in the Link 2 position, and Link 0 is in the Link 1 position. A right-most link is now available for the next Device card to be stacked below the first Device.

All Devices can be built using the same methodology as a single configuration. The Links used will always be the left most links or the rights most links depending if the Device gets stacked above or below the Host.

### 2.4.3 PEx16\_ENA# Signal

The PEG\_ENA# signal is used to indicate the presence of a device on the x16 Link. This signal is pulled up at the Host. Any Device that uses the x16 Link (or the x16 as an x8 or x4) attaches this signal to ground. When the Host sees this signal high, indicating that an x16 Device is not present, it may disable the x16 Link, or convert it to alternate uses, such as SDVO.

## 2.5. Stack-UP or Stack-DOWN Link Shifting

Connector A contains two differential Link Groups: the x1 PCIe Link Group, and the x4/x8 PCIe Link Group. Within each group are individual point-to-point links which must be automatically shifted if one or more links out of that group are used on a Device. The x16 Link does not constitute a group because there is only one Link. Therefore, it does not require Link shifting

Link shifting is utilized so that Devices can be built uniformly and consistently while using dedicated point-to-point connections. Without link shifting, Devices would have to be made with a specific link identified. This would then

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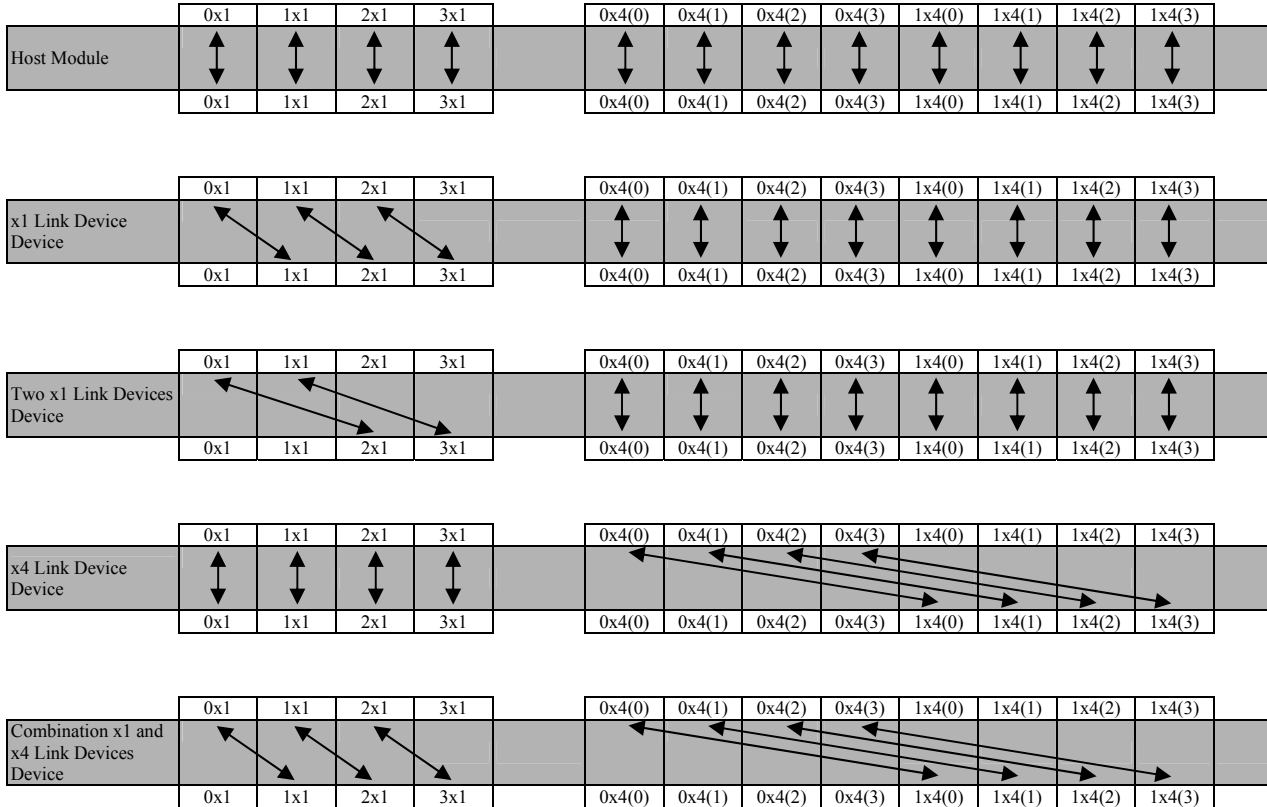
require each Device to have multiple configurations, one for each link position. Link shifting at the PCB level allows each Device to have only one universal configuration.

In addition to automatic Link shifting, highly embedded systems require that Devices be allowed to stack above or below the Host. The key to this capability is the ability for the Devices to use either the first links or the last links depending on whether the module is above or below the Host. The DIR line tells the Device its position relative to the Host.

Note: Devices should not be stacked above and below the Host at the same time in order to avoid signal integrity degradation.

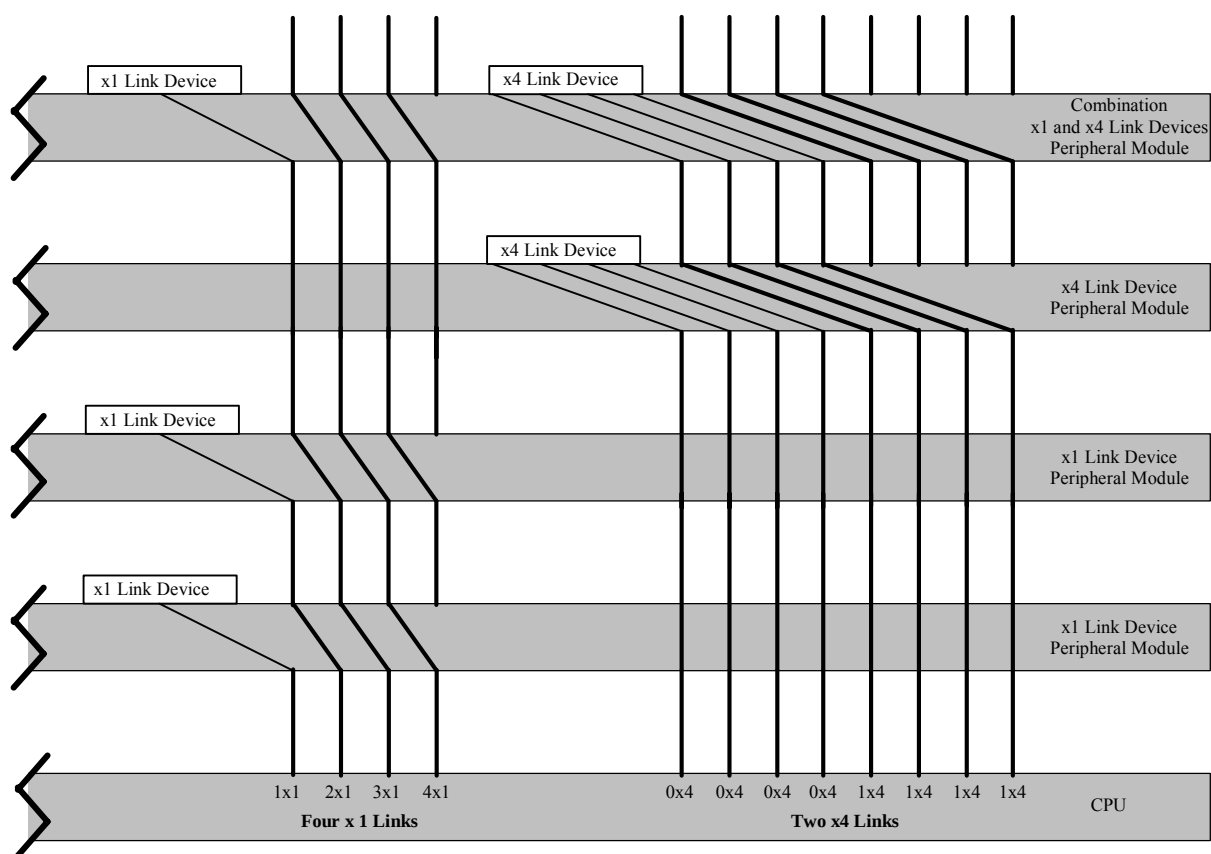
## 2.5.1 PCB Link Shifting

As a demonstration of link shifting in the presence of multiple link groups, the x1 PCIe and x4 PCIe link groups are used in Figure 2-3: Automatic Link Shifting Examples for Host and Various Devices for a Host and various Device configurations. Any Device may use one or more Links. If multiple Links are used then the necessary link shifting must be implemented on the Device PCB for each Link and Link Group. For example, in the case where two x1 Link devices are resident on the Device, it is required that the remaining two unused Links be shifted two locations in order that other Devices be able to use the remaining Links. It is not enough to shift only one link space as in the case of a one x1 Link Device.

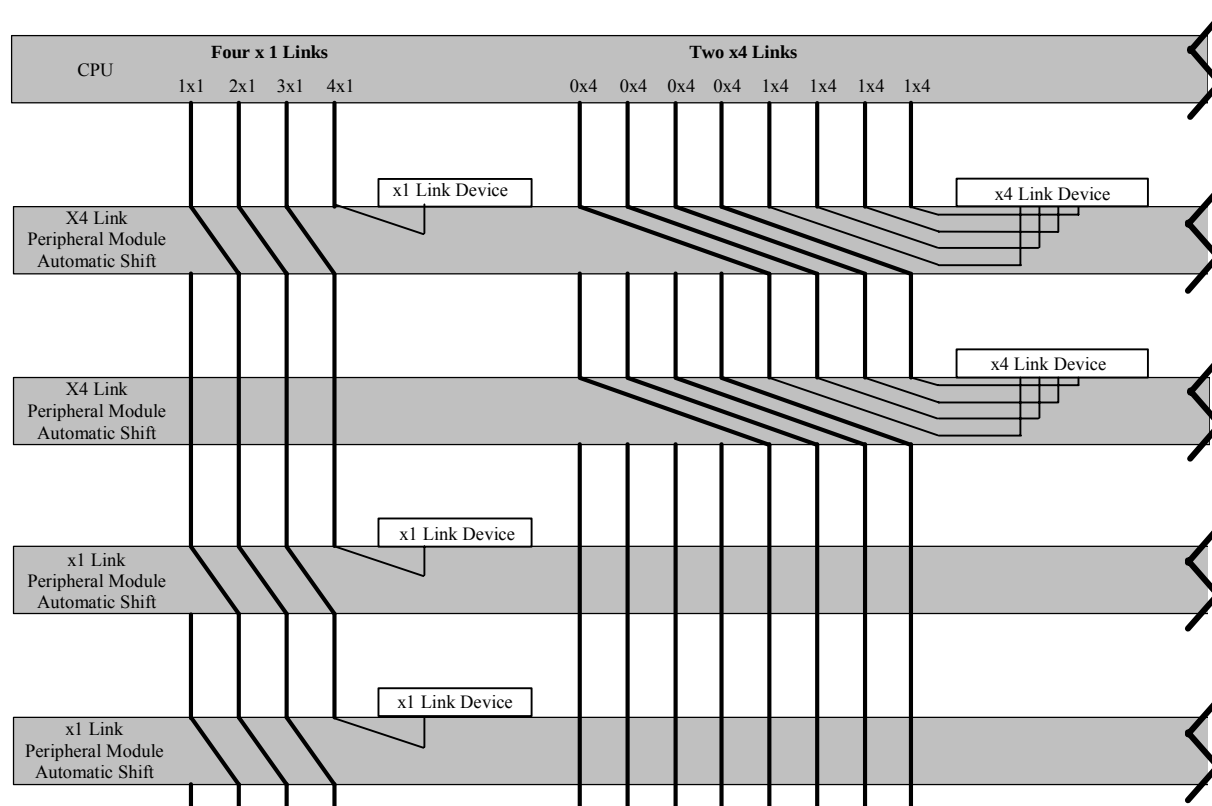


**Figure 2-3: Automatic Link Shifting Examples for Host and Various Devices**

## 2.5.2 Link Shifting Stack Examples



**Figure 2-4: Automatic Link Shifting Stack-Up Example Consisting of Two x1 Link Device, One x4 Link Device, and One Device with One x1 Link and One x4 Link**



**Figure 2-5: Automatic Link Shifting Stack-Down Example Consisting of Two x1 Link Device, One x4 Link Device, and One Device with One x1 Link and One x4 Link**

## 2.6. Switching

In order to be able to stack a PCIe/104 module above or below a Host, a PCIe signal switch is required on the Device.

### 2.6.1 Signal Switch

A signal switch is an analog multiplexer that can be used to select between the PCIe Link on the top connector and bottom connector. This switch must be able to perform well at the high data rates found in the PCIe signaling environment. Specifications for this switch are shown in Table 2-5.

**Table 2-5: PCIe Signal Switch Specification**

| Parameter                     | Min. | Max. | Units |
|-------------------------------|------|------|-------|
| Crosstalk @ f = 1.25 GHz      | -33  |      | dB    |
| Off Isolation @ f = 1.25 GHz  | -33  |      | dB    |
| Insertion Loss @ f = 1.25 GHz |      | -3.2 | dB    |

Several candidates for the Signal Switch have been identified. They are listed in Table 2-6.

**Table 2-6: PCIe Signal Switch or equivalent**

| Manufacturer           | Part Number  | Qualification Stage |
|------------------------|--------------|---------------------|
| Texas Instruments      | TS2PCIE2212  | None                |
| Pericom                | PI2PCIE2412  | None                |
| National Semiconductor | DS25MB100    | None                |
| NXP                    | CBTU0808EE/G | None                |

## 2.7. System Clocking

The PCIe architecture is based on a 100 MHz reference clock. In PCIe/104, this clock is distributed from the Host to the Devices.

The Host may also employ spread spectrum clocking as defined in the PCI Express Base Specification to reduce EMI. In this case it is required that the Device use the distributed clock as its reference clock. Using an on-board oscillator as a reference is not allowed.

PCIe/104 does not provide for any termination on unused clock lines, therefore the Host is required to disable any unused clocks.

Since there is only one x4\_x8\_x16 clock, it must be re-driven on add-in boards that use this clock.

## 2.8. Layout Recommendations

The Data rate for PCIe is 2.5 Gbps. This means that significant frequency content exists up to 1.25 GHz. At these speeds, PCB layout becomes very critical. Therefore, the following recommendations should be followed to avoid signal integrity problems:

- Route all PCIe signal lines (Transmit and Receive) as controlled impedance, 100 Ohm differential pairs and 55 Ohm single ended traces.
- Spacing from a link to its neighbor must be at least 20 mils in the main routing region, 15 mils for stripline breakout, and 12 mils for microstrip breakout.
- Symmetrical routing must be used between the two signals of a differential pair.
- Signals in a differential pair must be matched to within 5 mils.
- AC coupling capacitors must be provided on the TX lines. Values should be between 75nF and 200nF. A surface mount capacitor must be used.
- All PCIe signals should be routed in an adjacent layer to a ground plane.

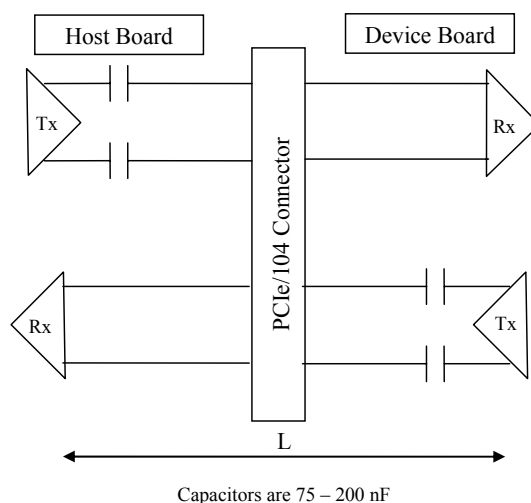
- No stubs except the short stub caused by the unused end of the Host connector. SI testing has shown this very short stub to be insignificant in a system with a Host and 6 add-in cards.
- Do not use 90 degree bends. Use 45 degree bends or curves.

**Table 2-7: Via and Trace Length Budget**

| Location                     | Max. Vias | Max. Trace Length | Notes                        |
|------------------------------|-----------|-------------------|------------------------------|
| Host TX lines                | 4         | 6000 mils         | Both sides of AC cap.        |
| Host RX lines                | 2         | 6000 mils         |                              |
| Device TX Lines              | 4         | 4000 mils         | Both sides of signal switch. |
| Device RX lines              | 4         | 4000 mils         | Both sides of signal switch. |
| Pass-through (lane shifting) | 2         | 1000 mils         | Includes stack height        |

## 2.9. Routing Topology

Figure 2-6 Capacitor Placement below shows the positioning of the DC blocking capacitor and PCIe connector in relation to the Host and Device. The DC blocking capacitor is placed on the transmit signals. This will be the signals the Host drives onto the Tx bus connector's pins and the signals the Device drives onto the Rx signals of the connector. The actual position is not critical; however the position must be closely matched between the signals of a differential pair.



**Figure 2-6 Capacitor Placement**

Table 2-8 below list the general guide lines for PCI Express routing.

**Table 2-8 PCI Express Routing Specification**

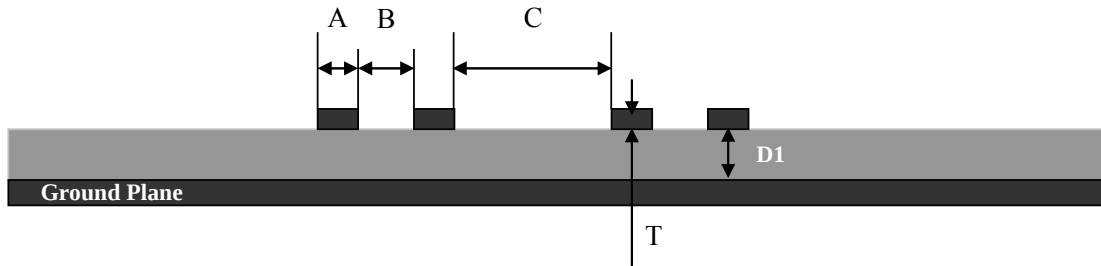
| Interface   | Single Ended Impedance (Ohm) | Differential Impedance (Ohm) | Matching in a pair mil (mm) | Matching pair to pair mil (mm) |
|-------------|------------------------------|------------------------------|-----------------------------|--------------------------------|
| PCI Express | 55 ±15%                      | 100 ±20%                     | 5 (1.27)                    | Not required                   |

### 2.9.1 Microstrip Example

Typical trace dimensions for a microstrip over a ground layer are shown in Table 2-9 and Figure 2-7 below. The actual trace dimensions are dependant on layer stackup. The dimensions should be chosen to result in a differential impedance of 100  $\Omega$  and a single ended impedance of 55  $\Omega$ . Microstrip technology is used on outer layers.

**Table 2-9 Typical Trace Dimensions for Microstrip with FR4**

| Units | Nom. Trace Width | Nom. Trace Space | Pair to Pair Space | Insulator Thickness | Trace Thickness |
|-------|------------------|------------------|--------------------|---------------------|-----------------|
|       | A                | B                | C                  | D1                  | T               |
| mil   | 5                | 7                | 20                 | 3.5 – 5.5           | 1.4 – 2.6       |
| mm    | 0.127            | 0.178            | 0.508              | 0.089 – 0.140       | 0.036 – 0.066   |



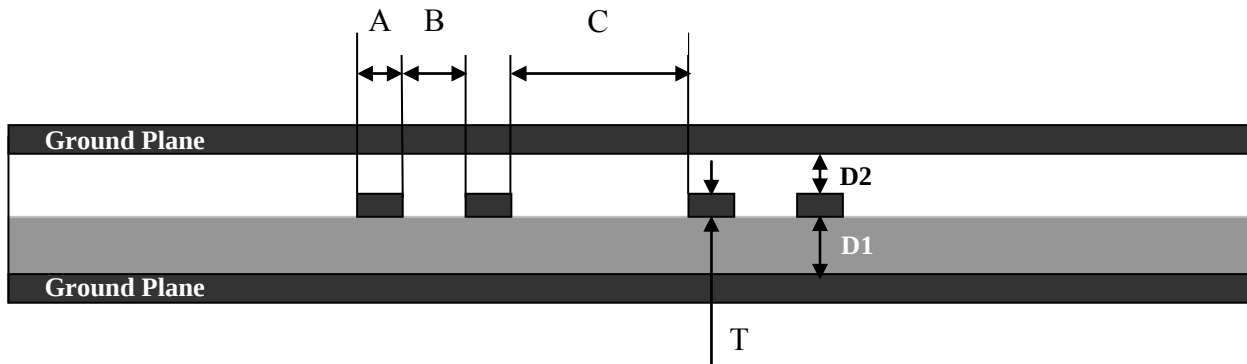
**Figure 2-7 MicroStrip Example**

## 2.9.2 Stripline Example

Typical trace dimensions for a stripline are shown in Table 2-10 and Figure 2-8 below. The actual trace dimensions are dependant on layer stackup. The dimensions should be chosen to result in a differential impedance of 100  $\Omega$  and a single ended impedance of 55  $\Omega$ . Stripline technology is used on inner layers.

**Table 2-10 Typical Trace Dimensions for Stripline with FR4**

| Units | Nom. Trace Width | Nom. Trace Space | Pair to Pair Space | Insulator Thickness | Insulator Thickness | Trace Thickness |
|-------|------------------|------------------|--------------------|---------------------|---------------------|-----------------|
|       | A                | B                | C                  | D1                  | D2                  | T               |
| mil   | 4                | 7                | 20                 | 3.5 – 5.75          | 6 – 14              | 1.1 – 1.3       |
| mm    | 0.102            | 0.178            | 0.508              | 0.089 – 0.146       | 0.152 – 0.356       | 0.028 – 0.033   |



**Figure 2-8 Stripline Example**

## 2.10. Device connector Break-Out Example

Figure 2-9 below shows an example of the routing from the Device connector to a Signal Switch. This drawing is not to scale and does not show controlled impedance lines. It is intended to show the general connections and lane shifting on a device for a x1 PCI Express link that can be stacked above or below the CPU.

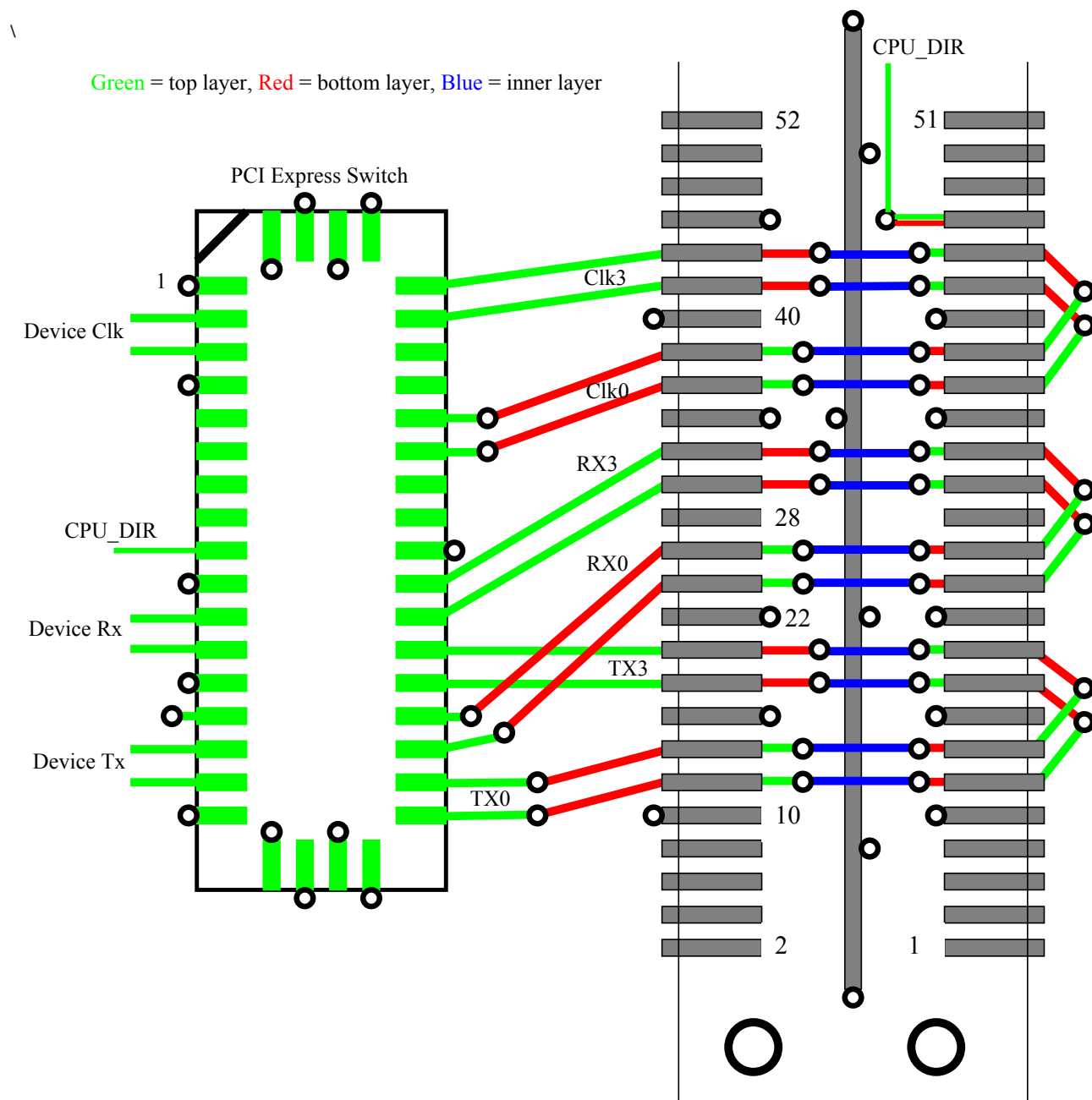


Figure 2-9 Example for breakout routing of connector bank 1 from bottom to top with shifting.

## **3. EXPANSION CONNECTOR B**

### **3.1. Description**

Expansion Connector B is the stackable PCI Expansion connector of the PC/104-*Plus* and PCI-104 specifications. For full details and connector location see the PC/104-*Plus* or PCI-104 Specifications published by the PC/104 Embedded Consortium

### **3.2. Functions**

- Four 32 bit, 33 MHz PCI Bus Links each capable of Bus Mastering
- +5V\_SB, PSON#, PME# for ATX power management
- Power: +3.3V, +5V, +12V, -12V

### 3.3. Signal Descriptions

Table 3-1 Connector B Signals

| # Pins | Signal Name | Group                  | Description                                                                                                                                                                                                  |
|--------|-------------|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 32     | AD[31:00]   | PCI Bus                | <b>Address and Data</b> are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases.                                                            |
| 4      | C/BE[0,3]#  |                        | <b>Bus Command/Byte Enables</b> are multiplexed. During the address phase of a transaction, they define the bus command. During the data phase, they are used as byte enables.                               |
| 1      | PAR         |                        | <b>Parity</b> is even parity across AD [31:00] and C/BE [3:0]#. Parity generation is required by all PCI signals.                                                                                            |
| 1      | FRAME#      |                        | <b>Cycle Frame</b> is driven by the current master to indicate the beginning of an access and will remain active until the final data cycle.                                                                 |
| 1      | TRDY#       |                        | <b>Target Ready</b> indicates the selected device's ability to complete the current data phase of the transaction. Both IRDY# and TRDY# must be asserted to terminate a data cycle.                          |
| 1      | IRDY#       |                        | <b>Initiator Ready</b> indicates the bus master's ability to complete the current data phase of the transaction.                                                                                             |
| 1      | STOP#       |                        | <b>Stop</b> indicates the current selected device is requesting the master to stop the current transaction.                                                                                                  |
| 1      | DEVSEL#     |                        | <b>Device Select</b> , when actively driven, indicates the driving device has decoded its address as the target of the current access.                                                                       |
| 4      | IDSEL[0,3]  |                        | <b>Initialization Device Select</b> is used as a chip-select during configuration read and write transactions.                                                                                               |
| 1      | LOCK#       |                        | <b>Lock</b> indicates an atomic operation to a bridge that may require multiple transactions to complete.                                                                                                    |
| 1      | PERR#       |                        | <b>Parity Error</b> is for reporting data parity errors.                                                                                                                                                     |
| 1      | SERR#       |                        | <b>System Error</b> is for reporting address parity errors.                                                                                                                                                  |
| 4      | REQ#[0,3]   |                        | <b>Request</b> indicates to the arbitrator that this device desires use of the bus.                                                                                                                          |
| 4      | GNT#[0,3]   |                        | <b>Grant</b> indicates to the requesting device that access has been granted.                                                                                                                                |
| 4      | CLK[0,3]    |                        | <b>Clock</b> provides timing for all transactions on the PCI bus and is an input to every PCI device.                                                                                                        |
| 1      | RST#        |                        | <b>Reset</b> is used to bring PCI-specific registers, sequencers, and signals to a consistent state.                                                                                                         |
| 1      | M66EN       |                        | <b>66 MHz Enable</b> indicates to a device whether the bus segment is operating at 33 MHz or 66 MHz. The PCI bus has been simulated at 33MHz. For the purpose of this specification, 66MHz is not supported. |
| 1      | INTA#       |                        | <b>Interrupt A</b> is used to request Interrupts.                                                                                                                                                            |
| 1      | INTB#       |                        | <b>Interrupt B</b> is used to request Interrupts.                                                                                                                                                            |
| 1      | INTC#       |                        | <b>Interrupt C</b> is used to request Interrupts.                                                                                                                                                            |
| 1      | INTD#       |                        | <b>Interrupt D</b> is used to request Interrupts.                                                                                                                                                            |
| 1      | PME#        | ATX<br>Power<br>Supply | <b>Power Management Event</b> such as wake-on-LAN                                                                                                                                                            |
| 1      | +5V_SB      |                        | <b>Standby Power</b> for advanced power saving modes. Always on                                                                                                                                              |
| 1      | PSON#       |                        | <b>Power Supply On</b> brings the ATX power supply out of sleep mode.                                                                                                                                        |
| 5      | VI/O        | Power                  |                                                                                                                                                                                                              |
| 10     | +3.3V       |                        | +3.3V power lines                                                                                                                                                                                            |
| 8      | +5V         |                        | +5V power lines                                                                                                                                                                                              |
| 1      | +12V        |                        | +12V power line                                                                                                                                                                                              |
| 1      | -12V        |                        | -12V power line                                                                                                                                                                                              |
| 25     | GND         |                        | Ground lines                                                                                                                                                                                                 |

Table 3-1 shows only the required pins, arranged in functional groups, which are required for the stackable PCI Expansion bus. This version of the PCI bus is intended as a 32-bit bus running at 33MHz as defined in the *PCI Local Bus Specification Revision 2.2*, and therefore, 64-bit extension and 66MHz<sup>1</sup> are not supported at this time. Also not supported are the boundary scan features (JTAG), *Present* (PRSNT [1:2]#), and *Clock running* (CLKRUN#). The direction indication on the pins assumes a combination master/target device.

<sup>1</sup> The PCI bus has been simulated at 33MHz. For the purpose of this specification, 66MHz is not supported. To support future enhancements, the M66EN signal should be grounded on any module that cannot support 66MHz and left open for modules that can support a 66MHz clock.

### 3.4. Pin Assignment

Signals are assigned in the same relative order as in the PCI Local Bus Specification Revision 2.2, but transformed to the corresponding header connector pins. Because of the stack-through nature of the bus, slot-specific signals are duplicated for each plug-in module. The system has been designed to accommodate 4 modules, which are PC/104-*Plus*, PCI-104, or a combination of the two, so multiple sets of the signals have been duplicated to accommodate one signal for each module. These four signal groups include: IDSEL[3:0], CLK[3:0], REQ#[3:0], GNT#[3:0]. Signal assignments for the J3/P3 connector are given in Table 3-2.

**Table 3-2 Connector Signal Assignment**

|    | A      | B      | C      | D       |
|----|--------|--------|--------|---------|
| 1  | GND    | +5V_SB | +5V    | AD00    |
| 2  | VI/O   | AD02   | AD01   | +5V     |
| 3  | AD05   | GND    | AD04   | AD03    |
| 4  | C/BE0# | AD07   | GND    | AD06    |
| 5  | GND    | AD09   | AD08   | GND     |
| 6  | AD11   | VI/O   | AD10   | M66EN   |
| 7  | AD14   | AD13   | GND    | AD12    |
| 8  | +3.3V  | C/BE1# | AD15   | +3.3V   |
| 9  | SERR#  | GND    | PSON#  | PAR     |
| 10 | GND    | PERR#  | +3.3V  | PME#    |
| 11 | STOP#  | +3.3V  | LOCK#  | GND     |
| 12 | +3.3V  | TRDY#  | GND    | DEVSEL# |
| 13 | FRAME# | GND    | IRDY#  | +3.3V   |
| 14 | GND    | AD16   | +3.3V  | C/BE2#  |
| 15 | AD18   | +3.3V  | AD17   | GND     |
| 16 | AD21   | AD20   | GND    | AD19    |
| 17 | +3.3V  | AD23   | AD22   | +3.3V   |
| 18 | IDSEL0 | GND    | IDSEL1 | IDSEL2  |
| 19 | AD24   | C/BE3# | VI/O   | IDSEL3  |
| 20 | GND    | AD26   | AD25   | GND     |
| 21 | AD29   | +5V    | AD28   | AD27    |
| 22 | +5V    | AD30   | GND    | AD31    |
| 23 | REQ0#  | GND    | REQ1#  | VI/O    |
| 24 | GND    | REQ2#  | +5V    | GNT0#   |
| 25 | GNT1#  | VI/O   | GNT2#  | GND     |
| 26 | +5V    | CLK0   | GND    | CLK1    |
| 27 | CLK2   | +5V    | CLK3   | GND     |
| 28 | GND    | INTD#  | +5V    | RST#    |
| 29 | +12V   | INTA#  | INTB#  | INTC#   |
| 30 | -12V   | REQ3#  | GNT3#  | GND     |

### 3.5. +5V\_SB, PSON#, and PME#

To support ATX power supplies and power down features three signals have been added to the PCI bus. They are +5V\_SB which is a power source that is always present when main power is supplied to the system, PSON# which is a power supply control signal that can turn the power supply on or off, and PME# which can be used to bring the CPU out of power down states such as wake-on-LAN.

These signals have been implemented on the reserved pins of the PCI expansion bus of the PC/104-*Plus* and PCI-104 Specifications at pins B1, C9, and D10. Not all manufacturers will implement these signals; therefore to maintain compatibility with existing products it is important for designs that implement these functions to protect against undriven inputs.

## **3.6. PCI Signaling Voltage (VI/O) Requirements**

### **3.6.1 PCI Host Module**

The PCI Host board will always determine the PCI signaling level on the bus by setting all VI/O pins to either +3.3V or +5V. If VI/O is set to 3.3V, then the system will use +3.3V I/O signaling and, likewise, if VI/O is set to +5V, then the system will use +5V I/O signaling. Some PCI host modules may only allow one of the options, while others may provide a jumper to allow the user to select the signaling level. Once the signaling level is selected, the remaining boards in the system must use that signaling level.

### **3.6.2 Add-In Modules**

Add-in cards can be 3.3V, 5V, or universal.

#### **3.6.2.1 3.3V Add-In Modules**

3.3V add-in modules operate in environments where VI/O has been set to +3.3V by the host module. Using 5V add-in modules on a 3.3V stack will result in the 3.3V modules being damaged.

#### **3.6.2.2 5V Add-In Modules**

5V add-in modules operate in environments where VI/O has been set to +5V by the host module. Using 3.3V add-in modules on a 5V stack will result in the 3.3V modules being damaged.

#### **3.6.2.3 Universal Add-In Modules**

Universal add-in boards can be used on either 3V or 5V I/O signaling buses. Universal boards either use the VI/O signal to determine its signaling level or are 3V signaling boards that have 5V-tolerant I/O. Many PCI interface chips have a "VI/O" pin that is the power for the I/O buffers that can be directly connected to VI/O. Universal boards will work on either 3V or 5V I/O signaling buses.

## **4. STACKING**

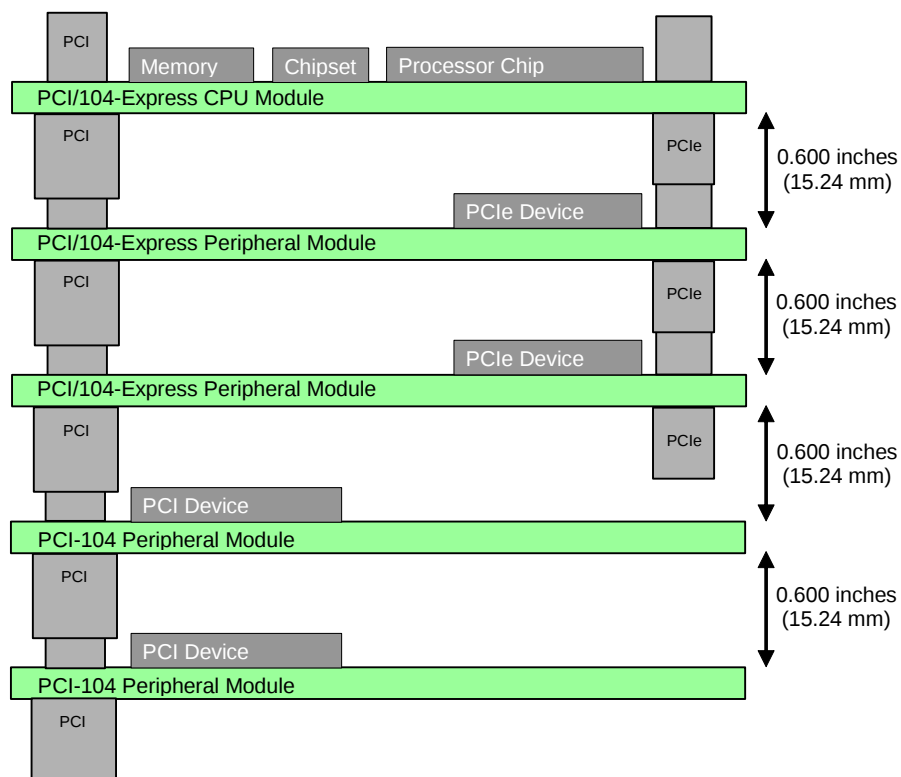
### **4.1. Add-in Device Rules**

- 1) A Device card must be able to be stacked above or below the Host. Therefore, the Device must be capable of selecting the TX, RX, and clock lines from the top connector or the bottom connector.
- 2) If any link(s) from a Link group (x1 PCIe, x4 PCIe, and x8 PCIe) is used on the module, the other links in that group must be shifted to the appropriate positions.
- 3) Any unused signals must be passed between top and bottom using no more than two vias and as short of a trace as possible.

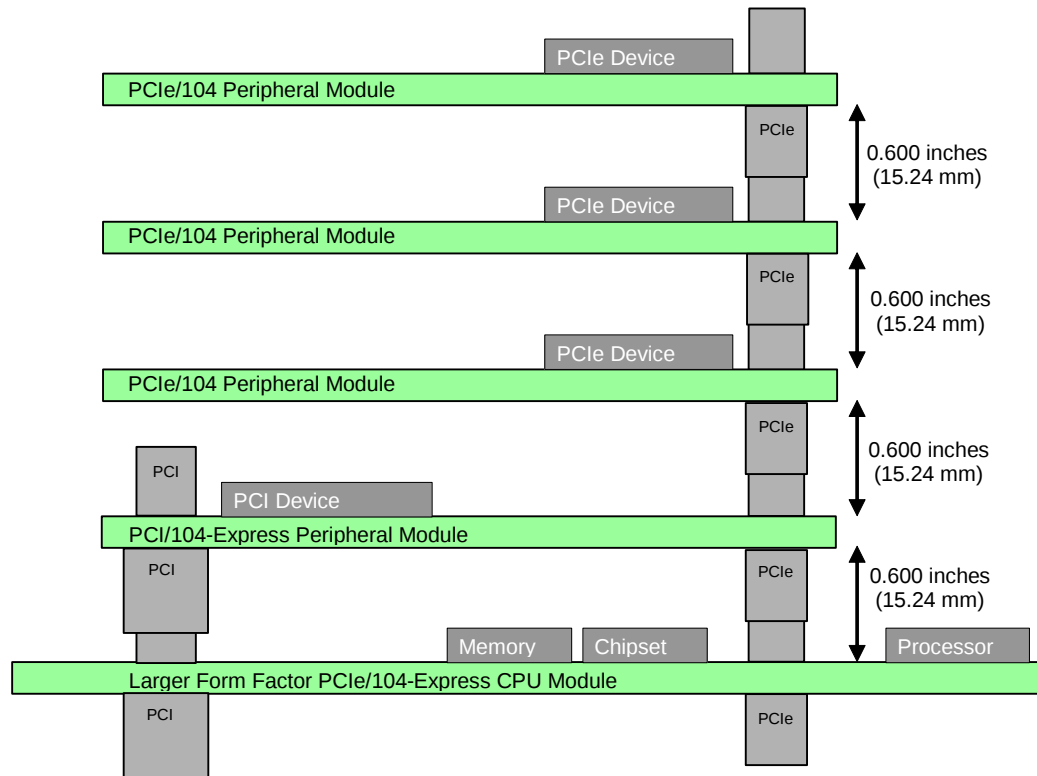
### **4.2. System Rules**

- 1) A PCI Express Link may only traverse up to six stacked PCI Express connector heights and all PCI Express modules should be on the same side of the host.
- 2) A PCIe Link may only be attached to a single connector on the Host.
- 3) A PCI bus may only traverse up to four stacked PCI connectors, and they must all be on the same side of the Host. Because of the requirements of trace length matching, all PCI Devices must be stacked together and must be next to the Host

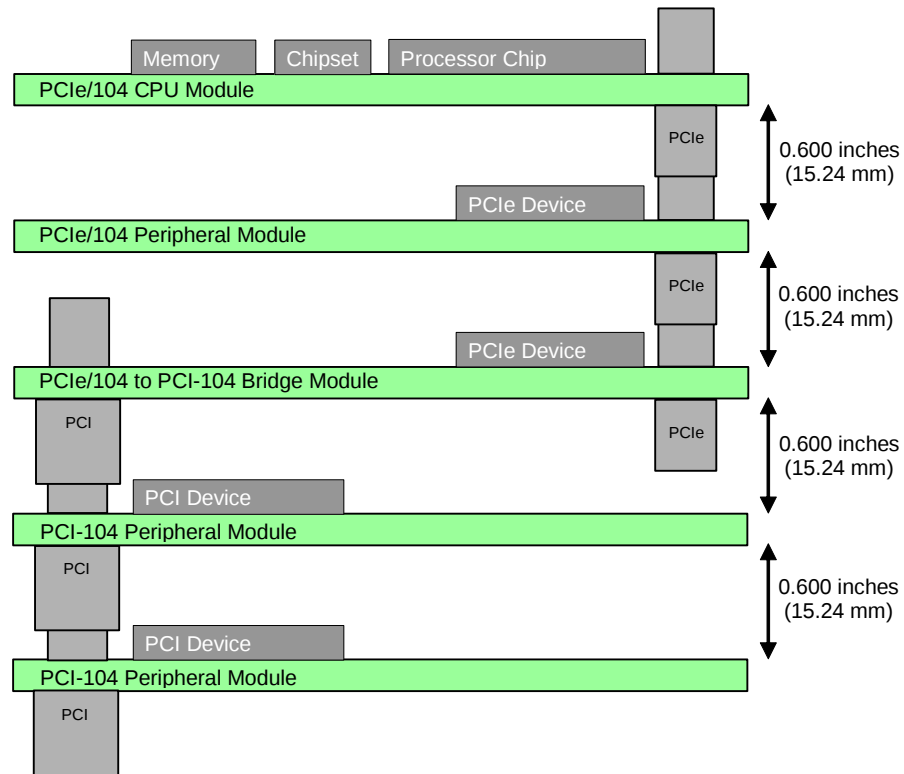
### 4.3. Stack Configuration Examples



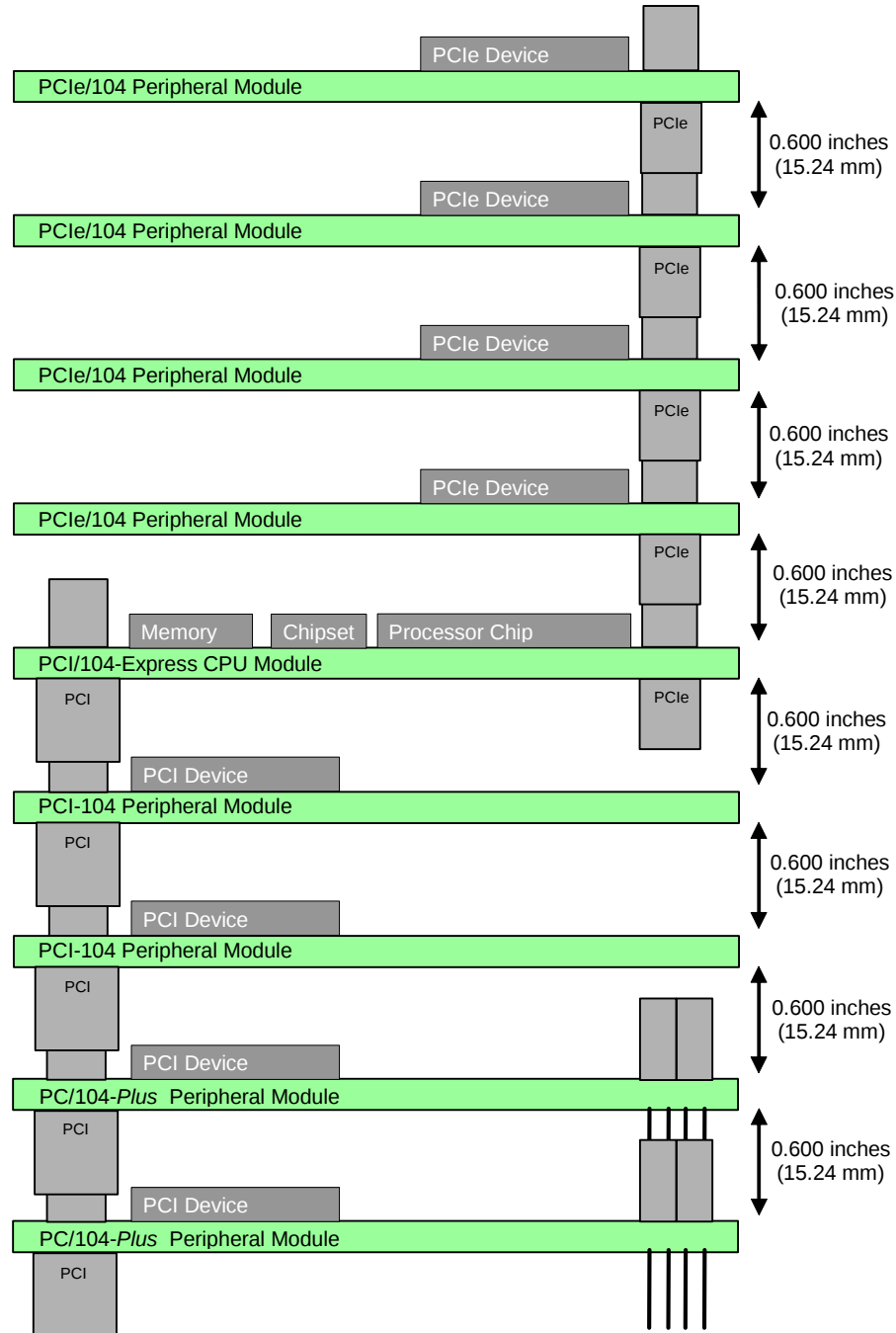
**Figure 4-1: Stack-DOWN Configuration Example**



**Figure 4-2: Stack-UP Configuration Example with Large Form Factor Host Baseboard**



**Figure 4-3 PCIe/104 with a PCI Express to PCI Bridge**



**Figure 4-4: Combined Stack-UP and Stack-DOWN Configuration Example**

Because of the requirement that each type of bus must completely reside on one side of the Host in order to avoid bus splits, only PCI-104 and PCIe/104 modules can be used in this configuration. In this example all of the PCI-104 boards are on the bottom side of the Host and all of the PCIe/104 modules are on the top side of the Host. The reverse configuration is also valid.

## 5. ELECTRICAL SPECIFICATION

### 5.1. Power and Ground

#### 5.1.1 Connector A Power Capabilities

Power on Connector A comes from +5Vaux, +3.3V, +5V, and +12V. The +5V and +12V are carried on central conductor planes which are dispersed among the three banks of Connector A. The +5Vaux is carried on individual pins. The current carrying capacities of the central panes and pins are shown in Table 5-1 below. Current values include a 20% industry standard de-rating factor at 85 °C. Note that at lower temperatures the current carrying capacities increase. There is a 2.9 to 1 ratio of current ground to current voltages which helps ensure good current paths.

| Voltage | Minimum Voltage (V) | Maximum Voltage (V) | Number of Pins | Current per Pin (A) | Total Current (A) | Total Power (W) |
|---------|---------------------|---------------------|----------------|---------------------|-------------------|-----------------|
| +3.3V   | 3.0                 | 3.6                 | 2              | 1.8                 | 3.6               | 11.9            |
| +5V     | 4.75                | 5.25                | 2 planes       | 8.4                 | 16.8              | 84.0            |
| +12V    | 11.40               | 12.60               | 1 plane        | 8.4                 | 8.4               | 100.8           |
| +5V_SB  | 4.75                | 5.25                | 2              | 1.8                 | 3.6               | 18.0            |
| GND     | n/a                 | n/a                 | 46             | 1.8                 | 82.8              | n/a             |

**Table 5-1: Connector A Power Delivery**

Standby power is supplied for wake capabilities. Because of the limited amount of power available during standby, it is important for Device cards to be designed to minimize power consumption from the standby rail. Note that during full power operation, the voltage on the Standby rail may exceed the voltage on the +5V rail. Therefore, if powering devices from both the standby and the +5V rail, care must be taken not to exceed the current limits of the Standby rail during normal operation.

The +12V rail is intended to provide additional power for high power devices

#### 5.1.2 Connector B Power Capabilities

| Voltage            | Minimum Voltage (V) | Maximum Voltage (V) | Number of Pins | Current per Pin (A) | Total Current (A) | Total Power (W) |
|--------------------|---------------------|---------------------|----------------|---------------------|-------------------|-----------------|
| +3.3V <sup>1</sup> | 3.00                | 3.60                | 10             | 1.0                 | 10.0              | 33.0            |
| +5V                | 4.75                | 5.25                | 8              | 1.0                 | 8.0               | 40.0            |
| +12V               | 11.4                | 12.6                | 1              | 1.0                 | 1.0               | 12.0            |
| -12V               | -12.6               | -11.4               | 1              | 1.0                 | 1.0               | 12.0            |
| GND                | n/a                 | n/a                 | 23             | 1.0                 | 23.0              | n/a             |

**Table 5-2: Connector B Power Delivery**

#### 5.1.3 Total PCI/104-Express Power Capabilities

| Voltage     | Minimum Voltage (V) | Maximum Voltage (V) | Total Current (A) | Total Power (W) |
|-------------|---------------------|---------------------|-------------------|-----------------|
| +3.3V       | 3.00                | 3.60                | 13.6              | 44.9            |
| +5V         | 4.75                | 5.25                | 24.8              | 124.0           |
| +12V        | 11.40               | 12.60               | 9.4               | 112.8           |
| -12V        | -12.6               | -11.4               | 1.0               | 12.0            |
| +5V Standby | 4.75                | 5.25                | 3.6               | 18.0            |
| GND         | n/a                 | n/a                 | 105.8             | n/a             |

**Table 5-3: Combined Connector A and B Power Delivery**

#### **5.1.4 Total PCIe/104 Power Capabilities**

Since PCIe/104 only utilizes Connector A, see Section 5.1.1 for total PCIe/104 power capabilities.

### **5.2. AC/DC Signal Specifications**

#### **5.2.1 Stackable PCI Express Expansion Bus**

For full details on the electrical requirements for the PCIe bus, reference the *PCI Express Base Specification* referenced in Section 1.5.

##### **5.2.1.1 Power and Ground Pins**

Power and ground planes are shared among all of the interfaces on Connector A. See Section 2 for more details.

#### **5.2.2 Stackable PCI Expansion Bus**

For full details on the electrical requirements for the stackable PCI bus, reference the *PC/104-Plus* or *PCI-104 Specifications* referenced in Section 1.5.

##### **5.2.2.1 Power and Ground Pins**

Power and ground planes are shared among all of the interfaces on Connector A. See Section 2 for more details.

#### **5.2.3 System Management Bus (SMBus)**

For full details on the electrical requirements for the SMBus, reference the *System Management Bus (SMBus) Specification* referenced in Section 1.5.

##### **5.2.3.1 Power and Ground Pins**

Power and ground planes are shared among all of the interfaces on Connector A. See Section 2 for more details.

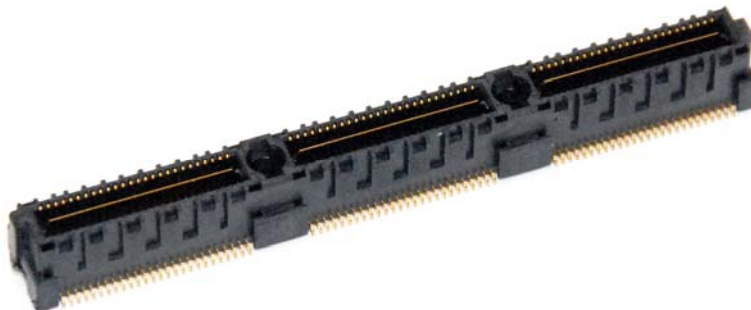
## 6. MECHANICAL SPECIFICATIONS

### 6.1. Connector A

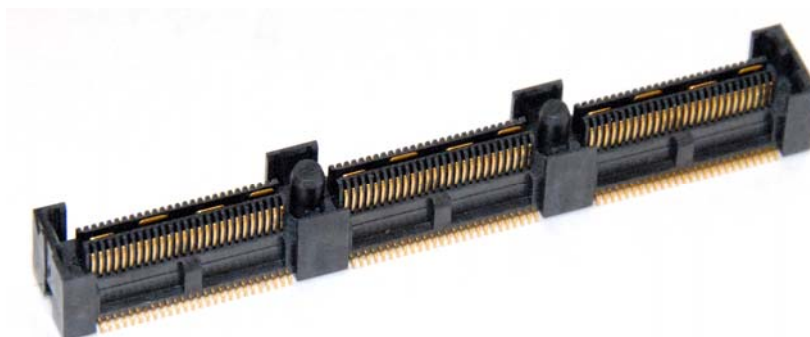
The QMS/QFS series connectors from Samtec's High Speed Interface line were designed for PC/104's 0.600 inch (15.24mm) stacking height and standoff tolerances. An equivalent connector can be used.

#### 6.1.1 Part Number

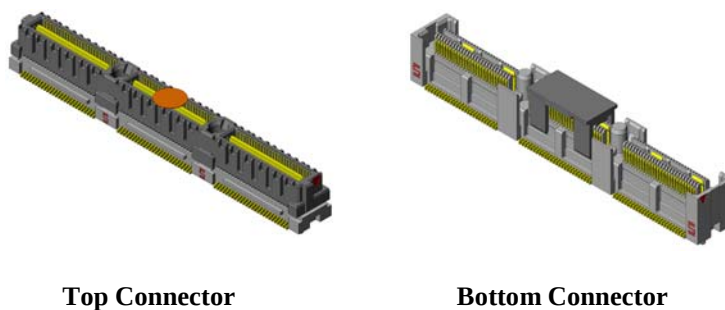
Top Connector: ASP-129637-03 with 0.600 inch (15.24 mm) stack height based on QMS or equivalent  
Bottom Connector: ASP-129646-03 with 0.600 inch (15.24 mm) stack height based on QFS or equivalent



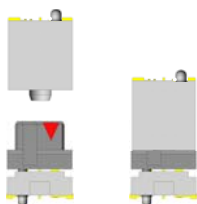
**Figure 6-1: Top Connector ASP-129637-03 or equivalent**



**Figure 6-2: Bottom Connector ASP-129646-03 or equivalent**



**Figure 6-3: Top Half and Bottom Half of Connector A Shown with Pick-and-Place Adapters**



**Figure 6-4: Mating of Top Half and Bottom Half of Connector A**

## **6.1.2 Connector A Specifications**

### **MATERIALS**

|                                   |                          |
|-----------------------------------|--------------------------|
| Housing:                          | Liquid Crystal Polymer   |
| Terminal & Ground Plane Material: | Phosphor Bronze          |
| Terminal Plating:                 | Au over 50μ" (1.27μm) Ni |
| Plane Plating:                    | Au over 50μ" (1.27μm) Ni |
| Terminal and Plane Tails:         | Tin                      |

### **CONTACT FINISH**

|                     |         |
|---------------------|---------|
| Socket Interface:   | 30μ" Au |
| Terminal Interface: | 30μ" Au |
| Underplate:         | 50μ" Ni |

### **MECHANICAL PERFORMANCE**

|                                     |                                          |
|-------------------------------------|------------------------------------------|
| Insertion Force:                    | 13.9 lbs initial & 16.8 lbs @ 100 cycles |
| Withdrawal Force:                   | 9.8 lbs initial & 10.0 lbs @ 100 cycles  |
| Normal Force @ nominal deflection:  | 69 grams                                 |
| Minimum stacking size:              | 14.8mm                                   |
| Nominal stacking size:              | 15.24mm                                  |
| Maximum stacking size:              | 15.50mm                                  |
| Contact wipe (at nom. Height):      | .044" [1.22mm]                           |
| Ground Plane wipe (at nom. Height): | .059" [1.50mm]                           |
| Durability:                         | 50 cycles                                |
| Operating Temp:                     | -55 °C to 125 °C                         |

### **ELECTRICAL PERFORMANCE**

|                                      |                                                                    |
|--------------------------------------|--------------------------------------------------------------------|
| Positions                            | Three banks of 52 pins and 1 plane for 156 total pins and 3 planes |
| Contact Resistance (initial):        | 30 mOhms                                                           |
| Contact Resistance (@ 1,000 cycles): | 50 mOhms                                                           |
| Contact Current Capacity:            | 1.8A at 85 °C and with 20% Industry Standard Derating Factor       |
| Ground Plane Resistance:             | 0.5 mOhms                                                          |
| Ground Plane Current Capacity:       | 8.4A at 85 °C and with 20% Industry Standard Derating Factor       |
| Dielectric Withstanding Voltage:     | 900 VAC                                                            |
| Working Voltage:                     | 300 VAC                                                            |
| Insulation Resistance:               | 50,000 megaOhms                                                    |

### **SOLDERABILITY**

|                                 |                                                |
|---------------------------------|------------------------------------------------|
| Maximum Processing Temperature: | 230 °C for 60 seconds or 260 °C for 20 seconds |
|---------------------------------|------------------------------------------------|

### **HIGH FREQUENCY PERFORMANCE**

|                                          |                                  |
|------------------------------------------|----------------------------------|
| Differential Pair Impedance              | 100 Ohms nominal +/- 10%         |
| Single-Ended Impedance                   | 50 Ohms nominal +/- 10%          |
| Differential Return Loss (SDD11):        | -15dB @ 1.25 GHz; -8dB @ 5 GHz   |
| Differential Insertion Loss (SDD21):     | -1dB @ 1.25 GHz; -3dB @ 5 GHz    |
| Differential Near End Crosstalk (SDD31): | -45dB @ 1.25 GHz; -35dB @ 5 GHz  |
| Differential Far End Crosstalk (SDD41):  | -45dB @ 1.25 GHz; -25 dB @ 5 GHz |



### 6.1.3 ASP-129637-03 or equivalent (Top Connector) Mechanical Drawings

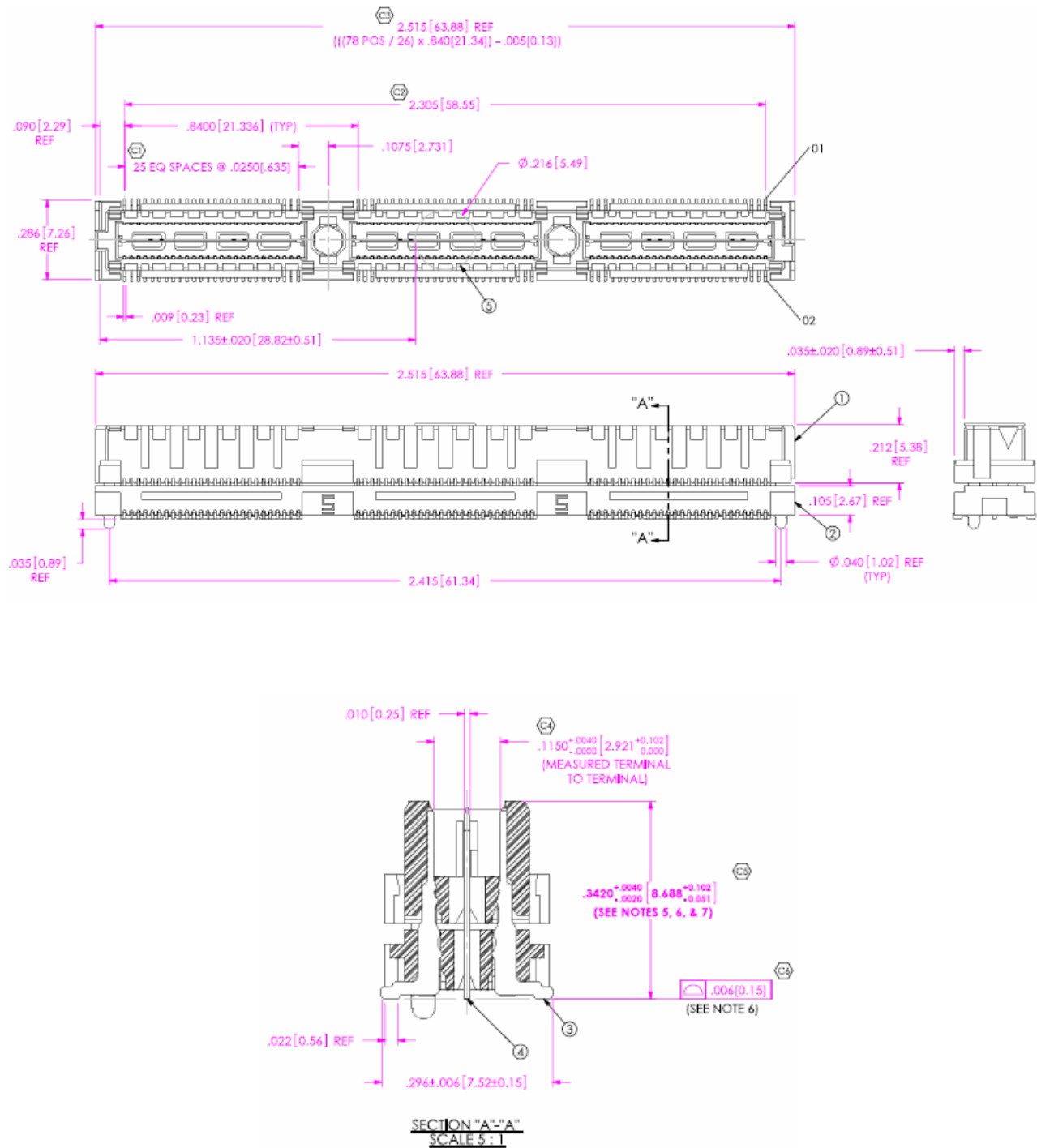
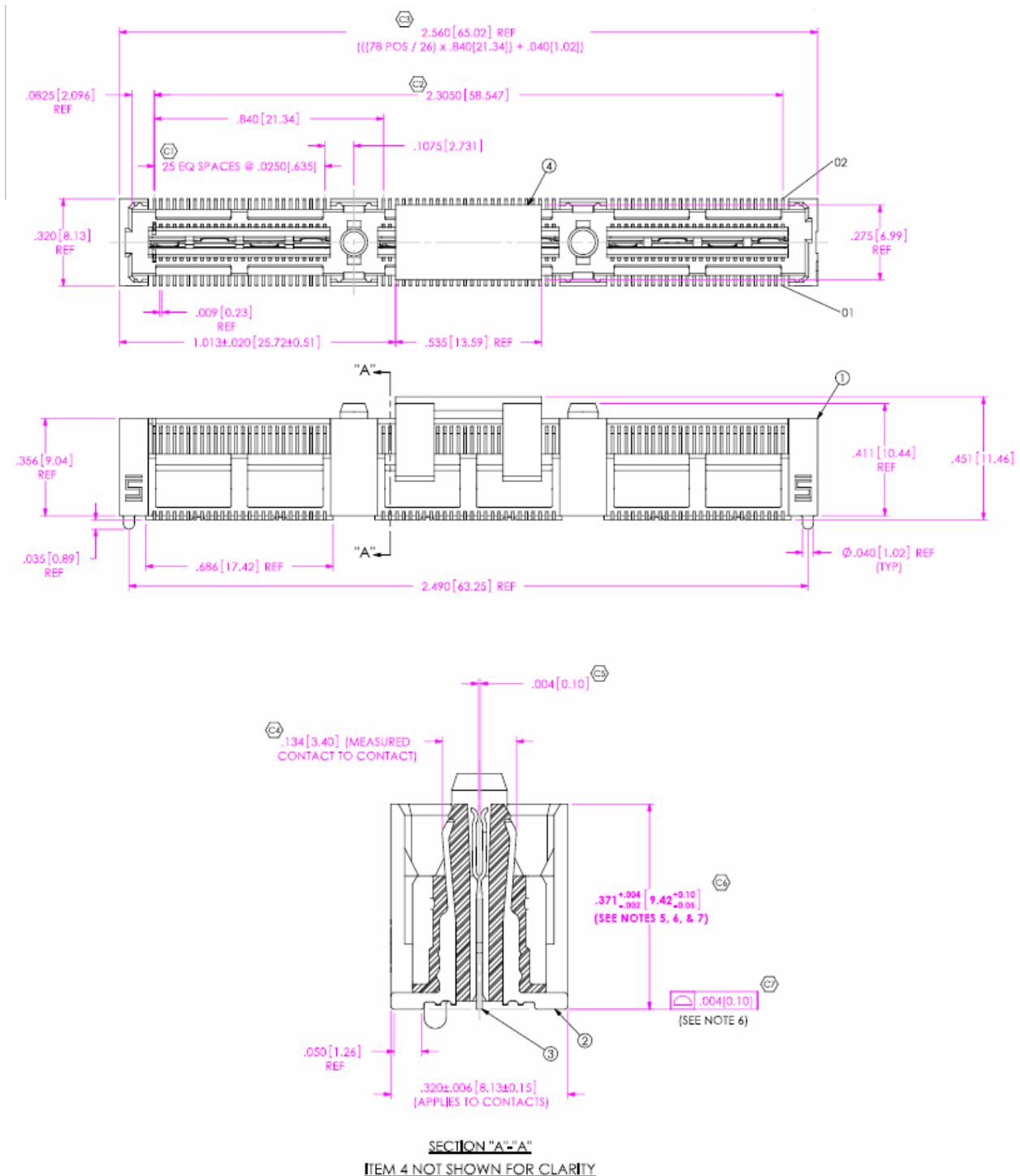


Figure 6-5: ASP-129637-03 or equivalent Mechanical Drawings

## 6.1.4 ASP-129646-03 or equivalent (Bottom Connector) Mechanical Drawings



**Figure 6-6: ASP-129646-03 or equivalent Mechanical Drawings**

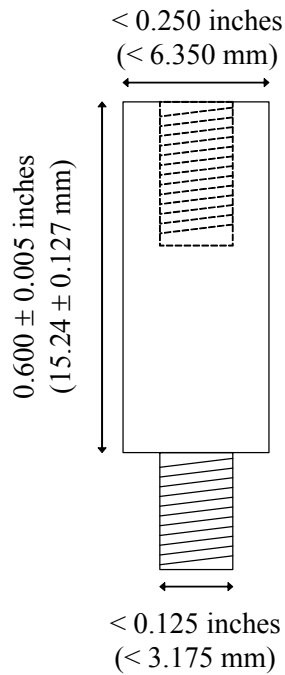
## 6.2. Connector B

Connector B is the standard PCI bus that is used on PC/104-*Plus* and PCI-104 modules. See the PC/104-*Plus* or PCI-104 Specification for mechanical specification details of the connector.

## 6.3. Standoff

Standoffs are used to ensure stacked boards retain their connectivity. The standoffs are preferably made from stainless-steel to provide for maximum strength and height tolerance. Pads must be provided for the standoffs, with the same plating as the pads for the PCIe connectors.

All critical dimensions are listed. It is up to the user to define the thread typed. The height of the standoff shall be  $0.600'' \pm 0.005''$ . The width of the standoff must be able to fit on the Standoff pad called out on the Board Layout & Dimensions Section. The width of the threaded section must be able to fit into the standoff pad hole called out in the Board Layout & Dimensions Section.

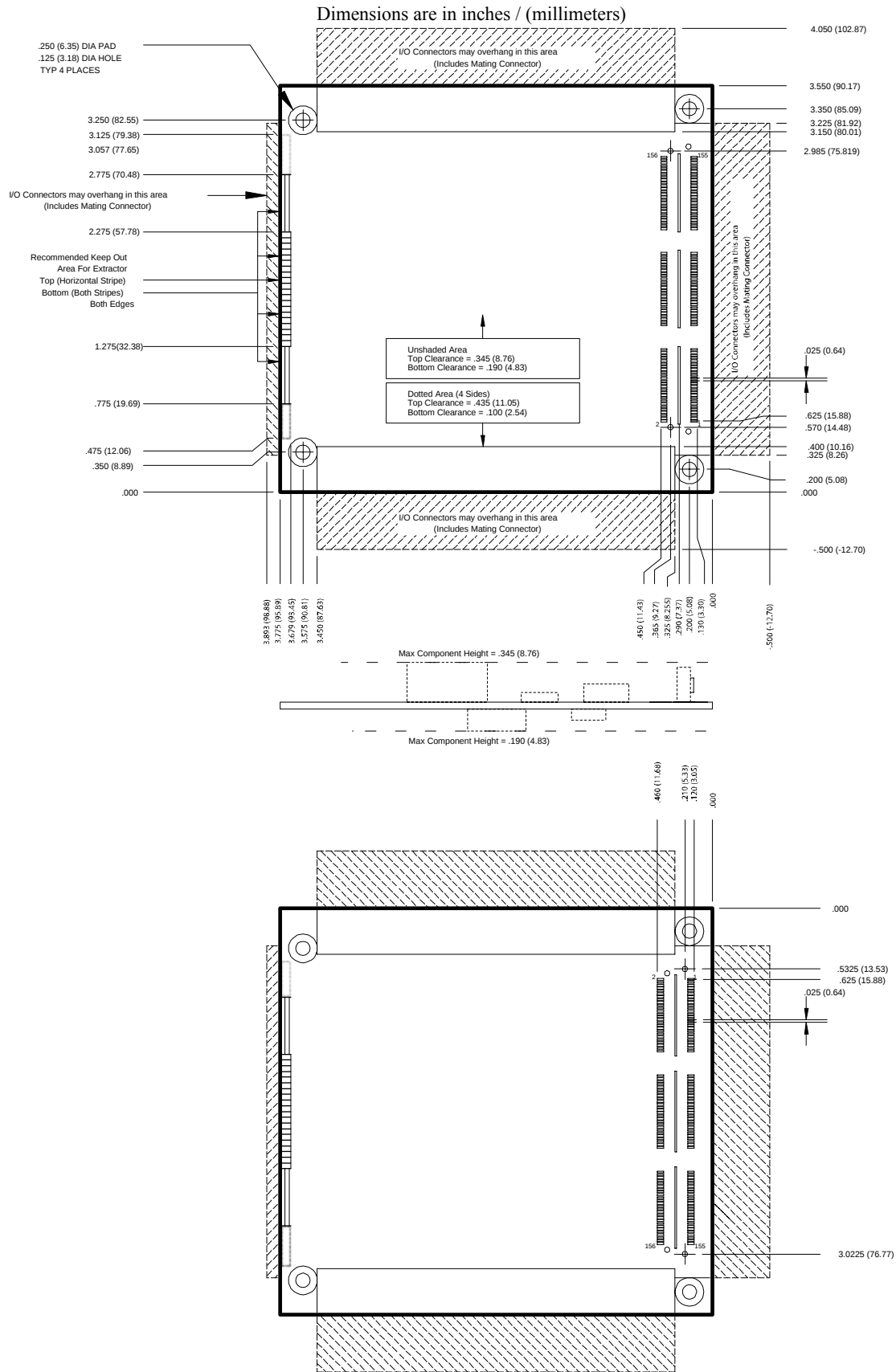


**Figure 6-7: Standoff Mechanical Dimensions**

## **6.4. Board Layout & Dimensions**

### **6.4.1 PCIe/104 Layout & Dimensions**

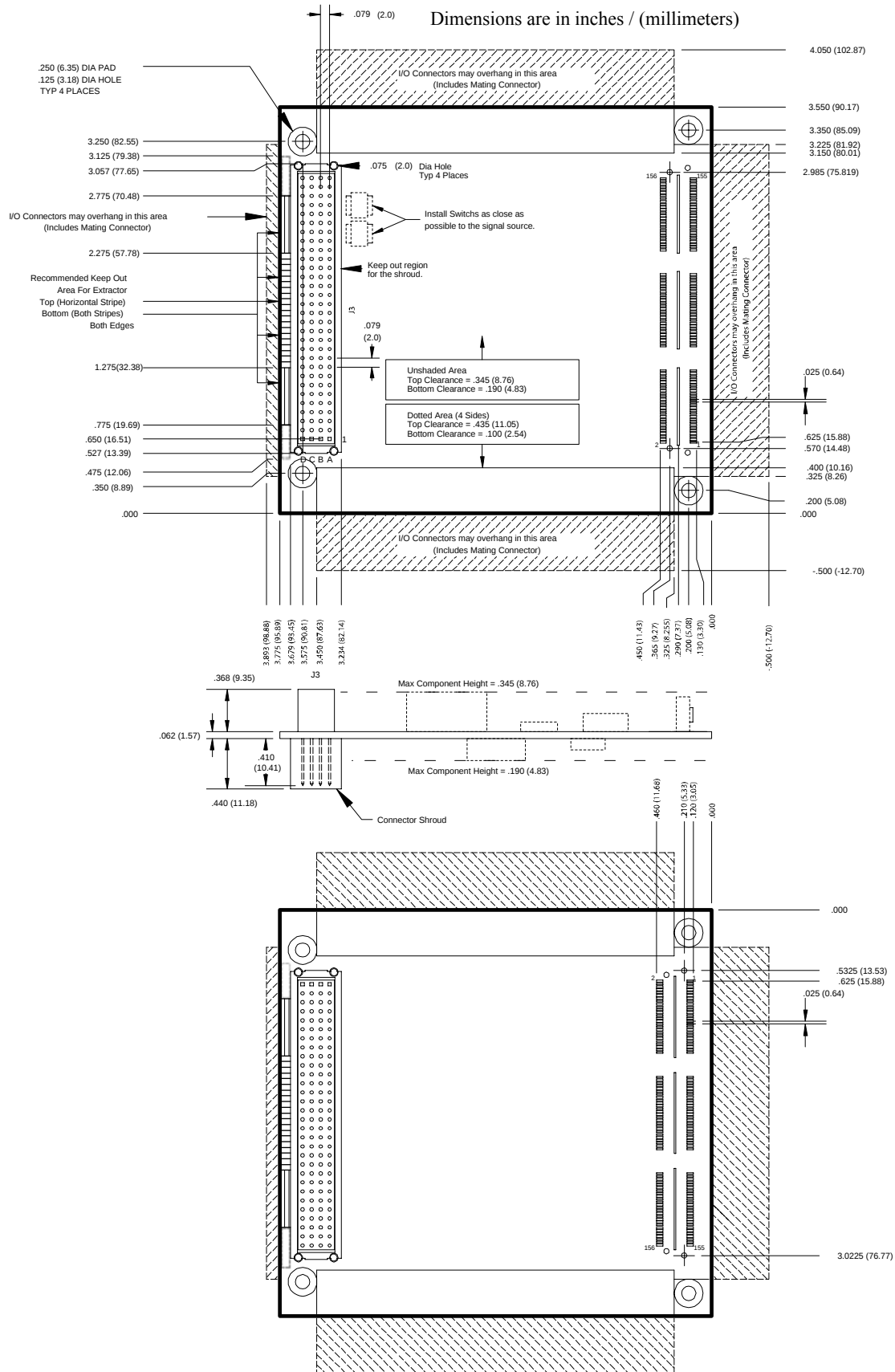
The outer mechanical dimensions for this module are identical to PCI/104-Express Specification with the exception of the removal of the PCI connector and some modifications to the I/O connector area.



**Figure 6-8 PCIe/104 Module Dimensions**

## **6.4.2 PCI/104-Express Layout & Dimensions**

The outer mechanical dimensions for this module are identical to PC/104-*Plus* Specification with the exception of the added connector (J3) and some modifications to the I/O connector area, and changes to the component height restrictions. The component height on the top has been reduced from 0.435" to 0.345" and the bottom has been increased from 0.100" to 0.190". Exceptions are the three regions on the sides of the module (indicated by the dotted region in Figure 6-9 which have a maximum height of 0.435" for the top and 0.100" for the bottom.



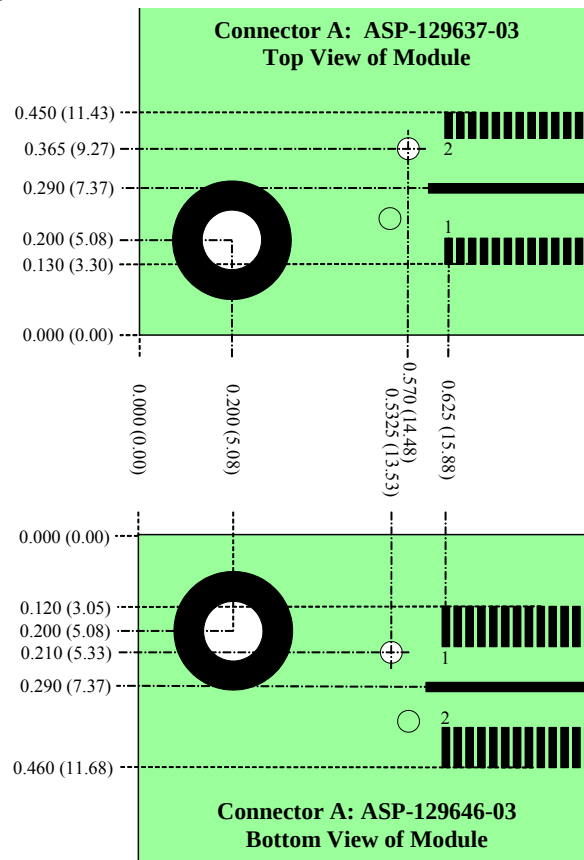
**Figure 6-9 PCI/104-Express Module Dimensions**

### 6.4.3 Connector A Placement Details

Since the QFS (ASP-129646-03) connector is larger than the QMS (ASP-129637-03), the QFS was used to determine the placement of both the QFS and the QMS. The maximum width of the QFS is determined by the recommend solder pad size and placement which is larger than the outer plastic dimensions of the QFS connector. The connector was lined up so that the base of the bottom solder pad lined up with the bottom of the AT ISA connector found on the PC/104 and PC/104-*Plus* form factors. This allows the retention of the traditional keep out region. With this placement the centerline of the connector (which placement should be based on) is located at 0.310 inches (7.874 mm) from the edge of the board.

The horizontal positioning of the QFS connector was calculated by positioning it in the center of the PCB and rounding off to a reasonable even multiple of 0.025 inches (0.635 mm) since this is the distance between two solder pads. The result was the first solder pad being located 0.625 inches (15.875 mm) from the left edge of the PCB as shown in Figure 6-10.

With the placement of the topside QFS connector, the QMS connector placement points are determined. The vertical placement point for the QMS is the same as that for the QFS which is 0.310 inches (7.874 mm) from the edge of the PCB to the center ground planes of the connector.



**Figure 6-10: Top Side and Bottom Side Views of Connector Placements**

Dimensions are in inches / [millimeters]

## **APPENDIX A: PC/104 BRIDGE CARD**

Maintaining the stackable PCI bus was chosen over the stackable ISA bus for two reasons. First, many current and most future modern chipsets support both PCI and PCIe. None support ISA. Second, backward compatibility to PC/104, PC/104-*Plus*, and PCI-104 is easier to achieve if the stackable PCI bus is retained over the stackable ISA bus.

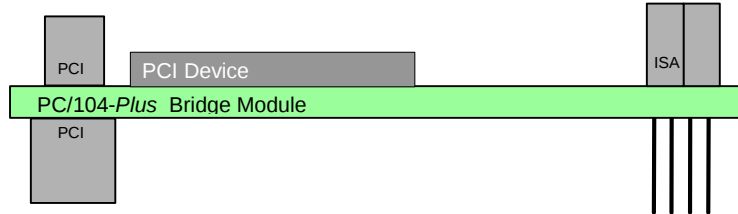
If PCIe/104 maintained the stackable ISA bus, the natural position for the stackable PCIe bus would be in the location of the stackable PCI bus as is found on the PC/104-*Plus* specification. In order to be backward compatible with PC/104-*Plus* and PCI-104 modules, a PCIe-to-PCI bridge module would need to be created because you cannot realize a PCI bus through an ISA. The problem with this scheme is that the stackable PCI bus and the stackable PCIe bus are competing in the same location. And since the stackable PCI bus uses a stack-through connector, you cannot have both the stackable PCIe connector and the stackable PCI connector on the same bridge board. Thus, a two board bridge module is required. This has potential power and signal integrity issues when routing over such large distances.

To realize the stackable ISA bus, one merely needs to create a single board PCI-to-ISA bridge module using off-the-shelf PCI-to-ISA bridge chips or FPGA cores. This will get a basic ISA bus without DMA or IRQs. With the addition of three signals (SDMA\_REQ, SDMA\_GNT, and SIRQ) which are present on many chipsets and can be cabled to a bridge board, a full ISA bus can be realized for complete backward compatibility to all PC/104 specifications without any mechanical or electrical interference or deficiency issues.

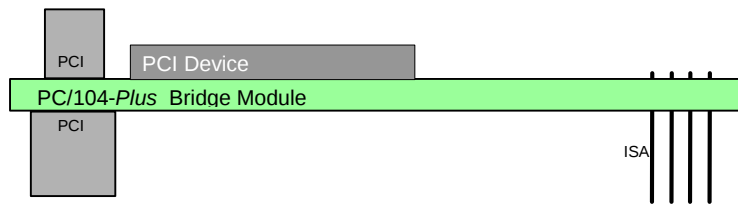
And since the ISA bus is created using a PCI-to-ISA bridge chip, it is a natural electrical and mechanical extension to create the ISA bus off of the PCI expansion bus to support the number of ISA legacy cards already on the market. If the ISA bus was retained then creating a PCI bus off of the PCIe bus would be easy electrically, but mechanically you have problems because the both the PCI expansion bus and the PCI Express expansion bus would reside in the same location. This would then require a two board solution to support the number of PC/104-*Plus* and PCI-104 cards already on the market.

## A.1 Bridge Module Configurations

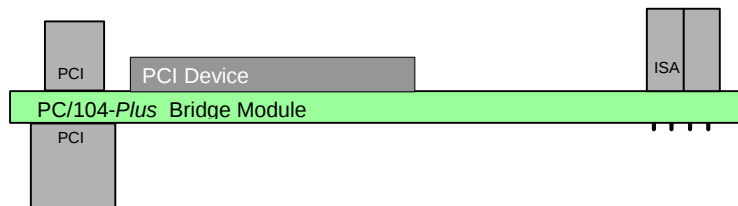
The PCI-to-ISA Bridge module has three possible configurations: Basic, Stack-UP only, and Stack-DOWN Only. Because of the heights of the Q2 (PCI/104-Express and PCIe/104) connectors and the ISA Bus (PC/104-*Plus*) connector and because they reside in the same general location, interference can occur if a PCI-to-ISA Bridge module is placed next to PCI/104-Express or PCIe/104 module.. In this case a Stack-UP Only or a Stack-DOWN Only version must be used. If there is a PCI-104 module between the PCI-to-ISA Bridge module and a PCI/104-Express or PCIe/104 module then a Basic configuration can be used.



**Figure 6-11: Basic Configuration of the PCI-to-ISA Bridge Module**

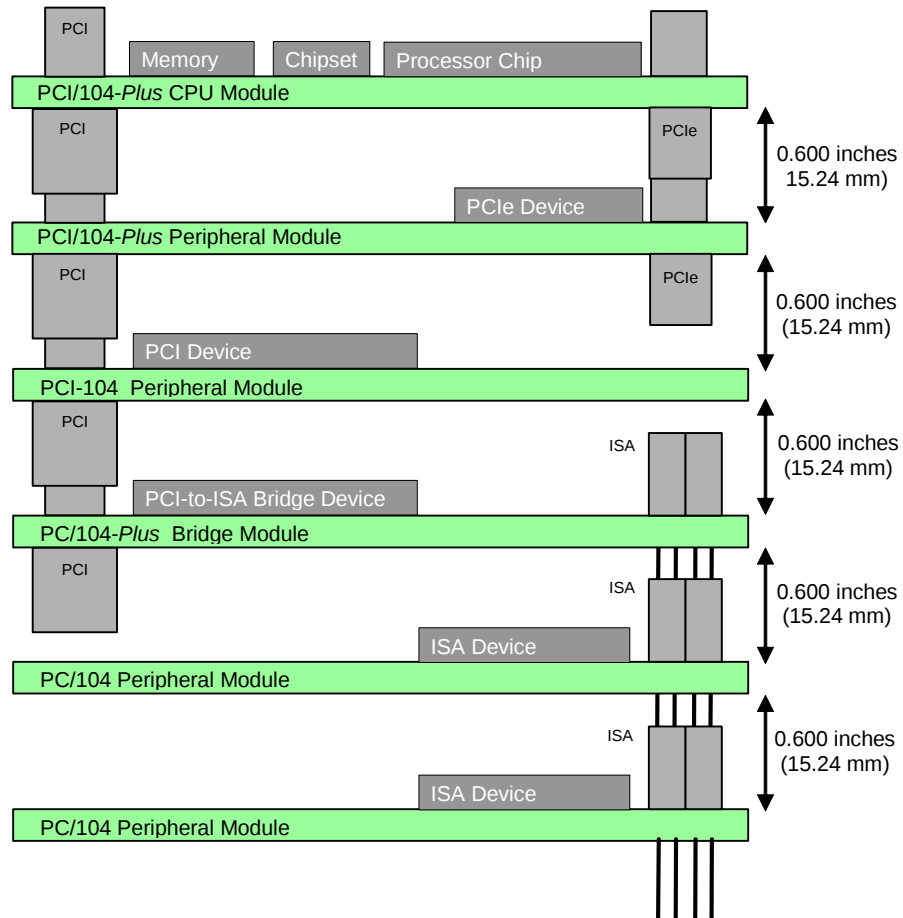


**Figure 6-12: Stack-DOWN Configuration of the PCI-to-ISA Bridge Module**

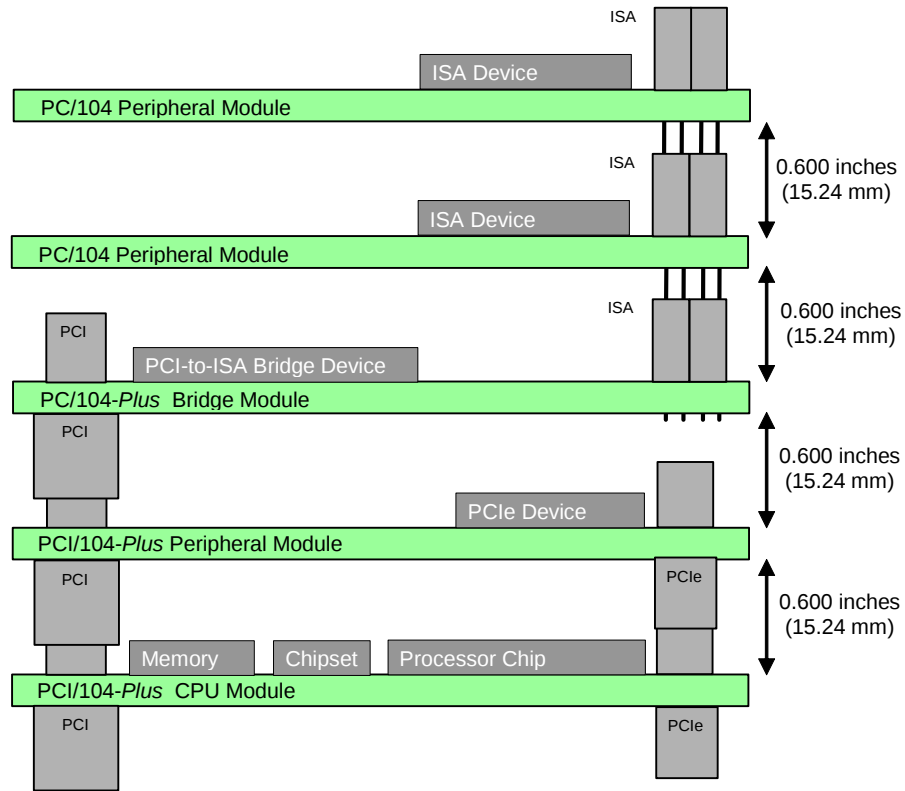


**Figure 6-13: Stack-UP Configuration of the PCI-to-ISA Bridge Module**

## A.2 Stack Configuration Examples



**Figure 6-14: Stack-DOWN Configuration Example**



**Figure 6-15: Combined Stack-UP Configuration Example**

## APPENDIX B: EPIC FORM FACTOR

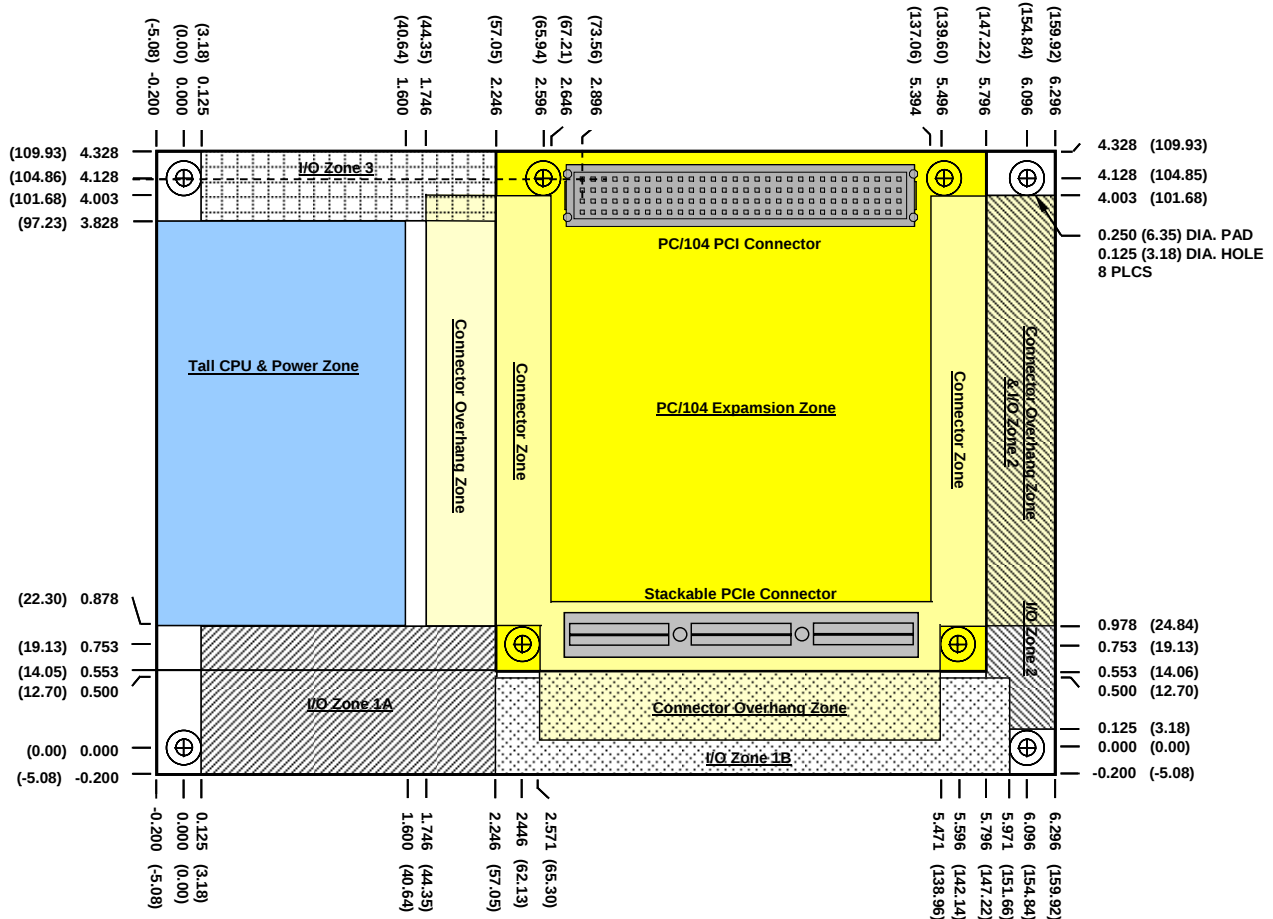


Figure 6-16: EPIC with PCI/104-Express

## APPENDIX C: EBX FORM FACTOR

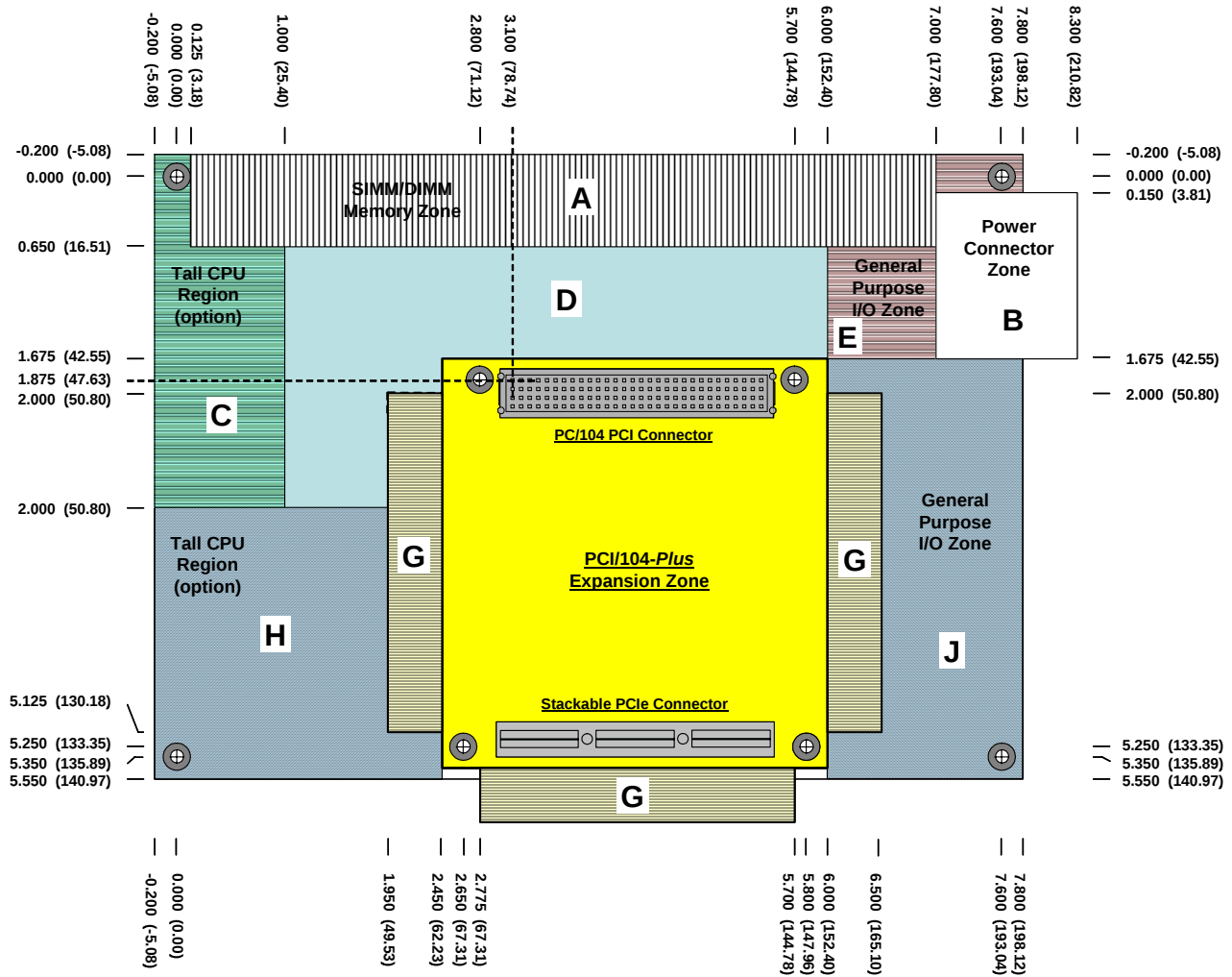


Figure 6-17: EBX with PCI/104-Express