LittleBoard™ 620
Single Board Computer
Reference Manual

P/N 50-1Z033-1000 Revision 1.0

Notice Page

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REVISION HISTORY

Revision	Reason for Change	Date
A, A	Initial Release	Nov/07
A, B	Added header pinouts to hardware chapter	June/08
B, A	Added SATA interface; changed default of JP19 in table 2-3; revised RS-422/RS-485 info in ch 3; added PCI to ISA bridge section to ch 4	May/09
1.0	Revised Fig 3-2 pin numbering; removed all references to RS-422 from manual; revised the document part number to 50-1Z033-1000	Nov/09

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Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

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Chapter 1 About This Manual

Purpose of this Manual

This manual is for designers of systems based on the LittleBoard™ 620 single board computer (SBC). This manual contains information that permits designers to create an embedded system based on specific design requirements.

Information provided in this reference manual includes:

- LittleBoard 620 specifications
- Environmental requirements
- Major integrated circuits (chips) and features implemented
- LittleBoard 620 connector/pin numbers and definitions
- BIOS Setup information

Information not provided in this reference manual includes:

- Detailed chip specifications
- Internal component operation
- Internal registers or signal operations
- Bus or signal timing for industry standard busses and signals

References

The references in the following list may be helpful for you to complete your design successfully.

Specifications:

- EBX Spec Revision 2.0, March 1 2005

  For the latest version of the EBX specifications, contact the PC/104 Consortium, at:

  Web site: http://www.pc104.org
- PC/104 Spec Revision 2.5, November 2003
- PC/104-Plus Spec Revision 2, November 2003

  For latest revision of the PC/104 specifications, contact the PC/104 Consortium, at:

  Web site: http://www.pc104.org
- PCI 2.2 Compliant Specifications

  For latest revision of the PCI specifications, contact the PCI Special Interest Group Office at:

  Web site: http://www.pcisig.com

Chip specifications used on the LittleBoard 620:

- AMD, Inc., Geode LX 800 processor (with integrated Northbridge)

  Web site:

  http://www.amd.com/files/connectivitysolutions/geode/geode_lx/33234F_LX_databook.pdf
- AMD, Inc. CS5536, used for the I/O Hub (Southbridge)

  Web site:
  http://www.amd.com/files/connectivitysolutions/geode/geode_lx/33238G_cs5536_db.pdf

- Intel Corporation and the 82551QM and 82551ER chips, used as Ethernet 1 and Ethernet 2 controllers, respectively.

  Web site: http://www.intel.com/design/network/datashts/82551QM_ds.htm

  Web site: http://www.intel.com/design/network/datashts/82551ER_ds.htm

- Winbond Electronics, Corp. and the W83627HG chip used as the Super I/O controller

  Web site: http://www.winbond-usa.com/products/winbond_products/pdfs/PCIC/W83627HF_F_HG_Ga.pdf

- Realtek and the ALC203-LF chip, used for the Audio CODEC.

  Web site: http://www.realtek.com.tw/search/default.aspx?keyword=alc203

- ITE Tech. Inc. and the IT8888G chip, used for the PCI-to-ISA bridge conversion.

  Web site: http://www.ite.com.tw/EN/products_more.aspx?CategoryID=3&ID=5,76

NOTE If you are unable to locate the datasheets using the links provided, copy the whole link into your web address bar and press enter. Otherwise, go to the manufacturer's web site where you should be able to perform a search using the chip datasheet number or name listed, including the extension, htm, pdf, etc.

Chapter 2 Product Overview

This introduction presents general information about the EBX architecture and the LittleBoard 620 single board computer (SBC). After reading this chapter you should understand:

- EBX Architecture
- LittleBoard 620 architecture
- LittleBoard 620 features
- Major components
- Connectors
- Jumper definitions
- Specifications (physical, environmental, power, cooling)

EBX Architecture

The “Embedded Board, eXpandable” (EBX) standard is the result of a collaboration between industry leaders, Motorola and Ampro, to unify the embedded computing industry on a full featured embedded single-board computer (SBC) standard. The EBX standard principally defines physical size, mounting hole pattern, and power connector locations. It does not specify processor type or electrical characteristics. There are recommended connector placements for serial/parallel, Ethernet, graphics, and memory expansion.

Derived from the LittleBoard form-factor originated in 1984, EBX combines a standard footprint with open interfaces. The EBX form-factor is small enough for deeply embedded applications, yet large enough to contain the functions of a fully embedded SBC (single board computer) including CPU, memory, mass storage interfaces, display controller, serial/parallel ports, today’s advanced operating systems, and other system functions. This embedded SBC standard ensures that embedded system OEMs can standardize their designs and that embedded computing solutions can be designed into space constrained environments with off-the-shelf components.

The EBX standard boasts highly flexible and adaptable system expansion, allowing easy and modular addition of functions such as additional USB 2.0 ports, Firewire or wireless networking not usually contained in standard product offerings. The EBX system expansion is based on popular existing industry standards, PC/104™ and PC/104-Plus™. PC/104 places the ISA bus on compact 3.6" x 3.8" modules with self-stacking capability. PC/104-Plus adds the power of a PCI bus to PC/104 while retaining the basic form-factor. Using PC/104 expansion cards, the PC/104 standard offers access to PC cards from the mobile and handheld computing markets.

The EBX standard integrates all these off-the-shelf standards into a highly embeddable SBC form-factor. EBX supports the legacy of PC/104, hosting the wide variety of embedded system oriented expansion modules from hundreds of companies worldwide. PC/104 brings the advantages of the latest portable and mobile system expansion technologies to embedded applications. See Figure 2-1 on page 4.

The EBX standard also brings stability to the embedded board market and offers OEMs assurance that a wide range of products will be available from multiple sources – now and in the future. The EBX standard is open to continuing technology advancements since it is processor independent. It creates opportunity for economies of scale in chassis, power supply, and peripheral devices.

The EBX specification is freely available to all interested. For further technical information on the EBX standard, go to the PC/104 Consortium web site at www.pc104.org.

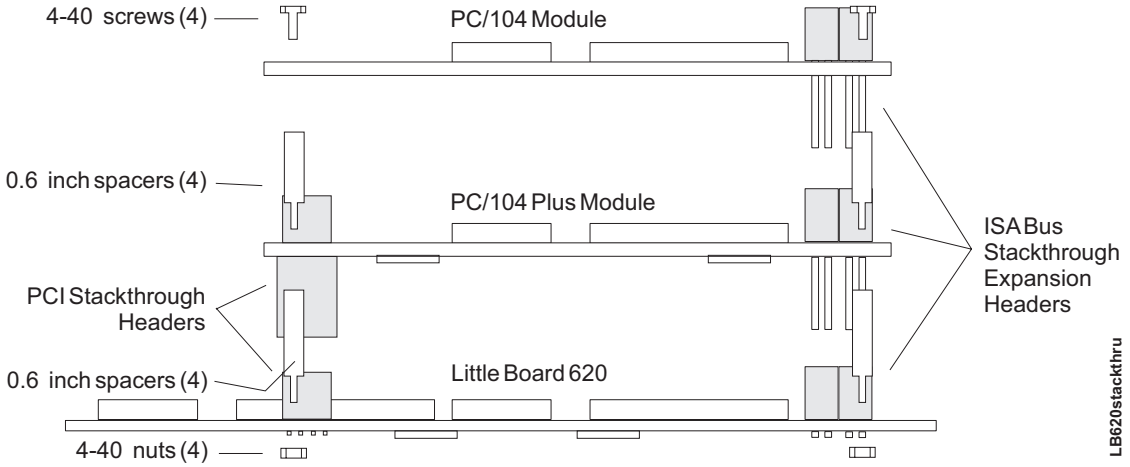

Figure 2-1. Stacking PC/104 Modules with the LittleBoard 620

Product Description

The LittleBoard 620 is an exceptionally high integration, high performance, rugged, and high quality single-board system, which contains all the component subsystems of a PC motherboard plus the equivalent of up to 3 expansion boards. Based on the AMD Geode™ LX 800 processor, the LittleBoard 620 provides designers a complete, high performance embedded processor that conforms to the EBX V2.0 specification.

Each LittleBoard 620 incorporates an AMD Geode CS5536 chipset for the Graphics and Memory Hub (the Northbridge integrated in the CPU) and the I/O Hub (Southbridge) controllers. The Winbond Electronics Corp. Super I/O controller, W83627HF, adds I/O functions. Together, the AMD and Winbond chips provide four serial ports, a floppy and EPP/ECP parallel ports, four USB 2.0 ports, PS/2 keyboard and mouse interfaces, an Ultra/DMA 33/66 IDE controller supporting two IDE drives and one Compact Flash socket, a graphics controller, which provides CRT and LVDS/TTL flat panel video interfaces, and an audio AC'97 CODEC on the board. The LittleBoard 620 also supports two 10/100BaseT Ethernet interfaces, two SATA ports (DNP on certain models), and up to 1 GB of non-ECC DDR RAM in a single 184-pin DIMM socket. To provide the ISA bus on the board through the PC/104 connector, an ITE, IT8888G, PCI-to-ISA Bridge is included.

The LittleBoard 620 can be expanded through the PC/104 and PC/104-Plus expansion for additional system functions, as these buses offer compact, self-stacking, modular expandability. The PC/104 and PC/104-Plus buses are the embedded system version of the signal set provided on a desktop PC's ISA and PCI buses at 8MHz and 33MHz clock speeds, respectively.

Among the many embedded-PC enhancements on the LittleBoard 620 that ensure embedded system operation and application versatility are a Watchdog Timer, serial console support, battery-free boot, Compact Flash disk, and OEM logo customization (Splash Screen).

The LittleBoard 620 is particularly well suited to either embedded or portable applications and meets the size, power consumption, temperature range, quality, and reliability demands of embedded system applications. It can be stacked with ADLINK MiniModules™ or other PC/104-compliant expansion boards or it can be used as a powerful computing engine.

Board Features

- CPU features
  - Provides a 500 MHz AMD Geode LX800 processor
  - 64-bit DDR memory interface up to 400 MHZ
- Memory
  - Single standard 184-pin DDR DIMM slot

- Supports +2.5V DDR RAM up to 1GB
- Supports up to PC2700 DDR 333

- PC/104-Plus Bus Interfaces
  - PCI Bus at 33MHz
  - PCI 2.2 compliant signals
  - PC/104 (ISA) Bus at 8MHz
- Serial ATA Interface (SATA) - [DNP on certain models]
  - Provides two 7-pin SATA ports
  - Provides 1.5 Gb/second data transfer rate
- IDE Interfaces
  - Provides one enhanced IDE controller
  - Supports dual bus master mode
  - Supports Ultra DMA 33/66/100 modes
  - Supports ATAPI and DVD peripherals
  - Supports IDE native and ATA compatibility modes
  - Provides Compact Flash socket (on Primary IDE bus with Master/Slave jumper)
- Floppy Disk Interface
  - Supports one standard floppy disk drive interface
  - Supports all standard PC/AT formats: 360KB, 1.2MB, 720KB, 1.44MB, 2.88MB
- Parallel Port
  - Provides a standard printer interface
  - Supports IEEE standard 1284 protocols of EPP and ECP outputs
  - Supports Bi-directional data lines
  - Supports 16 byte FIFO for ECP mode
- Serial Ports
  - Provides four buffered serial ports with full handshaking
  - Provides 16550-equivalent controllers, each with a built-in 16-byte FIFO buffer
  - Supports full modem capability on all four ports
  - Supports RS232 operation on each port
  - Supports RS232 or RS485 operation on two ports (COM1 and COM2)
  - Supports programmable word length, stop bits, and parity
  - Supports 16-bit programmable baud-rate generator and an interrupt generator
- USB Ports
  - Provides two root USB hubs
  - Provides up to four USB ports
  - Supports USB boot devices
  - Supports USB v2.0 EHCI and v1.1 OHCI
  - Supports over-current detection status

- Keyboard/Mouse Interface
  - Provides PS/2 keyboard interface
  - Provides PS/2 mouse interface
- Audio interface
  - Provides AC'97 CODEC on board
  - Supports AC'97 2.3 standard
- Ethernet Interface
  - Provides two fully independent Ethernet ports
  - Provides integrated LEDs on each port (Link/Activity and Speed)
  - Provides Intel 82551ER and 82551QM controller chips
  - Supports IEEE 802.3 10/100BaseTX compatible physical layers
  - Supports Auto-negotiation for speed, duplex mode, and flow control
  - Supports full-duplex or half-duplex mode
    - Full-duplex mode supports transmit and receive frames simultaneously
    - Supports IEEE 802.3x Flow control in full duplex mode
    - Half-duplex mode supports enhanced proprietary collision reduction mode
- Video Interfaces (CRT/TTL/LVDS)
  - Support CRT (1920 x 1440 at 85Hz and 1600 x 1200 at 100 Hz) with up to 254MB UMA (Unified Memory Architecture)
  - Provide 10-pin VGA header
  - Provide TTL, 24-bit, flat panel outputs pared with resolution up to 1600 x 1200
  - Provide LVDS flat panel outputs (single channel, five differential signals) on 30-pin header
- Miscellaneous
  - Real-Time Clock (RTC) with replaceable battery
  - Battery-free boot (Boots even if battery is dead or missing)
  - Supports both on-board or external battery for Real-Time Clock operation
  - Thermal and Voltage monitoring
  - Oops! Jumper (BIOS recovery) support
  - Serial Console
  - Watchdog Timer (WDT)
  - USB Boot
  - LAN Boot (PXE)

Block Diagram

Figure 2-2 shows the functional components of the board.

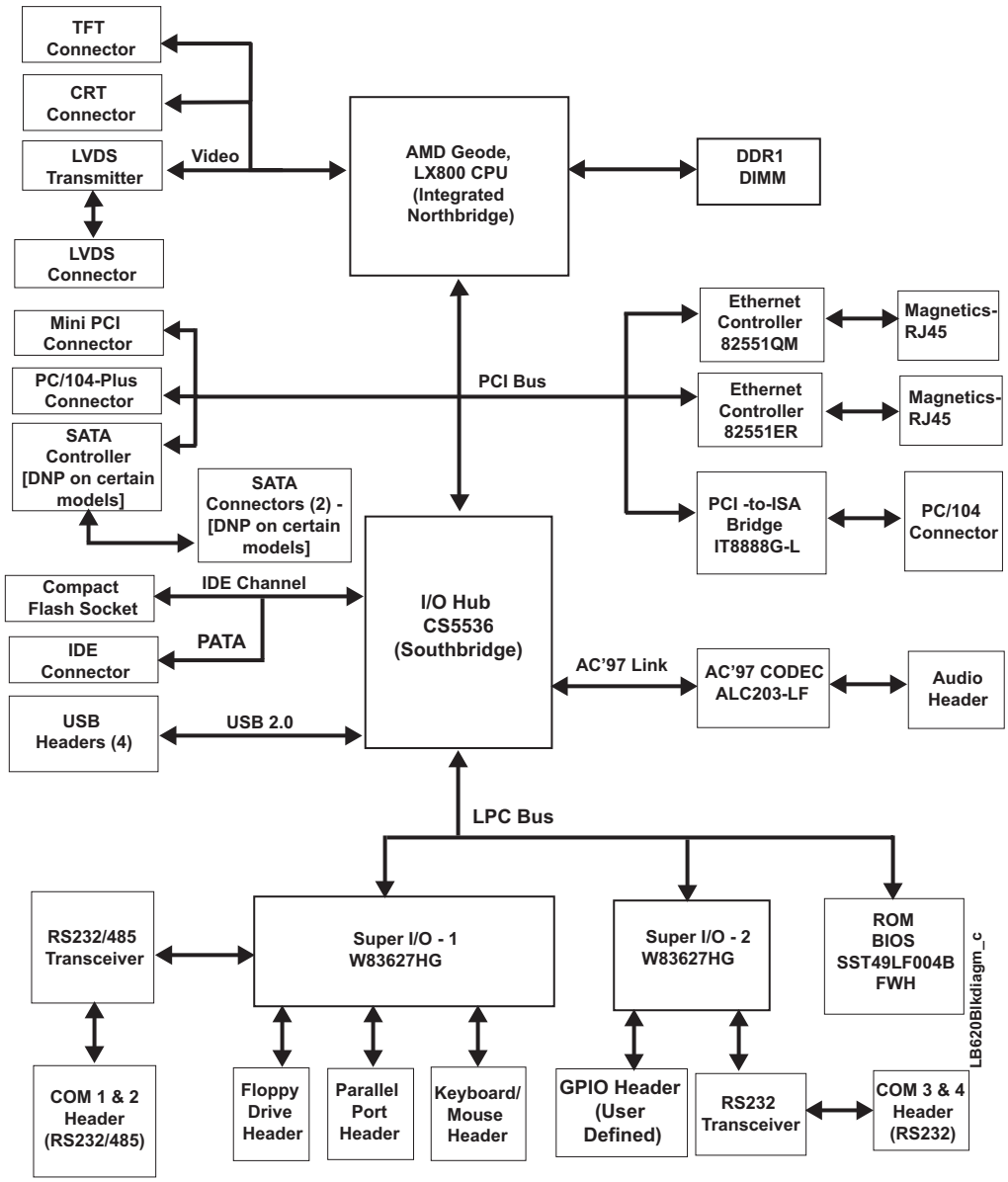

Figure 2-2. Functional Block Diagram

Major Components (ICs)

Table 2-1 lists the major ICs, including a brief description of each, on the LittleBoard 620. Figures 2-3 and 2-4 show the locations of the ICs.

Table 2-1. Major Components Descriptions and Functions

Chip Type	Mfg.	Model	Description	Function
CPU (U1)	AMD	Geode LX800	500 MHz CPU	Memory and video
I/O Hub (U3)	AMD	CS5536	Southbridge functions (provides some of standard I/O functions)	I/O Functions
Audio (U7)	Realtek	ALC203-LF	Audio '97 CODEC for Audio In/ Out signals	Audio In/Out
Super I/O 1 (U14) [See Figure 2-4]	Winbond Electronics, Corp.	W83627HG	Super I/O controller (provides Floppy, Parallel, Keyboard, and Mouse)	I/O Functions
Super I/O 2 (U16) [See Figure 2-4]	Winbond Electronics, Corp.	W83627HG	Super I/O controller (provides GPIO and RS232 transceiver)	I/O Functions
Ethernet 1 Controller (U9) [See Figure 2-4]	Intel	82551QM	Ethernet chip (provide two independent 10/100BaseT based network channels)	Ethernet functions
Ethernet 2 Controller (U11) [See Figure 2-4]	Intel	82551ER	Ethernet chip (provide two independent 10/100BaseT based network channels)	Ethernet functions
SATA Controller (U15) [See Figure 2-4 - DNP on certain models]	VIA	VT6421L	PCI-to-SATA control	I/O functions
ISA Bridge (U51) [See Figure 2-4]	ITE	IT8888G-L	PCI-to-ISA bridge conversion	ISA Bus

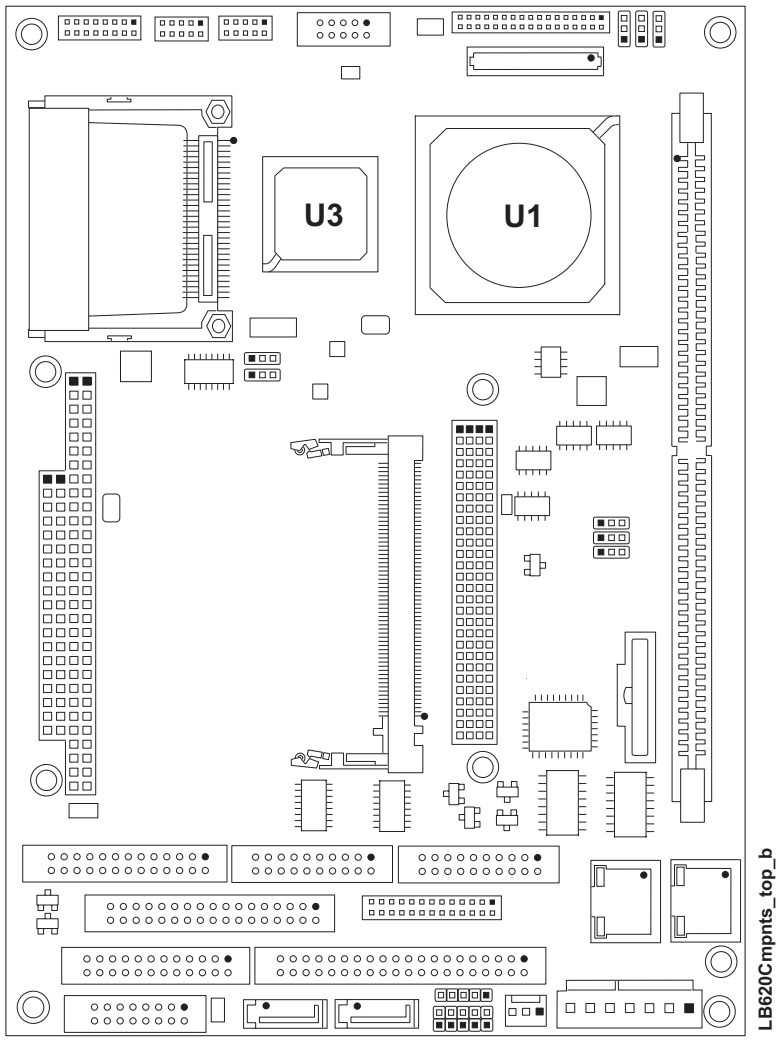

Figure 2-3. Component Location (Top view)

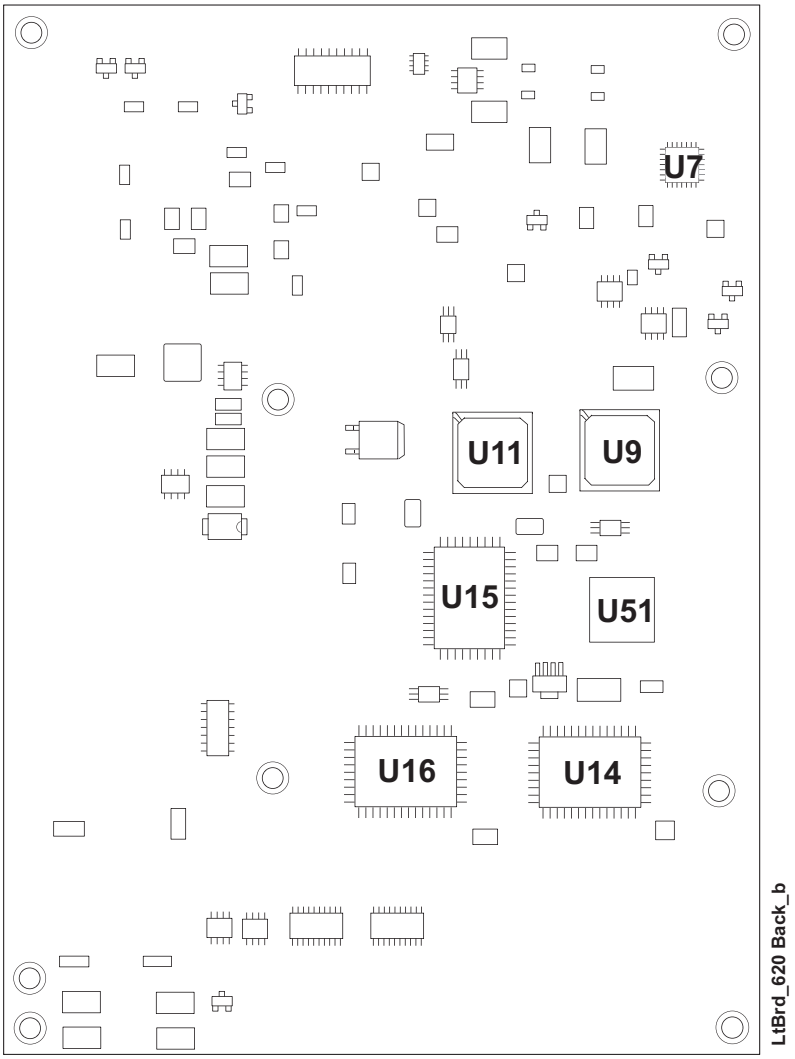

Figure 2-4. Component Locations (Bottom view)

Header Definitions

Table 2-2 describes the headers shown in Figure 2-6 on page 12. All I/O headers use 0.100" (2.54mm) pitch unless otherwise indicated. All standard headers and connectors do not indicate pitch.

Table 2-2. Header Descriptions

Jack #	Name	Description
BAT1	Battery Socket	Battery socket for 3 volt Lithium battery
DIMM1	Memory	184-pin, 0.050" (1.27mm), slot for a single DDR RAM DIMM
J1A,B, C,D	PC/104	104-pin, standard connector for ISA bus
J2A,B, C,D	PC/104-Plus	120-pin, standard connector for PCI bus
J3	CRT Video	10-pin header for output to a CRT type monitor

Table 2-2. Header Descriptions (Continued)

J5	Mini PCI	124-pin, 0.032" (0.80mm) connector for mini PCI cards
J6	Power On	3-pin header for ATX Power On functions
J7	IDE header	40-pin header for the IDE interface
J8	Compact Flash	50-pin, 0.050" (1.27mm), socket accepts Type 1 or Type II Compact Flash cards
J9	Audio In/Out	16-pin, 0.079" (2mm), header for all of the audio signals (input/output)
J10	LAN 2	8-pin RJ45 connector for 10/100BaseT Ethernet port
J11	Serial B	20-pin, header for serial ports 3 and 4 (COM 3 & COM 4)
J12	Serial A	20-pin, header for serial ports 1 and 2 (COM 1 & COM 2)
J13	Utility 2	24-pin header for mouse and SMBus
J14	GPIO	26-pin, 0.079" (2mm) header for general purpose I/O signals
J15	Utility 1	16-pin header for keyboard, external battery, reset switch, speaker
J16	Parallel	26-pin header for parallel port
J17	Floppy	34-pin header for floppy disk drive interface
J18	TTL Video	50-pin, 0.039" (1mm) header for TTL video displays
J19	Power In	7-pin, 0.156" (3.96mm) header for input power
J23	LAN 1	8-pin, standard RJ45 connector for 10/100BaseT Ethernet port
J26	LVDS Video	30-pin, 0.079" (2mm), header for LVDS video displays
J27	SATA1	7-pin, standard connector for serial ATA - [DNP on certain models]
J28	SATA2	7-pin, standard connector for serial ATA - [DNP on certain models]
J29	USB	10-pin, 0.079" (2mm) header for USB 1 and USB 2 ports
J30	USB	10-pin, 0.079" (2mm) header for USB 3 and USB 4 ports
J32	Reset and Power-On	5-pin header for reset switch and power-on button

NOTE The pinout tables in Chapter 3 of this manual identify pin sequence using the following methods: A 20-pin header with two rows of pins, using odd/even numbering, where pin 2 is directly across from pin 1, is noted as 20-pin, 2 rows, odd/even (1, 2). Alternately, a 20-pin connector using consecutive numbering, where pin 11 is directly across from pin 1, is noted in this way: 20-pin, 2 rows, consecutive (1, 11). The second number in the parenthesis is always directly across from pin-1. See Figure 2-5.

Figure 2-5. Header Pin Sequence Identification

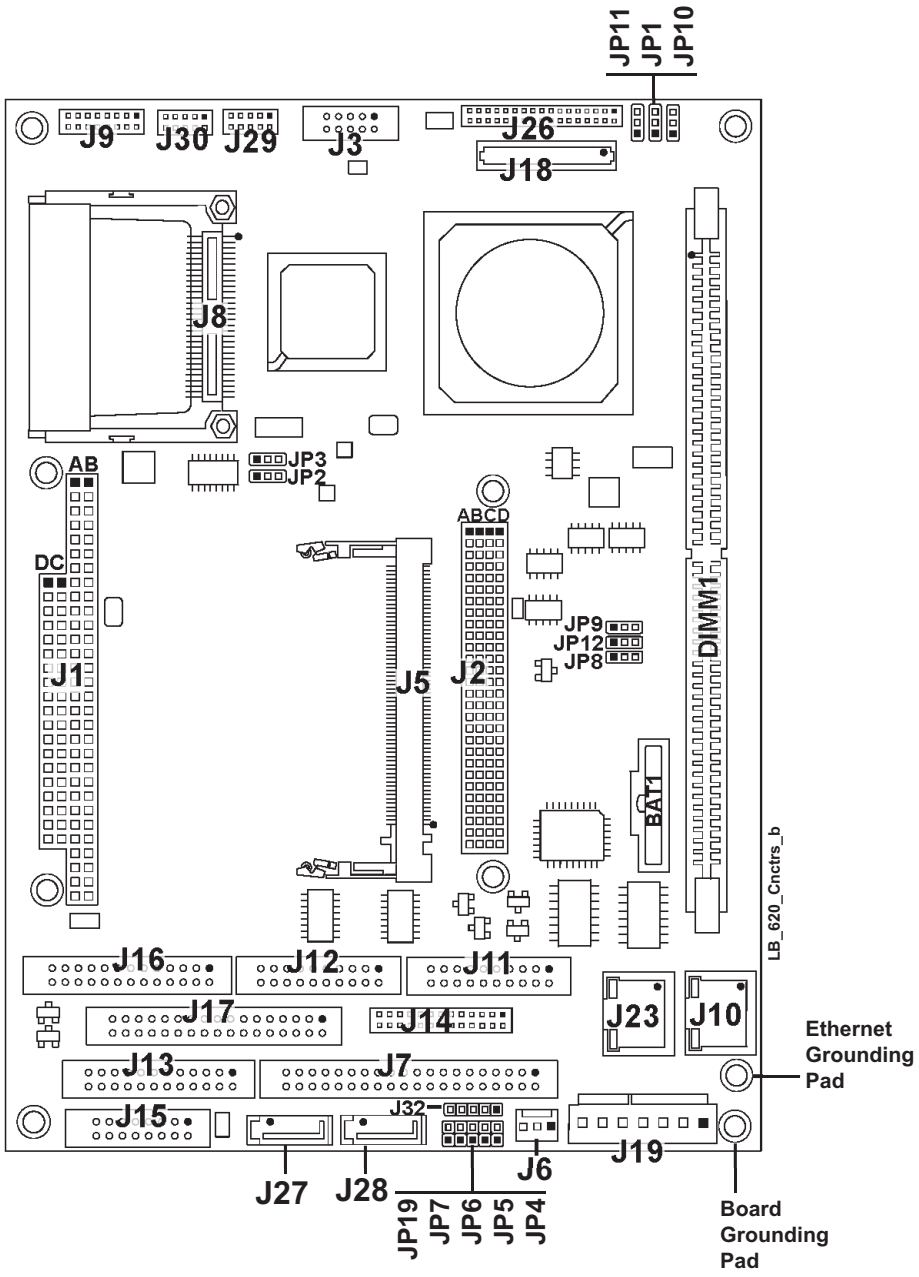

Figure 2-6. Header Locations (Top view)

CAUTION	The two Ethernet ports share a common ground (transformer center tap), that is floating until you determine how the common ground is connected. The grounding holes (8) of the LittleBoard 620 are connected to ground potential (return) of the DC power supply connected to the board through J19.

NOTE	Pin-1 is shown as a black pin (square or round) on all connectors and headers in all illustrations.

Jumper Header Definitions

Table 2-3 describes the jumper headers shown in Figure 2-6.

Table 2-3. Jumper Settings

Jumper #	Installed	Removed/Installed
JP1 – LVDS PWR SEL	Enable +3.3V (pins 1-2) **Default**	Enable +5V (pins 2-3)
JP2 – Compact Flash Master/Slave	Enable Slave (pins 1-2)	Enable Master (pins 2-3) **Default**
JP3 – Compact Flash Voltage Selection	Enable +5V (pins 1-2)	Enable +3.3V (pins 2-3) **Default**
JP4 – Serial Port 1 RS485 Termination	Enable Termination (pins 1-2) [SER0 Data P]	Disable Termination (Removed) **Default - RS232**
JP5 – Serial Port 2 RS485 Termination	Enable Termination (pins 1-2) [SER1 Data N]	Disable Termination (Removed) **Default - RS232**
JP6 – Serial Port 1 RS485 Termination	Enable Termination (pins 1-2) [SER0 Data N]	Disable Termination (Removed) **Default - RS232**
JP7 – Serial Port 2 RS485 Termination	Enable Termination (pins 1-2) [SER1 Data P]	Disable Termination (Removed) **Default - RS232**
JP8 – Oops jumper	Normal (pins 1-2) **Default**	Clear CMOS (pins 2-3)
JP9 – PCI REQ SEL	Mini PCI (pins 1-2) **Default**	PC/104-Plus (pins 2-3)
JP10 – TTL PWR SEL	Enable +3.3V (pins 1-2) **Default**	Enable +5V (pins 2-3)
JP11 – TTL BKLT SEL	Enable +5V (pins 1-2) **Default**	Enable +12V (pins 2-3)
JP12 – PCI GNT SEL	Mini PCI (pins 1-2) **Default**	PC/104-Plus (pins 2-3)
JP19 – AT Power Button	Enable AT Power (pins 1-2)	Enable ATX Power (Removed) **Default**

NOTE Only the jumper headers listed above are populated on the board. All listed jumper headers use 0.079" (2mm) pitch. A jumper that is removed may be placed on one of the jumper pins for safe keeping.

Specifications

Physical Specifications

Table 2-4 gives the physical dimensions of the board.

Table 2-4. Weight and Footprint Dimensions

Item	Dimension
Weight	0.28kg (0.61 lb)
Height (overall)	24.94mm (0.982")
Width	146mm (5.75")
Length	203mm (8.0")
Thickness	2.36mm (0.093")

NOTE Overall height is measured from the upper board surface to the highest permanent component (battery in socket) on the upper board surface. This measurement does not include the various heatsinks or various size DIMMs inserted into the socket. The DIMMs or heatsinks could increase this dimension.

Environmental Specifications

Table 2-5 provides the most efficient operating and storage condition ranges required for this board.

Table 2-5. Environmental Requirements

	Parameter	500MHz Geode LX 800 Conditions
Temperature	Operating	–20° to +70°C (–4° to +158°F)
	Extended (Optional)	–40° to +85°C (–40° to +185°F)
	Storage	–55° to +85°C (–67° to +185°F)
Humidity	Operating	5% to 90% relative humidity, non-condensing
	Non-operating	5% to 95% relative humidity, non-condensing

Power Specifications

Table 2-6 shows the power requirements for the LittleBoard 620.

Table 2-6. Power Supply Requirements

Parameter	500MHz Geode LX 800 Characteristics
Input Type	Regulated DC voltages
In-rush Current (Typical)	7.16A (35.80W)
Idle Power (Typical)	1.57A (7.87W)
BIT* Current (Typical)	2.17A (10.85W)

Operating configurations:

- In-rush operating configuration includes video and 512MB DDR RAM.
- Idle operating configuration includes the In-rush configuration as well as an I/O board, one IDE hard drive with Windows XP SP2, floppy, keyboard, and mouse.
- *BIT = Burn-In-Test. Operating configuration includes idle configuration as well as four serial loop-backs, one parallel loop-back, one USB Jump Drive, one on-board Compact Flash drive with 64MB Compact Flash, two Ethernet connections, two USB Compact Flash readers with 64MB Compact Flash, one external-power USB CD-ROM.

Thermal/Cooling Requirements

The LittleBoard 620 is designed to operate at the maximum speed of the 500 MHz CPU without heatsinks or fans.

Mechanical Specifications

Figure 2-7 shows the top view of the LittleBoard 620 with the mechanical mounting dimensions.

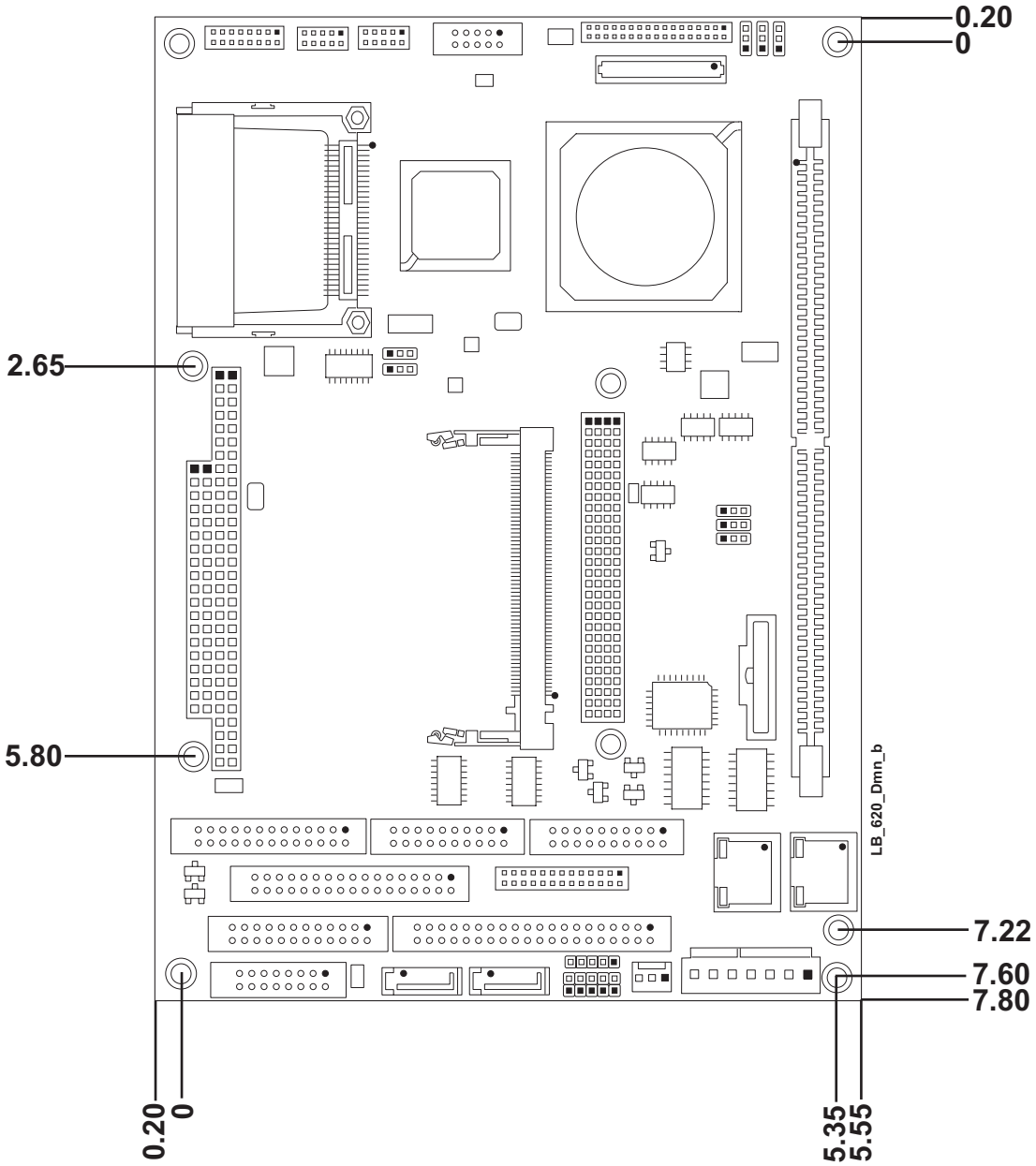

Figure 2-7. LittleBoard 620 Dimensions (Top view)

NOTE	All dimensions are given in inches.

Chapter 3 Hardware

Overview

This chapter discusses the following features of the connectors:

- Interrupt Channel Assignments
- Memory Map
- I/O Address Map
- Floppy Interface
- Serial Interfaces
- Parallel Interface
- Utility Interfaces
  - Keyboard
  - Mouse
  - Battery
  - Reset Switch
  - Speaker
  - SMBus
- Audio Interface
- USB Interfaces
- CRT/TTL/LVDS Video Interfaces
- Miscellaneous
  - User GPIO Signals
  - Time of Day/RTC
  - Temperature Monitoring
  - Oops! Jumper (BIOS recovery)
  - Serial Console
  - Watchdog Timer
- Power Interface

NOTE ADLINK Technology, Inc. only supports the features/options tested and listed in this manual. The main integrated circuits (chips) used in the LittleBoard 620 may provide more features or options than are listed for the LittleBoard 620, but some of these chip features/options are not supported on the board and may not function as specified in the chip documentation.

This chapter does not include pinout tables for standard headers and connectors such as PC/104, PC/104-Plus, Ethernet RJ45, 40-pin IDE, SATA, and Compact Flash.

Interrupt Channel Assignments

The interrupt channel assignments are shown in Table 3-1.

Table 3-1. Interrupt Channel Assignments

Device vs IRQ No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer	X															
Keyboard		X														
Secondary Cascade			X													
COM1				O	D											
COM2				D	O											
COM3					O					O	O	D				
COM4				O						O	D	O				
Floppy							D									
Parallel						O		D								
RTC									X							
IDE Primary															D	O
Math Coprocessor														X		
PS/2 Mouse													X			
PCI INTA	Automatically Assigned															
PCI INTB	Automatically Assigned															
PCI INTC	Automatically Assigned															
PCI INTD	Automatically Assigned															
USB	Automatically Assigned															
VGA	Automatically Assigned															
Ethernet	Automatically Assigned															

Legend: D = Default, O = Optional, X = Fixed

> **NOTE** The IRQs for the Ethernet, Video, USB, and PCI are automatically assigned by the BIOS Plug and Play logic. Local IRQs assigned during initialization can not be used by external devices.

Memory Map

Table 3-2 provides the common PC/AT memory allocations. Memory below 000500h is used by the BIOS.

Table 3-2. Memory Map

Base Address			Function
00000000h	-	0009FFFFh	Conventional Memory
000A0000h	-	000AFFFFh	Graphics Memory
000B0000h	-	000B7FFFh	Mono Text Memory
000B8000h	-	000BFFFFh	Color Text Memory
000C0000h	-	000C7FFFh	Standard Video BIOS
000D0000h	-	000DFFFFh	Reserved for Extended BIOS
000E0000h	-	000FFFFFh	System BIOS Area (Storage and RAM Shadowing)
00100000h	-	Top of DRAM	Extended Memory (If on-board VGA is enabled, then the amount of memory assigned is subtracted from extended memory.)
FFF80000h	-	FFFFFFFFh	System Flash

I/O Address Map

Table 3-3 shows the I/O address map.

Table 3-3. I/O Address Map

Address (hex)	Subsystem
000-00F	Primary DMA Controller
020-021	Master Interrupt Controller
040-043	Programmable Interrupt Timer (Clock/Timer)
060-06F	Keyboard Controller
070-07F	CMOS RAM, NMI Mask Reg, RT Clock
080-09F	DMA Page Registers
102	Video subsystem register
0A0-0BF	Slave Interrupt Controller
0C0-0DF	Slave DMA Controller #2
0F0-0FF	Math Coprocessor
1F0-1F8	IDE Hard Disk Controller
201	Watchdog Timer (WDT)
278-27F	Parallel Printer
2E8-2FF	Serial Port 4 (COM4)
2F8-2FF	Serial Port 2 (COM2)
378-37F	Parallel Port (Standard and EPP)
3C0-3DF	VGA
3E8-3EF	Serial Port 3 (COM3)
3F0-3F7	Floppy Disk Controller
3F8-3FF	Serial Port 1 (COM1)
778-77A	Parallel Port (ECP Extensions) (Port 378+400)

Table 3-3. I/O Address Map (Continued)

A79	ISA PnP Ports
CF8-CFF	PCI bus Configuration Address and Data

Floppy Drive Interface

The Super I/O - 1 controller (W83627HF) provides the floppy controller and supports one floppy drive. The floppy signals are provided through the standard 34-pin header (J17). The floppy controller will support a 360k, 720k, 1.2M, 1.44M, or 2.88M drive.

The floppy drive connector has 34 pins, 2 rows, odd/even, (1, 2) with 0.100" (2.54mm) pitch.

Parallel Port Interface

Parallel port supports standard parallel, Bi-directional, ECP and EPP protocols. The Super I/O - 1 controller (W83627HF) provides the parallel port interface.

The parallel header has 26 pins, 2 rows, odd/even, (1, 2), with 0.100" (2.54mm) pitch.

Table 3-4. Parallel Interface Pin/Signal Descriptions (J16)

Pin #	Signal	In/Out	Description
1	Strobe*	Out	Strobe* – This is an output signal used to strobe data into the printer. I/O pin in ECP/EPP mode.
2	AFD*	Out	Auto Feed* – This is a request signal into the printer to automatically feed one line after each line is printed.
3	PD0	I/O	Parallel Port Data 0 – These pins (0 to 7) provide parallel port data.
4	ERR*	Out	Error* – This is a status output signal from the printer. A Low State indicates an error condition on the printer.
5	PD1	I/O	Parallel Port Data 1 – Refer to pin-3 for more information.
6	INIT*	Out	Initialize* – This signal used to Initialize printer. Output in standard mode, I/O in ECP/EPP mode.
7	PD2	I/O	Parallel Port Data 2 – Refer to pin-3 for more information.
8	SLIN	Out	Select In – This output signal is used to select the printer. I/O pin in ECP/EPP mode.
9	PD3	I/O	Parallel Port Data 3 – Refer to pin-3 for more information.
10, 12	GND		Ground
11	PD4	I/O	Parallel Port Data 4 – Refer to pin-3 for more information.
13	PD5	I/O	Parallel Port Data 5 – Refer to pin-3 for more information.
14, 16	GND		Ground
15	PD6	I/O	Parallel Port Data 6 – Refer to pin-3 for more information.
17	PD7	I/O	Parallel Port Data 7 – Refer to pin-3 for more information.
18, 20	GND		Ground
19	ACK*	In	Acknowledge* – This printer output status indicates it has received the data and is ready to accept new data if the signal state is Low.
21	BUSY	In	Busy – This printer output status indicates the printer is not ready to accept data if the signal state is High.
22, 24	GND		Ground
23	PE	In	Paper End – The printer output status indicates the printer is out of paper if the signal state is High.

Table 3-4. Parallel Interface Pin/Signal Descriptions (J16)

25	SLCT	In	Select – This printer output status indicates the printer is selected and powered on if the signal state is high.
26	Key/NC		Key - Not connected

Note: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Serial Interfaces

The LittleBoard 620 supports 4 independent serial ports, using two separate chips. The Super I/O - 1 controller (W83627HG) provides serial ports 1 and 2 through the Serial A header (J12) and the Super I/O - 2 controller (W83627HG) provides serial ports 3 and 4 through Serial B header (J11). The four serial ports support the following features:

- Auto Direction Control for RS485
- Four individual 16550-compatible UARTs
- Programmable word length, stop bits and parity
- 16-bit programmable baud rate generator
- Interrupt generator
- Loop-back mode
- Four individual 16-bit FIFOs
- Serial A Interface (J12)
  - Serial Port 1 (COM1) supports RS232 full modem and RS485 half duplex (2-wire)
  - Serial Port 2 (COM2) supports RS232 full modem and RS485 half duplex (2-wire)

> **NOTE** The RS232 and RS485 modes are selected for Serial A in the BIOS Setup Utility under the submenu, Super I/O Configuration in the Advanced menu screen for Serial ports 1 (COM1) and 2 (COM2). However, the RS232 mode is the default (Standard) for any serial port.
>
> RS485 mode termination must also be set using jumper pins JP4 and JP6, pins 1-2 (COM1), and JP5 and JP7, pins 1-2 (COM2), when the RS485 mode is selected in BIOS Setup Utility. Refer to Table 2-3 on page 13 for more information.

- Serial B Interface (J11)
  - Serial Port 3 (COM3) supports RS232 full modem support
  - Serial Port 4 (COM4) supports RS232 full modem support

Table 3-5 provides the pins and corresponding signals for the Serial A interface connector (Serial Ports 1 and 2), and Table 3-6 provides the pins and corresponding signals for the Serial B interface connector (Serial Ports 3 and 4).

Both Serial A and B headers have 20 pins, 2 rows, odd/even, (1, 2) pin sequence, with 0.100" (2.54mm) pitch.

Table 3-5. Serial A Interface Pin/Signal Descriptions (J12)

Pin #	Pin # DB9	Signal	Description
1	1(COM1)	DCD1*	Data Carrier Detect 1 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR1 as part of the DTR/DSR handshake.
2	6	DSR1*	Data Set Ready 1 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR1 for overall readiness to communicate.
3	2	RXD1	Receive Data 1 – Serial port 1 receive data in.
4	7	RTS1* Data 1+	Request To Send 1 – Indicates Serial port 1 is ready to transmit data. Used as hardware handshake with CTS1 for low level flow control. Data 1+ – If in RS485 mode, this pin is Transmit Data 1+ /Receive Data 1+.
5	3	TXD1 Data 1-	Transmit Data 1 – Serial port 1 transmit data out. Data 1- – If in RS485 mode, this pin is Transmit Data 1- /Receive Data 1-.
6	8	CTS1*	Clear to Send 1 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS1 for low level flow control.
7	4	DTR1*	Data Terminal Ready 1 – Indicates this Serial port is powered, initialized, and ready. Used as hardware handshake with DSR1 for overall readiness to communicate.
8	9	RI1*	Ring Indicator 1 – Indicates external serial communications device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
9	5	GND1	Ground
10	NC	KEY/ NC	Key Not connected
11	1(COM2)	DCD2*	Data Carrier Detect 2 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR2 as part of the DTR/DSR handshake.
12	6	DSR2*	Data Set Ready 2 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR2 for overall readiness to communicate.
13	2	RXD2	Receive Data 2 – Serial port 2 receive data in.
14	7	RTS2* Data 2+	Request To Send 2 – Indicates Serial port 2 is ready to transmit data. Used as hardware handshake with CTS2 for low level flow control. Data 2+ – If in RS485 mode, this pin is Transmit Data 2+ /Receive Data 2+.
15	3	TXD2 Data 2-	Transmit Data 2 – Serial port 2 transmit data out Data 2- – If in RS485 mode, this pin is Transmit Data 2- / Receive Data 2-.

Table 3-5. Serial A Interface Pin/Signal Descriptions (J12) (Continued)

16	8	CTS2* RX2+	Clear To Send 2 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS2 for low level flow control. RX2+ – If in RS485 mode, this pin is Receive Data 2 -.
17	4	DTR2*	Data Terminal Ready 2 – Indicates Serial port 1 is powered, initialized, and ready. Used as hardware handshake with DSR2 for overall readiness to communicate.
18	9	RI2	Ring Indicator 2
19	5	GND2	Ground
20	NC	NC	Not connected

Note: The shaded area denotes power or ground. Signals are listed in the table with RS232 first, followed by RS485.

Table 3-6. Serial B Interface Pin/Signal Descriptions (J11)

Pin #	Pin # DB9	Signal	Description
1	1 (COM3)	DCD3*	Data Carrier Detect 3 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR3 as part of the DTR/DSR handshake.
2	6	DSR3*	Data Set Ready 3 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR3 for overall readiness to communicate.
3	2	RXD3	Receive Data 3 – Serial port 3 receive data in
4	7	RTS3*	Request To Send 3 – Indicates Serial port 3 is ready to transmit data. Used as hardware handshake with CTS3 for low level flow control.
5	3	TXD3	Transmit Data 3 – Serial port 3 transmit data out
6	8	CTS3*	Clear To Send 3 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS3 for low level flow control.
7	4	DTR3*	Data Terminal Ready 3 – Indicates this Serial port is powered, initialized, and ready. Used as hardware handshake with DSR3 for overall readiness to communicate.
8	9	RI3*	Ring Indicator 3 – Indicates external serial communications device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
9	5	GND1	Ground
10	NC	KEY	Not Connected
11	1(COM4)	DCD4*	Data Carrier Detect 4 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR4 as part of the DTR/DSR handshake.
12	6	DSR4*	Data Set Ready 4 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR4 for overall readiness to communicate.
13	2	RXD4	Receive Data 4 – Serial port 4 receive data in

Table 3-6. Serial B Interface Pin/Signal Descriptions (J11) (Continued)

14	7	RTS4*	Request To Send 4 – Indicator to serial output port 4 is ready to transmit data. Used as hardware handshake with CTS4 for low level flow control.
15	3	TXD4	Transmit Data 4 – Serial port 4 transmit data out
16	8	CTS4*	Clear To Send 4 – Indicator to serial port 4 that external serial communications device is ready to receive data. Used as hardware handshake with RTS4 for low level flow control.
17	4	DTR4*	Data Terminal Ready 4 – Indicates this Serial port is powered, initialized, and ready. Used as hardware handshake with DSR4 for overall readiness to communicate.
18	9	RI4	Ring Indicator 4
19	5	GND	Ground
20	NC	NC	Not connected

Note: The shaded areas denote power or ground.

Utility Interfaces

The Utility interfaces consist of two connectors that provide the standard interface signals for the following devices:

- Utility 1
  - Keyboard
  - External battery connection
  - Reset Switch
  - Speaker
- Utility 2
  - PS/2 Mouse
  - SMBus signals
  - Power button signal

Utility 1 Interface

The Utility 1 (J15) interface uses a 16-pin connector and provides the various interface signals to an external I/O board with external connections for the respective connectors such as, keyboard, speaker, etc. Table 3-7 provides the pin-outs and interface signals for Utility 1 interface and has 16 pins, 2 rows, odd/even, (1, 2) with 0.100" (2.54mm) pitch.

- Keyboard
- Battery
- Reset Switch
- Speaker

Keyboard Interface

The signal lines for a PS/2 keyboard are provided through the Utility 1 interface, which is also fully PC/AT compatible.

External Battery

An external battery input connection is provided through a Utility 1 interface for the Real-Time Clock's operation in the event the on-board battery is not used.

Reset Switch

The signal lines for a reset switch are provided through the Utility 1 interface. See Table 3-7.

Speaker

The signal lines for a speaker port with 0.1-watt drive are provided through a Utility 1 interface (J15).

Table 3-7. Utility 1 Interface Pin/Signal Descriptions (J15)

Pin #	Signal	I/O	Description
1	NC	I	Not connected
2	GND1	I	Ground
3	NC	I	Not connected
4	GND2	I	Ground
5	LED	O	Power On LED – This on-board +3.3 volts is provided through 330 ohm resistor to an external Power-On LED.
6	NC	-	Not connected
7	SPKR+	O	+ Speaker Output – This signal drives external PC "Beep" speaker.
8	GND3	I	Ground
9	RESET SW*	I	Reset Switch – This signal (ground) provided from external reset switch.
10	NC	-	Not connected
11	KBD DATA	I/O	Keyboard Data – Data signal provided to external keyboard connector.
12	KBD CLK	I/O	Keyboard Clock – Clock signal provided to external keyboard connector.
13	GND4	I	Keyboard Ground
14	KBD PWR	O	Keyboard Power – This +5 volts is provided to external keyboard connector. Requires external fuse for keyboard/mouse protection.
15	BATV+	I	Backup Battery – This connection provides an additional backup battery from an external source. It can also be used in place of the on-board backup battery, BAT1, shipped with all LittleBoard 620s. Each RTC battery input is protected with a zener diode.
16	BATV-	I	Battery - Return (Grounded)

Note: The shaded areas denote power or ground. The signals marked with * = Negative true logic.

Utility 2 Interface

The Utility 2 (J13) interface consists of a 24-pin header used to interface various signals to the external board with external connections, or directly to the respective connector such as the mouse and power button etc. Table 3-9 on page 26 provides the pin-outs and interface signals for the Utility 2 interface. The J13 connector has 24 pins, 2 rows, odd/even (1, 2) pin sequence with 0.100" (2.54mm) pitch.

- SMBus signals
- PS/2 Mouse signals
- Power button signal

System Management Bus (SMBus)

The I/O Hub, CS5536, (Southbridge) contains both a host and slave SMBus port; but the host cannot access the slave internally. The slave port allows an external master access to the I/O Hub through the header (J13). The master contained in the CS5536 is used to communicate with the SDRAM DDR DIMM and the clock generator. Table 3-8 provides the addresses for these components and the corresponding binary addresses of the SMBus.

Table 3-8. SMBus Reserved Addresses

Component	Address Binary
SDRAM EPROM	$1010,000x_b$
Clock Generator (MK1491-09FLNTR)	$1101,001x_b$
I/O Hub (CS5536)	$0000,000x_b$ (default) Programmable Master

Mouse, Power Button, and SMBus Interfaces

The signal lines for a PS/2 mouse, Power Button, and SMBus are provided through the Utility 2 interface (J13).

Table 3-9. Utility 2 Interface Pin/Signal Descriptions (J13)

Pin #	Signal	I/O	Description
1	NC	-	Not connected
2	PWRBT*	I	Power Button – This signal from an external switch to the I/O Hub is not used with AT Power supplies.
3	BATLOW*		Battery Low – This signal from external battery indicates to the I/O Hub there is insufficient power to boot the system.
4	NC	-	Not connected
5	NC	-	Not connected
6	NC	-	Not connected
7	GND1	-	Ground
8	VCC1	-	+5 Volts
9	MDATA	I/O	Mouse Data – Data signal provided to external mouse connector.
10	MCLK	I/O	Mouse Clock – Clock signal provided to external mouse connector.
11	GND2	-	Ground
12	VCC2	-	+5 Volts
13	SMBCLK	-	SMBus Clock – Clock signal provided to external devices.
14	SMBDATA	-	SMBus Data – Data signal provided to external devices.
15	NC	-	Not connected

Table 3-9. Utility 2 Interface Pin/Signal Descriptions (J13) (Continued)

16	NC	-	Not connected
17	NC	-	Not connected
18	NC	-	Not connected
19	NC	-	Not connected
20	NC	-	Not connected
21	NC	-	Not connected
22	NC	-	Not connected
23	NC	-	Not connected
24	NC	-	Not connected

Note: The shaded areas denote power or ground. The signals marked with * = Negative true logic.

Audio Interface

The audio solution on the LittleBoard 620 is provided by the (Southbridge) I/O Hub (CS5536) and the on-board Audio CODEC (ALC203-LF). These two chips use a digital interface to communicate between the two, which is defined by AC'97 and is revision 2.3 compliant. The input or output signals for the audio interface go through the 16-pin connector (J9) to an external cable and/or board, which has the respective audio connections. The PC Beep Speaker signal from the I/O Hub is also fed to the on board Audio CODEC to provide a PC Beep signal for the stereo line out connections.

Audio CODEC (ALC203-LF) features

- AC'97 Rev 2.3 compliant
- 18-bit full duplex performance
- Independent variable sampling rate
- Stereo (Left and Right) Line In
- Stereo (Left and Right) Line Out
- Microphone (Mono) In
- PC "Beep" speaker signal is also fed to the CODEC for the Line Out (Left and Right) channels

Table 3-10 describes the Audio interface pin/signals on 16-pins, 2 rows, odd/even (1, 2) with 0.079" (2mm) pitch.

Table 3-10. Audio Interface Pin/Signal Descriptions (J9)

Pin #	Signal	Description
1, 3	NC	Not Connected
2, 4, 7, 8, 11, 12, 13, 14, 16	GND_AUD	Audio ground
5	LINE_OUTL	Line Out signal left channel
6	LINE_OUTR	Line Out signal right channel
9	LINE_INL	Line In signal left channel
10	LINE_INR	Line In signal right channel
15	MICIN	Microphone signal In

Note: The shaded area denotes power or ground.

USB Interfaces

The I/O Hub (CS5536) provides the USB solution for both OHCI controller (legacy) and EHCI controller (USB 2.0) support. The I/O Hub (Southbridge) contains port-routing logic that determines which controller (OHCI or EHCI) handles the USB data signals. Two 10-pin headers, J29 and J30, provide four USB ports.

USB 2.0 Support

The I/O Hub contains an Enhanced Host Controller Interface (EHCI) compliant host controller, which supports up to 4 high-speed USB 2.0 Specification compliant root ports. The higher speed USB 2.0 specification allows data transfers up to 480 Mbps using the same pins as the 4 Full-speed/Low-speed USB OHCI ports. The I/O Hub port-routing logic determines which of the controllers (OHCI or the EHCI) processes the USB signals.

- One EHCI host controller for all four USB ports on headers J29 and/or J30
- Supports USB v2.0 Specification
- Over-current fuses, located on the board, where USB1 and USB2 share a single fuse (F3) and USB3 and USB4 share a single fuse (F2).

Legacy USB Support

The I/O Hub supports two USB Open Host Controller Interfaces (OHCI), and each Host Controller includes a root hub with two USB ports each, for a total of 4 USB ports. The USB Legacy features implemented on the USB ports include the following:

- One root hub and two USB ports on connector J29
- One root hub and two USB ports on connector J30
- Supports USB v.1.1 and OHCI v.1.1 with integrated physical layer transceivers
- Supports improved arbitration latency for OHCI controllers
- OHCI controllers support Analog Front End (AFE) embedded cell instead of USB I/O buffers to allow for USB High-speed signaling rates
- Over-current fuses, located on the board, are used on all four USB ports

Primary USB0 and USB1

Table 3-11 describes USB 0 & 1, with 10-pins, 2 rows, odd/even (1, 2) and 0.079" (2mm) pitch.

Table 3-11. USB 0 & 1 Interface Pin/Signal Descriptions (J29A/B)

Pin #	Signal	Description
1, 2	VCC	USB Voltage – +5V
3	USBP0-	Universal Serial Bus Port 0 Data Negative
4	USBP1-	Universal Serial Bus Port 1 Data Negative
5	USBP0+	Universal Serial Bus Port 0 Data Positive
6	USBP1+	Universal Serial Bus Port 1 Data Positive
7, 8, 9, 10	GND	Ground

Note: The shaded area denotes power or ground.

Secondary USB2 and USB3

Table 3-12 describes USB 2 & 3, with 10-pins, 2 rows, odd/even (1, 2) and 0.079" (2mm) pitch.

Table 3-12. USB 2 & 3 Interface Pin/Signal Descriptions (J30A/B)

Pin #	Signal	Description
1, 2	VCC	USB Voltage – +5V
3	USBP2-	Universal Serial Bus Port 2 Data Negative
4	USBP3-	Universal Serial Bus Port 3 Data Negative
5	USBP2+	Universal Serial Bus Port 2 Data Positive
6	USBP3+	Universal Serial Bus Port 3 Data Positive
7, 8, 9, 10	GND	Ground

Note: The shaded area denotes power or ground.

Video Interfaces

The Graphics and Memory Hub (Northbridge)—integrated in the Geode LX processor—provides the graphics control and video signals to the traditional glass CRT monitors and the LVDS flat panel displays. The chip features are listed below:

- Supports 2D graphics with extensive set of instructions including:
  - BLT operations
  - Hardware video up/down scalar
  - Legacy RGB mode

CRT features:

- Provide an integrated 350 MHz, 24-bit RAMDAC to drive a progressive scan analog monitor, and outputs to three 8-bit DACs provide the R, G, and B signals to the monitor.
- Support resolutions up to 1920 x 1440.
- Support a maximum allowable video frame buffer size of 254 MB UMA (Unified Memory Architecture).

LVDS and TTL Flat Panel features:

- Support (3.3V or 5V) output to TFT flat panels through a 24-bit interface.
- Support TFT panel sizes from VGA (600 x 480) up to UXGA (1600 x 1200).
- Support a 24-bit single channel LVDS flat panel interface.
- Support panel up-scaling (to fit a smaller source image onto a specific native panel size) as well as panning and centering.

TTL Flat Panel Interface

Table 3-13 describes the signals of the TTL interface with 50 pins, 2 rows, odd/even, (1, 2) and 0.039" (1mm) pitch.

Table 3-13. TTL Flat Panel Interface Pin/Signal Descriptions (J18)

Pin #	Signal	Description
1	NC	Not connected
2	NC	Not connected
3	NC	Not connected
4	NC	Not connected
5	NC	Not connected
6	NC	Not connected
7	NC	Not connected
8	NC	Not connected
9	NC	Not connected
10	NC	Not connected
11	NC	Not connected
12	NC	Not connected
13	NC	Not connected
14	FP21	Flat Panel Data Output, R5
15	FP23	Flat Panel Data Output, R7
16	FP22	Flat Panel Data Output, R6
17	FP16	Flat Panel Data Output, R0
18	FP20	Flat Panel Data Output, R4
19	FP17	Flat Panel Data Output, R1
20	FP18	Flat Panel Data Output, R2
21	FP19	Flat Panel Data Output, R3
22	FP14	Flat Panel Data Output, G6
23	FP13	Flat Panel Data Output, G5
24	FP12	Flat Panel Data Output, G4
25	FP15	Flat Panel Data Output, G7
26	FP11	Flat Panel Data Output, G3
27	FP7	Flat Panel Data Output, B7
28	FP10	Flat Panel Data Output, G2
29, 30	VCC_TTL	Jumper (JP10) determines voltage (pins 1-2 = +3.3V or pins 2-3 = +5V).
31	FP9	Flat Panel Data Output, G1
32	FP8	Flat Panel Data Output, G0
33	FP4	Flat Panel Data Output, B4
34	FP6	Flat Panel Data Output, B6
35	FP3	Flat Panel Data Output, B3
36	FP5	Flat Panel Data Output, B5
37	FP2	Flat Panel Data Output, B2

Table 3-13. TTL Flat Panel Interface Pin/Signal Descriptions (J18) (Continued)

38	FP1	Flat Panel Data Output, B1
39	FPDEN	Flat Panel Data Enable – This signal to settle the horizontal display position.
40	FP0	Flat Panel Data Output, B0
41	FPCLKS	Flat Panel Shift Clock
42	DISPEN	Reserved
43	ENVDD	Flat Panel Enable VDD – This is power sequencing output for LCD driver.
44	FPVS	Flat Panel VSync (FLM) – This signal is digital monitor equivalent of VSYNC.
45	DISPEN	Flat Panel Enable VEE – This signal is used for power sequencing.
46	FPHS	Flat Panel HSync (LP) – This signal is the digital monitor equivalent of HSYNC.
47, 48	GND	Ground
49, 50	VCC_BKLT	Jumper (JP11) determines back light inverter voltage (pins 1-2 = +5V, or pins 2-3 = +12V.) **Note:** The +12V voltage is supplied externally from the AT/ ATX power supply input connector.

Note: The shaded areas denote power or ground.

LVDS Interface

Table 3-14 describes the signals of the LVDS interface with 30 pins, 2 rows, odd/even, (1, 2) and 0.079" (2mm) pitch.

Table 3-14. LVDS Interface Pin/Signal Descriptions (J26)

Pin #	Signal	Description	Line	Channel	NOTE N/A
1	VCC_INVTR	+12 Volts			
2	VCC_LCD	+3.3 Volts or +5 Volts Depends on JP1 setting (+3.3V **Default, 1-2**)			
3	GND	Ground	GND		
4	GND	Ground			
5	NC	Not connected		Channel 2	
6	NC	Not connected			
7	NC	Not connected	3		
8	NC	Not connected			
9	NC	Not connected	2		
10	NC	Not connected			
11	NC	Not connected	1		
12	NC	Not connected			
13	NC	Not connected	0		
14	NC	Not connected			
15	NC	Not connected			
16	LCD_EN	LCD Enable			
17	LVDSP_Clk+	Data Positive Output	Clk	Channel 1	
18	LVDSN_Clk-	Data Negative Output			
19	LVDSA_Y3+	Data Positive Output	3		
20	LVDSA_Y3-	Data Negative Output			
21	LVDSA_Y2+	Data Positive Output	2		
22	LVDSA_Y2-	Data Negative Output			
23	LVDSA_Y1+	Data Positive Output	1		
24	LVDSA_Y1-	Data Negative Output			
25	LVDSA_Y0+	Data Positive Output	0		
26	LVDSA_Y0-	Data Negative Output			
27	LVDS_I2CCLK	Serial I2C for Clock			
28	LVDS_I2CDAT	Serial I2C for Data			
29	LVDS_BKL_EN	Enable Backlight Inverter			
30	NC	Not connected			

Note: The shaded areas denote power or ground.

Miscellaneous

User GPIO Signals

The LittleBoard 620 provides 22 GPIO pins for custom use, and the signals are routed to the J14 header.

For more information about the GPIO pin operation, refer to the datasheet specifications or Programming Manual for the Super I/O (W83627HG) controller at:

http://www.winbond-usa.com/products/winbond_products/pdfs/PCIC/W83627HF_F_HG_Ga.pdf

Table 3-15 defines the GPIO pin signals which use a 28-pin header of 2 rows, with odd/even (1, 2) pin sequence, and 0.079" (2mm) pitch.

Table 3-15. User GPIO Signals Pin/Signal Descriptions (J14)

Pin #	Signal	Description
1	VCC1	+5 Volts DC +/- 5%
2	VCC2	+5 Volts DC +/- 5%
3	SIO1_GP17	User defined
4	SIO2_GP17	User defined (Unsupported in the BIOS)
5	SIO1_GP16	User defined
6	SIO2_GP16	User defined (Unsupported in the BIOS)
7	SIO1_GP15	User defined
8	SIO2_GP15	User defined (Unsupported in the BIOS)
9	SIO1_GP14	User defined
10	SIO2_GP14	User defined (Unsupported in the BIOS)
11	SIO1_GP13	User defined
12	SIO2_GP13	User defined (Unsupported in the BIOS)
13	SIO1_GP12	User defined
14	SIO2_GP12	User defined (Unsupported in the BIOS)
15	SIO1_GP11	User defined
16	SIO2_GP11	User defined (Unsupported in the BIOS)
17	SIO1_GP10	User defined
18	SIO2_GP10	User defined (Unsupported in the BIOS)
19	SIO1_GP23	User defined (Unsupported in the BIOS)
20	SIO2_GP23	User defined (Unsupported in the BIOS)
21	SIO1_GP25	User defined (Unsupported in the BIOS)
22	SIO2_GP24	User defined (Unsupported in the BIOS)
23	SIO2_GP35	User defined (Unsupported in the BIOS)
24	SIO2_GP34	User defined (Unsupported in the BIOS)
25	GND1	Ground
26	GND2	Ground

Note: The shaded area denotes power or ground.

Real-Time Clock (RTC)

The LittleBoard 620 contains a Real-Time Clock (RTC). The BIOS (CMOS) RAM is backed up with a Lithium Battery. If the battery is not present, the BIOS has a battery-free boot option to complete the boot process.

Temperature Monitoring

The Super I/O controller (W83627HG) performs the CPU temperature monitoring function and receives inputs directly from the thermal diode in the CPU.

Oops! Jumper (BIOS Recovery)

The Oops! jumper is provided in the event the BIOS settings you have selected prevent you from booting the system. By using the Oops! jumper you can prevent the current BIOS settings in the EEPROM from being loaded, forcing the use of the default settings. Connect the DTR pin to the RI pin on serial port 1 (COM 1) prior to boot up to prevent the present BIOS settings from loading. After booting with the Oops! jumper in place, remove the Oops! jumper and go into BIOS Setup. Change the desired BIOS settings, or select the default settings, and save changes before rebooting the system.

To convert the Serial A interface to an Oops! jumper, short together the DTR (7) and RI (8) pins on Serial A (J12) header for Serial Port 1. As an alternate, short the equivalent pins, 4 and 9, on the back of the Serial Port 1 DB9 cable connector as shown in Figure 3-1.

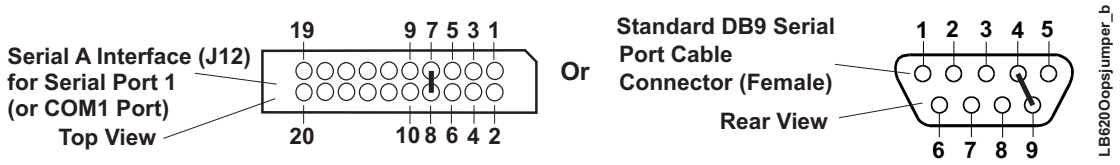

Figure 3-1. Oops! Jumper Connection

Serial Console

The LittleBoard 620 supports the serial console (or console redirection) feature. This I/O function is provided by an ANSI-compatible serial terminal, or an equivalent terminal emulation software running on another system. This can be very useful when setting up the BIOS on a production line for systems that are not connected to a keyboard and display.

Serial Console Setup

The serial console feature is implemented by connecting a standard null modem cable or modified serial cable (or “Hot Cable”) between one of the serial ports, such as Serial 1 (J12) and the serial terminal, or a PC with communications software. The BIOS Setup Utility controls the serial console settings on the LittleBoard 620.

Hot (Serial) Cable

To convert a standard serial cable to a Hot Cable, specific pins must be shorted together at the Serial port connector or on the DB9 cable connector. For example, short the RTS (7) and RI (9) on the respective DB9 port cable connector as shown in Figure 3-2.

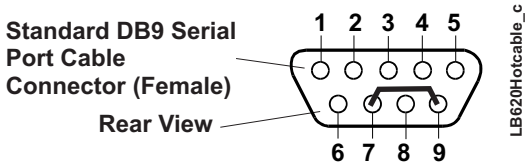

Figure 3-2. Hot Cable Jumper

Watchdog Timer

The Watchdog Timer (WDT) restarts the system if a mishap occurs, ensuring proper start-up after the interruption. Possible problems include failure to boot properly, the application software's loss of control, failure of an interface device, unexpected conditions on the bus, or other hardware or software malfunctions.

The WDT (Watchdog Timer) can be used both during the boot process and during normal system operation.

- During the Boot process – If the operating system fails to boot in the time interval set in the BIOS, the system will reset.

  Enable the WDT in Boot Settings Configuration of BIOS Setup. Set the WDT for a time-out interval in seconds, between 1 and 255, in one-second increments in the Boot Setting Configuration screen. Ensure you allow enough time for the boot process to complete and for the OS to boot. The OS or application must tickle the WDT as soon as it comes up. This can be done by accessing the hardware directly or through a BIOS call.

- During System Operation – An application can set up the WDT hardware through a BIOS call, or by accessing the hardware directly. Some ADLINK Board Support Packages provide an API interface to the WDT. The application must tickle the WDT in the time set when the WDT is initialized or the system will be reset. You can use a BIOS call to tickle the WDT or access the hardware directly.

  The BIOS implements interrupt 15 function 0C3h to manipulate the WDT.

Power Interfaces

Power In

The LittleBoard 620 uses five separate voltages on the board, but only one of the voltages is provided externally (+5 volts) through the external header, which uses a 7-pin vertical header with 0.156" (3.96mm) pitch. All the onboard voltages are derived from the externally supplied +5 volts DC +/- 5%. The onboard voltages include the CPU core voltages as well as the other voltages used on the board.

Table 3-16 lists the signals for power supply input with 7 pins, single row, and 0.156" (3.96mm) pitch.

Table 3-16. Power In Pin/Signal Descriptions (J19)

Pin #	Signal	Description
1	+5V	+5.0 Volts – This +5.0 volts DC +/- 5% is the only voltage required for internal operation.
2	GND	Ground
3	GND	Ground
4	+12V	+12 Volts
5	+3.3V	+3.3 Volts
6	GND	Ground
7	+5V	+5.0 Volts – This +5.0 volts DC +/- 5% is the only voltage required for internal operation.

Note: The shaded areas denote power or ground. The +12V and +3.3V on the Power In header (J19) are used for the PCI, ISA bus, TTL, and LVDS functions and are supplied externally and not generated on the LittleBoard 620.

Power On

The signals on this header allow the ATX power supply to be turned off (soft off) from the LittleBoard 620 by operating system (OS) control. However, if you use a non-ATX power supply you will not have the soft off feature normally provided by ATX power supplies.

Table 3-17 lists the signals for the J6 Power On header with 3 pins, single row, and 0.100" (2.54mm) pitch.

Table 3-17. Power On Pin/Signal Descriptions (J6)

Pin #	Signal	Description
1	PS_ON*	Power Supply On – This signal is sent to the ATX power supply by the LittleBoard 620 to turn On the ATX power supply. This signal can also be used to turn Off the ATX power supply.
2	GND	Ground
3	VCCSB	+5V suspend voltage (+5V, 2A** Standby) – This voltage is supplied from the ATX power supply. This voltage is required for normal operation.

Note: The shaded areas denote power or ground. The signals marked with * = Negative true logic. **The power supply must be capable of delivering 2 amps for 5VSB.

Power-On Button

A Power-On Button signal is provided by connecting ground to pin 1 on this header (J32). A Reset Switch signal is provided by connecting ground to pin 3 on this header. The J32 header uses a single row of 5 pins with 0.100" (2.54mm) pitch.

Table 3-18. Power-On Button Interface Pin/Signal Descriptions (J32)

Pin #	Signal	Description
1	PWRON	Power-On Button input (connect between pins 1 & 2)
2	GND	Ground
3	RST_SW	Reset Switch input or output (connect between pins 3 & 2)
4	NC	Not Connected
5	NC	Not Connected

Note: The shaded area denotes power or ground.

Chapter 4 BIOS Setup

Introduction

This section assumes the user is familiar with BIOS Setup and does not attempt to describe the inner workings of BIOS functions. Refer to the appropriate PC reference manuals for information about the on-board, ROM-BIOS software interface. If ADLINK has added to or modified the standard functions, these functions will be described.

Entering BIOS Setup (VGA Display)

To enter BIOS Setup using a VGA display for the LittleBoard 620:

1. Turn on the VGA monitor and the power supply to the LittleBoard 620.
2. Start Setup by pressing the [Del] key, when the following message appears on the boot screen.

   ```
   Press DEL to run Setup
   ```

NOTE	If the setting for *Memory Test* is set to Fast, you may not see this prompt appear on screen if the monitor is too slow to display it on start up. If this happens, press the <Del> key early in the boot sequence to enter BIOS Setup.

3. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen.
4. Follow the instructions at the bottom of each screen to navigate through the selections and modify any settings.

Entering BIOS Setup (Remote Access)

Once you set up the BIOS Utility for Remote Access (serial console or console redirection) in VGA mode, entering the BIOS in the remote access mode is very similar to the method used when entering the BIOS with a VGA display.

1. Turn on the power supply to the LittleBoard 620 and access the BIOS Setup Utility in VGA mode.
2. Set the BIOS feature *Remote Access* to [Enabled] under the **Advanced** menu.
3. Accept the default options or make your own selections for the balance of the Remote Access fields and record your settings.
4. Ensure you select the type of remote serial terminal you will be using and record your selection.
5. Select *Save Changes and Exit* and then shut down the LittleBoard 620.
6. Connect the remote serial terminal (or the PC with communications software) to the COM port you selected on the LittleBoard 620 using a Hot Cable or a standard null-modem serial cable.
7. Turn on the remote serial terminal (or the PC with communications software) and set it to the settings you selected and recorded earlier in the BIOS Setup Utility.

   COM1, 115200, 8 bits, 1 stop bit, no parity, no flow control, and [Always] for *Redirection After BIOS POST* are the default settings for the LittleBoard 620.
8. Restore power to the LittleBoard 620 and look for the screen prompt shown below.

   ```
   Press ^C to run SETUP
   ```

9. Press the CTRL–C keys to enter Setup early in the boot sequence if *Quick Boot* is set to [Enabled].

   If *Quick Boot* is set to [Enabled], you may never see the screen prompt.

10. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen.

> **NOTE** The serial console port is not hardware protected, and is not listed in the COM table within BIOS Setup Utility. Diagnostic software that probes hardware addresses may cause a loss or failure of the serial console functions.

PCI-ISA Bridge Mapping

The LittleBoard 620 supports ISA bus based modules with an on-board PCI-ISA bridge. The PCI-ISA bridge optionally maps the following resources to ISA based modules:

- Memory
- I/O Ports
- IRQs
- DMA Channels

The LittleBoard 620 system BIOS maps the above resources, based on information provided in the BIOS Setup screens. By default, only some of the I/O ports are mapped to ISA modules and any memory, IRQs or DMA channels to be mapped must be explicitly specified by the user in the BIOS Setup screens.

The IRQs are mapped with the “PCIPnP/IRQx” fields in BIOS setup (where x specifies the IRQ number.) The IRQs 3, 4, 5, 7, 9, 10, 11, 14, and 15 can be mapped to ISA based modules by changing the default setting for these IRQs from “Available” to “Reserved”.

ISA I/O ports, Memory, and DMA channels can be mapped to ISA modules on the “Boot/Boot Settings Configuration” BIOS setup screen. Six I/O port “windows” and four memory “windows” are available for mapping I/O Port or Memory regions to ISA modules by specifying the window length and base address.

By default, the following I/O port windows are mapped to ISA modules:

- 200-240h
- 240-260h
- 279h
- 300-340h
- 340-360h
- A79h

> **NOTE** 279h and A79 are the ISA PnP ports used by the BIOS and an OS that supports this feature to recognize ISA PnP (Plug and Play) cards.

By default, no memory windows are mapped to ISA modules.

Any of the DMA channels 0, 1, 2, 3, 5, 6, 7 can be mapped to ISA modules by changing the default setting of “LPC Bridge” to “ISA Bridge”.

For example, to configure an ISA Soundblaster PnP card with resources 220/5/1/5 (Port/IRQ/DMA/DMA) so that the Soundblaster would work in Windows XP, the following BIOS Setup changes would be required:

- ISA I/O Ports – no changes necessary. 220h is already mapped to ISA by default.
- IRQ – set IRQ5 to “Reserved” in BIOS Setup. See the paragraph above on mapping IRQs.
- DMA1 and DMA5 – set DMA Channels 1 and 5 to “ISA Bridge” in BIOS Setup. See paragraph above on mapping DMA Channels.

Logo Screen Utility (Splash Screen)

The LittleBoard 620 BIOS supports a graphical logo utility, which can be customized by the user and displayed on screen when enabled through the BIOS Setup Utility. The graphical image can be a company logo or any custom image the user wants to display during the boot process. The custom image can be displayed as the first image displayed on screen during the boot process and remain there, depending on the options selected in BIOS Setup, while the OS boots.

Logo Screen Image Requirements

The user's image may be customized with any image editing tool, and the system will automatically convert the image into an acceptable format to the tools (files and utilities) provided by ADLINK.

The LittleBoard 620 OEM logo screen utility supports the following image formats:

- Bitmap image
- Exactly 640 x 480 pixels
- Exactly 16 colors

> **NOTE** For procedures on loading custom images, see the logo screen utility document available on the ADLINK web site.

- Bitmap image
  - 16-Color, 640x480 pixels
  - 256-Color, 640x480 pixels
- JPG image
  - 16-Color, 640x480 pixels
- PCX image
  - 256-Color, 640x480 pixels
- A file size of not larger than the sample image

> **NOTE** For procedures on loading custom images, see the OEM Logo Utility document available on the ADLINK web site.

Appendix A Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed in the Table A-1 below. Requests for support through Ask an Expert are given the highest priority, and usually will be addressed within one working day.

- ADLINK Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the Ampro By ADLINK web site at http://www.adlinktech.com/AAE/. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.

  ADLINK strongly suggests that you register with the web site. By creating a profile on the ADLINK web site, you will have a portal page called "My ADLINK" unique to you with access to exclusive services and account information.

- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receivean immediate confirmation e-mail that your request has been entered. Once you have submitted your request, you must log in to My Stuff where you can check status, update your request, and access other features.

- Download Service – This service is also free and available 24 hours a day at http://www.adlinktech.com. For certain downloads such as technical documents and software, you must register online before you can log in to this service.

Table A-1. Technical Support Contact Information

Method	Contact Information
Ask an Expert	http://www.adlinktech.com/AAE/
Web Site	http://www.adlinktech.com
Standard Mail	**ADLINK Technology Inc.** Address: 9F, No.166 Jian Yi Road, Chungho City, Taipei County 235, Taiwan 台北縣中和市建一路 166 號 9 樓 Tel: +886-2-8226-5877 Fax: +886-2-8226-5717 Email: service@adlinktech.com **Ampro ADLINK Technology Inc.** Address: 5215 Hellyer Avenue, #110, San Jose, CA 95138, USA Tel: +1-408-360-0200 Toll Free: +1-800-966-5200 (USA only) Fax: +1-408-360-0222 Email: info@adlinktech.com **ADLINK Technology Beijing** Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室 (100085) Rm. 801, Power Creative E, No. 1, B/D Shang Di East Rd., Beijing 100085, China Tel: +86-10-5885-8666 Fax: +86-10-5885-8625 Email: market@adlinktech.com

Table A-1. Technical Support Contact Information

	ADLINK Technology Shanghai Address: 上海市漕河泾高科技开发区钦江路 333 号 39 幢 4 层 (200233) Tel: +86-21-6495-5210 Fax: +86-21-5450-0414 Email: market@adlinktech.com **ADLINK Technology Shenzhen** Address: 深圳市南山区科技园南区高新南七道 数字技术园 A1 栋 2 楼 C 区 (518057) 2F, C Block, Bld. A1, Cyber-Tech Zone, Gao Xin Ave. Sec 7, High-Tech Industrial Park S., Shenzhen, 518054 China Tel: +86-755-2643-4858 Fax: +86-755-2664-6353 Email: market@adlinktech.com **ADLINK Technology Inc. (German Liaison Office)** Address: Nord Carree 3, 40477 Duesseldorf, Germany Tel: +49-211-495-5552 Fax: +49-211-495-5557 Email: emea@adlinktech.com **ADLINK (French Liaison Office)** Address: 15 rue Emile Baudot, 91300 MASSY Cedex, France Tel: +33 (0) 1 60 12 35 66 Fax: +33 (0) 1 60 12 35 66 Email: france@adlinktech.com **ADLINK Technology Japan Corporation** Address: 151-0072 東京都渋谷区幡ヶ谷 1-1-2 朝日生命幡ヶ谷ビル 8F Asahiseimei Hatagaya Bldg. 8F 1-1-2 Hatagaya, Shibuya-ku, Tokyo 151-0072, Japan Tel: +81-3-4455-3722 Fax: +81-3-5333-6040 Email: japan@adlinktech.com **ADLINK Technology Inc. (Korean Liaison Office)** Address: 서울시 서초구 서초동 1506-25 한도 B/D 2 층 2F, Hando B/D, 1506-25, Seocho-Dong, Seocho-Gu,Seoul, 137-070, Korea Tel: +82-2-2057-0565 Fax: +82-2-2057-0563 Email: korea@adlinktech.com **ADLINK Technology Singapore Pte Ltd.** Address: 84 Genting Lane #07-02A, Cityneon Design Centre, Singapore 349584 Tel: +65-6844-2261 Fax: +65-6844-2263 Email: singapore@adlinktech.com **ADLINK Technology Singapore Pte Ltd. (Indian Liaison Office)** Address: No. 1357, "Anupama", Sri Aurobindo Marg, 9th Cross, JP Nagar Phase I, Bangalore - 560078, India Tel: +91-80-65605817 Fax: +91-80-22443548 Email: india@adlinktech.com

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