ReadyBoard™ 820
Single Board Computer
Reference Manual

P/N 50-1Z064-1000

Notice Page

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REVISION HISTORY

Revision	Reason for Change	Date
A, A	Initial Release	Jan/07
B, A	Added 1.0GHz CPU version; added PCI-104, USB 4&5, parallel / floppy; changed connector and component ID numbers; removed 1.8 Mhz CPU version, LCD interface; revised power specifications	Feb/08
B, B	Changed system memory requirement from 'Up to 2GB' to 'Up to 1GB'; corrected chipset from 915GM to 915GME; added Caution for Table 3-17; updated table 3-1; corrected pin 1 of J14 in fig 2-6	June/09
1000	Removed requirement from the Power On section under Table 3-18 that the J2 header requires Standby voltage; changed memory specification to 'Up to 2GB'; changed document part number to 50-1Z064-1000	Oct/10

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Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

Contents

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Chapter 1 About This Manual

Purpose of this Manual

This manual is for designers of systems based on the ReadyBoard 820 Single Board Computer (SBC). The information in this manual helps designers create embedded systems based on specific design requirements.

Information provided in this reference manual includes:

- ReadyBoard 820 Specifications
- Environmental requirements
- Major integrated circuits (chips) and features implemented
- ReadyBoard 820 connector/pin numbers and definitions
- BIOS Setup information

Information not provided in this reference manual includes:

- Detailed chip specifications
- Internal component operation
- Internal registers or signal operations
- Bus or signal timing for industry standard busses and signals

References

The following list of references may help you successfully complete your design.

Specifications

- EPIC Specification Revision 1.0, January 2005

  Web site: http://www.ampro.com/RP/EPIC_Specification_v1.0.pdf

- Audio CODEC 1997 Standard, including all revisions

  For the latest version of the Audio (AC'97) standard developed by Intel Corporation, refer to:

  Web site: http://inst.eecs.berkeley.edu/~cs150/Documents/ac97_r23.pdf

- Compact Flash Specification Revision 4.0, July 2006

  For the latest revision of the Compact Flash specification, refer to the Compact Flash Association at:

  Web site: http://www.CompactFlash.org

Chip specifications used on the ReadyBoard 820:

- Intel Corporation and the Celeron® M 373 and Pentium® M 738 CPUs; the chips 915GME and 82801FBM ICH6-M, used for the Memory Hub (Northbridge/Video controller) and I/O Hub (Southbridge), respectively.

  Web site: http://www.intel.com

- Winbond Electronics, Corp. and the W83627HF chip used for the Super I/O controller

  Web site: http://www.winbond-usa.com/products/winbond_products/pdfs/PCIC/627hf.pdf

- Fintek and the F81216D chip used for the Secondary I/O (LPC UART) controller (48-pin)

  Web site: http://www.fintek.com.tw/eng/

- Intel Corporation and the Gigabit Ethernet PCI Express 82573V, used for the Gigabit Ethernet controller.

  Web site: http://www.intel.com/design/network/products/lan/controllers/82573.htm

- Intel Corporation and the 82551QM, used for the Fast Ethernet controller.

  Web site: http://www.intel.com/design/network/products/lan/controllers/82551qm.htm

NOTE	If you are unable to locate the datasheets using the links provided, search the internet to find the manufacturer's web site and locate the documents you need.

Chapter 2 Product Overview

This overview presents general information about the EPIC form factor and the ReadyBoard 820 Single Board Computer (SBC). After reading this chapter you should understand:

- EPIC architecture
- Product Description
- ReadyBoard 820 features
- Major components
- Connectors
- Specifications

EPIC Architecture

In 2004, five companies collaborated to fill the void between the EBX size and the PC/104 size with a new industry standard form factor (115mm x 165mm, or 4.5" x 6.5") called “Embedded Platform for Industrial Computing™ (EPIC).” The EPIC standard principally defines physical size, mounting hole pattern, and power connector locations. It does not specify processor type or electrical characteristics. There are recommended connector placements for I/O, graphics, and memory expansion. This embedded SBC standard ensures that embedded system OEMs can standardize their designs and that full featured embedded computing solutions can be designed into even more space constrained environments than ever before.

The EPIC standard boasts the same highly flexible and adaptable system expansion as EBX, allowing easy and modular addition of functions such as Firewire or wireless networking not usually contained in standard product offerings. The EBX system expansion is based on popular existing industry standards, PC/104™, PC/104-Plus™, and PCI-104™. PC/104 places the ISA bus on compact 3.6" x 3.8" modules with self-stacking capability. PC/104-Plus adds the power of a PCI bus to PC/104 while retaining the basic form factor, but PCI-104 expansion cards only provide the PCI Bus to the PC/104 form factor. Using PC/104 expansion cards, an EPIC board can be easily adapted to meet a variety of embedded applications. See Figures 2-1 and 2-2.

The EPIC standard also brings stability to the mid-sized embedded board market and offers OEMs assurance that a wide range of products will be available from multiple sources – now and in the future. The EPIC specification is freely available to all interested companies, and may be used without licenses or royalties. For further technical information on the EPIC standard, visit the web site at: http://www.epic-sbc.org.

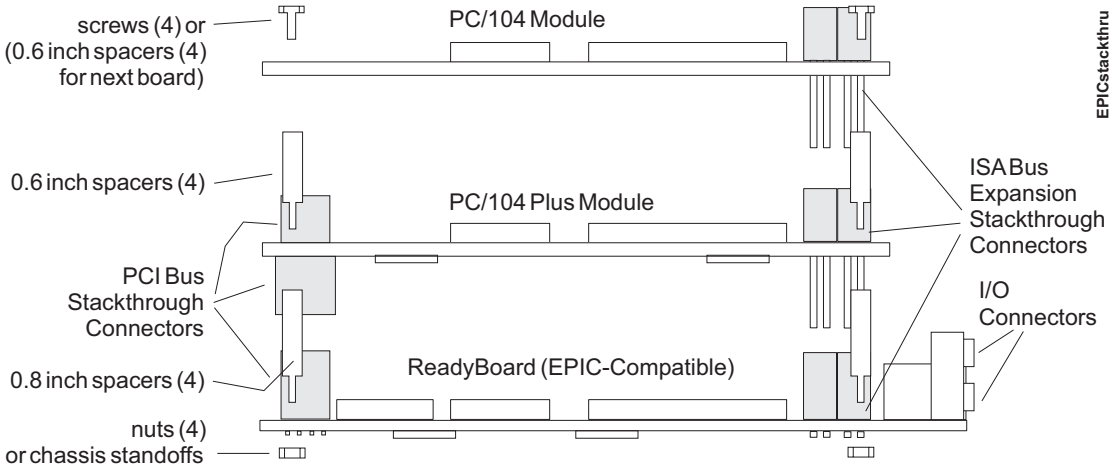


Figure 2-1. Typical ReadyBoard and PC/104 Module Stack

Product Description

The ReadyBoard 820 is a mid-sized, EPIC-compatible, high quality single-board system, which contains all the component subsystems of a PC/AT PCI motherboard plus the equivalent of up to 4 PCI expansion boards. The ReadyBoard 820 is based on the ultra high performance, high-integration, Intel Celeron M or Pentium M processors. One of these processors with the matching chipset give designers a complete integration solution based on the EPIC form factor that conforms to the Revision 1.0 of the EPIC standard.

Each ReadyBoard 820 incorporates an Intel® 915GME chipset for the Memory Hub (Northbridge) and I/O Hub (Southbridge) controllers. The chipset consists of the Intel 82915GME memory hub, which controls graphics and memory interfaces and the Intel 82801FBM I/O Hub Controller which controls I/O functions. The Winbond Electronics Corp. Super I/O controller, W83627HF, adds I/O functions. Together, the Intel, Winbond, and Fintek chips provide four serial ports, a floppy or EPP/ECP parallel port, four USB 2.0 ports, two SATA ports, PS/2 keyboard and mouse interfaces, an Ultra/DMA 33/66/100 IDE controller supporting two IDE drives or one IDE drive and one Compact Flash socket, AGP 4X graphics equivalent controller, which provides CRT and LVDS flat panel video interfaces for the most popular flat panels, and an audio AC'97 CODEC. The ReadyBoard 820 also supports two independent Ethernet interfaces, 10/100BaseT and 1000BaseT, and up to 2 GB of non-ECC DDR2 RAM in a single 200-pin SODIMM socket.

The ReadyBoard 820 can be expanded through the PCI-104 expansion bus to accept PCI-104 cards that offer compact, self-stacking, modular expandability for additional system functions. The PCI-104 bus only implements the signal set for the PCI bus and is available on the 120-pin (4 rows of 30 pins) expansion bus connector. If required for an application, the PC/104 bus—an embedded system version of the signal set provided on a desktop PC's ISA bus—is provided by the optional ADLINK MiniModule ISA expansion board. The PCI bus operates at 33 MHz clock speed, and if included as an option, the ISA bus operates at 8 MHz clock speed. See Figure 2-2.

Among the many embedded enhancements on the ReadyBoard 820 that ensure embedded system operation and application versatility are a watchdog timer, serial console support, battery-free boot, customizable logo screen, on-board high-density Compact Flash socket, and ACPI support for sleep states.

The ReadyBoard 820 is particularly well suited to embedded applications by meeting the size, power consumption, temperature range, quality, and reliability demands of embedded system applications. It can be stacked with ADLINK MiniModules™ or other PCI-104 compliant expansion boards, or it can be used as a powerful computing engine. The ReadyBoard 820 requires only a +5V power supply.

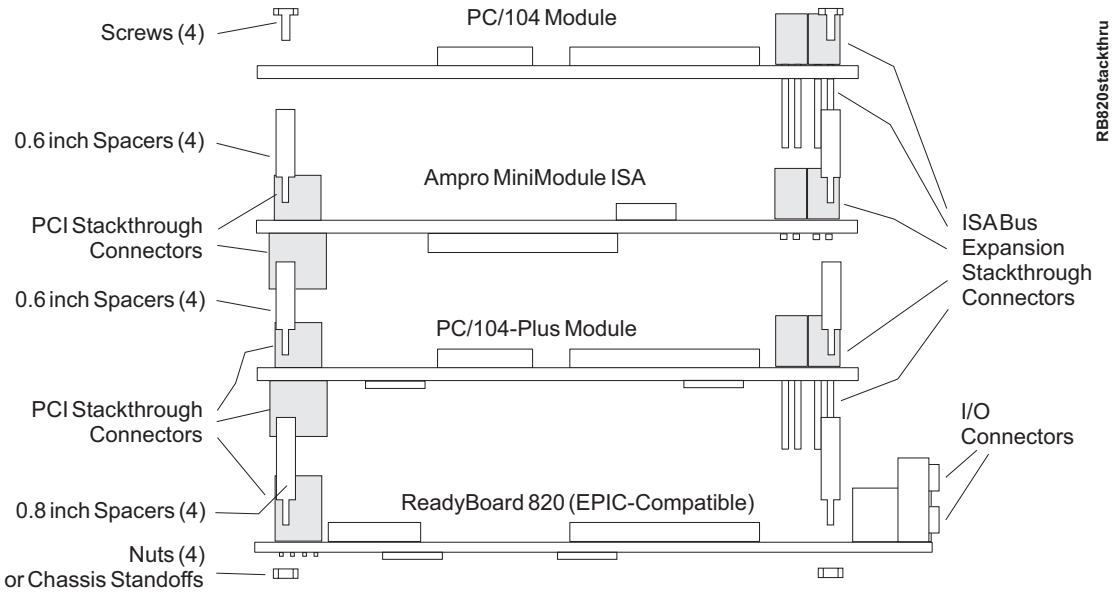


Figure 2-2. PC/104 Modules Stacked on a ReadyBoard 820

Board Features

- CPU Features
  - Provide 1.0 GHz Low Voltage (LV) Celeron M 373 or 1.4GHz Low Voltage (LV) Pentium® M 738 processors
  - Support a Front Side Bus (FSB) of 400MHz
- Memory
  - Provides a single standard 200-pin DDR2 SODIMM socket
  - Supports a single +1.8V DDR2 SODIMM up to 2GB
  - Supports up to 2GB DDR2 (400MHz) SDRAM
  - Supports unregistered/unbuffered non-ECC DDR2 SDRAM
- PCI-104 Bus Interface
  - Supports PCI 2.3 standard
  - Supports 33 MHz PCI Bus speed
  - Supports optional PC/104 standard (add-on MiniModule ISA expansion board) at 8 MHz
- Serial ATA Interface (SATA)
  - Provides two 7-pin SATA ports
  - Provides 1.5 GB/second data transfer rate
- IDE Interface
  - Provides one enhanced IDE controller (2 devices)
  - Provides one 44-pin IDE connector
  - Supports dual bus master mode
  - Supports Ultra DMA 33/66/100 modes
  - Supports ATAPI and DVD peripherals
  - Supports IDE native and ATA compatibility modes
- Floppy/Parallel Interface
  - Shared floppy/parallel connector
  - Supports one floppy disk drive (1 standard 34-pin floppy drive)
  - Supports all standard PC/AT formats: 360 kB, 1.2 MB, 720 kB, 1.44 MB, 2.88 MB
  - Supports standard printer port
  - Supports IEEE standard 1284 protocols of EPP and ECP outputs
  - Bi-directional data lines
  - Supports 16 byte FIFO for ECP mode
- USB Ports
  - Provide three root USB hubs
  - Provide six USB ports
  - Provide two standard USB connectors (USB 0 and 1) and two 10-pin headers (USB 2 and 3 and USB 4 and 5)
  - Support USB bootable devices

- Support USB 2.0 and legacy USB v1.1
- Provide over-current fuses on board

- Serial Ports
  - Provide four buffered serial ports with full handshaking
  - Provide two 20-pin headers for four serial ports
  - Provide 16550-equivalent controllers, each with a built-in 16-byte FIFO buffer
  - Support RS232 capability on all four ports
  - Support full modem capability on three of the four ports
  - Support RS485 or RS422 operation on two of the four ports (COM3 & COM4)
  - Support programmable word length, stop bits, and parity
  - Support 16-bit programmable baud-rate generator and an interrupt generator
- Infrared Interface
  - Provides a five-pin IrDA interface header
  - Supports IrDA v1.1
  - Supports HPSIR and ASKIR infrared modes
  - Supports IR mode select from the Super I/O chip
- Keyboard/Mouse Interface
  - Provides PS/2 keyboard interface (shared with mouse)
  - Provides PS/2 mouse interface (shared with keyboard)
  - Provides shared over-current fuse
- Audio Interface
  - Supports AC'97 audio standard
  - AC'97 CODEC on board
  - Provides non-amplified Stereo Line In/Out
  - Provides non-amplified MIC in (Mono)
- Ethernet Interface – Gigabit and 10/100
  - Includes two fully independent RJ45 Ethernet ports
  - Integrated LEDs on each port (Link/Activity and Speed)
  - Supports IEEE 802.3 10BaseT/100BaseTX compatible physical layer
  - Supports IEEE 802.11 10BaseT/100BaseTX/1000BaseT compatible physical layer
  - Supports auto-negotiation for speed, duplex mode, and flow control
  - Supports full duplex or half-duplex mode
    - Full-duplex mode supports transmit and receive frames simultaneously
    - Supports IEEE 802.3x flow control in full duplex mode
    - Half-duplex mode supports enhanced proprietary collision reduction mode
  - Supports LAN Boot

- Video Interfaces (CRT/PanelLink/LVDS)
  - Support CRT (2048x1536) with 64MB BIOS dependent UMA (Unified Memory Architecture)
  - Integrated graphics controller
  - PanelLink outputs (allow capacity to bring out TMDS signals to a DVI connector)
  - LVDS outputs (1 or 2 channel, four differential signals: 3-bits + clock)
- Miscellaneous
  - Provides real-time clock (RTC) with replaceable battery
  - Supports battery-free boot
  - Provides external battery connection for RTC operation
  - Provides user GPIO interface header
  - Thermal and voltage monitoring
  - Provides connector for optional CPU fan (+12 volt power supply required)
  - Supports a customizable Logo (Splash) Screen
  - Supports Serial Console
  - Provides Watchdog Timer

Block Diagram

Figure 2-3 shows the functional components of the ReadyBoard 820.

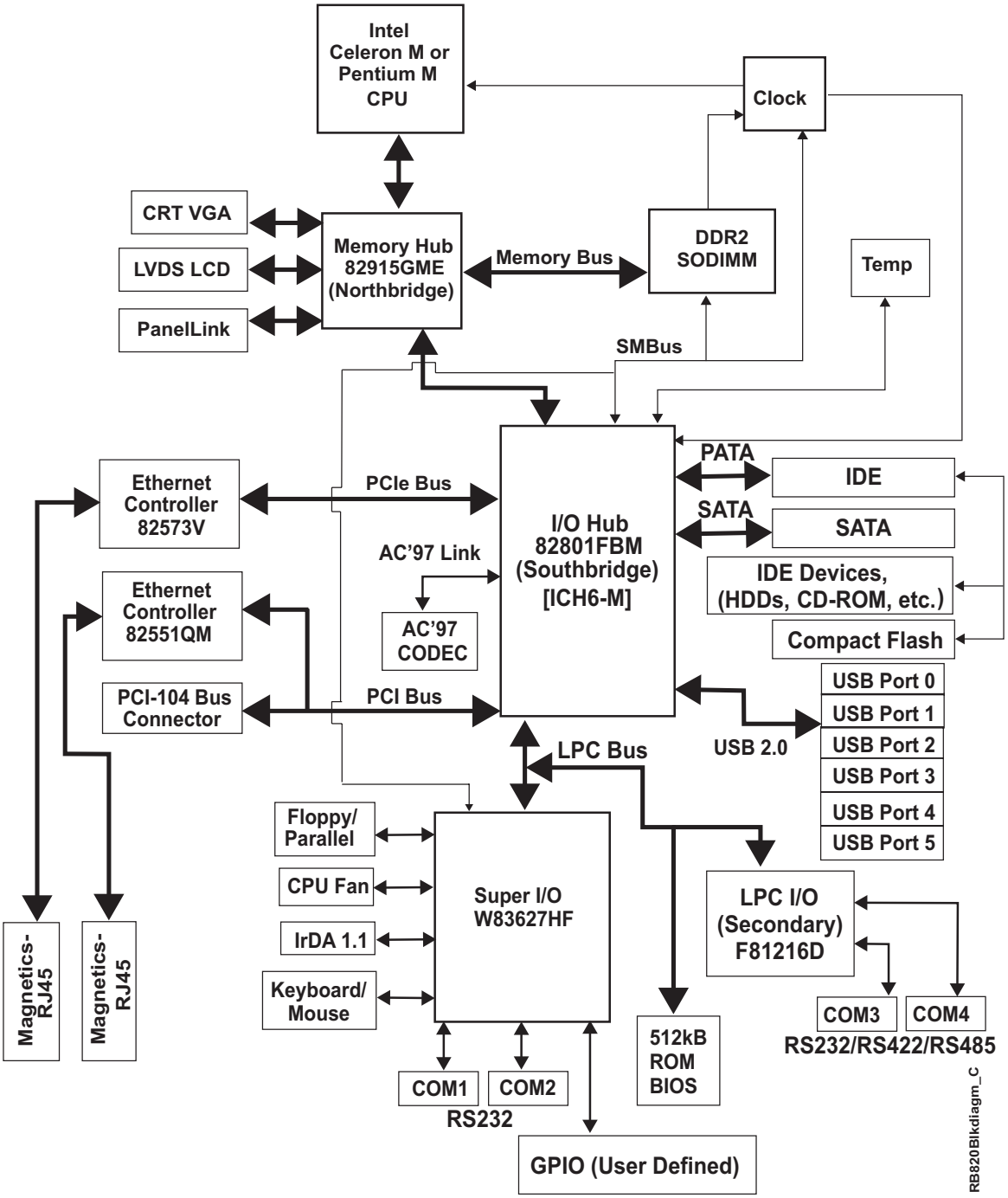


Figure 2-3. Functional Block Diagram

Major Integrated Circuits

Table 2-1 lists the major Integrated Circuits (ICs) on the ReadyBoard 820, including a brief description of each, and Figure 2-4 shows the locations of the major chips.

Table 2-1. Major Integrated Circuit Descriptions and Functions

Chip Type	Mfg.	Model	Description	Function
CPU (U2)	Intel	Celeron M Pentium M	LV 1.0GHz (Celeron M) or LV 1.4GHz (Pentium M)	Embedded CPU
Memory Hub (U3)	Intel	915GME	Northbridge - Memory and Video functions	Memory and Video
I/O Hub (U4)	Intel	82801FB (ICH6-M)	Southbridge - Provides some of the I/O functions (HDD, Audio, USB, LAN, PCI)	I/O Functions
Super I/O (U8)	Winbond	W83627HF	Provides most of remaining I/O functions (FDD, COM1/2, KB, MS, LPT, Fan, IrDA)	I/O Functions
LPC (I/O) UART Controller (U20 - on back of the board)	Fintek	F81216D	LPC controller for Serial Ports 3 & 4 (COM 3 & 4)	UART (I/O) Controller
Audio '97 CODEC (U21 - on back of the board)	Realtek	ALC655	Audio '97 CODEC for audio In/Out signals	Audio In/ Out
Ethernet Controller (U11)	Intel	82573V	Gigabit Ethernet – This chip provides one independent 1000BaseT network channel	Ethernet function
Ethernet Controller (U10)	Intel	82551QM	Fast Ethernet – This chip provides one independent 10/100BaseTX network channel	Ethernet function

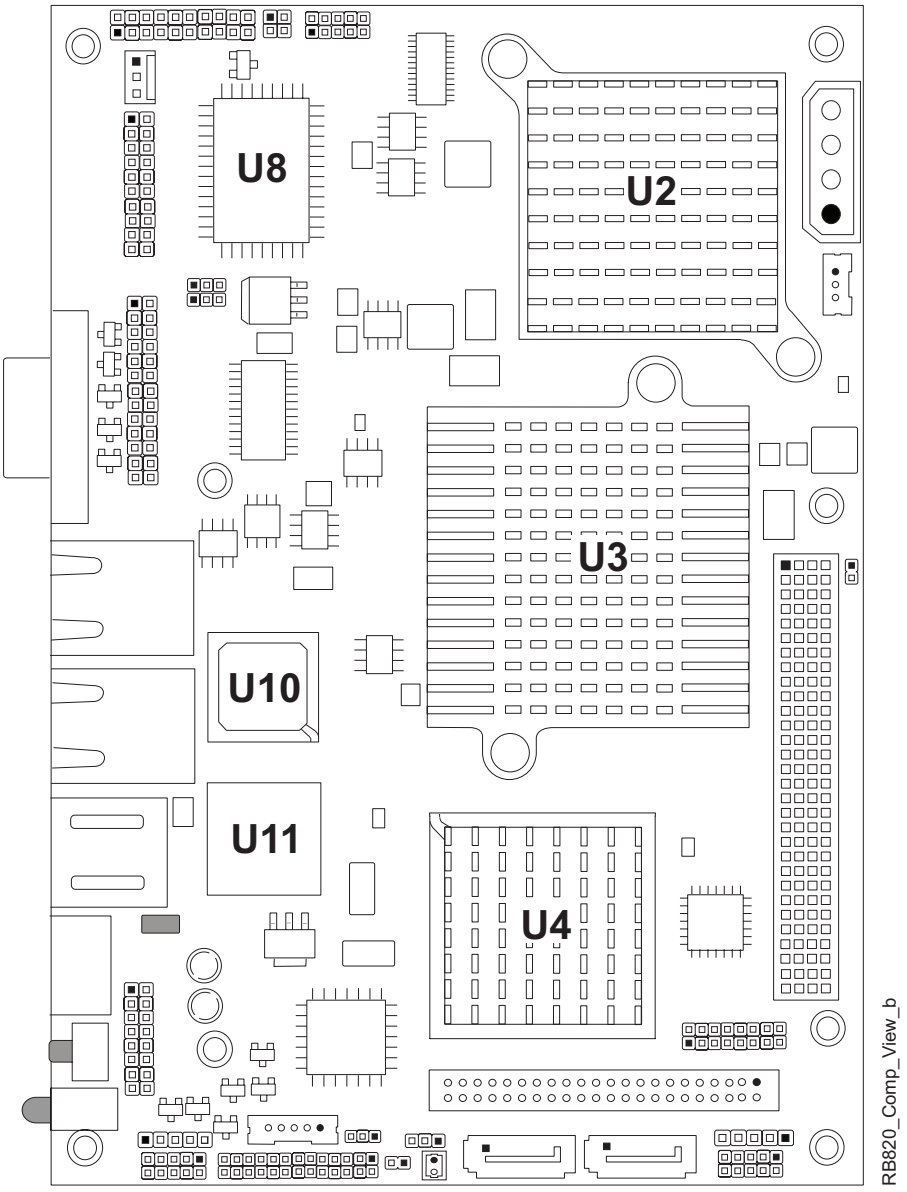


Figure 2-4. Component Locations

Header and Connector Definitions

Table 2-2 describes the headers and connectors shown in Figure 2-6. All I/O headers and connectors use 0.100" (2.54mm) pitch unless otherwise indicated.

Table 2-2. Header and Connector Descriptions

Jack #	Signal/Device	Description
BT1	RTC Battery (B1)	2-pin, 0.049" (1.25mm) header for battery input
D6	Power and IDE Activity LEDs	Yellow diode indicates IDE activity, and green diode indicates power activity. Reside on the ReadyBoard 820.
DIMM1	SODIMM (on back of the board)	200-pin socket for DDR2 SODIMM
J1	Power In	4-pin, 0.200" (5.08mm) header for input power +5V, +12V, GND

Table 2-2. Header and Connector Descriptions (Continued)

Jack #	Signal/Device	Description
J2	Power On	3-pin, 0.079" (2mm) header for Power On and +5V standby voltages
J3	PCI-104	120-pin, 0.079" (2mm) connector for PCI bus
J4	USB 2 & 3	10-pin, 0.079" (2mm) header provides USB2 and USB3 output
J5	PanelLink	16-pin, 0.079" (2mm) header for Digital Visual Interface (DVI) output
J6	IrDA	5-pin, header for IrDA signals
J7	Factory Only	Not loaded
J8	SATA1	7-pin connector for serial ATA
J9	IDE	44-pin, 0.079" (2mm) header for the IDE interface
J10	SATA0	7-pin connector for serial ATA
J11	USB 4 & 5	10-pin, 0.079" (2mm) header provides USB4 and USB5 output
J12	GPIO	10-pin, 0.079" (2mm) header for GPIO signals
J13	SMBus	5-pin, 0.079" (2mm) SMBus header for external device connection
J14	Floppy/Parallel Port	26-pin, 0.079" (2mm) header for floppy/parallel port interface
J15	Serial B	20-pin, 0.079" (2mm) header for Serial ports 3 & 4 (COM3 & COM4)
J16	Utility	5-pin, header for external Battery, Reset, Speaker
J17	Fan	3-pin, header provides +5v, tach, and ground to fan
J18	Serial A	20-pin, 0.079" (2mm) header for Serial ports 1 & 2 (COM1 & COM2)
J19	Video (LVDS)	30-pin, 0.079" (2mm) header for LVDS video display
J20	Audio In/Out	16-pin, 0.079" (2mm) header for Line In L/R, Line Out L/R, Mic in
J21	Fast 10/100 Ethernet + LEDs	14-pin connector for 8-pin RJ45 and LEDs for Ethernet port
J22	Gigabit Ethernet + LEDs	14-pin connector for 8-pin RJ45 and LEDs for Ethernet port
J23A/B	USB 0 & 1	8-pin connector for two 4-pin interfaces provides USB0 and USB1 output
J24	Keyboard/Mouse	6-pin, 0.079" (2mm) PS/2 Keyboard/Mouse connector (dual output cable)
J25	Reset Switch	4-pin, push-button switch for hard reset
J26	Video (CRT VGA)	15-pin connector for output to a CRT monitor
J27	Compact Flash (on back of the board)	50-pin, 0.050" (1.27mm) socket accepts Compact Flash cards (Type I or II)

NOTE The pinout tables in Chapter 3 of this manual identify pin sequence using the following methods: A 20-pin header with two rows of pins, using odd/even numbering, where pin 2 is directly across from pin 1, is noted as 20-pin, 2 rows, odd/even (1, 2). Alternately, a 20-pin connector using consecutive numbering, where pin 11 is directly across from pin 1, is noted in this way: 20-pin, 2 rows, consecutive (1, 11). The second number in the parenthesis is always directly across from pin-1. See Figure 2-5.

Figure 2-5. Header Pin Identifications

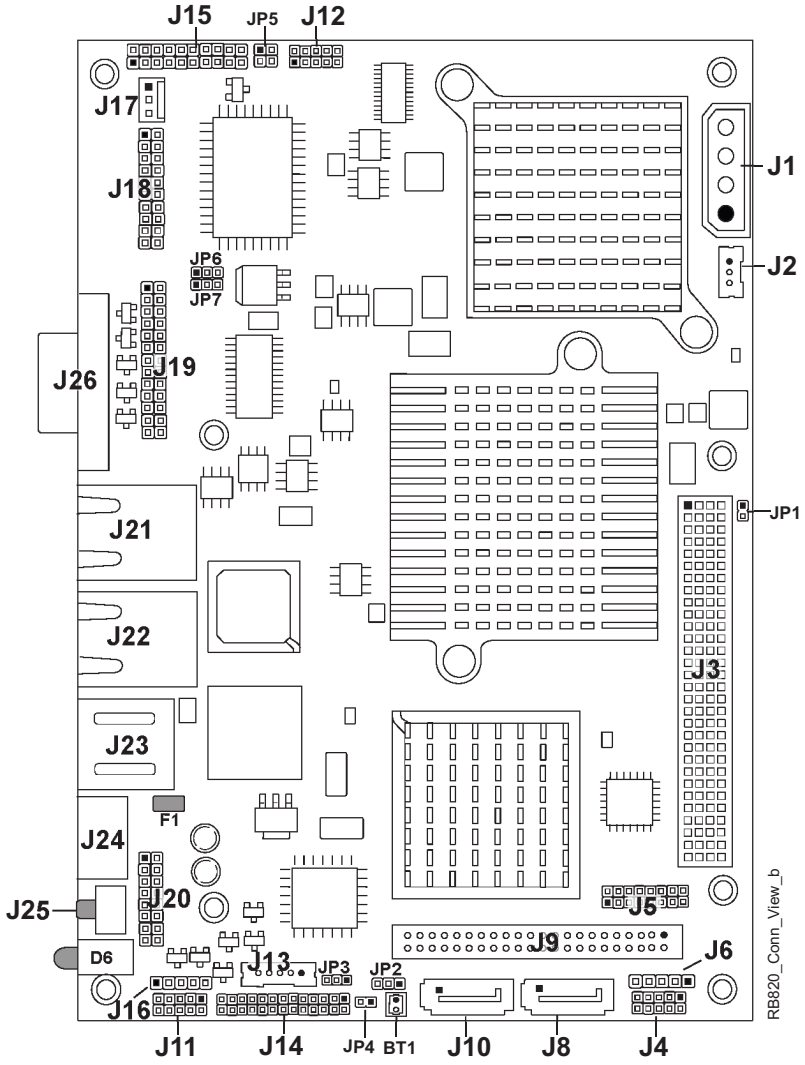


Figure 2-6. Headerand Connector Locations

NOTE	Pin 1 is shown as a black pin (square or round) on all headers in all illustrations.

Additional Components

Fuse F1, in Table 2-3, is shown in Figure 2-6. Fuses F2, F3, and F4 can be found on the back of the board.

Table 2-3. Additional Component Descriptions

Component	Description
Fuse F1 (on front of the board)	Auto reset, 1.1A, overcurrent fuse for the Keyboard/Mouse (J24)
Fuse F2 (on back of the board)	Auto reset, 1.6A, overcurrent fuse for the USB 2 & 3 (J4)
Fuse F3 (on back of the board)	Auto reset, 1.6A, overcurrent fuse for the USB 4 & 5 (J11)
Fuse F4 (on back of the board)	Auto reset, 1.6A, overcurrent fuse for the USB 0 & 1 (J23)

Jumper Header Definitions

Table 2-4 describes the jumper headers shown in Figure 2-6 on page 12.

Table 2-4. Jumper Settings

Jumper #	Installed	Removed/Installed
JP1* – PC/104+ SERIRQ (SerialIRQ)	Enabled (pins 1-2)	Disabled (removed) **Default**
JP2 – Clear CMOS Setup	Normal (pins 1-2) **Default**	Clear CMOS Setup (pins 2-3)
JP3 – Compact Flash Voltage Setup	+3.3V (pins 1-2)	+5V (pins 2-3) (removed) **Default**
JP4 – Compact Flash Card Setup	Master (pins 1-2)	Slave (removed) **Default**
JP5 – COM3 RS422/485	Termination (pins 1-2)	No Termination (removed) **Default**
JP5 – COM4 RS422/485	Termination (pins 3-4)	No Termination (removed) **Default**
JP6 – LCD Backlight Voltage Setup	+5V (pins 1-2) **Default**	+12V (pins 2-3)
JP7 – LCD Voltage Setup	+3.3V (pins 1-2) **Default**	+5V (pins 2-3)

NOTE *The ISA interrupts are required on pin 31 of the PCI-104 connector, when using the MiniModule ISA board. Use the ISA IRQ jumper (JP1) to enable ISA interrupts. For full PCI-104 compatibility, the jumper should be removed (default setting). Refer to the MiniModule ISA manual for more information.

Specifications

Power Specifications

Table 2-5 lists the power requirements for the ReadyBoard 820.

Table 2-5. Power Supply Requirements

Parameter	1.0GHz Intel Celeron M Characteristics	1.4GHz Intel Pentium M Characteristics
Input Type	Regulated DC voltages	Regulated DC voltages
In-rush Current	8.06A (40.30W)	8.06A (40.30W)
Idle Power	2.51A (12.54W)	2.75A (13.75W)
BIT Current	3.62A (18.12W)	4.20A (21.02W)

Operating configurations:

- In-rush operating configuration includes video and 512MB RAM.
- Idle operating configuration includes the in-rush configuration as well as one IDE hard drive with Windows XP, keyboard, and mouse.
- BIT (Burn-In-Test) operating configuration includes idle configuration as well as four serial loop-backs, one on-board Compact Flash drive with 64MB Compact Flash, two Ethernet connections, two USB Compact Flash readers with 64MB Compact Flash, two SATA hard drives, one external-power USB CD-ROM, one USB Jump drive.

Environmental Specifications

Table 2-6 provides the most efficient operating and storage condition ranges required for this board.

Table 2-6. Environmental Requirements

	Parameter	1.0MHz Celeron M Conditions	1.4MHz Pentium M Conditions
Temperature	Operating	+0 to +60°C (+32° to +140°F)	+0 to +60°C (+32° to +140°F)
	Storage	–20° to +75°C (–4° to +167°F)	–20° to +75°C (–4° to +167°F)
Humidity	Operating	5% to 90% relative humidity, non-condensing	5% to 90% relative humidity, non-condensing
	Non-operating	5% to 95% relative humidity, non-condensing	5% to 95% relative humidity, non-condensing

Thermal/Cooling Requirements

The CPU, Memory Hub (Northbridge), I/O Hub (Southbridge), and voltage regulators are the main sources of heat on the board. The ReadyBoard 820 is designed to operate at its maximum CPU speed of 1.0 or 1.4GHz. Both CPU versions, the I/O Hub, and the Memory Hub require heatsinks.

Physical Specifications

Table 2-7 lists the physical dimensions of the board, and Figure 2-7 on page 15 shows the dimensions of the I/O panel.

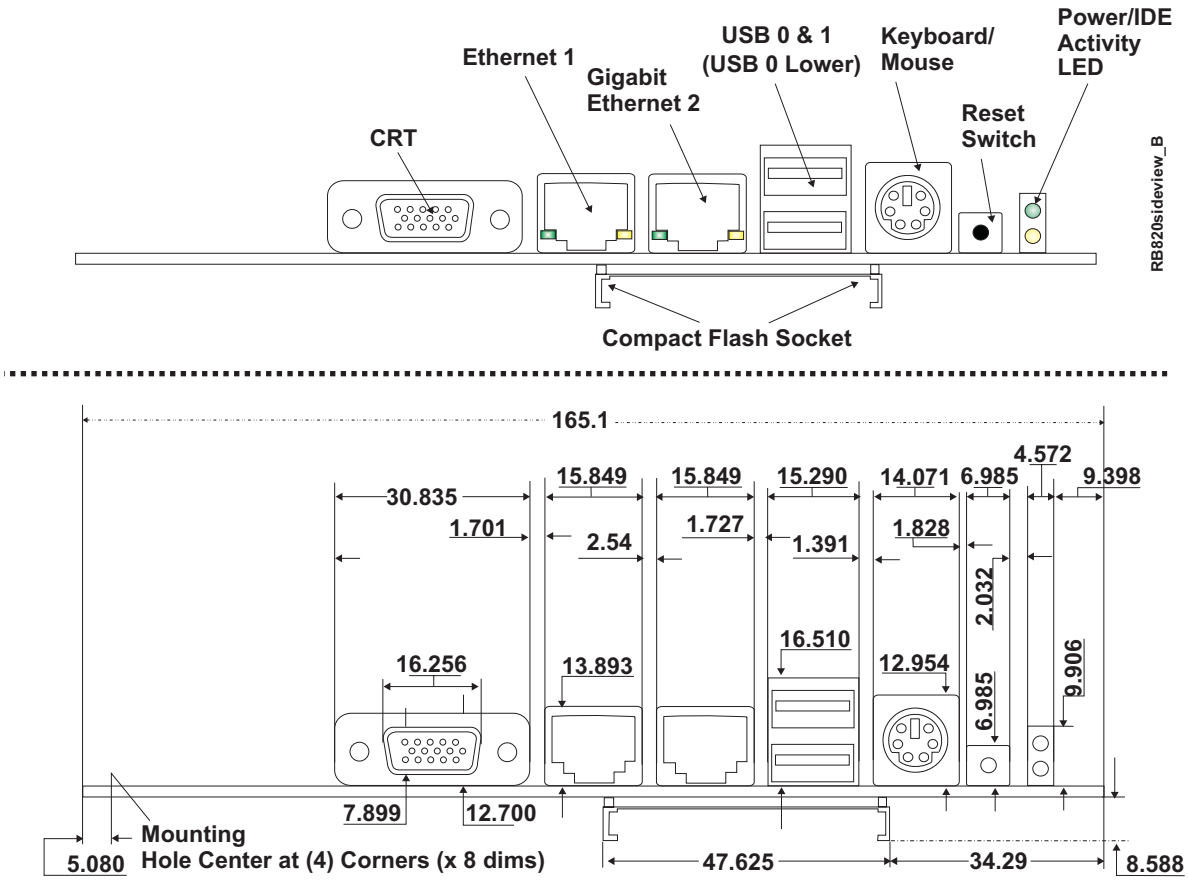
Table 2-7. Weight and Footprint Dimensions

Item	Dimension
Weight	0.24kg. (0.52lbs.)
Height (overall)	16.51mm (0.65")
Width	115mm (4.5")
Length	165mm (6.5")
Thickness	1.57mm (0.062")

NOTE Overall height is measured from the upper board surface to the highest permanent component (USB connector, J23) on the upper board surface. This measurement does not include the heatsinks or fan available for this board.

Mechanical Specifications

Figure 2-7 shows the I/O panel dimensions of the ReadyBoard 820.



All Dimensions in this drawing section are in Millimeters and are approximate.
Board thickness is 1.574mm

Figure 2-7. I/O Panel Dimensions

Chapter 3 Hardware

Overview

This chapter discusses features of the ReadyBoard 820 in the following order:

- Channel Interrupt Assignments
- Memory Map
- I/O Address Map
- Floppy/Parallel Interface
- Serial Interfaces
- USB Interfaces
  - USB 2.0 Support
  - Legacy USB Support
- Audio Interface
- Video Interfaces
  - CRT
  - PanelLink
  - LVDS
- Infrared (IrDA)
- Utility Interface
  - External Power-On Switch
  - External Reset Switch
  - External Speaker (Beep)
- Miscellaneous
  - Real Time Clock (RTC)
  - External Battery (BT1)
  - Temperature Monitoring
  - User GPIO Signals
  - Serial Console
  - Infrared (IrDA) Port
  - System Management Bus (SMBus)
  - Watchdog Timer
- Power Interface
  - Power In
  - Power On
  - Optional System Fan

- Power and Sleep States
  - Power-On Switch
  - Sleep States (ACPI)
  - Wake Up Activities

> **NOTE** ADLINK Technology, Inc. supports only the features/options tested and listed in this manual. The main integrated circuits (chips) used in the ReadyBoard 820 may provide more features or options than are listed for the ReadyBoard 820, but some of these chip features/options are not supported on the board and may not function as specified in the chip documentation.
>
> This chapter does not include pinout tables for standard headers and connectors such as PCI-104, Ethernet RJ45, 44-pin IDE, and Compact Flash.

Channel Interrupt Assignments

The channel interrupt assignments are shown in Table 3-1.

Table 3-1. Channel Interrupt Assignments

Device vs IRQ No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer	X															
Keyboard		X														
Secondary Cascade			X													
COM1					D											
COM2				D												
COM3						O						D				
COM4						D						O				
Floppy							X									
Parallel						O		D								
RTC									X							
IDE															D	
Math Coprocessor														X		
PS/2 Mouse													X			
PCI INTA	Automatically Assigned															
PCI INTB	Automatically Assigned															
PCI INTC	Automatically Assigned															
PCI INTD	Automatically Assigned															
PCI INTE	Automatically Assigned															
PCI INTF	Automatically Assigned															
PCI INTH	Automatically Assigned															
USB	Automatically Assigned															
VGA	Automatically Assigned															
Ethernet	Automatically Assigned															

Legend: D = Default, O = Optional, X = Fixed

NOTE The IRQs for the Ethernet, Video, and Internal LPC bus are automatically assigned by the BIOS Plug and Play logic. Local IRQs assigned during initialization can not be used by external devices.

Memory Map

The following table provides the common PC/AT memory allocations. These are DOS-level addresses. The OS typically hides these physical addresses by way of memory management. Memory below 000500h is used by the BIOS.

Table 3-2. Memory Map

Base Address			Function
00000000h	-	0009FFFFh	Conventional Memory
000A0000h	-	000AFFFFh	Graphics Memory
000B0000h	-	000B7FFFh	Mono Text Memory
000B8000h	-	000BFFFFh	Color Text Memory
000C0000h	-	000CFFFFh	Standard Video BIOS
000D0000h	-	000DFFFFh	Reserved for Extended BIOS
000E0000h	-	000EFFFFh	Extended System BIOS Area
000F0000h	-	000FFFFFh	System BIOS Area (Storage and RAM Shadowing)
00100000h	-	04000000h	Extended Memory (If onboard VGA is enabled, then the amount of memory assigned is subtracted from extended memory)
FFF80000h	-	FFFFFFFFh	System Flash

I/O Address Map

Table 3-3 shows the I/O address map. These are DOS-level addresses. The OS typically hides these physical addresses by way of memory management.

Table 3-3. I/O Address Map

Address (hex)	Subsystem
000-00F	Primary DMA Controller
020-021	Master Interrupt Controller
040-043	Programmable Interrupt Timer (Clock/Timer)
060-06F	Keyboard Controller
070-07F	CMOS RAM, NMI Mask Reg, RT Clock
080-09F	DMA Page Registers
092	Fast A20 gate and CPU reset
094	Motherboard enable
102	Video subsystem register
0A0-0BF	Slave Interrupt Controller
0C0-0DF	Slave DMA Controller #2
0F0-0FF	Math Coprocessor
1F0-1F8	IDE Hard Disk Controller
278-27F	Parallel Port
2E8-2FF	Serial Port 4 (COM4)
2F8-2FF	Serial Port 2 (COM2)
378-37F	Parallel Port (Standard and EPP)
3C0-3DF	VGA
3E8-3EF	Serial Port 3 (COM3)

Table 3-3. I/O Address Map (Continued)

3F0-3F7	Floppy Disk Controller
3F8-3FF	Serial Port 1 (COM1)
778-77A	Parallel Port (ECP Extensions) (Port 378+400)
CF8-CFF	PCIe bus Configuration Address and Data

Floppy/Parallel Interface

The Super I/O controller (W83627HF) provides the floppy controller and the parallel port controller. The floppy controller and the parallel port controller share the same output connector (J14) on the board and the device selection is made in the BIOS Setup Utility.

- Floppy Port Controller supports one floppy drive in the standard formats, such as 360 kB, 720 kB, 1.2 MB, 1.44 MB, or 2.88 MB drives.
- Parallel Port controller supports standard parallel, Bi-directional, ECP and EPP protocols.

> **NOTE** Due to the multiplexed nature of the signals for the floppy and parallel ports, you can only connect one of these devices at a time. Refer to Chapter 4, BIOS Setup Utility later in this manual when selecting the floppy or parallel device in the BIOS Setup Utility. A reboot is necessary for the change of BIOS settings to take affect.

Table 3-4 describes the floppy/parallel port (J14) pin/signals with 26-pins, 2 rows, consecutive (1, 14) with 2 mm pin spacing.

Table 3-4. Floppy/Parallel Interface Pin/Signal Descriptions (J14)

Pin #	Signal	Description
1	Strobe*	Parallel Strobe* – This is an output signal used to strobe data into the printer. I/O pin in ECP/EPP mode.
2	PD0	Parallel Port Data 0 – These pins (0 to 7) provide parallel port data signals.
	INDEX*	Floppy Index – Detects head positioned over the beginning of a track.
3	PD1	Parallel Port Data 1 – See pin-2 (PD0) for more information.
	TRK0*	Floppy Track 0 – Detects when head is positioned over track 0.
4	PD2	Parallel Port Data 2 – See pin-2 (PD0) for more information.
	WPRT*	Floppy Write Protect – Senses if diskette is write protected.
5	PD3	Parallel Port Data 3 – See pin-2 (PD0) for more information.
	RDATA*	Floppy Read Data – Raw serial bit stream from the drive for read operations.
6	PD4	Parallel Port Data 4 – See pin-2 (PD0) for more information.
	DSKCHG*	Floppy Disk Change – Senses when drive door is open or the diskette has been changed since the last drive selection.
7	PD5	Parallel Port Data 5 – See pin-2 (PD0) for more information.
8	PD6	Parallel Port Data 6 – See pin-2 (PD0) for more information.
9	PD7	Parallel Port Data 7 – See pin-2 (PD0) for more information.
10	ACK*	Parallel Acknowledge * – This is a status output signal from the printer. A Low State indicates it has received the data and is ready to accept new data.
	DS1*	Floppy Drive Select 1 – Select drive 1.

Table 3-4. Floppy/Parallel Interface Pin/Signal Descriptions (J14) (Continued)

11	BUSY	Parallel Busy – This is a status output signal from the printer. A High State indicates the printer is not ready to accept data.
	MTR1*	Floppy Motor Control 1 – Select motor on drive 1.
12	PE	Parallel Paper End – This is a status output signal from the printer. A High State indicates it is out of paper.
	WDATA*	Floppy Write Data – Encoded data to the drive for write operations.
13	PSLCT	Printer Select – This is a status output signal from the printer. A High State indicates it is selected and powered on.
	WGATE*	Floppy Write Enable – Drive signal to enable current flow in the write head.
14	AFD*	Parallel Auto Feed* – This is a request signal into the printer to automatically feed one line after each line is printed.
	DRVEN0*	Floppy Drive Density Select Bit 0
15	ERR*	Parallel Error – This is a error status output signal from the printer. A Low State indicates an error condition on the printer.
	HDSEL*	Floppy Head Select – Selects the side for Read/Write operations (0 = side 1, 1 = side 0)
16	PINIT*	Printer Initialize* – This signal is used to Initialize printer. Output in standard mode, I/O in ECP/EPP mode.
	DIR*	Floppy Direction – Direction of head movement (0 = inward motion, 1 = outward motion).
17	SLIN	Parallel Select In – This output signal to the printer is used to select the printer. I/O pin in ECP/EPP mode.
	STEP*	Floppy Step – Low pulse for each track-to-track movement of the head.
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	GND	Ground
24	GND	Ground
25	GND	Ground
26	NC	Not Connected

Note: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Serial Interfaces

The Super I/O (W83627HF) chip and the LPC UART controller (F81216D) provide the circuitry for the four serial ports. The Super I/O chip provides serial ports 1 and 2 through connector J18. The LPC UART controller provides serial ports 3 and 4 through connector J15. The four serial ports support the following features:

- Four individual 16550-compatible UARTs
- Programmable word length, stop bits and parity
- 16-bit programmable baud rate generator
- Interrupt generator
- Loop-back mode
- Four individual 16-bit FIFOs
- Serial A Interface
  - Serial Port 1 (COM1) supports RS232 and full modem support
  - Serial Port 2 (COM2) supports RS232 and full modem support
- Serial B Interface
  - Serial Port 3 (COM3) supports RS232/RS485/RS422 and full modem support
  - Serial Port 4 (COM4) supports RS232/RS485/RS422

> **NOTE** The RS232/RS485/RS422 modes are selected in BIOS Setup under the *Advanced/Super I/O Configuration* menu for Serial ports 3 (COM3) and 4 (COM4). However, the RS232 mode is the default (Standard) for any serial port.
>
> RS485 mode termination is selected with jumper connector JP5, pins 1-2 (COM3), and pins 3-4 (COM4), when the RS485 mode is selected in BIOS Setup.

To implement the two-wire RS485 mode on serial ports 3 or 4, you must tie the equivalent pins together for the selected port.

For example, on Serial Port 3, tie pin 3 to 5 and pin 4 to 6 at the Serial B interface header as shown in Figure 3-1. As an alternate, tie pin 2 to 3 and pin 7 to 8 on the DB9 connector for serial port 3 as shown in Figure 3-1. Refer to the following tables for the specific pin signals of serial ports 3 and 4 on the serial B connector.

The RS422 mode uses a four-wire interface and does not need any pins tied together, but you must select RS485 mode in BIOS Setup.

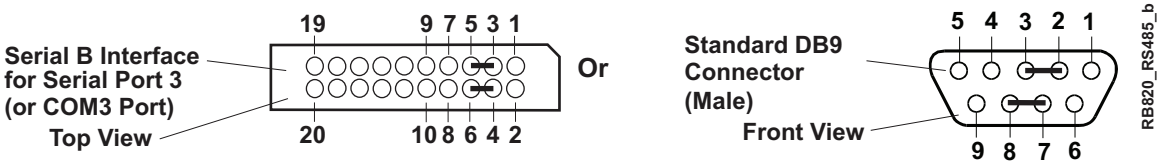


Figure 3-1. RS485 Serial Port Implementation

Table 3-5. Serial A (COM1 and COM2) Interface Pin/Signal Descriptions (J18)

Pin #	Signal	Description
1	DCD1*	Data Carrier Detect 1 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open).
2	DSR1*	Data Set Ready 1 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR1 for overall readiness to communicate.
3	RXD1	Receive Data 1 – Serial port 1 receive data in
4	RTS1*	Request To Send 1 – Indicates Serial port 1 is ready to transmit data. Used as hardware handshake with CTS3 for low level flow control.
5	TXD1	Transmit Data 1 – Serial port 1 transmit data out
6	CTS1*	Clear To Send 1 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS1 for low level flow control.
7	DTR1*	Data Terminal Ready 1 – Indicates Serial port 1 is powered, initialized, and ready. Used as hardware handshake with DSR1 for overall readiness to communicate.
8	RI1*	Ring Indicator 1 – Indicates external serial communications device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
9	GND	Ground
10	NC	Not connected
11	DCD2*	Data Carrier Detect 2 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open).
12	DSR2*	Data Set Ready 2 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR2 for overall readiness to communicate.
13	RXD2	Receive Data 2 – Serial port 2 receive data in
14	RTS2*	Request To Send 2 – Indicates Serial port 2 is ready to transmit data. Used as hardware handshake with CTS2 for low level flow control.
15	TXD2	Transmit Data 2 – Serial port 2 transmit data out
16	CTS2*	Clear To Send 2 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS2 for low level flow control.
17	DTR2*	Data Terminal Ready 2 – Indicates Serial port 2 is powered, initialized, and ready. Used as hardware handshake with DSR2 for overall readiness to communicate.
18	NC	Not connected
19	GND	Ground
20	NC	Not connected

Note: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Table 3-6. Serial B (COM3 and COM4) Interface Pin/Signal Descriptions (J15)

Pin #	Signal	Description
1	DCD3*	Data Carrier Detect 3 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR3 as part of the DTR3/DSR3 handshake.
2	DSR3*	Data Set Ready 3 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR3 for overall readiness to communicate.
3	RXD3 RX3-	Receive Data 3 – Serial port 3 receive data in RX3- – If in RS485 or RS422 mode, this pin is Receive Data 3 -.
4	RTS3* TX3+	Request To Send 3 – Indicates Serial port 3 is ready to transmit data. Used as hardware handshake with CTS3 for low level flow control. TX3+ – If in RS485 or RS422 mode, this pin is Transmit Data 3 +.
5	TXD3 TX3-	Transmit Data 3 – Serial port 3 transmit data out TX3- – If in RS485 or RS422 mode, this pin is Transmit Data 3 -.
6	CTS3* RX3+	Clear To Send 3 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS3 for low level flow control. RX3+ – If in RS485 or RS422 mode, this pin is Receive Data 3 -.
7	DTR3*	Data Terminal Ready 3 – Indicates Serial port 3 is powered, initialized, and ready. Used as hardware handshake with DSR3 for overall readiness to communicate.
8	RI3*	Ring Indicator 3 – Indicates external serial communications device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
9	GND	Ground
10	NC	Not connected
11	DCD4*	Data Carrier Detect 4 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR4 as part of the DTR4/DSR4 handshake.
12	DSR4*	Data Set Ready 4 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR4 for overall readiness to communicate.
13	RXD4 RX4-	Receive Data 4 – Serial port 4 receive data in RX4- – If in RS485 or RS422 mode, this pin is Receive Data 4 -.
14	RTS4* TX4+	Request To Send 4 – Indicates Serial port 4 is ready to transmit data. Used as hardware handshake with CTS4 for low level flow control. TX4+ – If in RS485 or RS422 mode, this pin is Transmit Data 4 +.
15	TXD4 TX4-	Transmit Data 4 – Serial port 4 transmit data out TX4- – If in RS485 or RS422 mode, this pin is Transmit Data 4 -.
16	CTS4* RX4+	Clear To Send 4 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS4 for low level flow control. RX4+ – If in RS485 or RS422 mode, this pin is Receive Data 4 +.

Table 3-6. Serial B (COM3 and COM4) Interface Pin/Signal Descriptions (J15) (Continued)

17	DTR4*	Data Terminal Ready 4 – Indicates Serial port 3 is powered, initialized, and ready. Used as hardware handshake with DSR4 for overall readiness to communicate.
18	NC	Not connected
19	GND	Ground
20	NC	Not connected

Note: The shaded area denotes power or ground. Signals are listed in the following order: RS232 followed by RS485/RS422. The signals marked with * = Negative true logic.

USB Interfaces

The I/O Hub (82801FBM) provides the USB solution for both legacy UHCI controller and EHCI controller (USB 2.0) support. The I/O Hub (Southbridge) contains port-routing logic that determines which controller (UHCI or EHCI) handles the USB data signals. The PC-style (or Standard) connector (J23) provides two of the six USB ports: USB0 and USB1. The J4 header provides USB2 and USB3, and J11 provides USB4 and USB5.

USB 2.0 Support

The I/O Hub (Southbridge) contains an Enhanced Host Controller Interface (EHCI) compliant host controller, which supports up to six high-speed USB 2.0 Specification compliant root ports. The higher speed USB 2.0 specification allows data transfers up to 480 Mbps using the same pins as the six full-speed/ low-speed USB UHCI ports. The I/O Hub (Southbridge) port-routing logic determines which of the controllers (UHCI or the EHCI) processes the USB signals.The USB 2.0 features implemented in the USB ports include the following:

- One EHCI host controller for all six USB ports
- Supports USB V2.0 Specification
- Over-current fuses, located on the board, where USB0 and USB1 share a single fuse (F4), USB2 and USB3 share a single fuse (F2), and USB4 and USB5 share a single fuse (F3). See Table 2-3 on page 13.

Legacy USB Support

The I/O Hub (Southbridge) supports three USB Universal Host Controller Interfaces (UHCI) and each Host Controller includes a root hub with two separate USB ports each, for a total of six USB ports. The USB Legacy features implemented in the USB ports include the following:

- Three root hubs for six USB ports
- Support for USB v1.1, UHCI with integrated physical layer transceivers
- Improved arbitration latency for UHCI controllers
- UHCI controllers support Analog Front End (AFE) embedded cell instead of USB I/O buffers to allow for USB high-speed signaling rates
- Three shared over-current fuses, located on the board, are used on all six USB ports

USB2 and USB3

Table 3-7 describes USB 2 & 3, J4: 10-pins, 2 rows, odd/even (1, 2) with 2 mm pin spacing.

Table 3-7. USB 2 & 3 Interface Pin/Signal Descriptions (J4)

Pin #	Signal	Description
1, 2	VCC	USB Voltage – +5V through shared fuse (F2)
3	USBP2-	Universal Serial Bus Port 2 Data Negative
4	USBP3-	Universal Serial Bus Port 3 Data Negative
5	USBP2+	Universal Serial Bus Port 2 Data Positive
6	USBP3+	Universal Serial Bus Port 3 Data Positive
7, 8, 9, 10	GND	Ground

Note: The shaded area denotes power or ground.

USB4 and USB5

Table 3-8 describes USB 4 & 5, J11: 10-pins, 2 rows, odd/even (1, 2) with 2 mm pin spacing.

Table 3-8. USB 4 & 5 Interface Pin/Signal Descriptions (J11)

Pin #	Signal	Description
1, 2	VCC	USB Voltage – +5V through shared fuse (F3)
3	USBP4-	Universal Serial Bus Port 2 Data Negative
4	USBP5-	Universal Serial Bus Port 3 Data Negative
5	USBP4+	Universal Serial Bus Port 2 Data Positive
6	USBP5+	Universal Serial Bus Port 3 Data Positive
7, 8, 9, 10	GND	Ground

Note: The shaded area denotes power or ground.

Audio Interface

The audio solution on the ReadyBoard 820 is provided by the I/O Hub, 82801DBM (Southbridge) and the on-board Audio CODEC (ALC655). These two chips use a digital interface to communicate between the two, which is defined by AC'97 and is revision 2.3 compliant. The input or output signals for the audio interface go through the 16-pin connector (J20), which has the respective audio connections, and are listed in Table 3-9.

Audio CODEC (ALC655) features

- AC'97 Rev 2.3 compliant
- 18-bit full duplex performance
- Variable sampling rate at 1Hz resolution
- Stereo (Left and Right) Line In
- Stereo (Left and Right) Line Out
- Microphone (mono) in
- PC Beep speaker signal also fed to CODEC for the Line Out (Left and Right) channels

Table 3-9. Audio Interface Pin/Signal Descriptions (J20)

Pin #	Signal	Description
1, 3	NC	Not Connected
2, 4, 7, 8, 11, 12, 13, 14, 16	GND_AUD	Audio ground
5	LINE_OUTL	Line Out signal left channel
6	LINE_OUTR	Line Out signal right channel
9	LINE_INL	Line in signal left channel
10	LINE_INR	Line in signal right channel
15	MICIN	Microphone signal in

Note: The shaded area denotes power or ground.

Video Interfaces

The Memory Hub, 82915GME (Northbridge) provides the graphics control and video signals for traditional CRT monitors, DVI high-resolution displays, and LVDS flat panel displays. The Memory Hub (Northbridge) features are listed below.

Support for 2D/3D graphics with extensive set of instructions including:

- 3D rendering and display
- BLT operations
- MPEG2 decode acceleration
- 3D overlay

CRT features:

- Support for an integrated 400-MHz, 24-bit RAMDAC to drive a progressive scan analog monitor and outputs to three, 8-bit DACs that provide the R, G, and B signals to the monitor
- Support for resolutions up to 1600 x 1200 at 85-Hz refresh, or up to 2048x1536 at 75-Hz refresh
- Support for a maximum allowable video frame buffer size of 64MB UMA (Unified Memory Architecture)

PanelLink features:

- Lossless (digital) transmission of video signal
- Display hardware independence
- Plug and play capabilities (EDID and DDC2B)
- Digital and analog support in a single connector

LVDS Flat Panel features:

- Support for an integrated dual channel LFP Transmitter interface
- Support for LVDS LCD panel resolutions up to UXGA (1600X1200)
- Support for a maximum pixel format of 18 bpp with SSC supported frequency range from 25 MHz to 112 MHz (single channel/dual channel)
- Support for 1 or 2 channel LVDS output
- The 82915GME chip supports the LVDS port on Pipe B of two pipelines

- Support for the LVDS port independently or simultaneously with the Analog Display (CRT) port
- Support for Spread Spectrum Clocking; center and down spread support utilizing an external SSC clock
- Support for panel up-scaling (to fit a smaller source image onto a specific native panel size) as well as panning and centering CRT interface

PanelLink

This header provides the capacity to bring out the TMDS signals to a DVI (Digital Visual Interface) connector.

Table 3-10. PanelLink Pin/Signal Descriptions (J5)

Pin #	Signal	Description
1	TDC2+	TMDS Data 2+
2	VCC5	+5 Volt Power
3	TDC2-	TMDS Data 2-
4	HPDET	Hot Plug Detect
5	TDC1+	TMDS Data 1+
6	GND	Digital Ground
7	TDC1-	TMDS Data 1-
8	GND	Digital Ground
9	TDC0+	TMDS Data 0+
10	SDADDC	DDC Data
11	TDC0-	TMDS Data 0-
12	SCLDDC	DDC Clock
13	TLC+	TMDS Clock+
14	GND	Digital Ground
15	TLC-	TMDS Clock-
16	GND	Digital Ground

Note: The shaded area denotes power or ground.

LVDS Interface (Low Voltage Differential Signaling)

Table 3-11. LVDS Interface Pin/Signal Descriptions (J19)

Pin #	Signal	Description	Line	Channel
1	VCC_INTRV	JP6 = +5 or +12V source		
2	VCC_LCD	JP7 = +3.3 or +5V source		
3	GND	Ground	Gnd	
4	GND	Ground		
5	LVDSB_Clk+	Clock Positive Output	Clk	Channel 2
6	LVDSB_Clk-	Clock Negative Output		
7	LVDSB_Y3	Not Connected	3	
8	LVDSB_Y3	Not Connected		
9	LVDSB_Y2+	Data Positive Output	2	
10	LVDSB_Y2-	Data Negative Output		
11	LVDSB_Y1+	Data Positive Output	1	
12	LVDSB_Y1-	Data Negative Output		
13	LVDSB_Y0+	Data Positive Output	0	
14	LVDSB_Y0-	Data Negative Output		
15	LVD_BKLTCtl	Backlight Control		
16	LCD_EN	LCD Enable		
17	LVDS_Clk+	Data Positive Output	Clk	Channel 1
18	LVDS_Clk-	Data Negative Output		
19	LVDS_Y3+	Not Connected	3	
20	LVDS_Y3-	Not Connected		
21	LVDS_Y2+	Data Positive Output	2	
22	LVDS_Y2-	Data Negative Output		
23	LVDS_Y1+	Data Positive Output	1	
24	LVDS_Y1-	Data Negative Output		
25	LVDS_Y0+	Data Positive Output	0	
26	LVDS_Y0-	Data Negative Output		
27	LDDCCLK	Clock		
28	LDDCDATA	Data		
29	LBKTLEN	Backlight Enable		
30	NC	Not connected		

NOTE Pins 17-26 constitute 1st channel interface of two channels, or a single channel interface. Pins 5-14 constitute 2nd channel interface of two channels.

Note: The shaded areas denote power or ground.

Utility Interface

- Power-On – This control signal externally is provided through a switch by connecting ground to pin 1 on the Utility connector (J16).
- Reset Switch – This signal is provided externally through a switch by connecting ground to pin 3 on the Utility connector (J16). This signal line is shared with Reset Switch (J25).
- PC Beep Speaker – The output signals from the Southbridge (82801FBM) and the Super I/O (W83627HF) are fed to pin 5 of the Utility connector (J16) through an OR circuit, and in conjunction with the +5V signal (pin 4), drives an external PC Beep speaker. The PC Beep speaker signal from the Southbridge is also fed to the on-board Audio CODEC to provide a PC Beep signal for the Line out connections.

Table 3-12. Utility Interface Pin/Signal Descriptions (J16)

Pin #	Signal	Description
1	PS_On	Power On input (connect between pins 1 & 2)
2	GND	Ground
3	RST_SW	Reset Switch input or output (connect between pins 3 & 2)
4	+5V	+5 Volts
5	Speaker	PC Beep Speaker + Output (connect between pins 5 & 4)

Note: The shaded area denotes power or ground.

Miscellaneous

Real Time Clock (RTC)

The ReadyBoard 820 contains a Real Time Clock (RTC). The CMOS RAM is backed up with a Lithium Battery. If the battery is not present, a battery-free boot option in the BIOS completes the boot process and resets the clock to the default date and time.

External Battery (BT1)

An external battery input connection is provided through the battery connector (BT1) for an external battery. The external battery is used to power the Real Time Clock. ADLINK provides a small Lithium battery, taped to the board and connected to the external battery connection (BT1). This small external Lithium battery serves as an on-board power source.

Temperature Monitoring

The Super I/O controller (W83627HF) performs the temperature monitoring function and receives input directly from one thermistor (RT2) on the front of the board.

NOTE	The ReadyBoard 820 requires heatsinks for the CPU, Northbridge, and Southbridge.

User GPIO Signals

The ReadyBoard 820 provides GPIO pins for custom use. The signals are routed to the J12 header, and the enable and initialize values are set in the BIOS.

For more information about GPIO pin operation, refer to the Programming Manual for the Super I/O (W83627HF) controller at:

http://www.winbond-usa.com/products/winbond_products/pdfs/PCIC/627hf.pdf

Table 3-13. User GPIO Signals Pin/Signal Descriptions (J12)

Pin #	Signal	Description
1	GND	Ground
2	VCC	+5 Volts DC +/ 5%
3	GPIO4	User defined
4	GPIO5	User defined
5	GPIO6	User defined
6	GPIO7	User defined
7	GPIO0	User defined
8	GPIO1	User defined
9	GPIO2	User defined
10	GPIO3	User defined

Note: The shaded area denotes power or ground.

Serial Console

The ReadyBoard 820 supports the serial console (or console redirection) feature. This I/O function is provided by an ANSI-compatible serial terminal, or the equivalent terminal emulation software running on another system. This can be very useful when setting up the BIOS on a production line for systems that are not connected to a keyboard and display.

Infrared (IrDA) Port

The Infrared Data Association (IrDA) signals pass through a two-way communications header for an external IrDA device using infrared as the transmission medium. There are two basic infrared implementations provided; the Hewlett-Packard Serial Infrared (HPSIR) and the Amplitude Shift Keyed Infrared (ASKIR) methods. HPSIR is a serial implementation of infrared developed by Hewlett-Packard. The IrDA (HPSIR and ASKIR) signals share the same header as the IrDA model select signals. These signals are operating system (OS) and/or application dependent and are based on the user's application, but can be configured and enabled in the BIOS Setup Utility.

The HPSIR method allows serial communication at baud rates up to 115k baud. Each word is sent serially beginning with a zero value start bit. A zero is sent when a single infrared pulse is sent at the beginning of the serial bit time. A one is sent when no infrared pulse is sent during the bit time.

The Amplitude Shift Keyed Infrared (ASKIR) allows serial communication at baud rates up to 19.2k baud. Each word is sent serially beginning with a zero value start bit. A zero is sent when a 500kHz waveform is sent for the duration of the serial bit time. A one is sent when no transmission is sent during the serial bit time.

Both of these methods require an understanding of the timing diagrams provided in the Super I/O controller (W83627HF) specifications available from the manufacture’s web site and referred to earlier in this manual.

For more information, refer to the W83627HF chip databook and the Infrared Data Association web site at http://www.irda.org.

> **NOTE** For faster speeds and infrared applications not covered in this brief description, refer to the W83627HF chip specifications by Winbond.

Table 3-14. Infrared (IrDA) Interface Pin/Signal Descriptions (J6)

Pin #	Signal	Description
1	VCC	+5 volts
2	IRTX	IR Transmit Data
3	CIRRX	IR Mode Select
4	IRRX	IR Receive Data
5	GND	Ground

Note: The shaded area denotes power or ground.

System Management Bus (SMBus)

The I/O Hub (Southbridge) chip (82801DBM) contains both a host and slave SMBus port; but the host cannot access the slave internally. The slave port allows an external master access to the I/O Hub through connector (J13). The master contained in the I/O Hub (82801DBM) is used to communicate with the SODIMM EPROM, Super I/O, Ethernet 1 and 2, and the clock generator. Table 3-15 lists the device name and corresponding reserved binary addresses on the SMBus. Table 3-16 lists the SMBus pin/signals on 5-pins, 1 row, 2 mm pin spacing on the external SMBus connector (J13).

Table 3-15. SMBus Reserved Addresses

Component	Address Binary
SODIMM EPROM	$1010,000x_b$
Clock Generator (ICS950201)	$1101,001x_b$
I/O Hub (82801DBM)	$1000,100x_b$
I/O Hub (82801DBM)	$0001,000x_b$

Note: The I/O Hub has two reserved addresses.

Table 3-16. SMBus Signals Pin/Signal Descriptions (J13)

Pin #	Signal	Description
1	VCC5Dual	+5V standby voltage
2	SMBCLK	SMBus Clock
3	SMBDATA	SMBus Data
4	SMBALERT*	SMBus Alert
5	GND	Ground

Note: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Watchdog Timer

The Watchdog Timer (WDT) restarts the system if a mishap occurs. Possible problems include failure to boot properly, the application software's loss of control, unexpected conditions on the bus, or other hardware or software malfunctions.

The WDT (Watchdog Timer) can be used both during the boot process and during normal system operation.

- During the Boot process – If the operating system fails to boot in the time interval set in the BIOS, the system will reset.

  Enable the WDT in the Boot Settings of BIOS Setup. Set the WDT for a time-out interval in seconds, between 1 and 255, in one second increments. Ensure you allow enough time for the operating system (OS) to boot. The OS or application must tickle the WDT before the timer expires.

- During System Operation – An application can set up the WDT hardware through a BIOS call, or by accessing the hardware directly. Some ADLINK Board Support Packages provide an API interface to the WDT. The application must tickle the WDT before the timer expires or the system will be reset. The BIOS implements interrupt 15 function 0C3h to manipulate the WDT.

Power Interfaces

The ReadyBoard 820 uses various voltages onboard, but only one voltage is required externally (+5 volts) through the external connector, which uses a 4-pin header with 0.200" (5.08 mm) spacing. The optional +12V volts is also provided on the input connector as a pass through voltage, but is not used on the board except for LVDS power, PCI-104 bus, and optional ISA bus power. All other onboard voltages, including the CPU core voltages, are derived from the externally supplied +5 volts DC +/- 5%.

Power In

Table 3-17 lists the pin signals for Power In header (J1).

CAUTION	This table matches the board even though the +5V and +12V are swapped in comparison to typical AT power supply cables.

Table 3-17. Power In Pin/Signal Descriptions (J1)

Pin #	Signal	Description
1	+5V	+5.0 volts DC +/- 5%
2	GND	Ground
3	GND	Ground
4	+12V	This pass through +12 voltage is primarily for PCI-104 bus power, and LCD power (may also be backlight power).

Note: The shaded area denotes power or ground. The +12V on the Power In connector (J1) is used for the LVDS (LCD panel), PCI-104 Bus, and optional ISA Bus power, but may also be supplied externally.

Power On

The signals on this header allow the ATX power supply to be turned off (soft off) from the ReadyBoard 820 by operating system (OS) control. However, if you use a non-ATX power supply, then you will not have the soft off feature for sleep states normally provided by ATX power supplies.

Table 3-18. Power On Header Pin/Signal Descriptions (J2)

Pin #	Signal	Description
1	VCC5SBY	+5V Standby Voltage – This voltage (refer to ATX Specification 2.2 or later for minimum requirement) is supplied from the ATX power supply and is required for normal operation and sleep states.
2	GND	Ground
3	PS_ON*	Power Supply On – This signal is sent to the ATX power supply from the ReadyBoard 820 to turn on the ATX power supply. This signal can also be used to turn off the ATX power supply or go into a suspended or standby state.

Note: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Optional System Fan

The ReadyBoard 820 has an optional system fan connector for those environmental situations where customers may require it.

Table 3-19. Optional System Fan Interface Pin/Signal Descriptions (J17)

Pin #	Signal	Description
1	DET	Fan Speed Detect – This is the fan speed tachometer signal.
2	+5	+5 volts DC +/- 5%
3	GND	Ground

Note: The shaded area denotes power or ground.

Power and Sleep States

The following information applies to the ReadyBoard 820 only if an ATX power supply is used to provide power. If a non-ATX power supply is used, the ReadyBoard 820 is controlled only by the Power On/Off switch on the power supply and the various sleep states are not available.

Power-On Switch

The Power-On switch turns the ReadyBoard 820 and its attached power supply to a fully On condition, if you are using an ATX power supply. Normally—if the operating system (OS) supports sleep states—the OS will turn off the ReadyBoard 820 and its power supply during the OS shut down process. If the OS supports sleep states, the Power-On switch will also transition the ReadyBoard and its power supply between a fully Powered-On state, various sleep states depending on the OS control setting, and a fully Powered-Off state. If the OS does not support sleep states, then the Power-On switch only turns on or off power to the ReadyBoard 820.

The sleep states are OS dependent and not available if your OS does not support power management based on the ACPI standard. An OS supporting ACPI will allow the Power-On switch to be configured through a user interface.

The Power-On switch is provided externally by connecting a momentary switch between pins 1 and 2 on the Utility connector (J16). The Power-On signal occurs when ground is placed on pin 2 of J16.

Sleep States (ACPI)

The ReadyBoard 820 supports the ACPI (Advanced Configuration and Power Interface) standard, which is a key component of certain Operating Systems' power management. The supported features (sleep states) listed here are only available when an ACPI-compliant OS is used for the ReadyBoard, such as Windows 2000/XP. The term "sleep" state refers to a reduced power consumption state, which can be re-started (awakened), restoring full operation to the ReadyBoard 820.

In these various sleep states, the ReadyBoard 820 appears to be off, indicated by such things as no display on the attached monitor and no activity for the connected CD-ROM or hard drives. However, when the ReadyBoard 820 detects certain types of activity (i.e. power button, mouse, keyboard, or LAN activity), it returns to a fully operational state. The type of activity detected is based on those supported by the ReadyBoard 820.

The ReadyBoard 820 supports at least four ACPI power states, depending on the operating system used and its ability to manage sleep states. Typically, the Power On switch is used to wake up from a sleep state, or transition from one state to another, but this is dependent on the operating system.

- 1st state is normal Power-On (S0).
  - To go to a fully powered on state, the ReadyBoard 820 must either be powered Off (S5), or in a sleep state (S1 or S4), and then the Power On/Off switch is pressed for less than 4 seconds (default).
  - The ReadyBoard 820 can transition from this state (S0) to the various states described below, depending on the power management capability of the OS and how it is programmed.
- 2nd state is a standby state (S1).

  In this state, no internal operations take place except for the internal RTC (Real Time Clock) and the contents of RAM. This typically includes no activity for the CPU, CD-ROM, or hard disk drives. The CPU may be active, and the peripheral devices may power down if no signals occur or power to the device(s) is not provided. The ReadyBoard 820 appears to be off including the Power-On LED.
  - Normally, to enter this sleep state, the ReadyBoard 820 must be fully powered on (S0) while the OS transitions the ReadyBoard into this standby state (S1) under user control.
  - To exit this sleep state, typically the power button is used to wake up the ReadyBoard 820 to restore full operation, including the Power-On LED. Typically, pressing the power switch for less than 4 seconds (default) will restore full operation.
- 3rd state is Suspend to RAM or Standby [Windows] (S3).

  In this state, main memory (RAM) and the internal RTC (Real Time Clock) are the only devices where power is maintained. This state (Suspend to RAM) stores the state of the operating system prior to shutdown including all open applications and open documents, etc. in main memory. This allows users to resume their work exactly where they left off just prior to entering this state (S3) when the system restores power and the contents of main memory.

  This state takes longer to restore and uses less power than S1 or S2, but if AC power is completely lost, the contents of main memory (RAM), including any changes to documents or data stored in RAM during S3, is also lost.
  - To enter the Suspend to RAM (S3) or Standby state, the computer must be fully powered on and the OS transitions the computer into this sleep state under user control.
  - To exit this sleep state, typically pressing the Power On switch for less then 4 seconds (default) will restore full operation.
- 4^{th} state is a hibernate or suspend-to-disk state (S4).

  In this state, no internal operations take place, except for the internal RTC. This includes no activity for the CPU, CD-ROM, or hard disk drives. The ReadyBoard 820 appears to be off, including the external Power-On LED if connected. Your system will take longer to wake-up in this sleep state, however, since your data is saved to the disk, it is more secure and should not be lost in the event of a power failure.
  - To enter a hibernate or suspend-to-disk state, the ReadyBoard 820 must be fully powered on while the OS transitions the ReadyBoard 820 into this sleep state (S4) under user control.

- To exit this sleep state, typically pressing the power switch for less than 4 seconds (default) will restore full operation.

- 5th state is the normal power off or shutdown (S5).

  All activity stops, except the internal clock, if there is a backup battery installed. Removing the power cord from the power source ensures all activity is stopped, except the internal clock.

  - To go to a fully powered down state, the ReadyBoard 820 must either be powered on, or in a sleep state, and then the Power On/Off switch is pressed for more than 4 seconds.
  - To go to a fully powered up state, press the power switch for less than 4 seconds (default) and full operation is restored.

The OS may provide additional programming features to change the activation time for each state, and to shutdown or transition the ReadyBoard 820 at certain times, depending on the way the OS interface is programmed. Refer to the OS vender's documentation for power management under the ACPI standard.

NOTE Some operating systems use the keyboard, mouse, Wake-on-Ring (serial port), and Wake-on-LAN (Ethernet port) as an activity to wake up the system from a sleep state. Refer to Table 3-20 for the wake up activity conditions supported by the ReadyBoard 820.

Wake Up Activities

The wake up events listed in Table 3-20 can be used to wake up the ReadyBoard 820 from any of the supported sleep states mentioned above.

Table 3-20. Wake Up Activities and Conditions

Signal/Device	Condition
Power On Switch	If the Power-On switch is pressed for more than 4 seconds, the system will wake up from any of the sleep states.
Ethernet Ports (2) (LAN Ports)	If Wake On LAN is [Enabled], then the system will wake from one of the sleep states through direct addressing, magic packets, or link status changes.
PS/2 Keyboard & Mouse	If you use a PS/2 keyboard or mouse, any activity from the keyboard or mouse could wake the system.
USB Devices	If you use a USB keyboard or mouse instead of a PS/2 device, the USB device could wake the system.
Serial Ports (2)	If Wake On Ring is [Enabled], then Serial Ports 1 and 2 can be used to wake the system.

Chapter 4 BIOS Setup

Introduction

This section assumes the user is familiar with general BIOS Setup. Refer to the appropriate PC reference manuals for information about the on-board ROM-BIOS software interface. If ADLINK has added to or modified the standard functions, these functions will be described.

Entering BIOS Setup (VGA Display)

To access BIOS Setup using a VGA display for the ReadyBoard 820:

1. Turn on the VGA monitor and the power supply to the ReadyBoard 820.
2. Start Setup by pressing the [Del] key when the following message appears on the boot screen.

```
Press DEL to run Setup
```

> **NOTE** If the setting for *Quick Boot* is [Enabled], you may not see this prompt appear on screen. If this happens, press the <Del> key early in the boot sequence to enter BIOS Setup.

3. Follow the instructions on the right side of the screen to navigate through the selections and modify any settings.

Entering BIOS Setup (Remote Access)

This section describes how to enable the Remote Access in VGA mode and enter the BIOS setup through a serial terminal or PC.

1. Turn on the power supply to the ReadyBoard 820 and enter the BIOS Setup Utility in VGA mode.
2. Set the BIOS feature *Remote Access Configuration* to [Enable] under the **Advanced** menu.
3. Accept the default options or make your own selections for the balance of the Remote Access fields and record your settings.
4. Ensure you select the type of remote serial terminal you will be using and record your selection.
5. Select *Save Changes and Exit* and then shut down the ReadyBoard 820.
6. Connect the remote serial terminal (or the PC with communications software) to the COM port you selected and recorded earlier in the BIOS Setup Utility.
7. Turn on the remote serial terminal or PC and set it to the settings you selected in the BIOS Setup Utility.

   The default settings for the ReadyBoard 820 are:

   - COM1
   - 115200
   - 8 bits
   - 1 stop bit
   - no parity
   - no flow control
   - [Always] for *Redirection After BIOS POST*

8. Restore power to the ReadyBoard 820 and press the F4 key after you see the following screen prompt.

```
Press <space bar> to update BIOS
```

> **NOTE** If *Quick Boot* is set to [Enabled], you may not see the screen prompt and might need to press F4 earlier in the boot sequence to enter Setup.

9. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen.

> **NOTE** The serial console port is not hardware protected. Diagnostic software that probes hardware addresses may cause a loss or failure of the serial console functions.

OEM Logo (Splash) Utility

The ReadyBoard 820 BIOS supports a graphical logo utility, which can be customized by the user and displayed when enabled through the BIOS Setup Utility. The graphical image can be a company logo or any custom image the user wants to display during the boot process. The custom image can be displayed as the first image displayed on screen during the boot process and remain there, depending on the options selected in BIOS Setup, while the OS boots.

Logo Image Requirements

The user's image may be customized with any image editing tool, and the system will automatically convert the image into an acceptable format to the tools (files and utilities) provided by ADLINK. The ReadyBoard 820 OEM Logo utility supports the following image formats:

- Bitmap image
  - 16-Color, 640x480 pixels
  - 256-Color, 640x480 pixels
- JPG image
  - 16-Color, 640x480 pixels
- PCX image
  - 256-Color, 640x480 pixels
- A file size not larger than the sample image

> **NOTE** For procedures on loading custom images, see the OEM Logo Utility document available on the Ampro By ADLINK web site.

Appendix A Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed below in Table A-1. Requests for support through the Ask an Expert are given the highest priority, and usually will be addressed within one working day.

- ADLINK's Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the Ampro By ADLINK web page at http://www.adlinktech.com/AAE/. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.

  ADLINK strongly suggests that you register with the web site. By creating a profile on the ADLINK web site, you will have a portal page called "My ADLINK" unique to you with access to exclusive services and account information.

- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to My Stuff area where you can check status, update your request, and access other features.

- Download Service – This service is also free and available 24 hours a day at http://www.adlinktech.com. For certain downloads such as technical documents and software, you must register online before you can log in to this service.

Table A-1. Technical Support Contact Information

Method	Contact Information
Ask an Expert	http://www.adlinktech.com/AAE/
Web Site	http://www.adlinktech.com
Standard Mail	Contact us should you require any service or assistance. **ADLINK Technology, Inc.** Address: 9F, No.166 Jian Yi Road, Chungho City, Taipei County 235, Taiwan 台北縣中和市建一路 166 號 9 樓 Tel: +886-2-8226-5877 Fax: +886-2-8226-5717 Email: service@adlinktech.com **Ampro ADLINK Technology, Inc.** Address: 5215 Hellyer Avenue, #110, San Jose, CA 95138, USA Tel: +1-408-360-0200 Toll Free: +1-800-966-5200 (USA only) Fax: +1-408-360-0222 Email: info@adlinktech.com **ADLINK Technology (China) Co., Ltd.** Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203) 300 Fang Chun Rd., Zhangjiang Hi-Tech Park, Pudong New Area, Shanghai, 201203 China Tel: +86-21-5132-8988 Fax: +86-21-5132-3588 Email: market@adlinktech.com

Table A-1. Technical Support Contact Information (Continued)

	ADLINK Technology Beijing Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室(100085) Rm. 801, Power Creative E, No. 1, B/D Shang Di East Rd., Beijing, 100085 China Tel: +86-10-5885-8666 Fax: +86-10-5885-8625 Email: market@adlinktech.com **ADLINK Technology Shenzhen** Address: 深圳市南山区科技园南区高新南七道 数字技术园 A1 栋 2 楼 C 区 (518057) 2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7, High-Tech Industrial Park S., Shenzhen, 518054 China Tel: +86-755-2643-4858 Fax: +86-755-2664-6353 Email: market@adlinktech.com **ADLINK Technology (Europe) GmbH** Address: Nord Carree 3, 40477 Duesseldorf, Germany Tel: +49-211-495-5552 Fax: +49-211-495-5557 Email: emea@adlinktech.com **ADLINK Technology, Inc. (French Liaison Office)** Address: 15 rue Emile Baudot, 91300 Massy CEDEX, France Tel: +33 (0) 1 60 12 35 66 Fax: +33 (0) 1 60 12 35 66 Email: france@adlinktech.com **ADLINK Technology Japan Corporation** Address: 151-0072 東京都渋谷区幡ヶ谷 1-1-2 朝日生命幡ヶ谷ビル 8F Asahiseimei Hatagaya Bldg. 8F 1-1-2 Hatagaya, Shibuya-ku, Tokyo 151-0072, Japan Tel: +81-3-4455-3722 Fax: +81-3-5333-6040 Email: japan@adlinktech.com **ADLINK Technology, Inc. (Korean Liaison Office)** Address: 서울시 서초구 서초동 1506-25 한도 B/D 2 층 2F, Hando B/D, 1506-25, Seocho-Dong, Seocho-Gu, Seoul 137-070, Korea Tel: +82-2-2057-0565 Fax: +82-2-2057-0563 Email: korea@adlinktech.com **ADLINK Technology Singapore Pte. Ltd.** Address: 84 Genting Lane #07-02A, Cityneon Design Centre, Singapore 349584 Tel: +65-6844-2261 Fax: +65-6844-2263 Email: singapore@adlinktech.com **ADLINK Technology Singapore Pte. Ltd. (Indian Liaison Office)** Address: No. 1357, "Anupama", Sri Aurobindo Marg, 9th Cross, JP Nagar Phase I, Bangalore - 560078, India Tel: +91-80-65605817 Fax: +91-80-22443548 Email: india@adlinktech.com

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