aTCA-3100 Series

AdvancedTCA Base/Fabric Switch Blade

User's Manual

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1 Introduction

1.1 Product overview

This aTCA-3100 Series is an AdvancedTCA switch blade supporting base and fabric Interfaces for ATCA shelves up to 14 slots (2 hub slots and 12 node slots). The board provides fabric switching of 1000Base-X gigabit Ethernet on each fabric slot.

The aTCA-3100 Series is based on the Vitesse® VSC7310 switch silicon and the Intel® 80219 600 MHz XScale® I/O processor. The basic aTCA-3100 base switch blade features a 24-port 10/100/1000BASE-T link including 12 node slots, 8 front panel egress RJ-45 ports, 2 ShMC ports, 1 inter-switch port, and 1 control plane CPU access port.

In addition to the aTCA-3100 features, the fabric aTCA-3110 switch blade features a 24-port 1000BASE-BX link including 14 PIGMG 3.1 option 1-compliant node slots, 2 front panel egress ports, and 8 reserved ports from Rear Transition Module I/O.

On top of the aTCA-3110 feature set, the aTCA-3120 highlights a fabric switch blade with 10GbE uplink support with an additional 10 gigabit Ethernet XFP uplink port.

Linux-based operating system runs on Intel® 80219 processor to provide a complete development platform for the management of Layer 2/3 packet switching and routing, plus sophisticated standards such as IEEE 802.1d Spanning Tree Protocol (STP), IEEE 802.1p Quality-of-Service (QoS), IEEE 802.1Q 4096 VLANs, IEEE 802.3ad Link aggregation, Port Mirroring, and DHCP services.

1.2 Features

- Control plane processor
  - Intel® 80219 XScale® I/O processor at 600 MHz
  - Configuration port (Serial)
  - Two 10/100/1000 Ethernet maintenance ports, one Ethernet, one ShMC
  - 64-bit, 66 MHz PCI bus
  - DDR200 SDRAM (up to 1 GB)
  - Up to 128 MB of flash program storage
  - Dual-flash boot capability
  - IPM controller
- Base interface
  - 1000Base-TX gigabit Ethernet
  - Layer 3 switching
  - Base interface support for 14 node slots
  - Base interface support for redundant switch card
  - Full-speed non-blocking switching (port-to-port)
  - Eight (8) front-panel GbE ports (base interface access)
  - Support for dual-Ethernet shelf manager control (ShMC port)
- Fabric interface (aTCA-3110 and aTCA-3120 only)
  - 1000Base-X gigabit Ethernet, Option 1, Link Type 2
  - Layer 3 switching
  - Supports 14-slot shelf
  - Fabric interface - one GbE ports per channel (13 ports)
  - Full-speed, non-blocking switching (port-to-port)
  - Two front panel GbE ports (fabric access)
  - Rear I/O GbE ports (fabric access, RTM required)

1.3 Reference specifications

- ▷ PICMG 3.0 R2.0 ECN001 ATCA Core Specification
- ▷ PICMG 3.1 R1.0 Option1 Ethernet Over PICMG 3.0

1.4 Block diagrams

1.4.1 aTCA-3100 base switch blade

Figure 1-1 shows the major components and sub-systems of the aTCA-3100 blade.

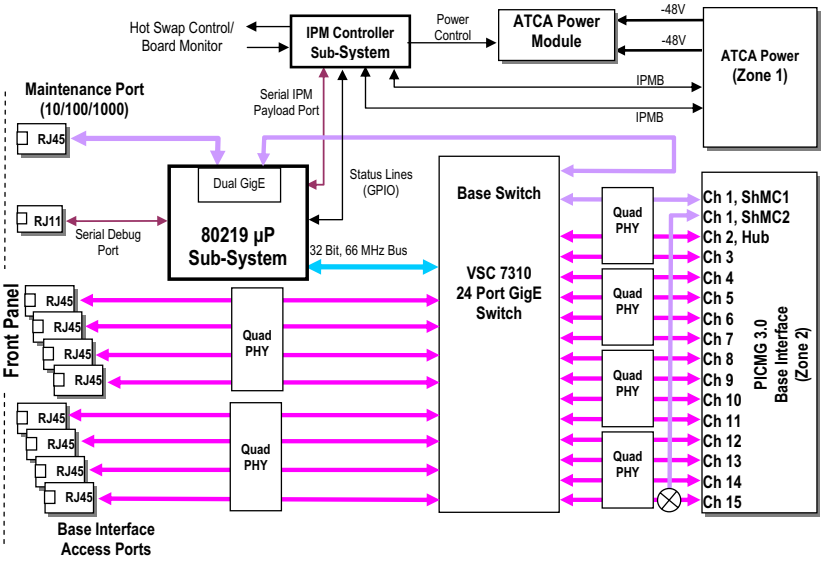


Figure 1-1: aTCA-3100 card-level block diagram

1.4.2 aTCA-3110/3120 fabric switch blade

Figure 1-2 shows the major components and sub-systems of the aTCA-3110 and aTCA-3120 blades.

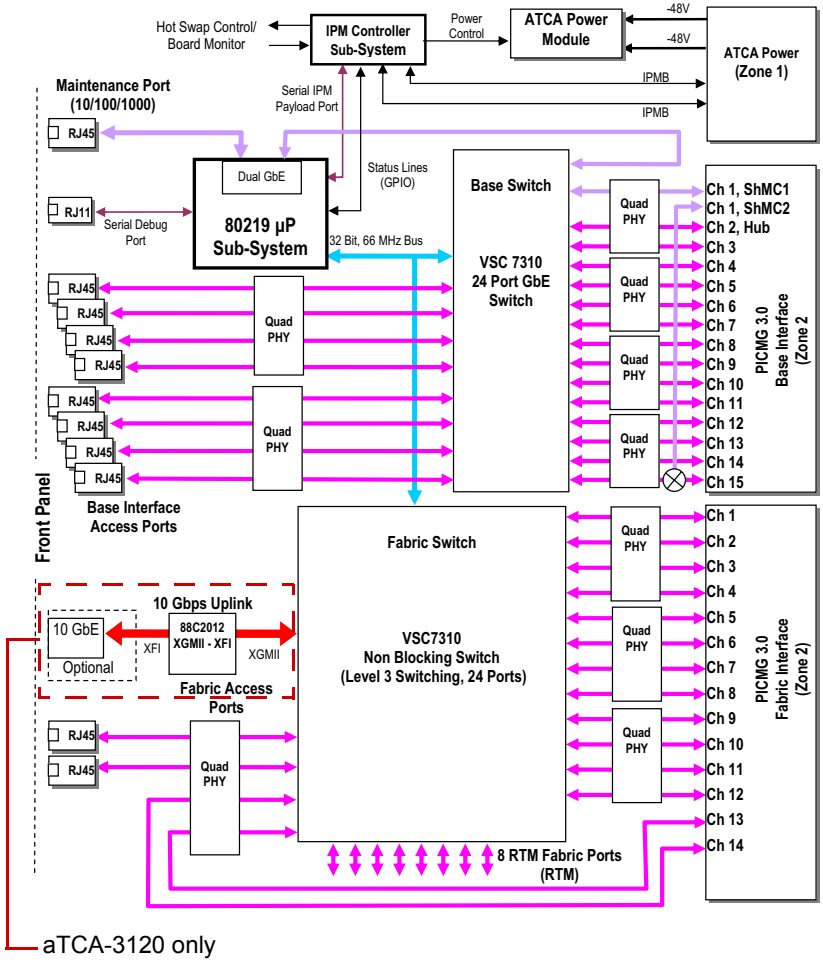


Figure 1-2: aTCA-3110/3120 card-level block diagram

The switch connects to the ATCA channels in such a way as to provide one GbE port for each ATCA channel.

Two of the fabric switch ports are allocated for front panel external access. Eight additional ports are routed to a rear RTM access connector.

An optional 10 gigabit uplink port on aTCA-3120 provides support for a high-speed external link to the shelf.

1.4.3 80219 CPU sub-system block diagram

Figure 1-3 shows the control processor sub-system.

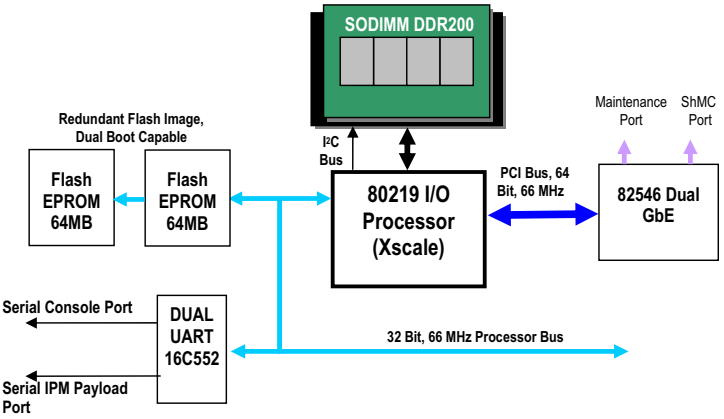


Figure 1-3: CPU sub-system block diagram

The processor sub-system consists of an Intel® 80219 Xscale I/O processor with 32 Mb Flash EPROM for program storage and a SODIMM slot that supports DDR200 SDRAM of up to 1 GB.

A dual-UART provides a debug port and an IPM payload interface port. A dual-GbE MAC delivers an external maintenance/debug port and a Shelf Management Controller access port (ShMC).

All other devices on the board are accessed via a 32-bit, 66 MHz PCI bus.

1.5 Functional Description

1.5.1 Control processor sub-system

Intel® 80219 Xscale I/O processor

The 80219 is an Intel® Xscale base I/O processor running at 600 MHz. It has a 200 MHz DDR interface, a 64-bit, 66 MHz PCI-X capable bus that runs on PCI mode. It also supports the flash and Dual-I2C interfaces.

Dual-flash EPROM

The processor subsystem supports up to 128 MB of flash memory using two 29GL512 or 64 MB devices.

DDR SODIMM

A SODIMM socket is onboard to support a single 200 MHz DDR module up to 1 GB.

Dual UART

An SC16C2550 provides dual-RS232 UART. One RS232 serial port serves as an external debug/maintenance port giving terminal access to the Redboot Boot loader and monitor program.

The other serial port serves as the payload port for IPM controller communications.

82546 dual-MAC

An Intel® 82546 dual-GbE MAC/PHY resides on the processor's PCI bus (64-bit, 66 MHz). One GbE port is connected externally to provide a maintenance port for debug and program update.

The other GbE ports provides access to the Shelf Management Controller (ShMC) through the base interface switch chip.

32-bit, 66 MHz PCI bus

The processor sub-system provides a 32-bit, 66 MHz PCI bus for dual-GbE MAC access. The Intel® 80219 provides a 32-bit, 66 MHz processor bus capable of performing 8-, 16-, or 32-bit access mode. This bus is used to access the flash EPROM, the dual-UART and both base and fabric switch chips for configuration.

I2C bus

The Intel® contains onboard I2C ports, one of which is used to access the Serial Presence Detect EEPROM on the DIMM module.

IPM controller sub-system

The aTCA-3100 Series uses the Pigeon Point Systems BMR-H8S-ATCA IPM controller sub-system design. The IPM controller controls and monitors the power, reset, and ATCA channel enables for the payload. Figure 1-4 shows the IPM controller sub-system.

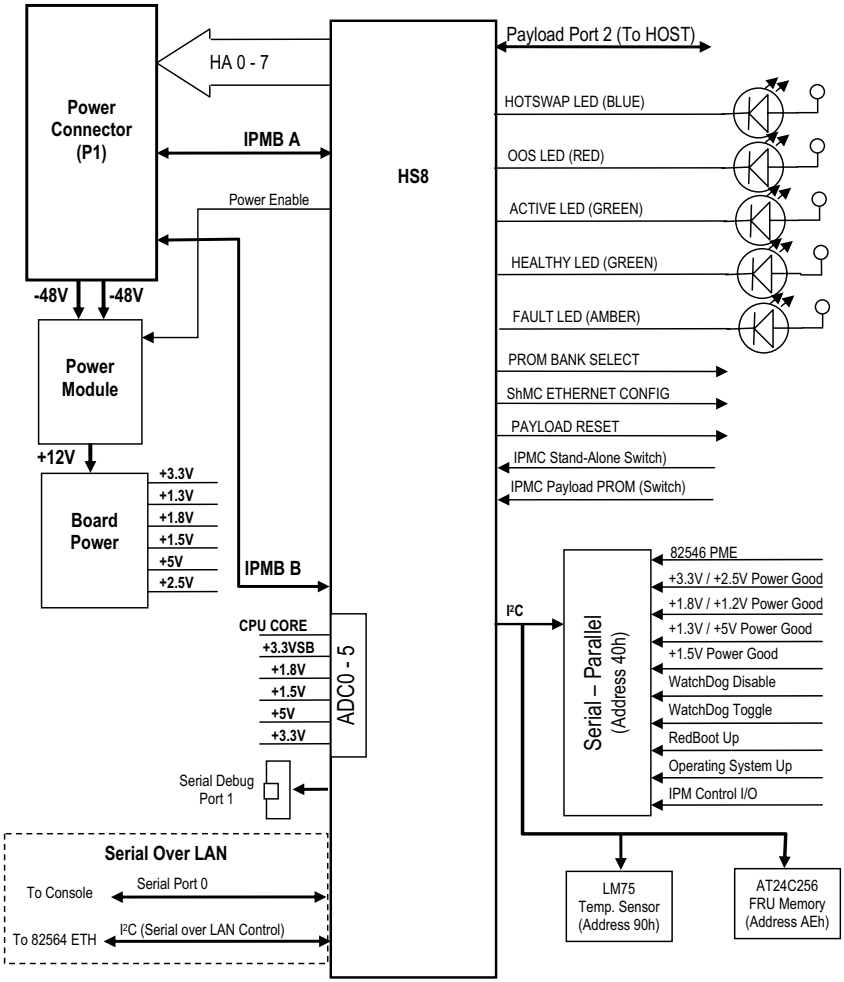


Figure 1-4: IPMC block diagram

1.5.2 Base interface

The ATCA base interface may be installed on a 14-slot shelf with two hub slots and 12 node slots.

VSC7310 switch

The base hub uses a Vitesse VSC7310 switch capable of Ethernet packet switching of Layer 2 and Layer 3 packets.

Shelf management port

The ATCA-3100 Series supports dual-shelf management access ports. This provides access through the base switch to the CPU as well as all node cards connected to the base interface. An external shelf manager can access all cards on the base interface for configuration, software updates, or status.

Dual-star base interface shelf topology

Figure 1-5 shows the dual-star base channel routing topology of a shelf with two aTCA-3100 Series cards installed on a 14-slot backplane. The aTCA-3100 Series supports shelf chassis with up to 14 slots.

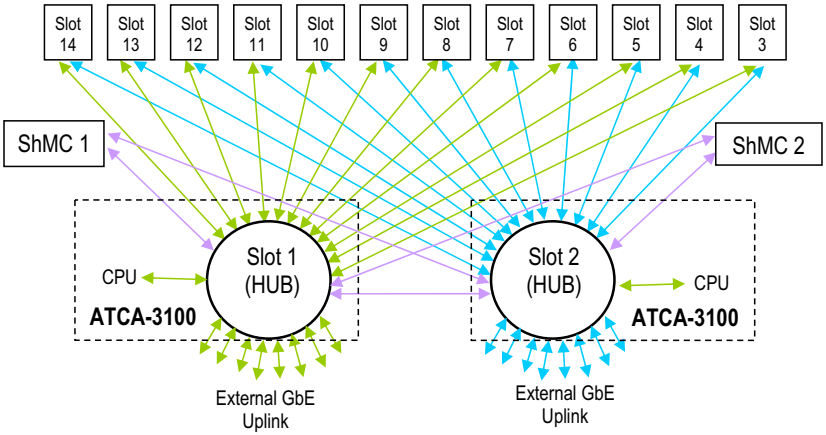


Figure 1-5: Dual-star base interface logical slot routing

1.5.3 Fabric interface

The ATCA fabric interface supports a shelf with up to 14 slots. This translates to two hub slots and 12 node slots.

Fabric switch

The aTCA-3110/3120 uses the Vitesse VSC7310 24-port switch for the fabric switch interface. This provides non-blocking switching on all ports. The fabric interface supports 14 ATCA GbE fabric slots (1 GbE per channel) with two front-panel ports and eight RTM interfaces (requires RTM with PHYs).

External GbE fabric access ports

Two front-panel fabric access GbE ports are also provided. These can be used as low speed uplink ports or simply as external device fabric access ports.

Rear I/O GbE fabric access ports

Eight ports forming the fabric switch are routed to an RTM access connector. These can be used as GbE uplink ports or simply as external device fabric access ports. The RTM connections are RGMII interfaces and requires a Rear Transition Module with GbE PHYs.

Dual-star fabric interface shelf topology

Figure 1-6 shows the dual-star fabric channel routing topology of a shelf with two aTCA-3110/3120 cards installed.

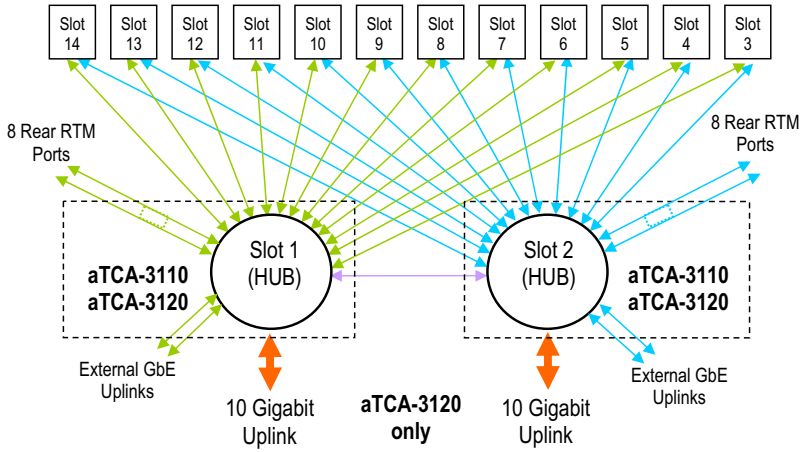


Figure 1-6: Dual-star fabric interface logical routing slot

1.6 Port slot mapping

This section describes the relationships between each switch chips channel, PHY port and external connection.

1.6.1 Base switch channel mapping

Table 1-1 shows the relationship between the physical switch port, PHY address, and the external connections for each channel of the base switch.

External Connection	Logical Port	Logical Slot Connection
Base Channel 1, PORT 0	Port 1	ShMC 1
Base Channel 2, PORT 0	Port 2	Slot 1 or 2, Inter-Switch Connection
Base Channel 3, PORT 0	Port 3	Slot 3
Base Channel 4, PORT 0	Port 4	Slot 4
Base Channel 5, PORT 0	Port 5	Slot 5
Base Channel 6, PORT 0	Port 6	Slot 6
Base Channel 7, PORT 0	Port 7	Slot 7
Base Channel 8, PORT 0	Port 8	Slot 8
Base Channel 9, PORT 0	Port 9	Slot 9
Base Channel 10, PORT 0	Port 10	Slot 10
Base Channel 11, PORT 0	Port 11	Slot 11
Base Channel 12, PORT 0	Port 12	Slot 12
Base Channel 13, PORT 0	Port 13	Slot 13
Base Channel 14, PORT 0	Port 14	Slot 14
Base Channel 15, PORT 0	Port 15	Slot 15 / ShMC 2
Payload CPU	Port 16	Internal
External Port 1	Port 17	Front Panel 1
External Port 2	Port 18	Front Panel 2
External Port 3	Port 19	Front Panel 3
External Port 4	Port 20	Front Panel 4
External Port 5	Port 21	Front Panel 5
External Port 6	Port 22	Front Panel 6
External Port 7	Port 23	Front Panel 7
External Port 8	Port 24	Front Panel 8

Table 1-1: Base switch channel mapping

1.7 Fabric Switch Channel Mapping

Table 1-2 shows the relationship between the physical switch port and the external connections for each channel of the fabric switch.

External Connection	Logical Port	Logical Slot Connection
External Port 1	Port 1	Front Panel
External Port 2	Port 2	Front Panel
Fabric Channel 3, PORT 0	Port 3	Slot 3
Fabric Channel 4, PORT 0	Port 4	Slot 4
Fabric Channel 5, PORT 0	Port 5	Slot 5
Fabric Channel 6, PORT 0	Port 6	Slot 6
Fabric Channel 7, PORT 0	Port 7	Slot 7
Fabric Channel 8, PORT 0	Port 8	Slot 8
Fabric Channel 9, PORT 0	Port 9	Slot 9
Fabric Channel 10, PORT 0	Port 10	Slot 10
Fabric Channel 11, PORT 0	Port 11	Slot 11
Fabric Channel 12, PORT 0	Port 12	Slot 12
Fabric Channel 13, PORT 0	Port 13	Slot 13
Fabric Channel 14, PORT 0	Port 14	Slot 14
Fabric Channel 15, PORT 0	Port 15	Slot 15
Fabric Channel 1, PORT 0	Port 16	Slot 1 or 2, Inter-Switch Connection
Rear I/O Port 1	Port 17	-
Rear I/O Port 2	Port 18	-
Rear I/O Port 3	Port 19	-
Rear I/O Port 4	Port 20	-
Rear I/O Port 5	Port 21	-
Rear I/O Port 6	Port 22	-
Rear I/O Port 7	Port 23	-
Rear I/O Port 8	Port 24	-

Table 1-2: Fabric switch channel mapping

1.8 Front panel

1.8.1 aTCA-3100

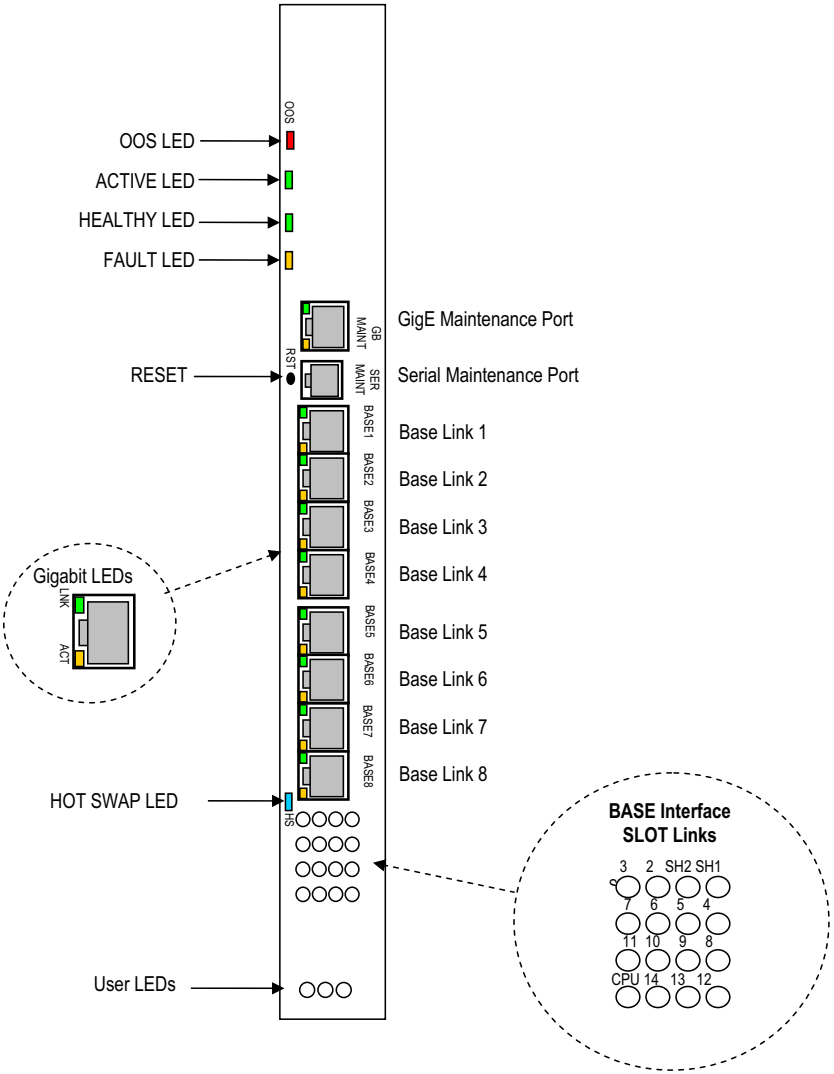


Figure 1-7: aTCA-3100 front panel

1.8.2 aTCA-3110

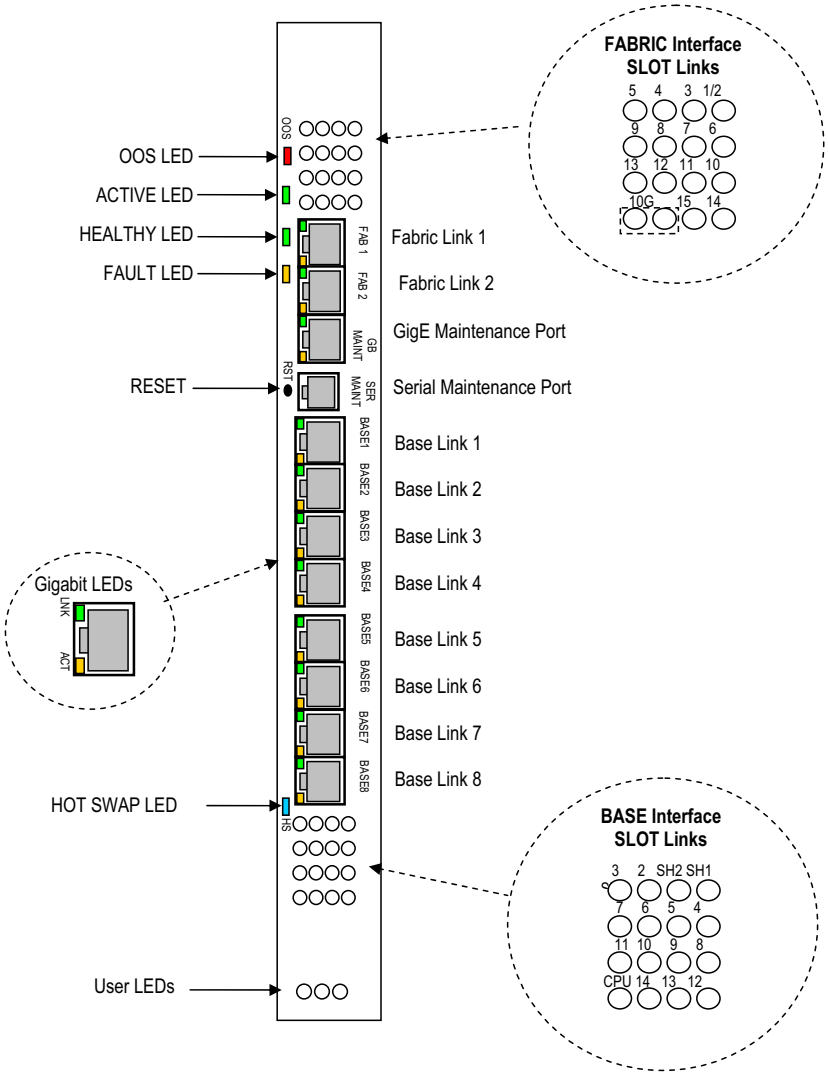


Figure 1-8: aTCA-3110 front panel

1.8.3 aTCA-3120

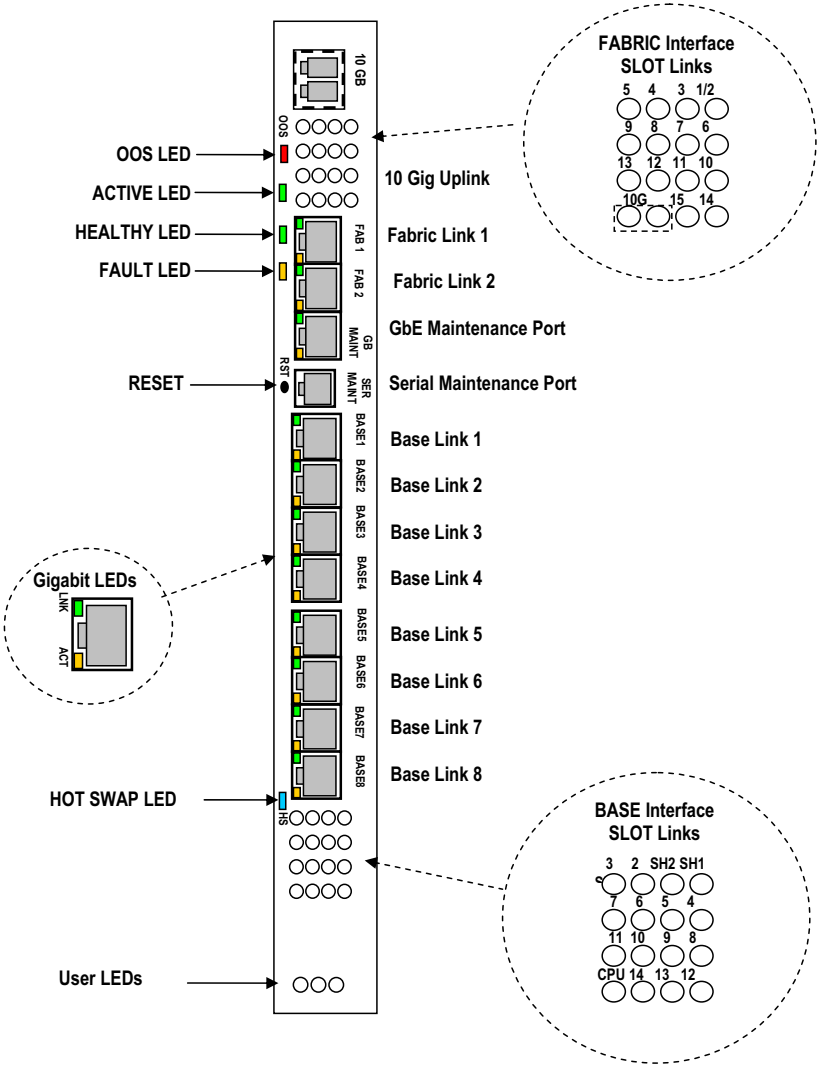


Figure 1-9: aTCA-3120 front panel

1.9 Configuration switches

The aTCA-3100 Series have two four position switch blocks that can be used for card configuration.

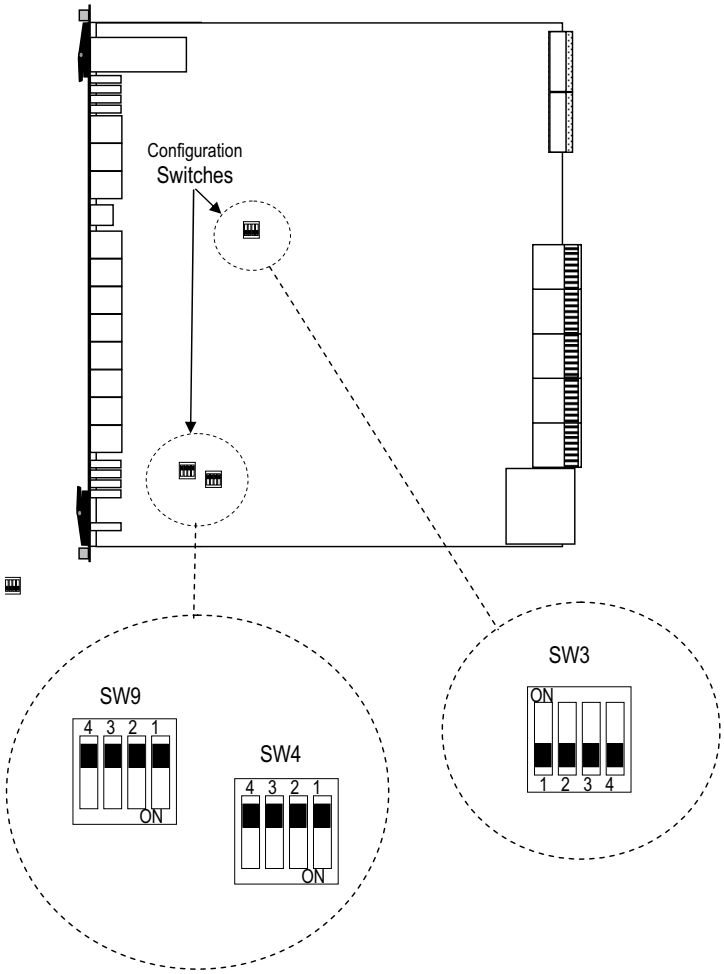


Figure 1-10: aTCA-3100 Series switch locations

1.9.1 Switch 3

SW3 is used as an option selection switch. The base and fabric configuration parameters are saved automatically based on the setting of these four switches.

Switch	Description
1	Payload Option Select Switch (ON = 0, OFF= 1)
2	Payload Option Select Switch (ON = 0, OFF= 1)
3	Payload Option Select Switch (ON = 0, OFF= 1)
4	Payload Option Select Switch (ON = 0, OFF= 1)

Table 1-3: Switch 3 description

Options selection

Options	Switch selections			
	4	3	2	1
Option 1 (Default)	0	0	0	0
Option 2	0	0	0	1
Option 3	0	0	1	0
Option 4	0	0	1	1
Option 5	0	1	0	0
Option 6	0	1	0	1
Option 7	0	1	1	0
Option 8	0	1	1	1
Option 9	1	0	0	0
Option 10	1	0	0	1
Option 11	1	0	1	0
Option 12	1	0	1	1
Option 13	1	1	0	0
Option 14	1	1	0	1
Option 15	1	1	1	0
Option 16	1	1	1	1

Table 1-4: Options selection for SW3

NOTE Refer to the aTCA-31xx Configuration Guide for additional information on option configuration files.

1.9.2 Switch 4

Switch	Description
1	IPMC Flash Write Enable (ON = Disable, OFF = Enable, Default = ON)
2	IPMC Payload PROM Boot Select Switch (Default = OFF)
3	ShMC Ethernet Select (OFF = Dual 100 Mb, ON = Single GbE, Default = OFF)
4	IPMC Stand-Alone Switch (ON = Stand-Alone, OFF = Normal)

Table 1-5: Switch 4 description

1.9.3 Switch 9

Switch	Description
1	IPMC NMI Configuration Selection (ON=0, OFF=1, Default = OFF)
2	IPMC MD2 Configuration Selection (ON=0, OFF=1, Default = OFF)
3	IPMC MD1 Configuration Selection (ON=0, OFF=1, Default = OFF)
4	IPMC MD0 Configuration Selection (ON=0, OFF=1, Default = OFF)

Table 1-6: Switch 9 description

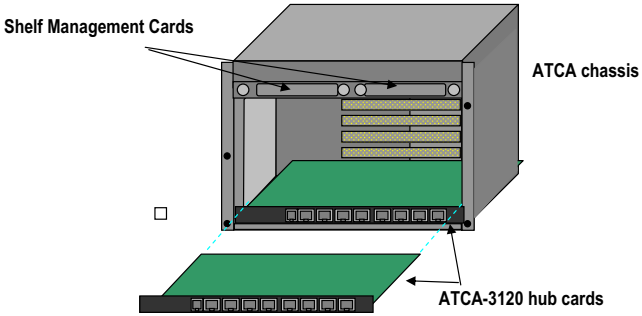
NOTE This switch is for IPMC debug purposes. The switches must be left in their default configurations (normal operating mode).

2 Installation

2.1 Installing the card

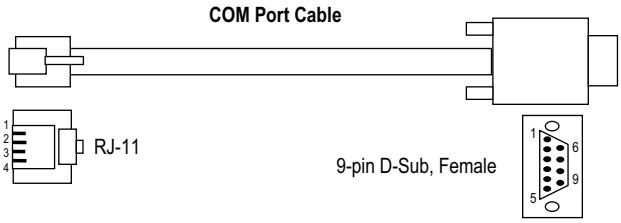
The aTCA-3100 Series switch blade installs into a standard AdvancedTCA chassis. The card is intended to be installed into switch slots that are logic slot 1 and 2 in the chassis.

When installing the card into a chassis, make sure that the card is seated correctly and the card ejector latches are fully engaged. If the left ejector latch is not engaged, the card will not power-up and boot.



2.1.1 Connecting the serial cable

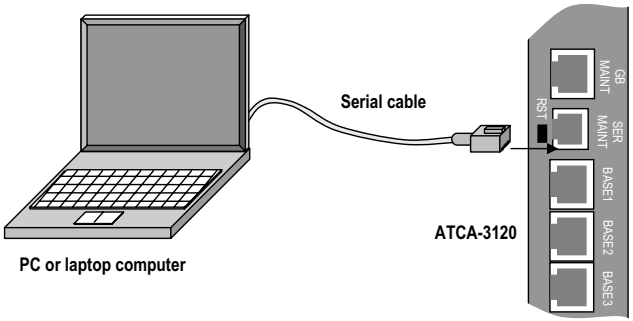
To initially use the card and develop applications you will need a serial cable. The serial cable required for use with standard COM ports is shown below. It is an RJ11 to female DB9 converter. This cable connects the card's serial port (RJ-11), to a standard PC COM port..



This table below shows the connections when using either a 6-pin or 4-pin RJ-11 connector.

6-pin RJ-11	4-pin RJ-11	9-pin D-Sub pin#	9-pin D-Sub pin#
1		(Not Used)	Chassis Ground
2	1	3	TX
3	2	2	RX
4	3	5	Ground
5	4	(Not Used)	Ground
6		(Not Used)	Ground

Connect the serial cable to the computer's serial port (COM1 or COM2) and to the aTCA-3100 Series card serial interface. Refer to the illustration below..



2.1.2 Accessing the aTCA-3100 Series card

Follow these steps to connect the aTCA-3100 Series card to the development platform host system:

1. Use the serial cable to connect the aTCA-3100 Series card to the serial port on the development host.
2. Run a terminal emulation program from the development host (e.g. HyperTerminal for Microsoft® Windows® systems or minicom for Linux systems), then configure the program for VT100 emulation with the following set of

communication settings: no flow control, no parity bits, 8 data bits, 1 stop bit, and 115200 baud rate.

3. Reset or power-up the aTCA-3100 Series card. It takes about one and a half minutes to boot to the Linux prompt after the shelf manager commands the board to power up.

2.1.3 Firmware boot sequence

The following boot sequence is executed when the board is powered.

- Boot Monitor (RedBoot)

  The Boot Monitor is based on RedBoot, which is an acronym for RedHat Embedded Debug and Bootstrap. RedBoot is used to load and boot Linux.

- Linux Kernel, Filesystem

  The RedBoot Loader automatically boots Linux. Refer to the aTCA-3100 Series Configuration Guide for more information on Linux configurations.

- Switch Software

  The switch software and drivers are automatically loaded under Linux. The switch software consists of background drivers and configuration utilities for both base and fabric interfaces. The base interface is configured using **cli-base** and the fabric interface can be configured using **cli-fabric**. Refer to the aTCA-3100 Series Configuration Guide for additional information.

3 Connector Pinouts

3.1 Zone 1 connector (P10)

Pin #	Signal	Description
1	(Reserved)	Reserved (Not Connected)
2	(Reserved)	Reserved, (Not Connected)
3	(Reserved)	Reserved, (Not Connected)
4	(Reserved)	Reserved, (Not Connected)
5	HA0	HA0 Hardware Address Bit 0
6	HA1	HA1 Hardware Address Bit 1
7	HA2	HA2 Hardware Address Bit 2
8	HA3	HA3 Hardware Address Bit 3
9	HA4	HA4 Hardware Address Bit 4
10	HA5	HA5 Hardware Address Bit 5
11	HA6	HA6 Hardware Address Bit 6d
12	HA7/P	HA7/P Hardware Address Bit 7 (Odd Parity Bit)
13	SCL_A	IPMB Clock, Port A
14	SDA_A	IPMB Data, Port A
15	SCL_B	IPMB Clock, Port B
16	SDA_B	IPMB Data, Port B
17	MT1_TIP	Unused (Not Connected)
18	MT2_TIP	Unused (Not Connected)
19	-RING_A	Unused (Not Connected)
20	-RING_B	Unused (Not Connected)
21	MT1_RING	Unused (Not Connected)
22	MT2_RING	Unused (Not Connected)
23	RRTN_A	Unused (Not Connected)
24	RRTN_B	Unused (Not Connected)
25	SHELF_GND	Connection to Shelf Ground and safety ground
26	LOGIC_GND	Ground reference and return for logic signals
27	ENABLE_B	Short pin for -48V Feed B power sequencing
28	VRTN_A	Voltage Return A -48 Volt return
29	VRTN_B	Voltage Return B -48 Volt return
30	EARLY_A	-48 Volt Early A -48 Volt input, Unused (Not Connected)
31	EARLY_B	-48 Volt Early B -48 Volt input, Unused (Not Connected)

Table 3-1: Zone 1 connector P10

Pin #	Signal	Description
32	ENABLE_A	Short pin for -48V Feed A power sequencing
33	-48V_A	-48 Volt input, Min power Feed A
34	-48V_B	-48 Volt input, Main Power Feed B

Table 3-1: Zone 1 connector P10

3.2 Zone 2 connectors

3.2.1 J20

ROWS	A	B	GND AB	C	D	GND CD	E	F	GND EF	G	H	GND GH
1	N/C	N/C	N/C	N/C	N/C	GND	N/C	N/C	GND	N/C	N/C	GND
2	N/C	N/C	GND	N/C	N/C	GND	N/C	N/C	GND	N/C	N/C	GND
3	N/C	N/C	GND	N/C	N/C	GND	N/C	N/C	GND	N/C	N/C	GND
4	N/C	N/C	GND	N/C	N/C	GND	N/C	N/C	GND	N/C	N/C	GND
5	N/C	N/C	GND	TERM	TERM	GND	N/C	N/C	GND	TERM	TERM	GND
6	N/C	N/C	GND	TERM	TERM	GND	N/C	N/C	GND	TERM	TERM	GND
7	N/C	N/C	GND	TERM	TERM	GND	N/C	N/C	GND	TERM	TERM	GND
8	N/C	N/C	GND	TERM	TERM	GND	N/C	N/C	GND	TERM	TERM	GND
9	N/C	N/C	GND	TERM	TERM	GND	N/C	N/C	GND	TERM	TERM	GND
10	FCH12_TXp	FCH12_TXn	GND	FCH12_RXp	FCH12_RXn	GND	N/C	N/C	GND	TERM	TERM	GND

Table 3-2: J20 connector

3.2.2 J21

ROWS	A	B	GND AB	C	D	GND CD	E	F	GND EF	G	H	GND GH
1	N/C	N/C	GND	TERM	TERM	GND	N/C	N/C	GND	TERM	TERM	GND
2	FCH11_TXp	FCH11_TXn	GND	FCH11_RXp	FCH11_RXn	GND	N/C	N/C	GND	TERM	TERM	GND
3	N/C	N/C	GND	TERM	TERM	GND	N/C	N/C	GND	TERM	TERM	GND
4	FCH10_TXp	FCH10_TXn	GND	FCH10_RXp	FCH10_RXn	GND	N/C	N/C	GND	TERM	TERM	GND
5	N/C	N/C	GND	TERM	TERM	GND	N/C	N/C	GND	TERM	TERM	GND
6	FCH9_TXp	FCH9_TXn	GND	FCH9_RXp	FCH9_RXn	GND	N/C	N/C	GND	TERM	TERM	GND
7	N/C	N/C	GND	TERM	TERM	GND	N/C	N/C	GND	TERM	TERM	GND
8	FCH8_TXp	FCH8_TXn	GND	FCH8_RXp	FCH8_RXn	GND	N/C	N/C	GND	TERM	TERM	GND
9	N/C	N/C	GND	TERM	TERM	GND	N/C	N/C	GND	TERM	TERM	GND
10	FCH7_TXp	FCH7_TXn	GND	FCH7_RXp	FCH7_RXn	GND	N/C	N/C	GND	TERM	TERM	GND

Table 3-3: J21 connector

3.2.3 J22

ROWS	A	B	GND AB	C	D	GND CD	E	F	GND EF	G	H	GND GH
1	N/C	N/C	GND	TERM	TERM	GND	N/C	N/C	GND	TERM	TERM	GND
2	FCH11_TXp	FCH11_TXn	GND	FCH11_RXp	FCH11_RXn	GND	N/C	N/C	GND	TERM	TERM	GND
3	N/C	N/C	GND	TERM	TERM	GND	N/C	N/C	GND	TERM	TERM	GND
4	FCH10_TXp	FCH10_TXn	GND	FCH10_RXp	FCH10_RXn	GND	N/C	N/C	GND	TERM	TERM	GND
5	N/C	N/C	GND	TERM	TERM	GND	N/C	N/C	GND	TERM	TERM	GND
6	FCH9_TXp	FCH9_TXn	GND	FCH9_RXp	FCH9_RXn	GND	N/C	N/C	GND	TERM	TERM	GND
7	N/C	N/C	GND	TERM	TERM	GND	N/C	N/C	GND	TERM	TERM	GND
8	FCH8_TXp	FCH8_TXn	GND	FCH8_RXp	FCH8_RXn	GND	N/C	N/C	GND	TERM	TERM	GND
9	N/C	N/C	GND	TERM	TERM	GND	N/C	N/C	GND	TERM	TERM	GND
10	FCH7_TXp	FCH7_TXn	GND	FCH7_RXp	FCH7_RXn	GND	N/C	N/C	GND	TERM	TERM	GND

Table 3-4: J22 connector

3.2.4 J23

ROWS	A	B	GND AB	C	D	GND CD	E	F	GND EF	G	H	GND GH
1	N/C	N/C	GND	TERM	TERM	GND	N/C	N/C	GND	TERM	TERM	GND
2	FCH1_TXp	FCH1_TXn	GND	FCH1_RXp	FCH1_RXn	GND	N/C	N/C	GND	TERM	TERM	GND
3	N/C	N/C	GND	TERM	TERM	GND	N/C	N/C	GND	TERM	TERM	GND
4	FCH0_TXp	FCH0_TXn	GND	FCH0_RXp	FCH0_RXn	GND	N/C	N/C	GND	TERM	TERM	GND
5	BCH1_Ap	BCH1_An	GND	BCH1_Bp	BCH1_Bn	GND	BCH1_Cp	BCH1_Cn	GND	BCH1_Dp	BCH1_Dn	GND
6	BCH2_Ap	BCH2_An	GND	BCH2_Bp	BCH2_Bn	GND	BCH2_Cp	BCH2_Cn	GND	BCH2_Dp	BCH2_Dn	GND
7	BCH3_Ap	BCH3_An	GND	BCH3_Bp	BCH3_Bn	GND	BCH3_Cp	BCH3_Cn	GND	BCH3_Dp	BCH3_Dn	GND
8	BCH4_Ap	BCH4_An	GND	BCH4_Bp	BCH4_Bn	GND	BCH4_Cp	BCH4_Cn	GND	BCH4_Dp	BCH4_Dn	GND
9	BCH5_Ap	BCH5_An	GND	BCH5_Bp	BCH5_Bn	GND	BCH5_Cp	BCH5_Cn	GND	BCH5_Dp	BCH5_Dn	GND
10	BCH6_Ap	BCH6_An	GND	BCH6_Bp	BCH6_Bn	GND	BCH6_Cp	BCH6_Cn	GND	BCH6_Dp	BCH6_Dn	GND

Table 3-5: J23 connector

3.2.5 J24

ROWS	A	B	GND AB	C	D	GND CD	E	F	GND EF	G	H	GND GH
1	BCH7_Ap	BCH7_An	GND	BCH7_Bp	BCH7_Bn	GND	BCH7_Cp	BCH7_Cn	GND	BCH7_Dp	BCH7_Dn	GND
2	BCH8_Ap	BCH8_An	GND	BCH8_Bp	BCH8_Bn	GND	BCH8_Cp	BCH8_Cn	GND	BCH8_Dp	BCH8_Dn	GND
3	BCH9_Ap	BCH9_An	GND	BCH9_Bp	BCH9_Bn	GND	BCH9_Cp	BCH9_Cn	GND	BCH9_Dp	BCH9_Dn	GND
4	BCH10_Ap	BCH10_An	GND	BCH10_Bp	BCH10_Bn	GND	BCH10_Cp	BCH10_Cn	GND	BCH10_Dp	BCH10_Dn	GND
5	BCH11_Ap	BCH11_An	GND	BCH11_Bp	BCH11_Bn	GND	BCH11_Cp	BCH11_Cn	GND	BCH11_Dp	BCH11_Dn	GND
6	BCH12_Ap	BCH12_An	GND	BCH12_Bp	BCH12_Bn	GND	BCH12_Cp	BCH12_Cn	GND	BCH12_Dp	BCH12_Dn	GND
7	BCH13_Ap	BCH13_An	GND	BCH13_Bp	BCH13_Bn	GND	BCH13_Cp	BCH13_Cn	GND	BCH13_Dp	BCH13_Dn	GND
8	BCH14_Ap	BCH14_An	GND	BCH14_Bp	BCH14_Bn	GND	BCH14_Cp	BCH14_Cn	GND	BCH14_Dp	BCH14_Dn	GND
9	N/C	N/C	GND	N/C	N/C	GND	N/C	N/C	GND	N/C	N/C	GND
10	N/C	N/C	GND	N/C	N/C	GND	N/C	N/C	GND	N/C	N/C	GND

Table 3-6: J24 connector

3.3 Zone 3 connectors

3.3.1 J2 Rear I/O connector

ROW #	A	B	C	D	E	F
19	N/C	N/C	N/C	N/C	N/C	GND
18	N/C	N/C	N/C	N/C	N/C	GND
17	N/C	N/C	N/C	N/C	N/C	GND
16	N/C	N/C	N/C	N/C	N/C	GND
15	N/C	N/C	N/C	N/C	N/C	GND
14	N/C	N/C	N/C	N/C	N/C	GND
13	GND	GND	GND	GND	GND	GND
12	GND	CH23_RD2	CH23_RD3	CH23_TD2	CH23_TD3	GND
11	GND	CH23_RD0	CH23_RD1	CH23_TD0	CH23_TD1	GND
10	GND	CH23_RXCLK	CH23_RXCTL	CH23_TXCLK	CH23_TXCTL	GND
9	GND	GND	GND	GND	GND	GND
8	GND	CH22_RD2	CH22_RD3	CH22_TD2	CH22_TD3	GND
7	GND	CH22_RD0	CH22_RD1	CH22_TD0	CH22_TD1	GND
6	GND	CH22_RXCLK	CH22_RXCTL	CH22_TXCLK	CH22_TXCTL	GND
5	GND	GND	GND	GND	GND	GND
4	GND	CH21_RD2	CH21_RD3	CH21_TD2	CH21_TD3	GND
3	GND	CH21_RD0	CH21_RD1	CH21_TD0	CH21_TD1	GND
2	GND	CH21_RXCLK	CH21_RXCTL	CH21_TXCLK	CH21_TXCTL	GND
1	GND	GND	GND	GND	GND	GND

Table 3-7: J2 RTM connector

3.3.2 J1 Rear I/O connector

ROW #	A	B	C	D	E	F
25	GND	CH20_RD2	CH20_RD3	CH20_TD2	CH20_TD3	GND
24	GND	CH20_RD0	CH20_RD1	CH20_TD0	CH20_TD1	GND
23	GND	CH20_RXCLK	CH20_RXCTL	CH20_TXCLK	CH20_TXCTL	GND
22	GND	GND	GND	GND	GND	GND
21	GND	CH19_RD2	CH19_RD3	CH19_TD2	CH19_TD3	GND
20	GND	CH19_RD0	CH19_RD1	CH19_TD0	CH19_TD1	GND
19	GND	CH19_RXCLK	CH19_RXCTL	CH19_TXCLK	CH19_TXCTL	GND
18	GND	GND	GND	GND	GND	GND
17	GND	CH18_RD2	CH18_RD3	CH18_TD2	CH18_TD3	GND
16	GND	CH18_RD0	CH18_RD1	CH18_TD0	CH18_TD1	GND
15	GND	CH18_RXCLK	CH18_RXCTL	CH18_TXCLK	CH18_TXCTL	GND
KEY						GND
11	GND	GND	GND	GND	GND	GND
10	GND	CH17_RD2	CH17_RD3	CH17_TD2	CH17_TD3	GND
9	GND	CH17_RD0	CH17_RD1	CH17_TD0	CH17_TD1	GND
8	GND	CH17_RXCLK	CH17_RXCTL	CH17_TXCLK	CH17_TXCTL	GND
7	GND	GND	GND	GND	GND	GND
6	GND	CH16_RD2	CH16_RD3	CH16_TD2	CH16_TD3	GND
5	GND	CH16_RD0	CH16_RD1	CH16_TD0	CH16_TD1	GND
4	GND	CH16_RXCLK	CH16_RXCTL	CH16_TXCLK	CH16_TXCTL	GND
3	GND	GND	GND	GND	GND	GND
2	+2.5V	MDIO	MDC	MINT0#	MINT1#	GND
1	+2.5V	+3.3V	+3.3V	+3.3V	+12V	GND

Table 3-8: J1 RTM Connector

3.3.3 DDR SODIMM connector

PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL
1	VREF	2	VREF	101	A9	102	A8
3	VSS	4	VSS	103	VSS	104	VSS
5	DQ0	6	DQ4	105	A7	106	A6
7	DQ1	8	DQ5	107	A5	108	A4
9	VDD	10	VDD	109	A3	110	A2
11	DQS0	12	DM0	111	A1	112	A0
13	DQ2	14	DQ6	113	VDD	114	VDD
15	VSS	16	VSS	115	A10/AP	116	BA1
17	DQ3	18	DQ7	117	BA0	118	RAS
19	DQ8	20	DQ12	119	WE	120	CAS
21	VDD	22	VDD	121	S0	122	S1
23	DQ9	24	DQ13	123	NC(A13)	124	NC
25	DQS1	26	DM1	125	VSS	126	VSS
27	VSS	28	VSS	127	DQ32	128	DQ36
29	DQ10	30	DQ14	129	DQ33	130	DQ37
31	DQ11	32	DQ15	131	VDD	132	VDD
33	VDD	34	VDD	133	DQS4	134	DM4
35	CK0	36	VDD	135	DQ34	136	DQ38
37	CK0	38	VSS	137	VSS	138	VSS
39	VSS	40	VSS	139	DQ35	140	DQ39
41	DQ16	42	DQ20	141	DQ40	142	DQ44
43	DQ17	44	DQ21	143	VDD	144	VDD
45	VDD	46	VDD	145	DQ41	146	DQ45
47	DQS2	48	DM2	147	DQS5	148	DM5
49	DQ18	50	DQ22	149	VSS	150	VSS
51	VSS	52	VSS	151	DQ42	152	DQ46
53	DQ19	54	DQ23	153	DQ43	154	DQ47
55	DQ24	56	DQ28	155	VDD	156	VDD
57	VDD	58	VDD	157	VDD	158	CK1
59	DQ25	60	DQ29	159	VSS	160	CK1

Table 3-9: DDR SODIMM connector

PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL
61	DQS3	62	DM	161	VSS	162	VSS
63	VSS	64	VSS	163	DQ48	164	DQ52
65	DQ26	66	DQ30	165	DQ49	166	DQ53
67	DQ27	68	DQ31	167	VDD	168	VDD
69	VDD	70	VDD	169	DQS6	170	DM6
71	CB0	72	CB4	171	DQ50	172	DQ54
73	CB1	74	CB5	173	VSS	174	VSS
75	VSS	76	VSS	175	DQ51	176	DQ55
77	DQS8	78	DM8	177	DQ56	178	DQ60
79	CB2	80	CB6	179	VDD	180	VDD
81	VDD	82	VDD	181	DQ57	182	DQ61
83	CB3	84	CB7	183	DQS7	184	DM7
85	NC	86	(RESET)	185	VSS	186	VSS
87	VSS	88	VSS	187	DQ58	188	DQ62
89	CK2	90	VSS	189	DQ59	190	DQ63
91	CK2	92	VDD	191	VDD	192	VDD
93	VDD	94	VDD	193	SDA	194	SA0
95	CKE1	96	CKE0	195	SCL	196	SA1
97	NC	98	NC	197	VDDSPD	198	SA2
99	A12	100	A11	199	VDDID	200	NC
3	VSS	4	VSS	103	VSS	104	VSS
5	DQ0	6	DQ4	105	A7	106	A6
7	DQ1	8	DQ5	107	A5	108	A4
9	VDD	10	VDD	109	A3	110	A2
11	DQS0	12	DM0	111	A1	112	A0
13	DQ2	14	DQ6	113	VDD	114	VDD
15	VSS	16	VSS	115	A10/AP	116	BA1
17	DQ3	18	DQ7	117	BA0	118	RAS
19	DQ8	20	DQ12	119	WE	120	CAS
21	VDD	22	VDD	121	S0	122	S1
23	DQ9	24	DQ13	123	NC(A13)	124	NC
25	DQS1	26	DM1	125	VSS	126	VSS

Table 3-9: DDR SODIMM connector

PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL
27	VSS	28	VSS	127	DQ32	128	DQ36
29	DQ10	30	DQ14	129	DQ33	130	DQ37
31	DQ11	32	DQ15	131	VDD	132	VDD
33	VDD	34	VDD	133	DQS4	134	DM4
35	CK0	36	VDD	135	DQ34	136	DQ38
37	CK0	38	VSS	137	VSS	138	VSS
39	VSS	40	VSS	139	DQ35	140	DQ39
41	DQ16	42	DQ20	141	DQ40	142	DQ44
43	DQ17	44	DQ21	143	VDD	144	VDD
45	VDD	46	VDD	145	DQ41	146	DQ45
47	DQS2	48	DM2	147	DQS5	148	DM5
49	DQ18	50	DQ22	149	VSS	150	VSS
51	VSS	52	VSS	151	DQ42	152	DQ46
53	DQ19	54	DQ23	153	DQ43	154	DQ47
55	DQ24	56	DQ28	155	VDD	156	VDD
57	VDD	58	VDD	157	VDD	158	CK1
59	DQ25	60	DQ29	159	VSS	160	CK1
61	DQS3	62	DM3	161	VSS	162	VSS
63	VSS	64	VSS	163	DQ48	164	DQ52
65	DQ26	66	DQ30	165	DQ49	166	DQ53
67	DQ27	68	DQ31	167	VDD	168	VDD
69	VDD	70	VDD	169	DQS6	170	DM6
71	CB0	72	CB4	171	DQ50	172	DQ54
73	CB1	74	CB5	173	VSS	174	VSS
75	VSS	76	VSS	175	DQ51	176	DQ55
77	DQS8	78	DM8	177	DQ56	178	DQ60
79	CB2	80	CB6	179	VDD	180	VDD
81	VDD	82	VDD	181	DQ57	182	DQ61
83	CB3	84	CB7	183	DQS7	184	DM7
85	NC	86	(RESET)	185	VSS	186	VSS
87	VSS	88	VSS	187	DQ58	188	DQ62
89	CK2	90	VSS	189	DQ59	190	DQ63

Table 3-9: DDR SODIMM connector

PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL
91	CK2	92	VDD	191	VDD	192	VDD
93	VDD	94	VDD	193	SDA	194	SA0
95	CKE1	96	CKE0	195	SCL	196	SA1
97	NC	98	NC	197	VDDSPD	198	SA2
99	A12	100	A11	199	VDDID	200	NC

Table 3-9: DDR SODIMM connector

3.3.4 80219 JTAG debug connector

PIN	SIGNAL	PIN	SIGNAL
1	+3.3V	2	+3.3V
3	TRST#	4	GND
5	TDI	6	GND
7	TMS	8	GND
9	TCK	10	GND
11	GND	12	GND
13	TDO	14	GND
15	RESET	16	GND
17	N/C	18	GND
19	N/C	20	GND

Table 3-10: 80219 JTAG debug connector

3.3.5 RJ-11 serial port connector

PIN	SIGNAL
1	Chassis ground
2	RS232 TX
3	RS232 RX
4	Ground
5	Ground
6	Ground

Table 3-11: RJ-11 serial port connector

3.3.6 RJ-45 gigabit Ethernet ports

The following pinout applies to all egress gigabit Ethernet RJ-45 connectors.

PIN	SIGNAL
1	Data A+
2	Data A -
3	Data B +
4	Data B -
5	Data C +
6	Data C -
7	Data D +
8	Data D -

Table 3-12: RJ-45 Gigabit Ethernet ports

3.4 Electrical specifications

3.4.1 Absolute maximum ratings

CHRACTERISTICS	MIN	MAX	UNITS
Input Voltage	0	-75	Volts
Power Dissipation	-	86	Watts
Input Current	-	2.39	Amps
Operating Temperature	0	100	°C
Storage Temperature	-40	100	°C

Table 3-13: Absolute maximum ratings

3.4.2 Input characteristics

CHRACTERISTICS	MIN	TYP	MAX	UNITS
Operating Input Voltage	-36	-48	-74	Volts
Input Current	-	.5[a]	1.8	Amps
Power Dissipation	-	25[b]	86	Watts

Table 3-14: Input characteristics

a.Measured values at -48V

b.Measured values at -48V

Warranty Policy

Thank you for choosing ADLINK. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ADLINK's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: http://rma.adlinktech.com/policy/.
2. All ADLINK products come with a limited two-year warranty, one year for products bought in China:
   - The warranty period starts on the day the product is shipped from ADLINK's factory.
   - Peripherals and third-party products not manufactured by ADLINK will be covered by the original manufacturers' warranty.
   - For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ADLINK is not responsible for any loss of data.
   - Please ensure the use of properly licensed software with our systems. ADLINK does not condone the use of pirated software and will not service systems using such software. ADLINK will not be held legally responsible for products shipped with unlicensed software installed by the user.
   - For general repairs, please do not include peripheral accessories. If peripherals need to be included, be certain to specify which items you sent on the RMA Request & Confirmation Form. ADLINK is not responsible for items not listed on the RMA Request & Confirmation Form.

3. Our repair service is not covered by ADLINK's guarantee in the following situations:
   - Damage caused by not following instructions in the User's Manual.
   - Damage caused by carelessness on the user's part during product transportation.
   - Damage caused by fire, earthquakes, floods, lightening, pollution, other acts of God, and/or incorrect usage of voltage transformers.
   - Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).
   - Damage caused by leakage of battery fluid during or after change of batteries by customer/user.
   - Damage from improper repair by unauthorized ADLINK technicians.
   - Products with altered and/or damaged serial numbers are not entitled to our service.
   - This warranty is not transferable or extendible.
   - Other categories not protected under our warranty.
4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.
5. To ensure the speed and quality of product repair, please download an RMA application form from our company website: http://rma.adlinktech.com/policy. Damaged products with attached RMA forms receive priority.

If you have any further questions, please email our FAE staff: service@adlinktech.com.