aTCA-6890

Intel® Xeon-based

AdvancedTCA Processor Blade

User's Manual

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1 Introduction

1.1 Product Overview

The aTCA-6890 is the dual 64bit Intel® LV-Xeon processor based AdvancedTCA blade. It supports Intel® EM64T 64-bit technology and dual channel DDR2-400 REG/ECC system memory up to 16GB capacity. For data transport connectivity, it features dual 1000BASE-T GbE Base Interface channels and field-configurable quad 1000BASE-BX GbE Fabric Interface ports compliant with PICMG 3.1 Option1 or 2.

The front panel I/O includes dual 64-bit 66/100/133MHz PCI/PCI-X PMC sites, USB 2.0 ports, 1000BASE-T GbE ports, one analog video and a serialconsole. On-board peripherals includes two ATA100 channels withon-board DMA-enabled CF slot and one SATA 2.5" HDD site.

Compatible Rear Transition Module (RTM) features RAID0/1 SATA 2.5" HDD and PMC I/O module (PIM, VITA36). The Serial-Attached-SCSI (SAS) and Encryption expansion modules are also available.

Please refer to the following block diagram for the aTCA-6890 architecture.

Block Diagram

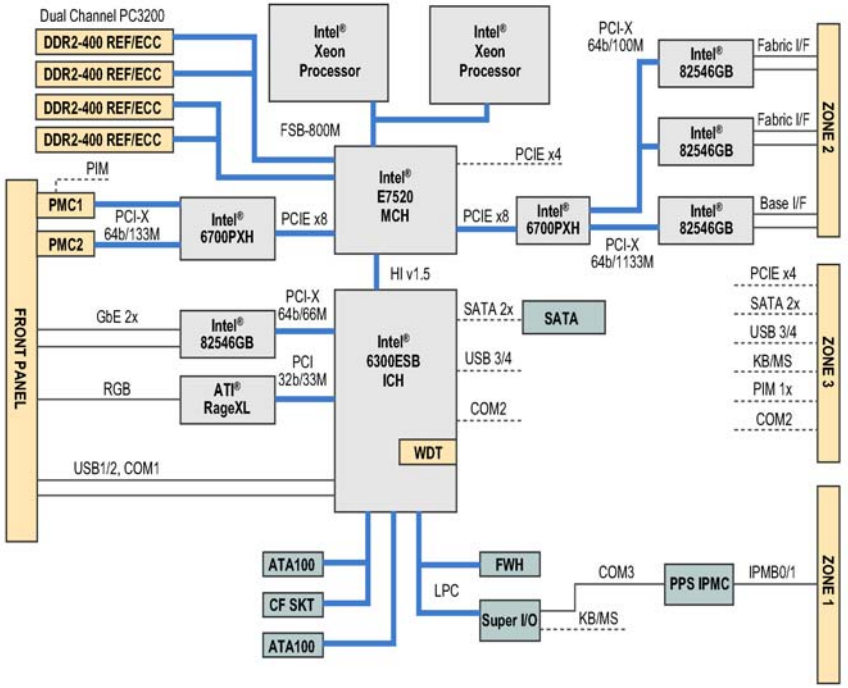


Figure 1-1: aTCA 6890 Functional Block Diagram

1.2 Features

The features of the aTCA-6890 are as follows:

- 800MHz FSB
- 1MB L2 Cache
- Hyper-Threading Processors
- Intel® EM64T 64-bit Extended Memory Technology
- Dual DDR2-400 REG/ECC Channels with 16GB Maximum Capacity
- Intel® E7520/6300ESB/6700PXH Chipset
- Dual 64-bit 33/66/100/133MHz PCI/PCI-X PMC with PIM
- Quad 1000BASE-BX GbE Fabric Interface Channels
- Configurable PICMG 3.1 Option1/2 Compliant
- RAID 0/1 Enabled RTM
- CPU: Dual 64bit Intel LV-Xeon 800FSB 2.8GHz
- Chipset: Intel E7520 MCH, 6300ESB ICH, 6700PXH Bridge
- Memory: Four DDR2-400 REG/ECC 240pin DIMM slots, up to 16GB capacity
- Flash: Award BIOS with 4Mb flash memory supporting Intel PXE pre-boot and serial console redirection
- Graphics: ATI® RageXL with 8MB VRAM, up to QXGA (2048 x 1536) resolution
- PMC
  - PMC1: PCI/PCI-X 64-bit 66/100/133MHz capable with PIM
  - PMC2: PCI/PCI-X 64-bit 66/100/133MHz capable
- LAN: Intel® 82546EB (GB) PCI-X dual port Gigabit Ethernet controllers
  - Dual 10/100/1000BASE-T Base interface channels
  - Quad 1000BASE-BX fabric interface channels
  - Dual 10/100/1000BASE-T front panel access
- Storage: Dual ATA-33/66/100 channels
  - On-board DMA-enabled CompactFlash socket
  - On-board 2.5" ATA/SATA HDD kits

- USB: Dual USB v2.0 ports
- Front Panel I/Os: PMC1/2, VGA, USB1/2, LAN1/2, COM1
- Standards
  - PICMG 3.0 R2.0 ECN001
  - PICMG 3.1 Ethernet over PICMG 3.0, R1.0 Option 1/2

1.3 Main Functions

This section details the major functional blocks in the aTCA-6890. The user interconnects and options are detailed.

Processor

The aTCA-6890 processor blade is designed for single Xeon™ or single/dual Low Voltage Xeon™ “Nocona” processors. Processors compatible with the aTCA-6890 are 90nm, 800MHz System Bus, 1MB of L2 cache and are in a 604 pin FCmPGA4 package. The processor used must be compatible with the E7520 MCH. Use of other Xeon processors might cause damage to the aTCA-6890 or processor. When using dual processors both processors must be the same S-Spec number. The aTCA-6890 is designed to be used with ADLINK’s thermal solution. Do not attempt to use the thermal solution provided in some of the boxed processor packages. The aTCA-6890 has been validated with the following long life processors:

Type	Speed	System Bus	Power	Max Temp	L2 Cache	Intel Part Number
Xeon	3.2GHz	800MHz	103W	80°C	1MB	RK80546KG0881M
LV Xeon	2.8GHz	800MHz	55W	86°C	1MB	RK80546KG0721M

Table 1-1: CPUs Validated for the ATCA-6890

Memory Interface

The Intel® E7520 MCH chipset supports two channels of registered DDR-II 400 (stacked or unstacked) memory. Peak theoretical memory bandwidth is 6.4GB/s. The maximum memory configuration supported is 16GB. The memory controller supports: memory mirroring which keeps a duplicate copy of data in the memory subsystem; memory hot-swap that allows removal of a defective DIMM without bringing down the system (not of use in aTCA); DIMM sparing which allows for one DIMM per channel to be held in reserve and brought on line if another DIMM becomes defective (DIMM sparing and mirroring are mutually exclusive); hardware memory scrubbing; retry on uncorrectable memory errors; 4x SDDC for memory error detection and correction of any number of bit failures in a single x4 memory device.

The memory controller supports two channels of memory, Channel A and Channel B. Each channel contains two SIMM sockets for a total of 4 DIMM sockets. The aTCA-6890 can be populated with one, two or four DIMM modules. When only one DIMM is used, it can be populated on either DDRII-A2 or DDRII-B2 socket. In case of two DIMMs, they can be populated on either DDRII-A2 and DDRII-B2 (dual channel mode), DDRII-A1 and DDRII-A2 or DDRII-B1 and DDRII-B2 (single channel mode). To achieve maximum memory throughput, ensure that sockets A1 and B1 and/or A2 and B2 have identically configured DIMM modules.

The table below outlines the aTCA-6890's memory interface SMB address functionality:

SMB Address	Function
A4h	DDRII Channel A DIMM 1
A6h	DDRII Channel A DIMM 2
ACh	DDRII Channel B DIMM 1
AEh	DDRII Channel B DIMM 2

Table 1-2: SMB Address Functionality

PCI Express

The E7520 MCH provides three x8 PCI Express interfaces. Each PCI-E interface can be configured as one x8 or two x4 links. Currently, two of the x8 ports are connected to two 6700PXH bridges, and the 3rd interface is configured as one x4 link to Zone 3 for future use.

PCI Express Port	Lower x4 Interface	Upper x4 Interface
A	PXH	
B	NC	RTM
C	PXH	

Table 1-3: PCI Express Configuration

Fabric Interface

The aTCA-6890 (configured by SWY2-Pin4) provides 4 gigabit Ethernet interfaces to the Fabric Interface using 2 82546 dual

gigabit Ethernet controllers. The Fabric Interface can be configured to run in two modes, PICMG 3.1, Option1 and Option2, configured by on-board DIP-switch SWY2-Pin4. In PICMG 3.1 Option1 mode, each GbE port is linked to Port0 of Fabric Interface Channel 1-4 (FCH[1:4]P0). The other mode complies with PICMG 3.1, Option 2, which configures the four GbE ports to Port0-1 of Fabric Interface Channel 1-2 (FCH[1:2]P[0:1]). As shipped, the aTCA-6890 is configured to operate in the PICMG 3.1 Option 1 mode. Refer to the table below for details.

		PICMG 3.1 Option	
Ethernet Controller	**Interface**	**Fabric Channel and Port (3.1 Option 1)**	**Fabric Channel and Port (3.1 Option 2)**
1	A	FCH1P0	FCH1P0
	B	FCH2P0	FCH2P0
2	A	FCH3P0	FCH1P1
	B	FCH4P0	FCH2P1

Table 1-4: Fabric Interface Options

Base Interface

The aTCA-6890 supports two Gigabit Ethernet connections to the Base Interface using a single 82546 dual channel Gigabit Ethernet controller.

PMC

The aTCA-6890 contains 2 PMC sites. Both PMC sites are keyed for 3.3V V(I/O). Each PMC site sits on an independent PCI-X bus. Each PMC can run at 64 bit up to 133MHz PCI-X. The PMC sites are on independent busses so the use of a slow speed PMC on one site will not impact performance of the other PMC. The upper PMC supports rear I/O out the Zone 3 connector. Contact ADLINK for information on Rear Transition Modules compatible with the aTCA-6890.

Video

The video interface is provided with a ATI Rage XL video controller. The video controller is on a 32 bit 33MHz PCI bus. Video memory of 8M bytes is available with resolutions up to QXGA (2048 x 1536). CRT signals are routed to the front panel only.

10/100/1000Mbit Ethernet Maintenance Port

Two 10/100/1000Mbit Ethernet ports are provided on the front panel.

Serial ATA Interface

Two SATA 150MB/s interfaces are provided. The SATA controllers are completely software transparent with the IDE (ATA) interface while providing lower pin count, higher performance and software RAID 0/1 features are available in BIOS options to be enabled on the two SATA ports. The two SATA host controllers are capable of independent DMA operation. The 2.5" SATA HDD mounting kit for two 2.5" drives is available on RTM.

For users only need one SATA HDD on PMC1 site, please contact with ADLINK FAE for installation instructions.

USB 2.0 Interfaces

Four USB 2.0 interfaces are provided by the ICH. Two of the USB 2.0 interfaces are routed to the front panel and the remaining two interfaces are routed to the Zone 3 connector.

Serial Ports

One of the ICH serial port is designed to front panel in RJ-45 jack, and the other from ICH is routed to RTM I/O. The COM3 provided by SuperI/O is dedicated to IPMC payload port as the host interface. The ports are 16550 compatible and will support 16550 compatible operation up to 115 kilobaud. The serial ports are relocatable in ISA I/O memory Map. The serial ports are ESD protected to 15KV.

Super I/O

The super I/O provides legacy controllers. It should be noted that the front board does not support PS/2 keyboard or mouse devices or parallel printer devices. These functions are intended to be provided using USB. Previous experiences have shown that some BIOS and operating software require that a keyboard controller register be present for proper operation. The SIO selected contains a keyboard controller but the keyboard port is not connected. The controller is provided for software compatibility reasons only. The PS/2 keyboard and mouse interfaces are routed to Zone 3 for use with the aTCA-6890 RTM.

IPMI Controller

The IPMI controller is based on the Pigeon Point Systems IPMC. It is fully compliant with the aTCA specification. Please refer to the appendix A for more information about IPMC.

EIDE Interface

Two optional 2.5” on-card ATA hard drive sites are available. The drives connect to ATA ports provided by the Intel® 6300ESB ICH. Each hard drive will take the space of one PMC site. We recommend using the upper PMC site for an optional on-board hard disk drive.

CMOS Battery

The real time clock and CMOS backup battery are socketed. The battery circuite has a series resistor and diode to conform to industry safety requirements. The battery has an expected shelf life of at least five years.

1.4 aTCA-6890 Mechanical Layout

aTCA-6890 Board Layout

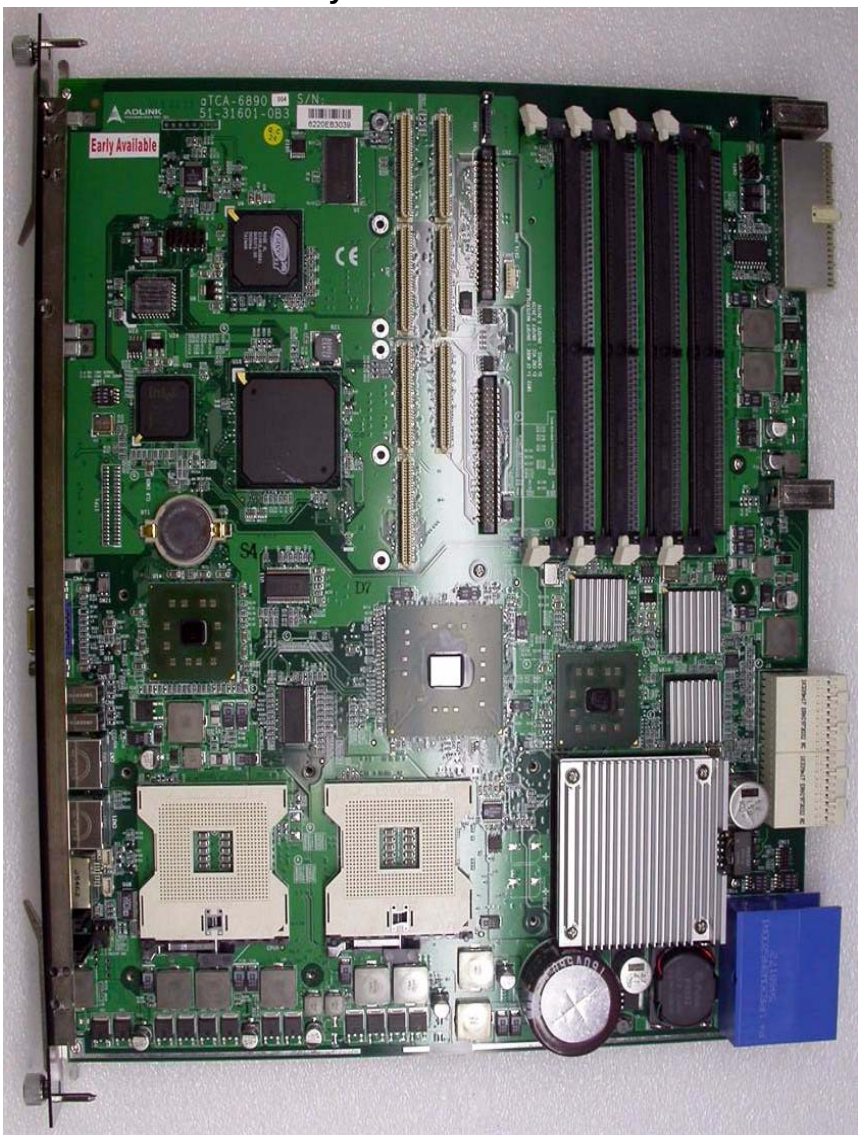


Figure 1-2: aTCA-6890 Board Layout

Front Panel LED Indicators and Reset

Front panel LEDs provide feedback to the user on the state of the aTCA-6890. A front panel reset switch is provided to allow a hard reset of the board.

LED	Color	Function
OOS	Red	Out Of Service: Indicates that the aTCA-6890 is not functional
HD	Green	Hard Disk: Indicates hard drive activity
USR	Amber	Indicates power on
HS	Blue	Hot Swap: Indicates that the board can be removed

Table 1-5: LED Indicator Legend

BCH1	1. Link/Activity LED, amber 2. Speed LED, 1Gbps-amber; 10/100Mbps-green
BCH2	Same as BCH1
Fabric I/F CH1	Fabric Interface Channel 1 Link/Activity LED
Fabric I/F CH2	Same as FCH1
Fabric I/F CH3	Same as FCH1
Fabric I/F CH4	Same as FCH1

Table 1-6: Base & Fabric Interface LEDs

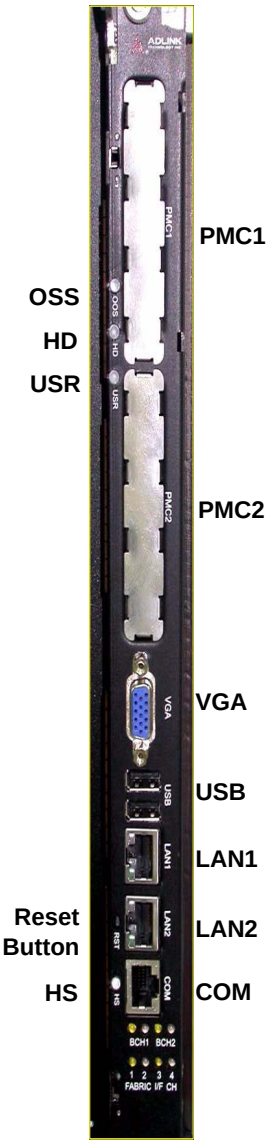


Figure 1-3: Front Panel

1.5 Unpacking Checklist

Check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the dealer for a replacement. Retain the shipping carton and packing materials for inspection by the dealer. Obtain authorization before returning any product to ADLINK.

Check the following items are included in the package, if there are any items missing, please contact your dealer:

Included Items
aTCA-6890 processor blade (CPU, RAM, and hard drive specifications will differ depending on options selected)
Heat sink
IDE HDD mounting kit
SATA HDD mounting kit
COM port RJ45-to-DB9 adapter
ADLINK All-in-One CD
This user's manual

Note: The packaging of the aTCA-6890 OEM version with non-standard configuration, functionality, or package may vary according to different configuration requests.

CAUTION: The aTCA-6890 processor blade must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the board. Wear a grounded wrist strap when servicing.

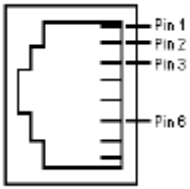
2 Connectors and Jumpers

This chapter will familiarize the user with the connectors and jumpers on the aTCA-6890.

2.1 Connector Pin Assignments

Detailed descriptions and pin-outs for each connector are given in the following section. Please refer to **Figure 1-2: aTCA-6890 Board Board Layout** and **Figure 1-3: aTCA-6890 Front Panel** for connector locations.

Serial Port (COM1))

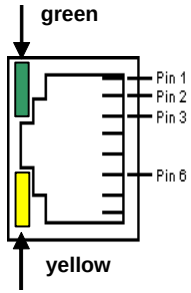


Pin	Signal	Function
1	DCD#	Data Carrier Detect
2	RTS#	Request to Send
3	DSR#	Data Set Ready
4	TXD	Transmit Data
5	RXD	Receive Data
6	GND	Ground
7	CTS#	Clear to Send
8	DTR#	Data Terminal Ready

Com Port Signal Definitions:

CTS Indicates that data set is ready to exchange data.
DCD Indicates data set has detected the data carrier.
DSR Indicates that data set is ready to establish a communications link.
DTR Indicates that a data set is ready to establish a communications link.
RI Indicates that a modem has received a telephone-ringing signal.
RTS Indicates to data set that UART is ready to exchange data.
RX Receives serial data input from communications link.
TX Sends serial output to communications link.

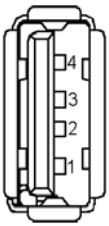
LAN RJ-45 Connector (LAN1, LAN2)



Pin	Signal	Function
1	MDX0+	Pair 0
2	MDX0-	
3	MDX1+	Pair 1
4	MDX1-	
5	MDX2+	Pair 2
6	MDX2-	
7	MDX3+	Pair 3
8	MDX3-	

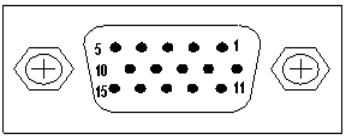
LED Color	Status	Function
Green (speed)	ON	1000Mbps
	OFF	100Mbps
Yellow (link)	ON	Link
	OFF	Link off
	blinking	Data transfer in progress

USB Connector (Port 0, Port 1)



PIN	SIGNAL
1	VCC
2	USB-
3	USB+
4	Ground

VGA Connector (Front Panel)



Pin	Signal Name	Pin	Signal Name
1	Red	9	+5V
2	Green	10	GND
3	Blue	11	NC
4	NC	12	DDCDAT
5	GND	13	HSYNC
6	GND	14	VSYNC
7	GND	15	DDCLK
8	GND	—	—

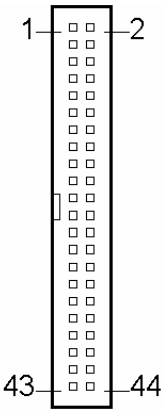
Video Signal Definitions:

RED	Red signal
GRN	Green signal
BLU	Blue signal
HSYNC	Horizontal synchronization
VSYNC	Vertical synchronization
DDCCLK	Display Data Channel clock signal for DDC2 support
DDCDAT	Display Data Channel data signal for DDC2 support

SATA 0 (CN1)

Pin	Signal
1	GND
2	Tx+
3	Tx-
4	GND
5	Rx-
6	Rx+
7	GND

IDE Connectors (CN2, CN3)



Signal	Pin	Pin	Signal
RESET#	1	2	Ground
DD7	3	4	DD8
DD6	5	6	DD9
DD5	7	8	DD10
DD4	9	10	DD11
DD3	11	12	DD12
DD2	13	14	DD13
DD1	15	16	DD14
DD0	17	18	DD15
Ground	19	20	N.C (key pin)
DMARQ	21	22	Ground
DIOW#	23	24	Ground
DIOR#	25	26	Ground
IORDY	27	28	CSEL
DMACK#	29	30	Ground
INTRQ	31	32	N/C
DA1	33	34	PDIAG#
DA0	35	36	DA2
CS0#	37	38	CS1#
DASP#	39	40	Ground
5V	41	42	5V
Ground	43	44	TYPE-

Zone 1 Connector

The ATCA-6890 uses the standard PICMG 3.0 Zone 1 connector for power and system management.

Pin	Designation	Description	Pin	Designation	Description
1	Reserved	Reserved	18	MT2_TIP	Metallic Test #2 Tip
2	Reserved	Reserved	19	-RING_A	Ring generator A Neg
3	Reserved	Reserved	20	-RING_B	Ring generator B Neg
4	Reserved	Reserved	21	MT1_RING	Metallic Test #1 Ring
5	HA0	Hardware Address Bit 0	22	MT2_RING	Metallic Test #2 Ring
6	HA1	Hardware Address Bit 1	23	RRTN_A	Ring generator A Rtn
7	HA2	Hardware Address Bit 2	24	RRTN_B	Ring generator B Rtn
8	HA3	Hardware Address Bit 3	25	SHELF_GND	Shelf Ground
9	HA4	Hardware Address Bit 4	26	LOGIC_GND	Logic Ground
10	HA5	Hardware Address Bit 5	27	ENABLE_B	Enable B
11	HA6	Hardware Address Bit 6	28	VRTN_A	Voltage Return A
12	HA7/P	Hardware Address Bit 7 (Odd Parity Bit)	29	VRTN_B	Voltage Return B
13	SCL_A	IPMB clock Port A	30	EARLY_A	-48 Volt Early A
14	SDA_A	IPMB Data Port A	31	EARLY_B	-48 Volt Early B
15	SCL_B	IPMB clock Port B	32	ENABLE_A	Enable A
16	SDA_B	IPMB Data Port B	33	-48V_A	-48 Volt A
17	MT1_TIP	Metallic Test #1 Tip	34	-48V_B	-48 Volt B

Note: Shaded pins are not connected on the ATCA-6890

Zone 2-J23 Pin Assignment (PICMG 3.1 Option1)

Signal	Row	AB		CD		EF		GH	
FCH2	1	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
	2	F2_T0+	F2_T0-	F2_R0+	F2_R0-	NC	TERM*	NC	TERM*
FCH1	3	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
	4	F1_T0+	F1_T0-	F1_R0+	F1_R0-	NC	TERM*	NC	TERM*
BCH1	5	BI_A0+	BI_A0-	BI_A1+	BI_A1-	BI_A2+	BI_A2-	BI_A3+	BI_A3-
BCH 2	6	BI_B0+	BI_B0-	BI_B1+	BI_B1-	BI_B2+	BI_B2-	BI_B3+	BI_B3-
NC	7	NC	NC	NC	NC	NC	NC	NC	NC
	8	NC	NC	NC	NC	NC	NC	NC	NC
	9	NC	NC	NC	NC	NC	NC	NC	NC
	10	NC	NC	NC	NC	NC	NC	NC	NC

TERM* means connect to the termination circuit on board.

Zone 2-J22 Pin Assignment (PICMG 3.1 Option1)

Signal	Row	AB		CD		EF		GH	
NC	1	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
	2	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
NC	3	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
	4	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
NC	5	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
	6	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
FCH4	7	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
	8	F4_T0+	F4_T0-	F4_R0+	F4_R0-	NC	TERM*	NC	TERM*
FCH3	9	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
	10	F3_T0+	F3_T0-	F3_R0+	F3_R0-	NC	TERM*	NC	TERM*

TERM* means connect to the termination circuit on board.

Zone 2-J23 Pin Assignment (PICMG 3.1 Option2)

Signal	Row	AB		CD		EF		GH	
FCH2	1	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
	2	F2_T0+	F2_T0-	F2_R0+	F2_R0-	F2_T1+	F2_T1-	F2_R1+	F2_R1-
FCH1	3	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
	4	F1_T0+	F1_T0-	F1_R0+	F1_R0-	F1_T1+	F1_T1-	F2_R1+	F2_R1-
BCH1	5	BI_A0+	BI_A0-	BI_A1+	BI_A1-	BI_A2+	BI_A2-	BI_A3+	BI_A3-
BCH2	6	BI_B0+	BI_B0-	BI_B1+	BI_B1-	BI_B2+	BI_B2-	BI_B3+	BI_B3-
NC	7	NC	NC	NC	NC	NC	NC	NC	NC
	8	NC	NC	NC	NC	NC	NC	NC	NC
	9	NC	NC	NC	NC	NC	NC	NC	NC
	10	NC	NC	NC	NC	NC	NC	NC	NC

TERM* means connect to the termination circuit on board.

Zone 2-J22 Pin Assignment (PICMG 3.1 Option2)

Signal	Row	AB		CD		EF		GH	
NC	1	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
	2	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
NC	3	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
	4	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
NC	5	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
	6	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
NC	7	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
	8	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
NC	9	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*
	10	NC	TERM*	NC	TERM*	NC	TERM*	NC	TERM*

TERM* means connect to the termination circuit on board.

Zone 3 Pin Assignment

Pin	A	B	C	D	E
25	PMC1/IO5	PMC1/IO4	PMC1/IO3	PMC1/IO2	PMC1/IO1
24	PMC1/IO10	PMC1/IO9	PMC1/IO8	PMC1/IO7	PMC1/IO6
23	PMC1/IO15	PMC1/IO14	PMC1/IO13	PMC1/IO12	PMC1/IO11
22	PMC1/IO20	PMC1/IO19	PMC1/IO18	PMC1/IO17	PMC1/IO16
21	PMC1/IO25	PMC1/IO24	PMC1/IO23	PMC1/IO22	PMC1/IO21
20	PMC1/IO30	PMC1/IO29	PMC1/IO28	PMC1/IO27	PMC1/IO26
19	PMC1/IO35	PMC1/IO34	PMC1/IO33	PMC1/IO32	PMC1/IO31
18	PMC1/IO40	PMC1/IO39	PMC1/IO38	PMC1/IO37	PMC1/IO36
17	PMC1/IO45	PMC1/IO44	PMC1/IO43	PMC1/IO42	PMC1/IO41
16	PMC1/IO50	PMC1/IO49	PMC1/IO48	PMC1/IO47	PMC1/IO46
15	PMC1/IO55	PMC1/IO54	PMC1/IO53	PMC1/IO52	PMC1/IO51
12-14	—				
11	PMC1/IO60	PMC1/IO59	PMC1/IO58	PMC1/IO57	PMC1/IO56
10	SM_CLK	PMC1/IO64	PMC1/IO63	PMC1/IO62	PMC1/IO61
9	SM_DAT	KBDAT	KBCLK	MSDAT	MSCLK
8	SATA0TXP	SATA0TXN	RST#	SATA0RXP	SATA0RXN
7	SATA1TXP	SATA1TXN	+12V	SATA1RXP	SATA1RXN
6	USB_P2P	USB_P2N	USBOC#2	USB_P3P	USB_P3N
5	CLK100_RPE	CLK100#_RPE	RTM_IN#	UART2_TXD	UART2_RXD
4	PE_B_RP6	PE_B_RN6	+5V	PE_B_RP7	PE_B_RN7
3	PE_B_RP4	PE_B_RN4	+5V	PE_B_RP5	PE_B_RN5
2	PE_B_TP6	PE_B_TN6	+5V	PE_B_TP7	PE_B_TN7
1	PE_B_TP4	PE_B_TN4	+5V	PE_B_TP5	PE_B_TN5

PMC Connectors

PMC1: P4 connector implemented

JN1				JN2			
Pin	**Signal**	**Signal**	**Pin**	**Pin**	**Signal**	**Signal**	**Pin**
1	TCK	-12V	2	1	+12V	TRST-	2
3	Ground	INTA-	4	3	TMS	TDO	4
5	INTB-	INTC-	6	5	TDI	Ground	6
7	BUSMODE1-	+5V	8	7	Ground	PCI-RSVD*	8
9	INTD-	PCI-RSVD*	10	9	PCI-RSVD*	PCI-RSVD*	10
11	Ground	PCI-RSVD*	12	11	BUSMODE2-	+3.3V	12
13	CLK	Ground	14	13	RST-	BUSMODE3-	14
15	Ground	GNT-	16	15	+3.3V	BUSMODE4-	16
17	REQ-	+5V	18	17	PCI-RSVD*	Ground	18
19	V (I/O)	AD[31]	20	19	AD[30]	AD[29]	20
21	AD[28]	AD[27]	22	21	Ground	AD[26]	22
23	AD[25]	Ground	24	23	AD[24]	+3.3V	24
25	Ground	C/BE[3]-	26	25	IDSEL	AD[23]	26
27	AD[22]	AD[21]	28	27	+3.3V	AD[20]	28
29	AD[19]	+5V	30	29	AD[18]	Ground	30
31	V (I/O)	AD[17]	32	31	AD[16]	C/BE[2]-	32
33	FRAME-	Ground	34	33	Ground	PMC-RSVD	34
35	Ground	IRDY-	36	35	TRDY-	+3.3V	36
37	DEVSEL-	+5V	38	37	Ground	STOP-	38
39	PCIXCAP	LOCK-	40	39	PERR-	Ground	40
41	SDONE-	SBO-	42	41	+3.3V	SERR-	42
43	PAR	Ground	44	43	C/BE[1]-	Ground	44
45	V (I/O)	AD[15]	46	45	AD[14]	AD[13]	46
47	AD[12]	AD[11]	48	47	M66EN	AD[10]	48
49	AD[09]	+5V	50	49	AD[08]	+3.3V	50
51	Ground	C/BE[0]-	52	51	AD[07]	PMC-RSVD	52
53	AD[06]	AD[05]	54	53	+3.3V	PMC-RSVD	54
55	AD[04]	Ground	56	55	PMC-RSVD	Ground	56
57	V (I/O)	AD[03]	58	57	PMC-RSVD	PMC-RSVD	58
59	AD[02]	AD[01]	60	59	Ground	PMC-RSVD	60
61	AD[00]	+5V	62	61	ACK64-	+3.3V	62
63	Ground	REQ64-	64	63	Ground	PMC-RSVD	64

JN3				JN4			
Pin	Signal	Signal	Pin	Pin	Signal	Signal	Pin
1	RESERVED	GND	2	1	+12V	TRST-	2
3	GND	CBE7#	4	3	TMS	TDO	4
5	CEB6#	CBE5#	6	5	TDI	Ground	6
7	CEB4#	GND	8	7	Ground	PCI-RSVD*	8
9	VIO	PAR64	10	9	PCI-RSVD*	PCI-RSVD*	10
11	AD63	AD62	12	11	BUSMODE2-	+3.3V	12
13	AD61	GND	14	13	RST-	BUSMODE3-	14
15	GND	AD60	16	15	+3.3V	BUSMODE4-	16
17	AD59	AD58	18	17	PCI-RSVD*	Ground	18
19	AD57	GND	20	19	AD[30]	AD[29]	20
21	VIO	AD56	22	21	Ground	AD[26]	22
23	AD55	AD54	24	23	AD[24]	+3.3V	24
25	AD53	GND	26	25	IDSEL	AD[23]	26
27	GND	AD52	28	27	+3.3V	AD[20]	28
29	AD51	AD50	30	29	AD[18]	Ground	30
31	AD49	GND	32	31	AD[16]	C/BE[2]-	32
33	GND	AD48	34	33	Ground	PMC-RSVD	34
35	AD47	AD46	36	35	TRDY-	+3.3V	36
37	AD45	GND	38	37	Ground	STOP-	38
39	VIO	AD44	40	39	PERR-	Ground	40
41	AD43	AD42	42	41	+3.3V	SERR-	42
43	AD41	GND	44	43	C/BE[1]-	Ground	44
45	GND	AD40	46	45	AD[14]	AD[13]	46
47	AD39	AD38	48	47	Ground	AD[10]	48
49	AD37	GND	50	49	AD[08]	+3.3V	50
51	GND	AD36	52	51	AD[07]	PMC-RSVD	52
53	AD35	AD34	54	53	+3.3V	PMC-RSVD	54
55	AD33	GND	56	55	PMC-RSVD	Ground	56
57	VIO	AD32	58	57	PMC-RSVD	PMC-RSVD	58
59	RESERVED	RESERVED	60	59	Ground	PMC-RSVD	60
61	RESERVED	GND	62	61	ACK64-	+3.3V	62
63	GND	RESERVED	64	63	Ground	PMC-RSVD	64

PMC2: P4 connector NOT implemented

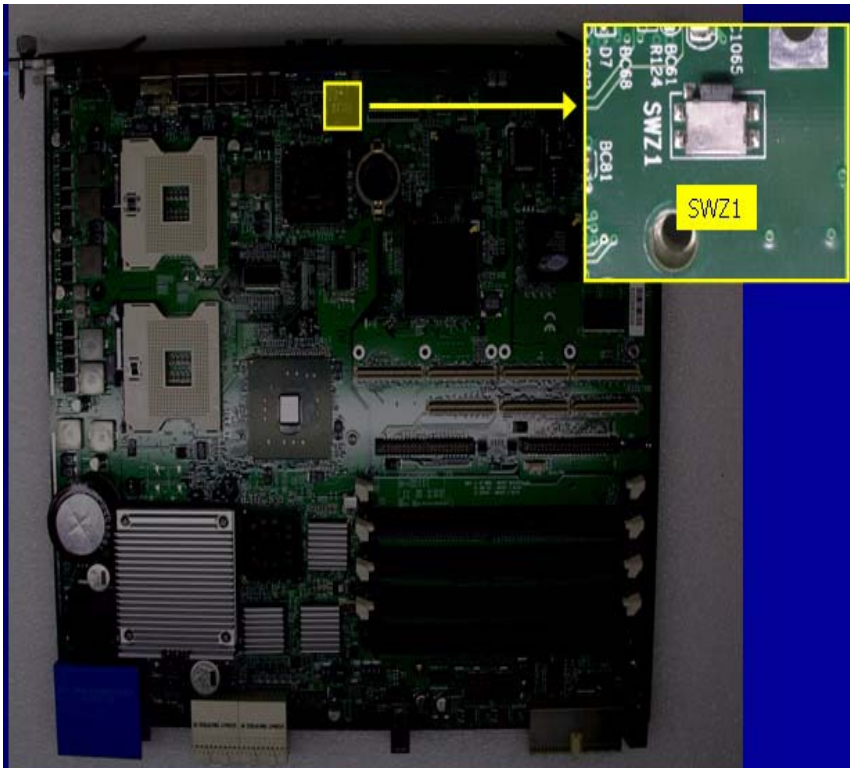
JN5				JN6			
Pin	**Signal**	**Signal**	**Pin**	**Pin**	**Signal**	**Signal**	**Pin**
1	TCK	-12V	2	1	+12V	TRST-	2
3	GND	PCIIRQ4#	4	3	TMS	TDO	4
5	PCIIRQ5#	PCIIRQ4#	6	5	TDI	Ground	6
7	BUSMODE1#	+5V	8	7	Ground	PCI-RSVD*	8
9	PCIIRQ5#	RESERVED	10	9	PCI-RSVD*	PCI-RSVD*	10
11	GND	+3.3V	12	11	BUSMODE2-	+3.3V	12
13	CLOCK	GND	14	13	RST-	BUSMODE3-	14
15	GND	GNT2#	16	15	+3.3V	BUSMODE4-	16
17	REQ2#	+5V	18	17	PCI-RSVD*	Ground	18
19	PMCVIO	AD[31]	20	19	AD[30]	AD[29]	20
21	AD[28]	AD[27]	22	21	Ground	AD[26]	22
23	AD[25]	GND	24	23	AD[24]	+3.3V	24
25	GND	C/BEJ[3]#	26	25	IDSEL	AD[23]	26
27	AD[22]	AD[21]	28	27	+3.3V	AD[20]	28
29	AD[19]	+5V	30	29	AD[18]	Ground	30
31	PMCVIO	AD[17]	32	31	AD[16]	C/BE[2]-	32
33	FRAME#	GND	34	33	Ground	PMC-RSVD	34
35	GND	IRDY#	36	35	TRDY-	+3.3V	36
37	DEVSEL#	+5V	38	37	Ground	STOP-	38
39	PCIXCAP	LCOK#	40	39	PERR-	Ground	40
41	RESERVED	RESERVED	42	41	+3.3V	SERR-	42
43	PAR	GND	44	43	C/BE[1]-	Ground	44
45	PMCVIO	AD[15]	46	45	AD[14]	AD[13]	46
47	AD[12]	AD[11]	48	47	M66EN	AD[10]	48
49	AD[9]	+5V	50	49	AD[08]	+3.3V	50
51	GND	C/BEJ[0]#	52	51	AD[07]	PMC-RSVD	52
53	AD[6]	AD[5]	54	53	+3.3V	PMC-RSVD	54
55	AD[4]	GND	56	55	PMC-RSVD	Ground	56
57	PMCVIO	AD[3]	58	57	PMC-RSVD	PMC-RSVD	58
59	AD[2]	AD[1]	60	59	Ground	PMC-RSVD	60
61	AD[0]	+5V	62	61	ACK64-	+3.3V	62
63	GND	REQ64 #	64	63	Ground	PMC-RSVD	64

JN7				JN8			
Pin	Signal	Signal	Pin	Pin	Signal	Signal	Pin
1	RESERVED	GND	2	1	—	—	2
3	GND	CBE7#	4	3	—	—	4
5	CEB6#	CBE5#	6	5	—	—	6
7	CEB4#	GND	8	7	—	—	8
9	VIO	PAR64	10	9	—	—	10
11	AD63	AD62	12	11	—	—	12
13	AD61	GND	14	13	—	—	14
15	GND	AD60	16	15	—	—	16
17	AD59	AD58	18	17	—	—	18
19	AD57	GND	20	19	—	—	20
21	VIO	AD56	22	21	—	—	22
23	AD55	AD54	24	23	—	—	24
25	AD53	GND	26	25	—	—	26
27	GND	AD52	28	27	—	—	28
29	AD51	AD50	30	29	—	—	30
31	AD49	GND	32	31	—	—	32
33	GND	AD48	34	33	—	—	34
35	AD47	AD46	36	35	—	—	36
37	AD45	GND	38	37	—	—	38
39	VIO	AD44	40	39	—	—	40
41	AD43	AD42	42	41	—	—	42
43	AD41	GND	44	43	—	—	44
45	GND	AD40	46	45	—	—	46
47	AD39	AD38	48	47	—	—	48
49	AD37	GND	50	49	—	—	50
51	GND	AD36	52	51	—	—	52
53	AD35	AD34	54	53	—	—	54
55	AD33	GND	56	55	—	—	56
57	VIO	AD32	58	57	—	—	58
59	RESERVED	RESERVED	60	59	—	—	60
61	RESERVED	GND	62	61	—	—	62
63	GND	RESERVED	64	63	—	—	64

2.2 Jumper Settings

Clear CMOS Jumper (SWZ1)

The ATCA-6890 has a clear CMOS jumper located near the CMOS battery to allow the user to clear CMOS values to default values if necessary (please refer to the following figure to clear CMOS values by pressing SWZ1.)



3 Getting Started

This chapter described the procedures for installing the CPUs, memory modules and additional hardware installation on the aTCA-6890. Note that the aTCA-6890 may be shipped with CPU, and RAM preinstalled, depending on the options your processor blade is ordered with.

3.1 CPU Installation

The aTCA-6890 supports up to two Intel® Xeon™ processors. Remove the CPU(s) from its packaging. Before installing, apply a small quantity of thermal grease to the top side of the CPU by carefully squeezing it out of the syringe. Smooth out the grease with the plastic film as shown below. This will allow the CPU to make efficient thermal contact with the heat sink.

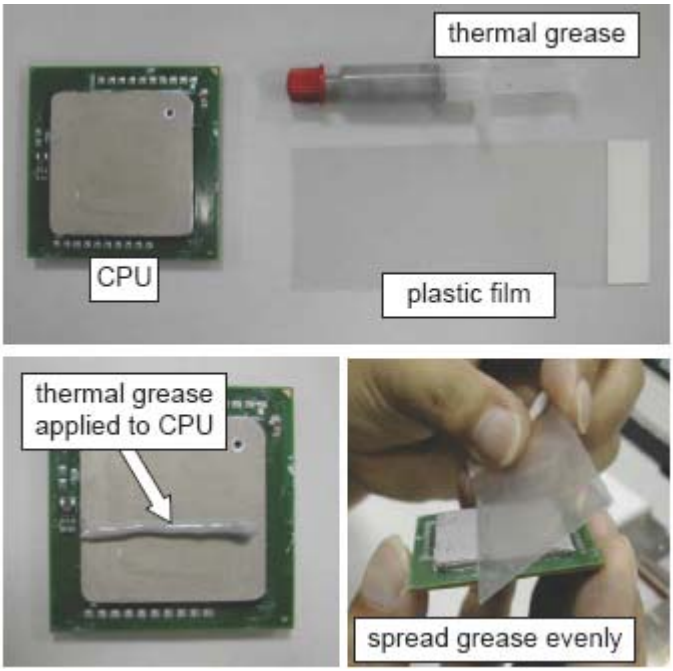


Figure 3-1: Apply thermal grease to CPU(s)

The CPU sockets are located on the aTCA-6890 as shown in **Figure 1-2: aTCA-6890 Board Layout**. Fully raise the CPU locking lever as far as it will go as shown in the R-hand socket in **Figure 3-2: CPU Installation** below. Carefully place the CPU (with thermal grease applied as described above) into the CPU socket. Be sure to align the gold triangle on the corner of the chip with the triangular cut-out in the corner of the socket. Press down gently on the chip to ensure that it is securely in place, and then press the lever down to lock the CPU into position. Repeat if required for the second CPU

Note: If you are only installing one CPU, it must be installed in the CPU0 socket.

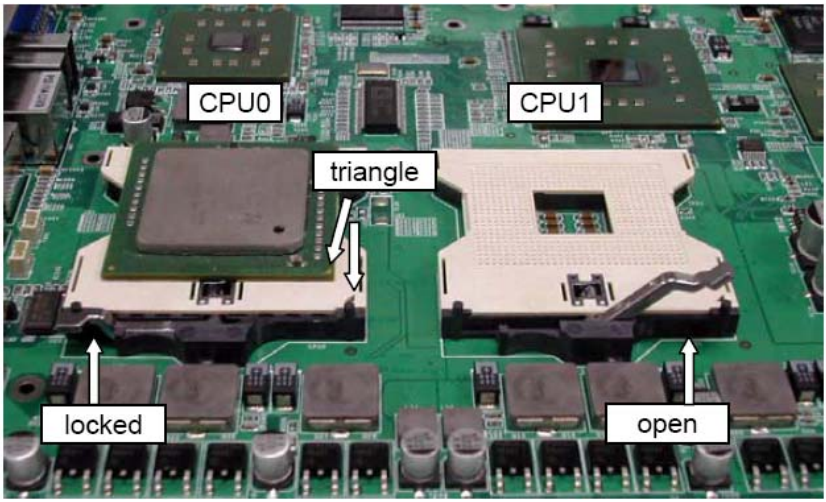


Figure 3-2: CPU Installation

Next, apply a pre-cut piece of thermal pad to the outside edge of the CPU as shown below.

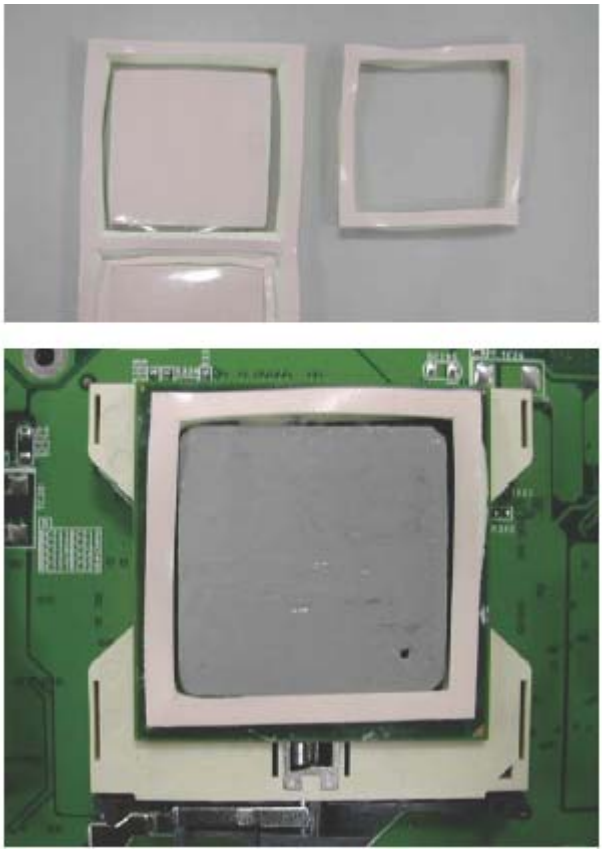


Figure 3-3: Apply thermal pad to outside edge of the CPU

3.2 Memory Installation

The aTCA-6890 CPU Module supports four DDR-II 400 240-pin DIMMs up to a maximum of 16GB. The aTCA-6890 can be populated with one, two, or four DIMM modules. The first module must be installed in slot 2 of either Channel A or B. The second module can be installed in the remaining DIMM 2 slot, or in slot 1 corresponding to the channel of the first memory module (see **Figure 3-4** below for slot locations). Refer to **Section 1.3 Main Functions, Memory Interface** for more detailed information on memory functionality.

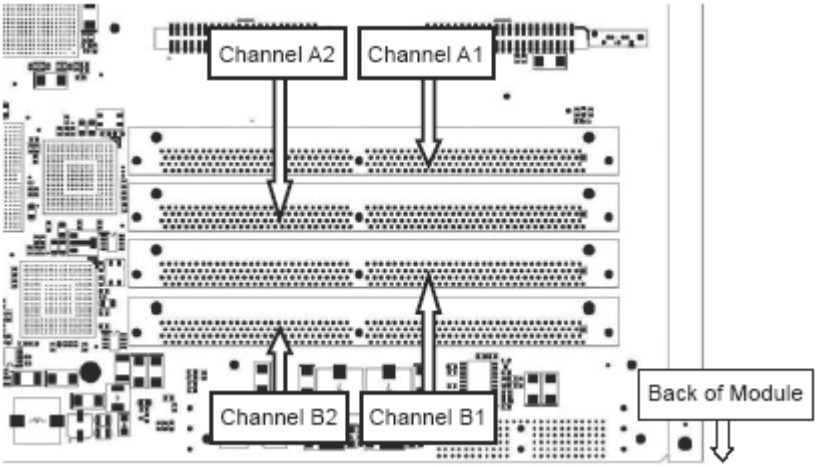


Figure 3-4: Memory slot locations

Installing the Memory Modules

Pull the ejector clips of the DIMM slot outwards. Align the notch in the memory module with the key in the DIMM slot and insert. Firmly push the memory module into the slot as shown in **Figure 3-5: Installing the Memory Modules** below, until the ejector clips pop in and lock the module in place. Repeat for the remaining memory modules.

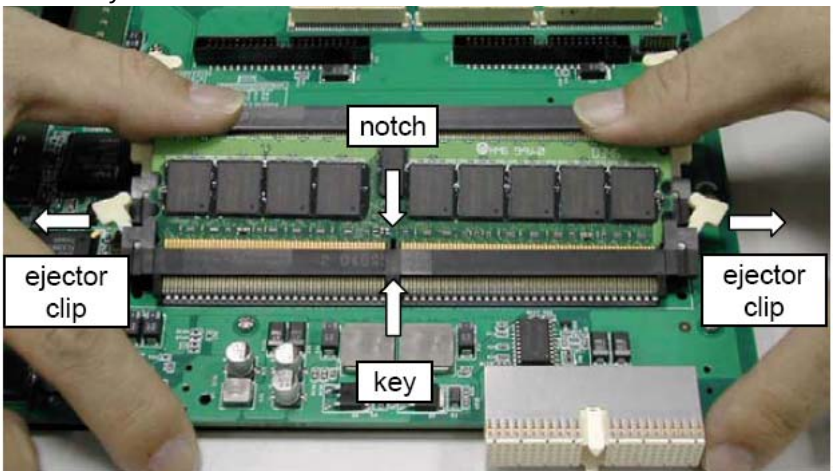


Figure 3-5: Installing the Memory Modules

3.3 Hard Drive Installation

The aTCA-6890 has two 2.5” on-card hard drive sites, each of which takes the space of one PMC site (we recommend using the upper PMC site). To install a hard drive, attach the hard drive brackets to each side of the hard drive as shown below in **Figure 3-6: Hard Drive Installation** using the screws provided. Then secure the hard drive/bracket assembly to the aTCA-6890 board with four screws from the back side of the board as shown.

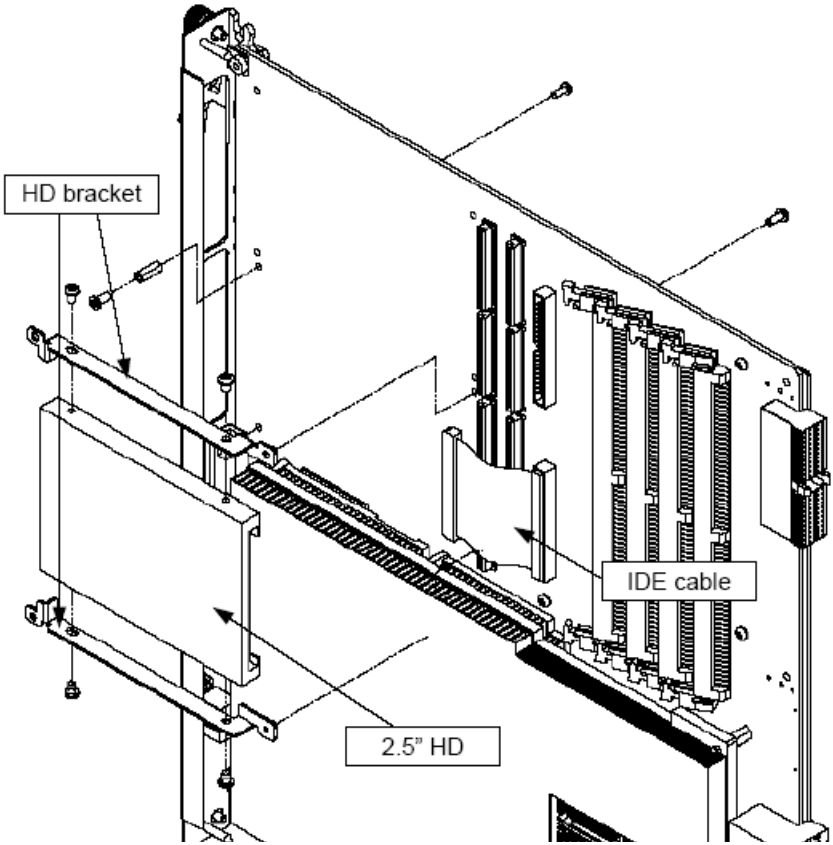


Figure 3-6: Hard Drive Installation

Connect the drive to either an IDE or SATA ribbon cable as appropriate. Plug the board end of the cable into the respective IDE (or SATA) connector on the aTCA-6890. Make sure pin 1 of the ribbon cable connector is aligned with pin 1 of the device connector.

3.4 Heat Sink Installation

Make sure you have all the required materials needed for this installation before you begin:

- Heatsink x1
- Spring-loaded Screw x8
- Insulator x2

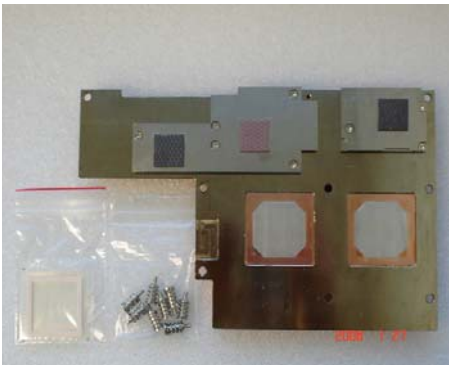


Figure 3-7: Pre-installation

Next, apply a pre-cut piece of insulator to the outside edge of the CPU or, for the uni-processors, the CPU0 as well. Please refer to the figure below for details.

Figure 3-8: Insulator

For dual processors, repeat the prior procedure on the second CPU.

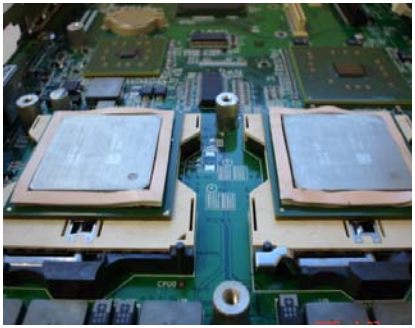
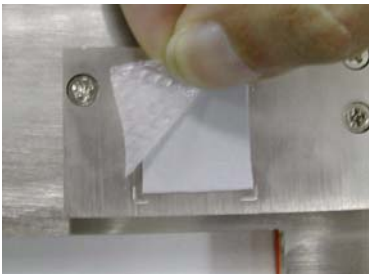


Figure 3-9: Dual processors

Remove the transparent plastic protectors from the three thermal pads circled in red on the underside of the heat sink.



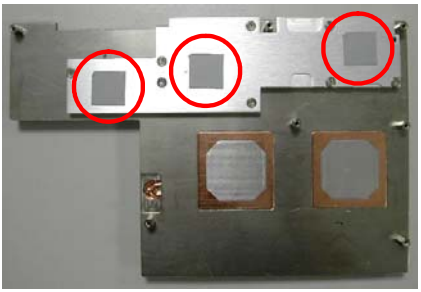


Figure 3-10: Heat Sink Installation

Gently place the heatsink on the board as shown in the figure below.

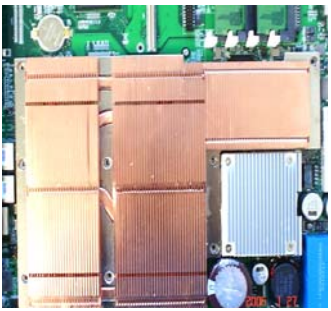


Figure 3-11: Heatsink Alignment

Make sure all the screws holes are well aligned to the stand-offs.

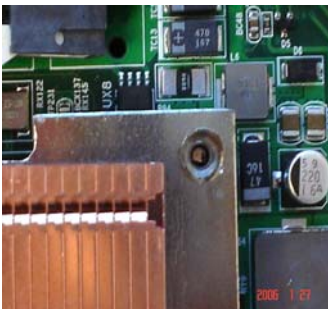


Figure 3-12: Screw Alignment

Install the heat sink on the aTCA-6890 board with eight screws from the top of the board. Be careful to screw them on straight and tighten the crews to only approximately 30% in depth in the initial installation. Wait until all the screws are securely seated before tightening screws 100% in depth.

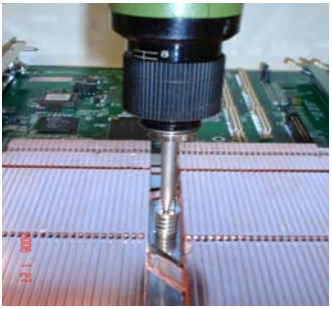


Figure 3-13: TIghtening screws

For balance reasons, tighten the screws in the following order: 1-8, as shown in the figure below.

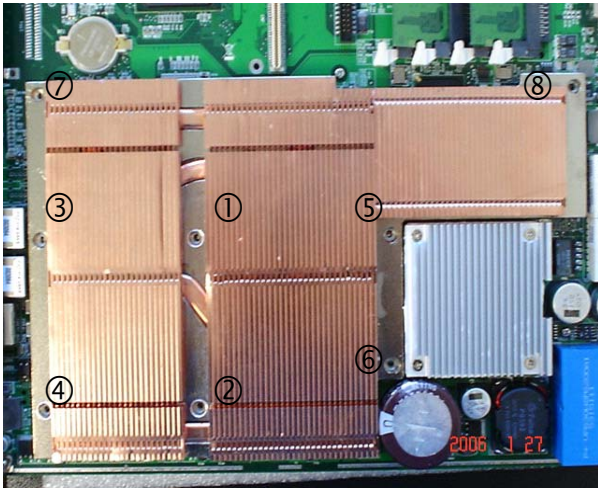


Figure 3-14: Order of screws

When disassembling the CPU heatsink, sometimes the PCM may be torn. In the base of a torn PCM, follow these procedures in order to fix this problem.

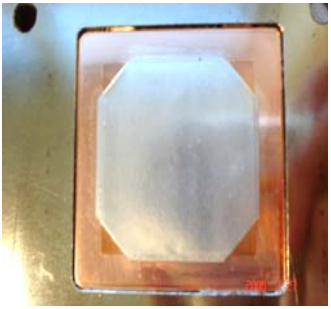


Figure 3-15: Phase-Change Material

Please contact ADLINK to apply for thermal grease. DO NOT USE OFF-THE-SELF SUBSTITUES. Proceed only when you have these items:

- Thermal grease from ADLINK
- Plastic peice

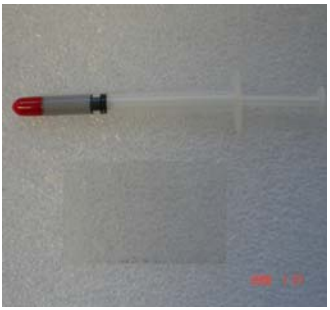


Figure 3-16: Thermal Grease

Be careful to thoroughly clean each CPU surface, as shown in the figure below.

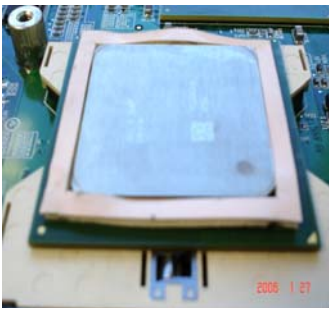


Figure 3-17: Clean CPU

Once you have cleaned each CPU surface, squeeze 1/5th - 1/4th of the tube of grease on each surface.

Figure 3-18: Volume of Grease

Use a plastic peice to spread the grease evenly on each CPU surface as shown in the figure below.

Figure 3-19: Spread the Grease

Now that this procedure is complete, the heatsink must be installed again. For instruction for installation the heatsink, refer to the step with **Figure 3-11: Heatsink Alignment** in the above procedures, to start where you must gently place the heatsink on the board.

3.5 CF Card Installation

To insert a CF card into the aTCA-6890, locate the cut-out for the CF card slot on the back side of the aTCA-6890 board behind the upper PMC site. Insert the CF card by placing it into the slot and pushing it firmly into place. To remove the CF card, grab it by the top edge and pull it out of the slot.

3.6 aTCA Module Installation & Removal

To install the aTCA-6890 module, follow these steps:

1. Carefully align the board edges with the chassis guide rails and insert the module into the chassis.

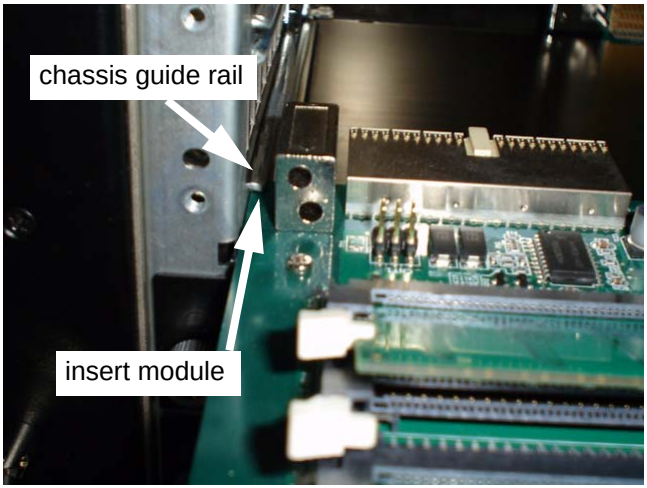


Figure 3-20: Insert the aTCA module into chassis guide rails

2. Check that the catch hooks and alignment pins at either end of the module are correctly inserted into the proper openings. Push inwards on the handles until the module is firmly seated in the chassis. (Do not force the handles if there is resistance as this may damage the connectors and/or backplane.)

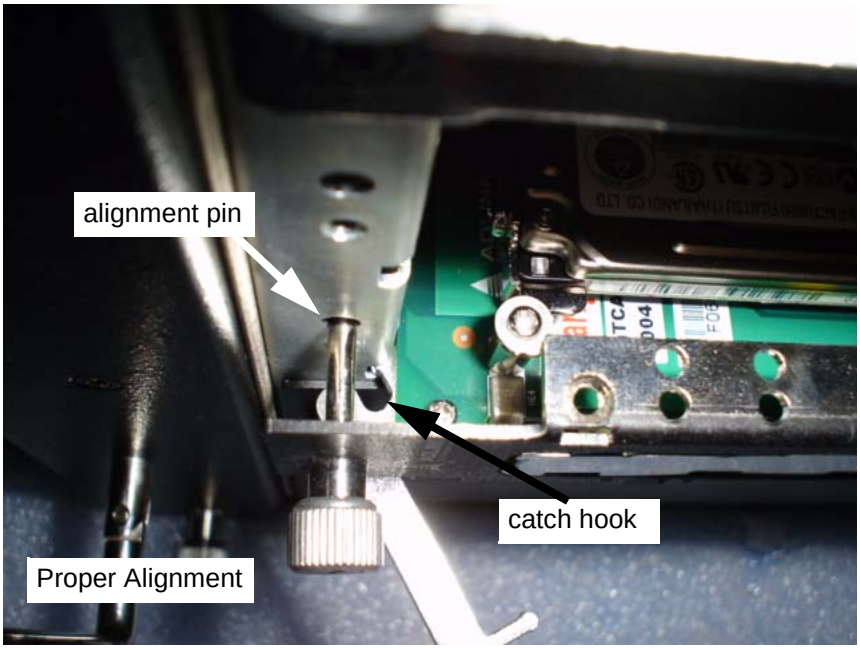


Figure 3-21: Ensure that catch hooks and alignment pins are correctly inserted

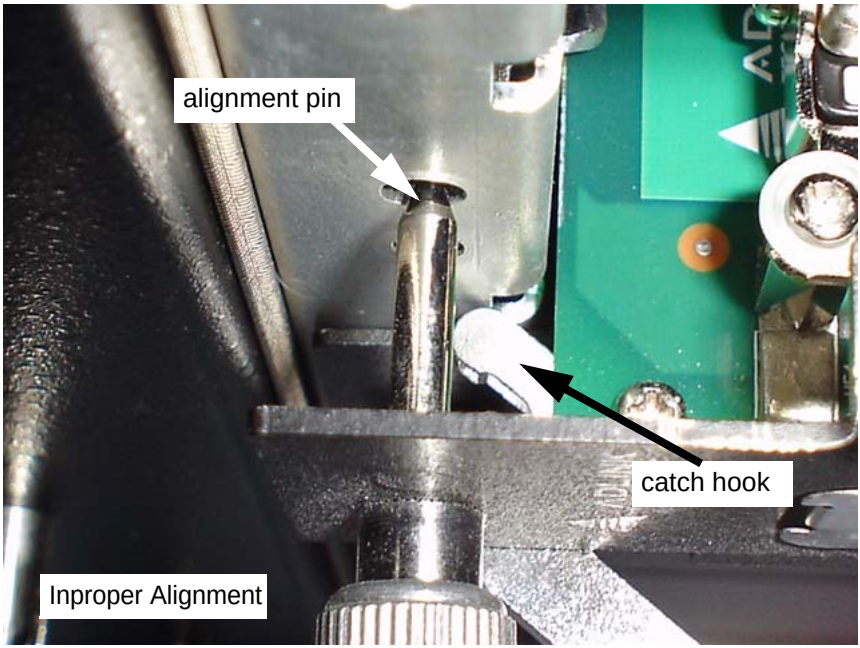


Figure 3-22: Incorrect alignment of the catch hook

3. Push the ejector handles into the faceplate.

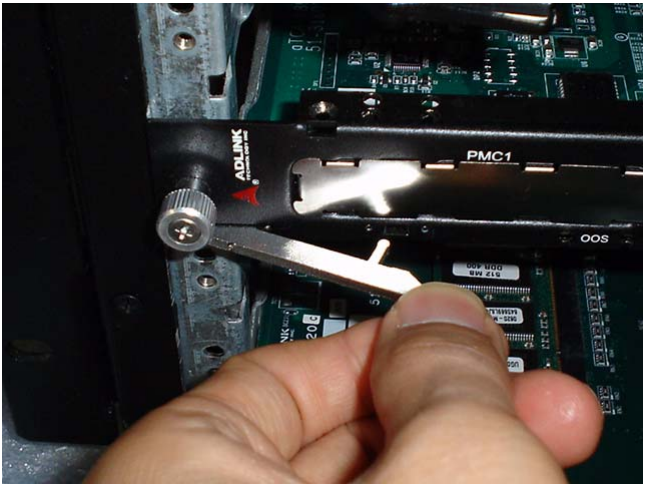


Figure 3-23: Push the ejector handles into faceplate

4. Close the ejectors handle

Figure 3-24: Close the ejector handles

5. Lock the module by turning the captive screws

Figure 3-25: Lock the module

To remove the aTCA-6890 module, undo the captive screws, pinch the ejector handle release mechanisms and pull outwards on the ejector handles to eject the module from the backplane. Pull the module towards you until it is free of the chassis.

3.7 Operating System Installation

For more detailed information about your operating system, refer to the documentation provided by the operating system vendor.

Installing peripheral devices: Peripheral devices are automatically configured by the BIOS during the boot sequence.

Most operating systems require initial installation on a hard drive from a floppy or CDROM drive. These devices should be configured, installed, and tested with the supplied drivers before attempting to load the new operating system.

Read the release notes and installation documentation provided by the operating system vendor. Be sure to read any README files or documents provided on the distribution disks, as these typically note documentation discrepancies or compatibility problems.

Select the appropriate boot device order in the BIOS Setup Utility boot menu depending on the OS installation media used. For example, if the OS includes a bootable installation floppy, select Floppy as the first boot device and reboot the system with the installation floppy installed in the floppy drive. (Note that if the installation requires a non-bootable CD-ROM, it is necessary to boot an OS with the proper CD-ROM drivers in order to access the CD-ROM drive).

Proceed with the OS installation as directed. Be sure to select appropriate device types if prompted. Refer to the appropriate hardware manuals for specific device types and compatibility modes of ADLINK products.

When installation is complete, reboot the system and set the boot device order in the Setup Utility boot menu appropriately.

4 Device Driver Installation

To install drivers for the aTCA-6890, refer to the installation information in this chapter. Basic driver installation information for Windows XP/2000 Professional is outlined in this section. The drivers are located in the following directories of the CD-Rom:

Chipset driver	X:\ATCA\ATCA-6890\chipset\
VGA driver	X:\ATCA\ATCA-6890\VGA\
LAN	X:\ATCA\ATCA-6890\LAN\

For information regarding BSP support for VXWorks and Montivista operating systems, please contact ADLINK.

4.1 Intel® E7520 MCH/6300ESB ICH Chipset

This section describes the installation procedure for the Intel® E7520 MCH/6300ESB ICH chipset device driver under Windows XP/2000 Professional.

System Requirements

One of the following operating systems must be fully installed on the system before installing any other driver, utilities, or software:

- Windows 2000 Professional
- Windows XP Professional

Intel® Chipset Software Installation Utility

This section describes how to install the *Intel® Chipset Software Installation Utility* on a system running Windows XP/2000 Professional.

1. Check the System Requirements. Windows 2000/XP must be fully installed and running on the system prior to running this software.
2. Close any running applications.
3. Place the ADLINK CD into the CD-ROM drive. Run **infinst_autol_6.2.1.1001.exe** under **X:\ATCA\ATCA-6890\chipset**, where X is the CD drive letter.

4. Click **Next** on the *Welcome* screen to read and agree to the license agreement. Click **Yes** if you agree to continue. NOTE: If you click **No**, the program will terminate.
5. Click **Next** on the *Readme Information* screen to install the INF files.
6. Click **Finish** to restart the system when prompted to do so.
7. Follow the screen instructions and use the default settings to complete setup when Windows XP/2000 Professional restarts. Upon restart, Windows may display that it has found new hardware and is installing drivers for them. Select **Yes**, if prompted to restart Windows XP/2000 Professional. This completes the installation of the *Intel® Chipset Software Installation Utility*.

4.2 VGA Driver Installation

Windows XP/2000 Professional will attempt to install a standard VGA driver automatically. To guarantee compatibility, manually install the most up-to-date VGA driver, which is provided on the ADLINK CD. After installing Windows XP/2000 Professional, install the most up-to-date driver by following these steps (note: different drivers for Windows XP and 2000 Professional):

1. Boot Windows XP/2000 Professional, then run the program **w2k-ragexl-5-0-2195-5012.exe** if running Windows 2000, or **wxp-ragexl-5-10-2600-6009.exe** if running Windows XP, under the directory **X:\ATCA\ATCA-6890\VGA**, where X is the CD drive letter.
2. The VGA driver will automatically be installed onto the system.
3. Restart the system.

4.3 LAN Driver Installation

Note: Before installing the LAN driver, the Intel® E7520 MCH/6300ESB ICH chipset device driver must first be installed as described in Section 4.1 above.

This section describes the LAN driver installation process for the **Intel® 82546GB Gigabit Ethernet Controllers** under Windows XP/2000 Professional. The Intel® software utilities package include a Diagnostics Utility, Makedisk Utility, and the 10/100/1000Mbps Ethernet device drivers. All drivers and utilities are stored in the ADLINK CD under the directory: **X:\ATCA\ATCA-6890\LAN,** where X is the CD drive letter. For driver installations under other operating systems, please refer to the the ADLINK CD.

During Windows XP/2000 Professional installation, the operating system will install a LAN driver automatically. To guarantee compatibility, manually install the most up-to-date driver, which is provided on the ADLINK CD. After installing the OS, update the driver by following these steps:

1. Run the self-extracting file **pro2kxpm_9.1.exe** in the following directory:**X:\ATCA\ATCA-6890\LAN**.
2. Click through the subsequent pages to extracte the files to the default location **c:\Intel9.1**.
3. Click **Install Software** to install the Intel® PRO Network Connections drivers.

5 Watchdog Timer

5.1 WDT Overview

The primary function of the Watchdog Timer is to monitor the aTCA-6890's operation and to generate an IRQ or to reset the system should the software fail to function as programmed. The major features of the Watchdog Timer are:

- Enabled and disabled through software control
- Armed and strobed through software control

The aTCA-6890's custom Watchdog Timer circuit is integrated into the south bridge 6300ESB and supports multiple modes: WDT and free-running. Free-running mode is a one stage timer and it will toggle WDT_TOUT# after a programmable time. WDT mode is a two stage timer and its operation is described as follows:

WDT Mode:

The two-stage Watchdog Timer (WDT) provides a resolution ranging from 1 micro second to 10 minutes. The timer uses a 35-bit down-counter. The counter is loaded with the value from the first Preload register. The timer is then enabled and starts counting down. The time at which the WDT first starts counting down is called the first stage. If the host fails to reload the WDT before the 35-bit down counter reaches zero the WDT generates an internal interrupt. After the interrupt is generated, the WDT loads the value from the second Preload register into the WDT's 35-bit down-counter and starts counting down. The WDT is now in the second stage. If the host still fails to reload the WDT before the second timeout, the WDT drives the WDT_TOUT# pin low. The WDT_TOUT# pin is held low until the system is reset.

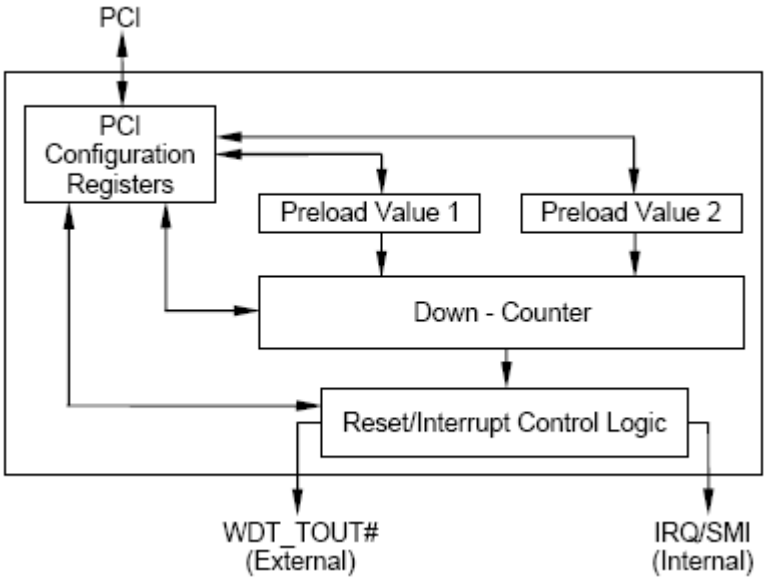


Figure 5-1: WDT Block Diagram

5.2 Configuration Registers

The Intel® 6300ESB ICH WDT, appears to BIOS as PCI Bus 0, Device 29, Function 4, and has the standard set of PCI Configuration register. The following describes the configuration registers.

Offset 10H: Base Address Register (BAR0)

This register determines the memory base for WDT down-counter setting. It will be used to set Preload value 1 register, Preload value 2 register, General Interrupt Status register and Reload register.

Preload Value 1 & 2 registers

These two registers are used to hold the preload value for the WDT timer. Its value will be automatically transferred into the down-counter every time the WDT enters the first and second stage. Preload Value 1 register is located at Base + 00H and Preload Value 2 register is located at Base + 04H. Only bit [19:0] are settable.

The register unlocking sequence is necessary whenever writing to the Preload registers. Instructions for writing a value into preload value 1 & 2 registers are as follows:

1. Write 80H to offset BAR0 + 0CH.
2. Write 86H to offset BAR0 + 0CH.
3. Write desired value to preload register. (BAR0 + 00H or BAR0 + 04H)

General Interrupt Status Register

This register is at Base + 08H. Bit 0 is set when the first stage of down-counter reaches zero.

Bit 0 = 0 – No Interrupt

Bit 1 = 1 – Interrupt Active

NOTE: This bit is not set in free running mode.

Reload Register

This register is at Base + 0CH. Write 1 to bit 8 will reload the down-counter's value. Following is the procedure of how to prevent a timeout.

1. Write 80H to offset BAR0 + 0CH
2. Write 86H to offset BAR0 + 0CH
3. Write a '1' to RELOAD[8] of the reload register

Offset 60 – 61H: WDT Configuration Register

Bit 5 indicates whether or not the WDT will toggle the WDT_TOUT# pin when WDT times out. (0 = Enabled, 1 = Disabled)

Bit 2 provides two options for prescaling the main down-counter. (0 = 1ms – 10min, 1 = 1us – 1sec)

Bit [1:0] allows the user to choose the type of interrupt desired when the WDT reached the end of the first stage without being reset. (00 = IRQ, 01 = reserved, 10 = SMI, 11 = Disabled)

NOTE: The WDT does not support SMI now. IRQ uses APIC 1, INT 10 and it is active low, level triggered.

Offset 68H: WDT Lock Register

Bit 2 is used to choose the functionality of the timer. (0 = Watchdog Timer mode, 1 = Free running mode) The free-running mode ignores the first stage and only uses Preload Value 2. In free-running mode it is not necessary to reload the timer as it is done automatically every time the down-counter reaches zero.

Bit 1 enables or disables the WDT. (0 = Disabled, 1 = Enabled)

Bit 0 will lock the values of this register until a hard reset occurs or power is cycled. (0 = unlocked, 1 = locked). The default is Unlocked.

5.3 GPIO Control Registers

There are three GPIOs on aTCA-6890 related to watchdog timer. They are listed as follows. The GPIO control base port is 480H.

WDT_TOUT# Pin Selection

WDT_TOUT# signal is multiplexed with GPIO32. When using WDT, this signal must be switched to WDT_TOUT# function. It uses bit 0 of GPIOBASE + 30H to set WDT_TOUT function. (0 = WDT_TOUT#, 1 = GPIO32)

User LED Control

GPO25 of 6300ESB is designed to control User LED. Two features of User LED are supported on aTCA-6890. User LED lights or blinks.

The user can program this GPIO when running WDT configuration.

User LED Light

Set bit 25 of GPIOBASE + 04H to 0. Bit 25 of GPIOBASE + 0CH determines the state of User LED. (0=dark, 1=light)

User LED Blink

Set bit 25 of GPIOBASE + 04H to 0. Bit 25 of GPIOBASE + 18H enables User LED blinking function. (0=function normally, 1=enable blinking) The high and low times have approximately 0.5 seconds each.

5.4 WDT Programming Procedure

1. Make sure WDT_TOUT# signal is enabled (not GPIO[32] function).
2. Set WDT output enable, prescaler and interrupt type into the WDT configuration register.
3. Get control base from the Base Address register.
4. Program Preload register's value according to unlocking sequence.
5. Set WDT timer mode into WDT Lock Register.
6. Enable WDT from WDT Lock register and program the functionality of the User LED.

To keep the timer from causing an interrupt or driving WDT_TOUT#, the timer must be reloaded periodically. The frequency of reloads required is dependent on the value of the preload values. To reload the down-counter, the register unlocking sequence must be performed.

To disable WDT, set bit 1 of WDT Lock Register to 0.

5.5 WDT Utilities

ADLINK provides a demo DOS utility, **hrwdt.exe**, to assist the user in using the Watchdog Timer. It is included on the All-in-One CD under the directory:

X:\ATCA\ATCA-6890\WDT

Under DOS, run "**hrwdt /?**" to access the onscreen help for the utility.

6 IPMC

6.1 IPMC Overview

The aTCA-6890 features a Pigeon Point Systems® powered BMR-AVRTM based IPM Controller (IPMC), which supports PICMG 3.0 R2.0 and IPMI 1.5 revision 1.1 specifications. The IPMC acts as a system level supervisor upon the aTCA-6890 blade, which is referred as Payload or FRU in this document. Including hot-swap behaviors, board-level cooling request, power budget allocation, and data transport E-keying exchange are all controlled by IPMC. This is a quick “HOW-TO…” guide to help users to access the payload state, to communicate with IPMC with supported IPM commands, to monitored sensor list, to read FRU EEPROM information, and to update the IPMC firmware in the field.

6.2 FRU States

ATCA specification defines two types of FRU that are visible to and controlled through the IPMI infrastructure:

1. Intelligent FRU, which physically include an IPM Controller.
2. Managed FRU, which are either Intelligent FRUs or represented by an Intelligent FRU and visible to the IPMI infrastructure.

Any FRU that enters an ATCA Shelf goes through a series of states to become active. The aTCA-6890 blade is defined as an Intelligent FRU to the ATCA shelf, so that its FRU states and state transitions are well defined as in Table-1: FRU States and Figure-1: FRU State Transitions.

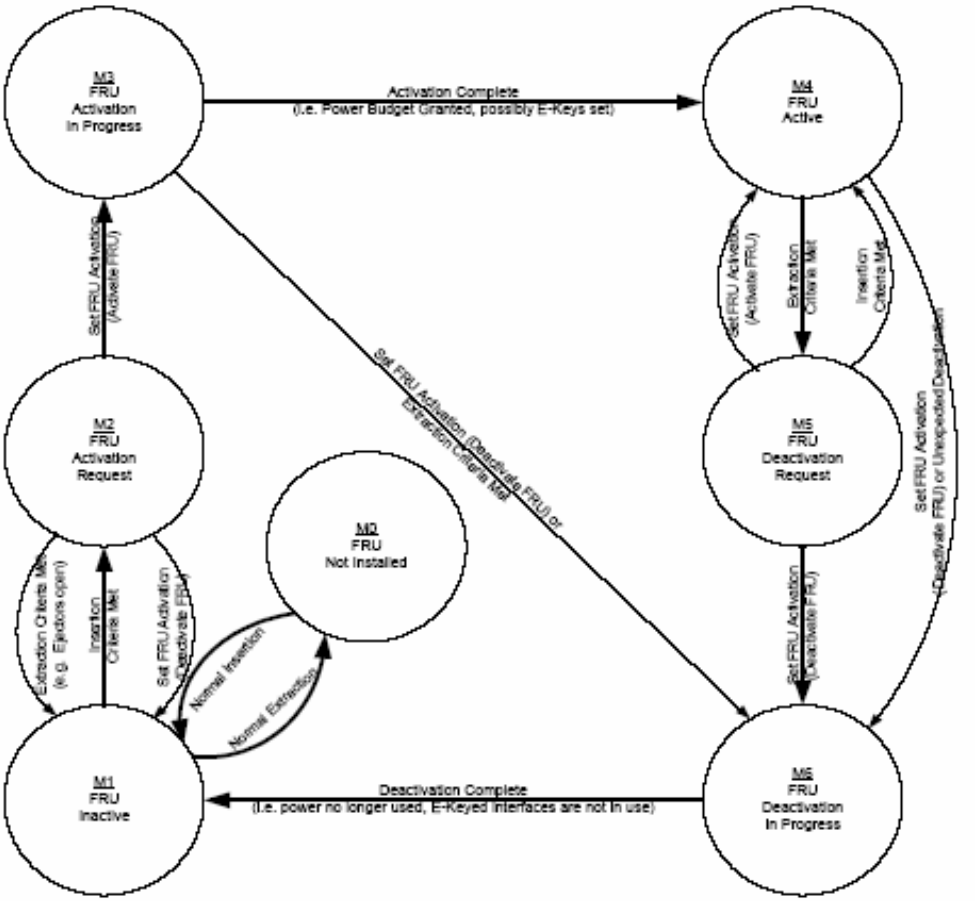


Figure 6-1: FRU State Transitions

State #	State name	Additional information	FRU Events generated	Notable commands received	BLUE LED
M0	FRU Not Installed	The FRU is not installed. Outputs and inputs to/from the FRU are fully disabled including all power.	HotSwap Event		off
M1	FRU Inactive	The FRU is installed and IPM Controller is operational, but Payload is not powered. Outputs and inputs to/from FRU Payload are fully disabled. FRU may be extracted safely.	HotSwap Event (State changed to M1 from M0 (optional), M2, or M6)	Set FRU Activation Policy	on
M2	FRU Activation Request	The FRU is ready to attempt activation. Outputs and inputs to/from FRU are fully disabled including Payload power. The FRU waits in M2 for the Shelf Manager to send the “Set FRU Activation” command. The Shelf Manager queries the FRU for important SDRs to expose to the System Manager.	HotSwap Event (State changed to M2 from M1)	SDR Repository related commands. Set FRU Activation (Activate FRU)	long blink
M3	FRU Activation in Process	The FRU is preparing to become active. The FRU cannot be extracted safely while in this state. The Shelf Manager negotiates with the FRU to allocate its power budget. Once granted a power budget, the Payload begins powering up and may perform initialization and/or self-tests during this time. The FRU automatically transitions to M4 at its discretion when it determines that activation is complete and the FRU is operational.	HotSwapEvent (State changed to M3 from M2)	Power and Cooling commands. E-keying Commands Set FRU Activation (Deactivate FRU)	off
M4	FRU Active	Normal operational state. Power has been applied, and the FRU cannot be extracted safely. The FRU may be reset and remain in this state. The FRU can initiate a deactivation request (i.e., move to M5) when Extraction Criteria Met occurs. Alternatively, the Shelf Manager can move the FRU to M6 by sending a “Set FRU Activation (Deactivate FRU)”.	HotSwapEvent (State changed to M4 from M3 or M5)	Set FRU Activation (Deactivate FRU)	off

Table 6-1: FRU States

State #	State name	Additional information	FRU Events generated	Notable commands received	BLUE LED
M5	FRU Deactivation Request	The FRU is requesting deactivation permission from the Shelf Manager. The FRU cannot yet be extracted safely. From the Payload's perspective, this is equivalent to M4.	HotSwapEvent (State changed to M5 from M4)	Set FRU Activation (Deactivate FRU | Activate FRU)	short blink
M6	FRU Deactivation In Progress	The FRU is closing down its application and preparing to be deactivated. I/O connections are being closed. The FRU cannot yet be extracted safely. The power to the FRU's Payload is turned off before leaving this state. The FRU automatically transitions to M1 when it determines that deactivation is complete and it can be safely extracted.	HotSwapEvent (State changed to M6 from M3, M4, or M5)		short blink
M7	Comm. Lost	This is an abnormal state and is described in Section 3.2.4.4Activation (Deactivate FRU)".			same as before M7 entry

Table 6-1: FRU States

6.3 Accessing the IPMC

There are three methods to access IPMC:

1. Shelf Management Controller (ShMC)

   ShMC can issue IPM commands via IPMB buses between ShMC and payload on the backplane.

2. Payload Port

   Payload can issue IPM commands via the serial port COM3 to the IPMC, with 9600 Baud rate. Please refer to the FIRMWARE /FRU EEPROM UPDATE section for more details.

3. IPMC Debug Port

   Users can set on-board DIP switch SWY1 to configure front panel COM1 directly connected to IPMC serial debug port. Please refer to the FIRMWARE /FRU EEPROM UPDATE section for more details.

Users can get IPMC firmware revision, operating mode, FRU state, debug messages, and alerts by one of the three access methods.

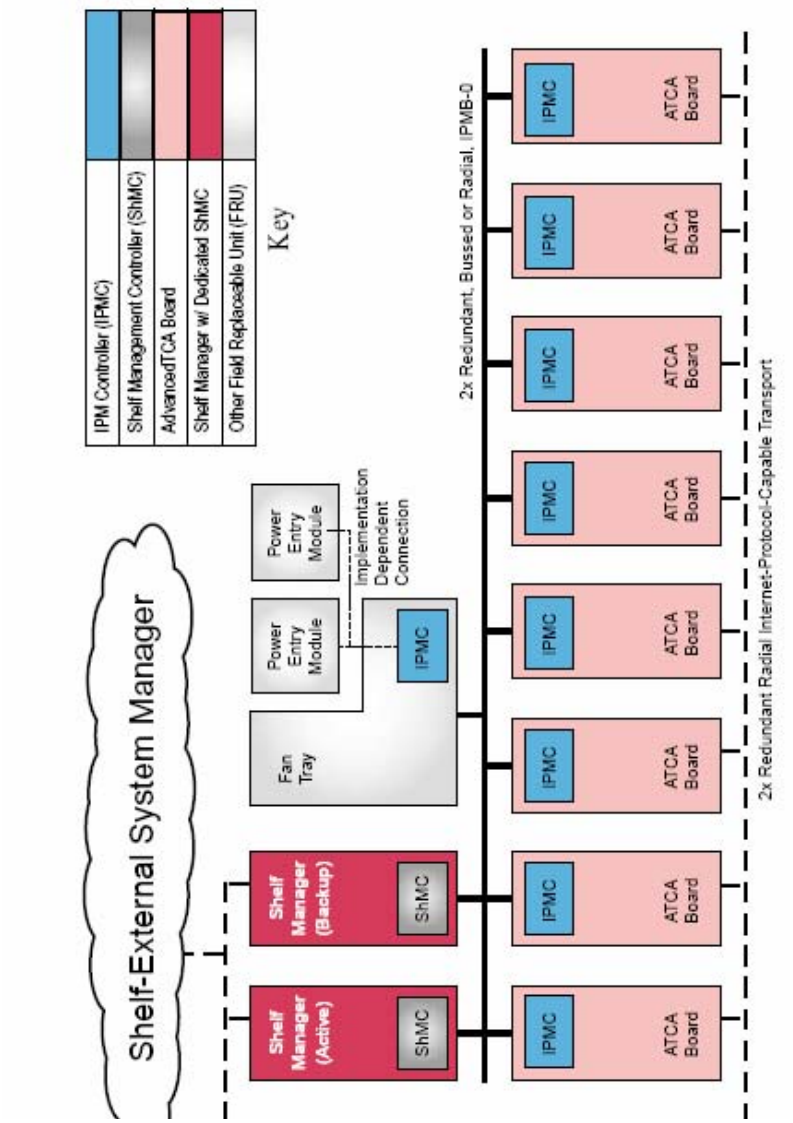


Figure 6-2: ATCA System Management Architechture

6.4 IPMI Command Set

The IPMC firmware is fully compliant with PICM 3.0 R2.0 and relevant ECN. Please refer to Table-2 for the commands supported:

Command	IPMI Spec	NetFn	CMD	IPM Controller Req
IPM Device "Global" Commands				
Get Device ID	17.1	App	01h	Mandatory
Cold Reset	17.2	App	02h	Optional
Warm Reset	17.3	App	03h	Optional
Get Self Test Results	17.4	App	04h	Mandatory
Get Device GUID	17.8	App	08h	Optional
Broadcast "Get Device ID"	17.9	App	01h	Mandatory
IPMI Messaging Support Commands				
Send Message	18.7	App	34h	Optional
BMC Watchdog Timer				
Reset Watchdog Timer	21.5	App	22h	Mandatory
Set Watchdog Timer	21.6	App	24h	Mandatory
Get Watchdog Timer	21.7	App	25h	Mandatory
Event Commands				
Set Event Receiver	23.1	S/E	00h	Mandatory
Get Event Receiver	23.2	S/E	01h	Mandatory
Platform Event (a.k.a. "Event Message")	23.3	S/E	02h	Mandatory
Sensor Device Commands				
Get Device SDR Info	29.2	S/E	20h	Mandatory
Get Device SDR	29.3	S/E	21h	Mandatory
Reserve Device SDR Repository	29.4	S/E	22h	Mandatory
Get Sensor Reading Factors	29.5	S/E	23h	Optional
Set Sensor Hysteresis	29.6	S/E	24h	Optional
Get Sensor Hysteresis	29.7	S/E	25h	Optional
Set Sensor Threshold	29.8	S/E	26h	Optional
Get Sensor Threshold	29.9	S/E	27h	Optional
Set Sensor Event Enable	29.10	S/E	28h	Optional
Get Sensor Event Enable	29.11	S/E	29h	Optional
Rearm Sensor Events	29.12	S/E	2Ah	Optional

Table 6-2: Supported IPMI Commands

Command	IPMI Spec	NetFn	CMD	IPM Controller Req
Get Sensor Event Status	29.13	S/E	2Bh	Optional
Get Sensor Reading	29.14	S/E	2Dh	Mandatory
FRU Device Commands				
Get FRU Inventory Area Info	28.1	Storage	10h	Mandatory
Read FRU Data	28.2	Storage	11h	Mandatory
Write FRU Data	28.3	Storage	12h	Mandatory
AdvancedTCA™				
Get PICMG Properties Command	3-9	PICMG	00h	Mandatory
Get Address Info	3-8	PICMG	01h	Optional
FRU Control Command	3-21	PICMG	04h	Mandatory
Get FRU LED Properties Command	3-23	PICMG	05h	Mandatory
Get LED Color Capabilities Command	3-24	PICMG	06h	Mandatory
Set FRU LED State	3-25	PICMG	07h	Mandatory
Get FRU LED State	3-26	PICMG	08h	Mandatory
Set IPMB State Command	3-47	PICMG	09h	Mandatory
Set FRU Activation Policy Command	3-16	PICMG	0Ah	Mandatory
Get FRU Activation Policy Command	3-17	PICMG	0Bh	Mandatory
Set FRU Activation Command	3-15	PICMG	0Ch	Mandatory
Get Device Locator Record ID Command	3-28	PICMG	0Dh	Mandatory
Get Port State	3-40	PICMG	0Eh	Mandatory
Set Port State	3-41	PICMG	0Fh	Mandatory
Compute Power Properties	3-56	PICMG	10h	Mandatory
Set Power Level	3-58	PICMG	11h	Mandatory
Get Power Level	3-57	PICMG	12h	Mandatory
Get Fan Speed Properties	3-59	PICMG	14h	Mandatory
Get Fan Level	3-60	PICMG	16h	Optional
Set Fan Level	3-61	PICMG	15h	Optional
Bused Resource Control (Release, Query, Force, Bus Free)	3-43	PICMG	17h	Mandatory

Table 6-2: Supported IPMI Commands

6.5 Sensor Data Record List

This section lists all sensor parameters in Sensor Data Record (SDR) and are organized according to type for easy reference. For threshold sensors, all threshold value and asset/dessert events are listed. For discrete sensors, only the name and type are listed. Detailed type and offset codes can be found in the IPMI and the ATCA specification.

No.	Name	Type
1	Hot Swap Hot	Swap
2	IPMB Physical	IPMB Link
3	BMC Watchdog	Watchdog2
4	W83784 system temp	
5	CPU#0 temp	
6	CPU#1 temp	
7	+3.3V	
8	+1.8V	
9	+1.5V	
10	+5.0V	
11	HW Monitor SMI	
12	HW Monitor Over Temperature	
13	HW Monitor WatchDog Time-out	
14	ICH WatchDog Time-out	
15	CPU FERR	
16	CPU IERR	
17	MCH/PXH OverTemperature	
18	Payload System Sleep State 5 (SLPS5#)	
19	Payload Power OK	
20	BIOS POST OK	

Table 6-3: Discrete Based Sensors

6.6 FRU Storage Information

FRU Storage holds text and static properties for this board. Here is a brief description of the FRU fields. Detailed access methods can be found in the IPMI Platform Management FRU Information Storage Definition V1.0, Document Revision 1.1.

For Option 1:

[Common Header]

Version = 1

[Board Info]

Version = 1

Language Code = en

Mfg Date/Time = 03/07/2005

Manufacturer = ADLINK Technology

Product Name = ATCA-6890

Serial Number = 0000000000

Part Number = ATCA-6890

FRU Programmer File ID = fru16-opt2.inf

[Product Info]

Version = 1

Language Code = en

Manufacturer = ADLINK Technology

Product Name = ATCA-6890 (board)

Part/Model Number = ATCA-6890

Product Version = Rev 1.6

Serial Number = 0000000000

Asset Tag = N/A

FRU File ID = fru16-opt2.inf

[Board Connectivity]

Base,1,0 = Base,0

Base,2,0 = Base,0

Fabric,1,0 = Ethernet,0

Fabric,2,0 = Ethernet,0

Fabric,1,1 = Ethernet,0

Fabric,2,1 = Ethernet,0

For Option 2:

[Common Header]

Version = 1

[Board Info]

Version = 1

Language Code = en

Mfg Date/Time = 05/02/2005

Manufacturer = ADLINK Technology

Product Name = ATCA-6890

Serial Number = 0000000000

Part Number = ATCA-6890

FRU Programmer File ID = fru17-opt2.inf

[Product Info]

Version = 1

Language Code = en

Manufacturer = ADLINK Technology

Product Name = ATCA-6890 (board)

Part/Model Number = ATCA-6890

Product Version = Rev 1.7

Serial Number = 0000000000

Asset Tag = N/A

FRU File ID = fru17-opt2.inf

[Board Connectivity]

Base,1,0 = Base,0

Base,2,0 = Base,0

Fabric,1,0 = Ethernet,0

Fabric,2,0 = Ethernet,0

Fabric,1,1 = Ethernet,0

Fabric,2,1 = Ethernet,0

Fabric,1,0 1 = Ethernet,0

Fabric,2,0 1 = Ethernet,0

6.7 Firmware/FRU EEPROM Update

As mentioned in the previous ACCESS IPMC section, there are three methods to update IPMC firmware and FRU EEPROM.

1. ShMC access. Users will need the update utilities to run on ShMC. The IPMC firmware / FRU EEPROM update utilities will be dependent and provided by the ShMC provider.
2. IPMC debug port. Users will need another system with at least one serial port cross-over linked to aTCA-6890 IPMC debug port. Contact ADLINK for the update utilities.
3. IPMC payload port. Users will only need ADLINK utilities to run on aTCA-6890 by IPMC payload port (COM3).

Note: The payload (aTCA-6890) will be reset by IPMC after firmware update completed.

Update Procedures

1. Decide which method to proceed

2. When IPMC debug port is used:

1. Tap on-board SWY1 (1,4:OFF; 2,3:ON) to switch IPMC debug port linked to COM1 connector.
2. Apply the RJ-45 to DB-9 male adapter on front panel COM1, and then use a cross-over DB-9 to DB-9 female cable connected after the adapter linking to the serial port of another Service system.
3. Power up the CPU blade and Service system. Run ADLINK IPMC firmware update utilities on the Service system, with the following syntax:

   upgradefw -s <device>:<baud rate> <image filename>

   where <device>= serial port on Service system (COM1/2/3 etc.) <baud rate>=9600 only.

   For Windows OS, use the following command in a DOS prompt: **upgradefw -s COM1:9600,N,8,1 upgrade.img**

For Linux OS, use the following command in a terminal shell: **upgradefw -s /dev/ttyS0:9600,N,8,1 upgrade.img**

4. The following messages will be shown as update completed.

   BMR-AVR firmware upgrade utility. Pigeon Point Systems © 2004

   Upgrade interface: serial, device: /dev/ttyS0, options:

   Firmware upgrade image: upgrade.img

   Preparing Master AVR for programming ..... OK

   Programming 43183 bytes to Master AVR at 000000 ... 100%

   Preparing Slave AVR for programming ... OK

   Programming 8161 bytes to Slave AVR at 000000 ... 100%

3. When IPMC payload port is used:

1. Prepare a DOS-bootable device, e.g. an USB flash.
2. Contact ADLINK for IPMC payload port utilities.
3. Power up the CPU blade and boot into DOS with utilities and updated images.
4. Run ADLINK IPMC payload port firmware update utilities on the CPU blade, with the following syntax:

   bmrupd –s COM3:9600 <image filename>

5. The following messages will be shown as update completed.

   BMR-AVR firmware upgrade utility. Pigeon Point Systems (c) 2004.

   DOS version 1.1 ported by ADLINK 2004/11/14.

   Upgrade interface: serial, device: COM3, options: 9600

   Firmware upgrade image: fw163o2.img

   Preparing Master AVR for programming ..... OK

   Programming 45945 bytes to Master AVR at 000000 ... 100%

Preparing Slave AVR for programming ... OK

Programming 7201 bytes to Slave AVR at 000000 ... 100%

4. FRU EEPROM update, use IPMC payload port:

1. Prepare as 3.1 to 3.3
2. Run ADLINK IPMC payload FRU EEP update utility on the CPU blade, with the following syntax:

   fruupd –s COM3:9600 –f <fru_image_filename>
3. The following messages will be shown as update completed.

   FRU UPDATE UTILITY v 1.1 11/14/2005 - BMR-AVR FRU update tool

   Copyright(c) 2005, ADLINK Technology. All Rights Reserved

   Opening port: COM3:9600

   Opening file: fru18o2.bin

   Sending data...Reading data... .....

   Sending data...Reading data... .....

   Sending data...Reading data... .....

   Sending data...Reading data... .....

   Sending data...Reading data... .....

   frutool: done!

6.8 Misc. Notes

SEL (System Event Log):

There is no local SEL. Events are sent to the shelf manager, and the payload is notified over the payload serial interface.

OOS LED (Out of Service):

OOS LED is ON when any of the following conditions is true:

- System power instable, (SYS_PWROK alarm), or
- System POST is not completed (POSTOK alarm), or
- CPU Internal Errors (CPU_FERR#, CPU_IERR# alarms), or
- System goes into SOFTOFF state (PM_SLPS5# alarm)

Ejector Handle and Power Button:

On detecting the lower handle opened, IPMC will issue a POWER BUTTON (PWRBTN#) event to notify system into SOFTOFF state (PM_SLPS5#)

Sleep S5:

When the payload enters the SOFTOFF state, its FRU state will deactivate and transition to M1. IPMC will turn off payload power, and turn on the blue HS LED.

If user shutdown the OS by commands, the lock bit will be enabled and caused the payload to enter SOFTOFF state, even the lower handle is closed. Users will need to open and close the handle to power-up the payload again and transition back to M4.

Shutdown:

The shutdown timeout is 25.5 second. The payload will be powered off after PM_SLPS5# is asserted or after the timeout expires. The blue LED will short blink while waiting to shutdown.

Warranty Policy

Thank you for choosing ADLINK. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ADLINK's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: http://rma.adlinktech.com/policy/.
2. All ADLINK products come with a limited two-year guarantee, one year for products bought in China:

   ▶The warranty period starts on the day the product is shipped from ADLINK's factory.

   ▶Peripherals and third-party products not manufactured by ADLINK will be covered by the original manufacturers' warranty.

   ▶For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ADLINK is not responsible for loss of data.

   ▶Please ensure the use of properly licensed software with our systems. ADLINK does not condone the use of pirated software and will not service systems using such software. ADLINK will not be held legally responsible for products shipped with unlicensed software installed by the user.

   ▶For general repairs, please do not include peripheral accessories. If peripherals need to be included, be certain to specify which items you sent on the RMA Request & Confirmation Form. ADLINK is not responsible for items not listed on the RMA Request & Confirmation Form.

3. Our repair service is not covered by ADLINK's guarantee in the following situations:

   ▶Damage caused by not following instructions in the User's Manual.

   ▶Damage caused by carelessness on the user's part during product transportation.

   ▶Damage caused by fire, earthquakes, floods, lightening, pollution, other acts of God, and/or incorrect usage of voltage transformers.

   ▶Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).

   ▶Damage caused by leakage of battery fluid during or after change of batteries by customer/user.

   ▶Damage from improper repair by unauthorized ADLINK technicians.

   ▶Products with altered and/or damaged serial numbers are not entitled to our service.

   ▶This warranty is not transferable or extendible.

   ▶Other categories not protected under our warranty.

4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.

If you have any further questions, please email our FAE staff: service@adlinktech.com.