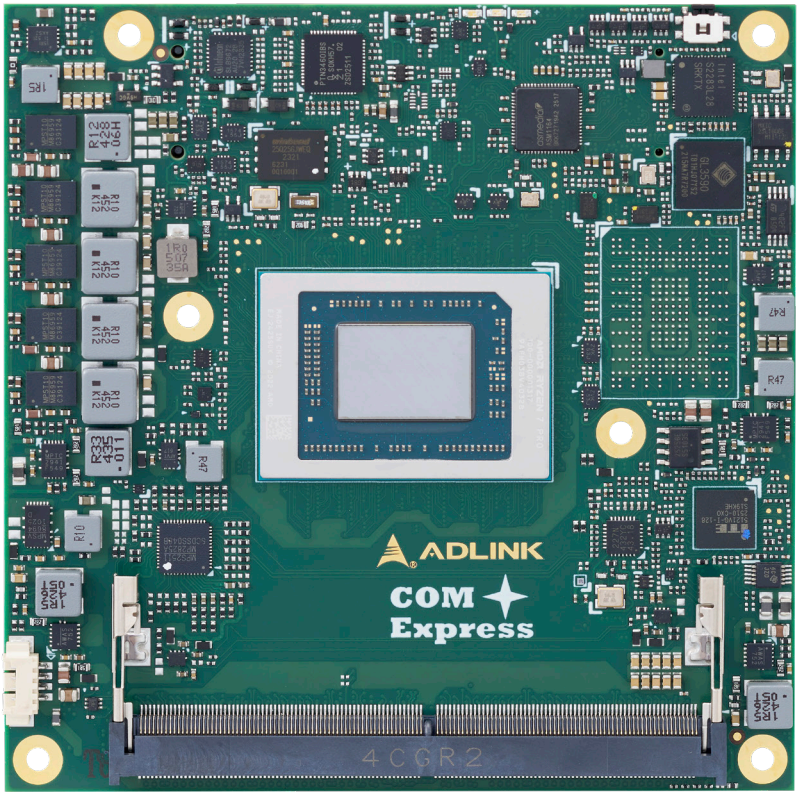
cExpress-R8

User's Guide

AMD



COM Express®

Revision: 1.1
Date: 2026-03-18
Part Number: 50M-72223-1010

ADLINK
LEADING EDGE COMPUTING

Revision History

Revision	Description	Date	Author
1.0	Initial release	2025-06-30	AL
1.1	Specifications, pinout and signal descriptions, and BIOS resources and setup updated	2026-03-18	AL

Note: This is an EA (Early Access) engineering manual; the content may not reflect the final product version.

Preface

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Safety Instructions

For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

Read these safety instructions carefully.

- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

Conventions

The following conventions may be used throughout this manual, denoting special levels of information

Note: This information adds clarity or specifics to text and illustrations.

Caution: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

Warning: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

Getting Service

Ask an Expert: https://www.adlinktech.com/en/Askanexpert

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1. Introduction

The cExpress-R8 is a COM.0 R3.1 compliant COM Express® Compact Size Type 6 module based on AMD Zen4 CPU and RDNA3 graphics architecture platform (SOC name "Ryzen Embedded 8000 series"). It features up to 8 Zen 4 CPU cores, 6 RDNA 3 graphics workgroups, and the first integrated XNDA™ architecture NPU delivering up to 16 TOPs (39 TOPs for total SOC), making it a powerful solution for demanding and diverse industrial computing workloads. It also supports AVX-512 to speed up CPU processing under heavy-load applications.

The cExpress-R8 supports up to 128GB DDR SO-DIMM memory with ECC functionality, operating at up to 5600MHz memory frequency across two memory channels. The default CPU TDP options are 28W/45W depending on the SKU, and configurable TDP (cTDP) can be adjusted via BIOS setting. These capabilities make it well-suited for mission-critical applications in resilient stationary and mobile edge use cases. With its powerful Integrated GPU and advanced NPU architecture, the module is ideal for a wide range of AI application scenarios.

The integrated AMD RDNA3 Graphics supports up to 6 workgroups (12 CUs). Graphics outputs include three DDI ports (supporting DP 2.1/UHBR10, HDMI 2.1 on Windows, and HDMI 2.0b on Linux), as well as one LVDS interface with resolution support up to 2K (optional eDP available). The three DDI ports can be configured via BIOS to output HDMI, DVI, or DisplayPort. The graphics video engine supports AV1 decode/encode, VP9, H.264, and H.265 decode (10-bit, up to 4K @ 60 FPS), as well as H.264/H.265 encode (8-bit, up to 4K @ 60 FPS and 8K encode with H.265). It includes features AMD APU/dGPU Smart Shift 2.0, which dynamically allocates power based on workload for optimal performance, and HDCP 2.3 support for secure transmission of video and image content. The cExpress-R8 is built with a powerful GPU and NPU that are specifically designed for customers with high-performance graphics processing requirements and AI acceleration applications.

Input/output features include up to eight PCIe Gen4 lanes, supporting up to 6 external high-speed PCIe devices, a single onboard 2.5Gigabit Ethernet port with optional Time Sensitive Network (TSN) support, up to four USB 3.2 Gen2/2.0 ports, four USB 2.0 ports, and four SATA 6 Gb/s ports. An optional onboard PCIe Gen4 NVMe SSD is offered on a project basis. The module also supports SMBus and I2C. It is equipped with SPI AMI EFI BIOS with CMOS backup, supporting embedded features such as a remote console, hardware monitor, and watchdog timer.

2. Specifications

2.1. Core System

CPU

AMD Zen4 Architecture Processor (formerly Ryzen 8000)

- AMD Ryzen™ 7 Pro 8845HS, 8C/16T, 24MB, 45W(35-54W cTDP), 6 WGPs
- AMD Ryzen™ 7 Pro 8840U, 8C/16T, 24MB, 28W(15-30W cTDP), 6 WGPs
- AMD Ryzen™ 5 Pro 8645HS, 6C/12T, 22MB, 45W(35-54W cTDP), 4 WGPs
- AMD Ryzen™ 5 Pro 8640U, 6C/12T, 22MB, 28W(15-30W cTDP), 4 WGPs

Supporting: AVX512 support

Note: Standard availability will be based on 45W and 28W SKUs. If you want to change the cTDP and or enable the TSN feature, please contact your local ADLINK representative for details.

Memory

Up to 128GB DDR5 SO-DIMM memory, up to 5600 MHz, ECC supported. Two SO-DIMM slots on module top side.

Embedded BIOS

AMI Aptio V UEFI with CMOS backup in a 32 MB SPI flash

2.2. Video

GPU

AMD Radeon RDNA3 graphics architecture with up to 6 workgroups (12 CUs)

Feature Support

- 4 independent and simultaneous combinations of DisplayPort/HDMI/LVDS/eDP (DP and HDMI can up to 4K @120Hz, or 8K@60Hz)
- eDP optional in place of LVDS, by project basis
- APU/dGPU Smart Shift 2.0 that efficient distribution of power usage.
- Support Variable Rate Shading, Ray Tracing Acceleration, 32b HDR Format.
- VCN4.0, H.265, H.264, AV1, VP9, JPEG HW decode with 8bit/10bit depth and up to 4K@ 60FPS.
- H.265, H.264, AV1 HW 8bit encode, up to 4K@ 60FPS.
- DirectX up to 12

Note: Availability of features is dependent on the operating system used (Windows 11 64-bit, Linux 64-bit).

2.2.1. Display Interface Support

LVDS: Single/dual channel 18/24-bit LVDS through eDP to LVDS IC, supports DE mode and Hsync/Vsync mode.
Max. resolution 1920x1200@60Hz in dual mode. Pixel clock frequency up to 112 MHz. VESA and JEIDA panel data formats supported.

eDP: eDP 1.5 up to 4 lane support, in place of LVDS (BOM option), up to 3840x2160@240Hz with DSC.

DDI x3: Digital Display Ports (DDI) support DisplayPort 2.1, HDMI 2.1 or DVI 1920x1200@60Hz.

2.3. Audio

AMD HD Audio DSP integrated

Located on carrier Express-BASE6 or Express-BASE6 R3.1 (ALC886 standard support)

2.4. Expansion Busses

1 PCI Express x8 Gen4: Lanes 16-23 (configurable to 1 x8 or 2 x4). Gen4 support dependent on carrier design (suitable for Graphic card, NVMe SSD).

8 PCI Express x1 Gen3: Lanes 0-3 (configurable to 4 x1, 2 x2, 1 x4, 1 x2 + 2 x1) and Lanes 4-7 (configurable to 4 x1, 2 x2, 1x4, 1 x2 + 2 x1)

Other: SMBus (system), I^2C (user), LPC bus (via eSPI to LPC bridge IC)

Note: 1. PCIe lanes 16-23 are recommended for use with discrete graphics and storage.

2.5. Ethernet

2.5GbE Intel® Ethernet Controller i226 Series (V or IT version)

Supports up to 2.5GbE and 1000/100/10 Mbit/s connections

IT version supports TSN feature on Linux OS, GbE0_SDP available if TSN support enabled

2.6. Multi I/O and Storage

USB

Up to 4x USB 3.2 Gen2/2.0/1.1 (USB3 0, 1 default support and USB3 2, 3 are BOM option by USB hub), 4x USB 2.0/1.1 (USB 4, 5, 6, 7)

SuperSpeedPlus, SuperSpeed, High-Speed, Full-Speed and Low-Speed USB signaling

Note: The carrier board must be designed for Gen2 operation.
USB 0, 1, 2, 3 are backward compatible with USB 2.0/1.1.

SATA

4x SATA 6Gb/s (SATA 0, 1, 2, 3, on board PCIe GEN4 NVMe SSD as BOM option)

Note: 1. For SATA 6Gb/s compatibility, it is strongly recommended to use a SATA re-driver on the carrier board.
2. SATA and NVMe SSD support only one option. If clients need to change the configuration, please contact your local representative.

GPIO ~~or SD~~

4 GPO and 4 GPI (GPI with interrupt)

On-board Storage

Soldered type PCIe NVMe SSD, available capacities: 128GB/256GB. Build option support by project basis

PCIe NVMe SSD co-lay with SATA bridge chip

Note: For the NVMe SSD build option, please contact your local ADLINK representative for details.

UART

Two UART interfaces SER0 and SER1 RX/TX on module

Console Redirection via COM 1 or COM 2 selectable in BIOS

Up to 4 serial ports supported by standard BIOS, including Super I/O on carrier board

COM Port	Description	IRQ	Address	Console Redirection Support
COM 1	Supported by module (SER0, A98/A99), via embedded controller	4	0x3F8	Yes
COM 2	Supported by module (SER1, A101/A102), via embedded controller	3	0x2F8	Yes
COM 3	Supported by Super I/O (W83627DHG) on carrier board	5	0x240	Yes
COM 4	Supported by Super I/O (W83627DHG) on carrier board	7	0x248	Yes

Note: SER0, SER1 from SoC HSUART are BOM option support by project basis

2.7. Trusted Platform Module (TPM)

Chipset: Infineon solution

Type: TPM 2.0 (SPI bus based)

2.8. SEMA Board controller

Supports voltage/current monitoring, power sequence debug, AT/ATX mode control, logistics and forensic information, flat panel control, general purpose I^2C, failsafe BIOS (dual BIOS, opt. support), watchdog timer, and fan control.

2.9. Debug

30-pin flat cable connector for use with DB-30 x86 debug module

Supports embedded controller access, SPI BIOS flashing, internal power rail test points, debug LEDs

2.10. Power

Power Modes: AT and ATX mode (AT mode startup controlled by SEMA Board Controller)

Standard Voltage Input: ATX: 12V±5% / 5Vsb ±5% or AT: 12V±5%
Wide Voltage Input: ATX: 8.5-20V, 5Vsb ±5% (TBD) or AT: 8.5-20V (TBD

Power Management: ACPI 6.0 compliant, Smart Battery support
Power States: C1-C6, S0, S1, S3 (TBD), S4, S5, S5 ECO mode (Wake-on-USB S3 (TBD)/S4, WoL S3/S4/S5)
ECO Mode support for deep S5 for 5Vsb power saving

Power Consumption
Please contact your ADLINK representative for the document "COM Express Module Power Consumption".

2.11. Mechanical and Environmental

Form Factor and specification

PICMG COM Express Rev 3.1 (COM.0 R3.1), Type 6, Compact size 95 x 95 mm

Operating Temperature

Standard 0°C to 60°C Storage: -20°C to 80°C

Humidity

5-90% RH operating, non-condensing, 5-95% RH storage (and operating with conformal coating)

Shock and Vibration

IEC 60068-2-64 and IEC-60068-2-27
MIL-STD-202F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D

HALT tested

Thermal Stress, Vibration Stress, Thermal Shock, and Combined Test

3. Block Diagram

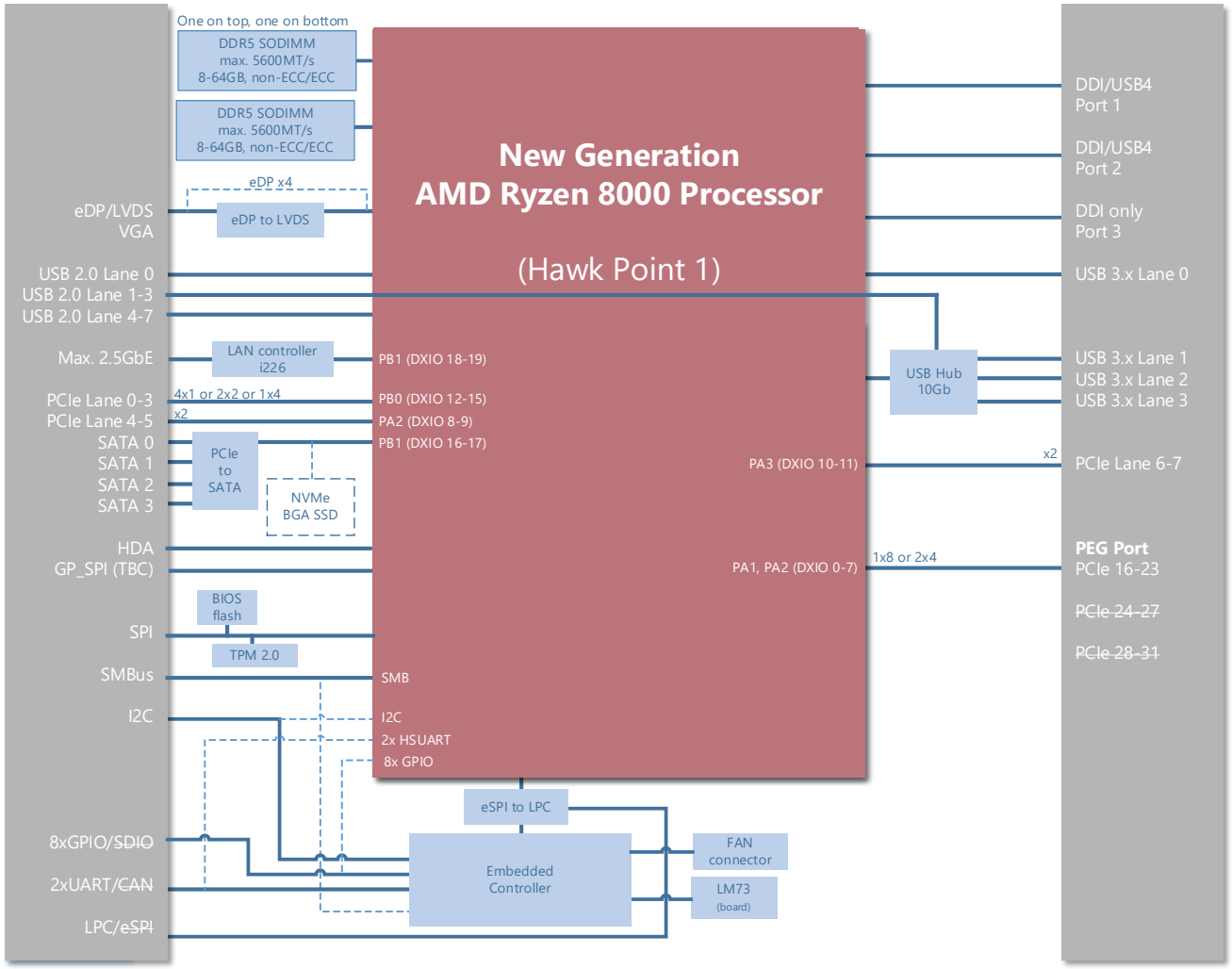

Figure 1 – Module function diagram

4. Pinout and Signal Descriptions (The pin definition will be updated before MP)

4.1. Pin Summary

The table below is a comprehensible list of all signal pins supported on the dual 220-pin COM Express connectors as defined for Type 6 in the PICMG COM.0 R3.1 specification. Signals described in the specification but not supported on the cExpress-R8 are marked with ~~strikethrough.~~

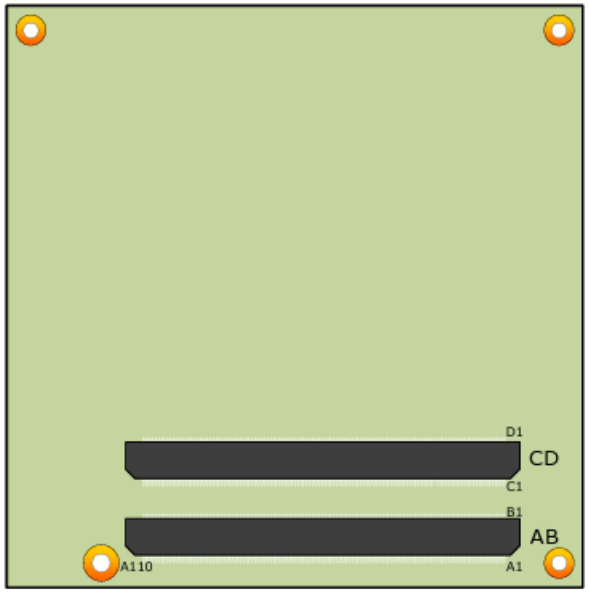

Figure 2 – Module rear side row and pin numbering

Row A			Row B			Row C			Row D	
A1	GND (FIXED)		B1	GND (FIXED)		C1	GND FIXED)		D1	GND FIXED)
A2	GBE0_MDI3-		B2	GBE0_ACT#		C2	GND		D2	GND
A3	GBE0_MDI3+		B3	LPC_FRAME#/ESPI_CS0#[1]		C3	USB_SSRX0-		D3	USB_SSTX0-
A4	GBE0_LINK_MID#		B4	LPC_AD0/ESPI_IO_0[1]		C4	USB_SSRX0+		D4	USB_SSTX0+
A5	GBE0_LINK_MAX#		B5	LPC_AD1/ESPI_IO_1[1]		C5	GND		D5	GND
A6	GBE0_MDI2-		B6	LPC_AD2/ESPI_IO_2[1]		C6	USB_SSRX1-		D6	USB_SSTX1-
A7	GBE0_MDI2+		B7	LPC_AD3/ESPI_IO_3[1]		C7	USB_SSRX1+		D7	USB_SSTX1+
A8	GBE0_LINK#		B8	~~LPC_DRQ0#/ESPI_ALERT0#~~		C8	GND		D8	GND
A9	GBE0_MDI1-		B9	~~LPC_DRQ1#/ESPI_ALERT1#~~		C9	USB_SSRX2-		D9	USB_SSTX2-
A10	GBE0_MDI1+		B10	LPC_CLK/ESPI_CK[1]		C10	USB_SSRX2+		D10	USB_SSTX2+
A11	GND (FIXED)		B11	GND (FIXED)		C11	GND (FIXED)		D11	GND (FIXED)
A12	GBE0_MDI0-		B12	PWRBTN#		C12	USB_SSRX3-		D12	USB_SSTX3-
A13	GBE0_MDI0+		B13	SMB_CK		C13	USB_SSRX3+		D13	USB_SSTX3+
A14	GBE0_CTREF		B14	SMB_DAT		C14	GND		D14	GND
A15	SUS_S3#		B15	SMB_ALERT#		C15	USB4_1_LSTX[1]		D15	DDI1_CTRLCLK_AUX+ /USB4_1_AUX+[1]
A16	SATA0_TX+		B16	SATA1_TX+		C16	USB4_1_LSRX[1]		D16	DDI1_CTRLDATA_AUX- /USB4_1_AUX-[1]
A17	SATA0_TX-		B17	SATA1_TX-		C17	USB4_RT_ENA[1]		D17	USB4_PD_I2C_ALERT#[1]
A18	SUS_S4#		B18	SUS_STAT#/ESPI_RESET#[1]		C18	GND		D18	PMCALERT#[1]
A19	SATA0_RX+		B19	SATA1_RX+		C19	PCIE_RX6+[1]		D19	PCIE_TX6+
A20	SATA0_RX-		B20	SATA1_RX-		C20	PCIE_RX6-[1]		D20	PCIE_TX6-
A21	GND (FIXED)		B21	GND (FIXED)		C21	GND (FIXED)		D21	GND (FIXED)
A22	SATA2_TX+		B22	SATA3_TX+		C22	PCIE_RX7+[1]		D22	PCIE_TX7+
A23	SATA2_TX-		B23	SATA3_TX-		C23	PCIE_RX7-[1]		D23	PCIE_TX7-
A24	SUS_S5#		B24	PWR_OK		C24	DDI1_HPD		D24	GND
A25	SATA2_RX+		B25	SATA3_RX+		C25	SML0_CLK[1]		D25	GND
A26	SATA2_RX-		B26	SATA3_RX-		C26	SML0_DAT[1]		D26	DDI1_PAIR0+ /USB4_1_SSTX0+[1]
A27	BATLOW#		B27	WDT		C27	SML1_CLK[1]		D27	DDI1_PAIR0- /USB4_1_SSTX0-[1]
A28	(S)ATA_ACT#		B28	~~HDA_SDIN2~~/SNDW0_CLK[2]		C28	SML1_DAT[1]		D28	GND
A29	HDA_SYNC		B29	HDA_SDIN1/SNDW0_DAT[2]		C29	USB4_PD_I2C_CLK[1]		D29	DDI1_PAIR1+ /USB4_1_SSRX0+[1]
A30	HDA_RST#		B30	HDA_SDIN0		C30	USB4_PD_I2C_DAT[1]		D30	DDI1_PAIR1- /USB4_1_SSRX0-[1]

Row A			Row B			Row C			Row D	
A31	GND (FIXED)		B31	GND (FIXED)		C31	GND (FIXED)		D31	GND (FIXED)
A32	HDA_BITCLK		B32	SPKR		C32	DDI2_CTRLCLK_AUX+ /USB4_2_AUX+[1]		D32	DDI1_PAIR2+ /USB4_1_SSTX1+[1]
A33	HDA_SDOUT		B33	I2C_CK		C33	DDI2_CTRLDATA_AUX- /USB4_2_AUX-[1]		D33	DDI1_PAIR2- /USB4_1_SSTX1-[1]
A34	BIOS_DIS0#/ESPI_SAFS[1]		B34	I2C_DAT		C34	DDI2_DDC_AUX_SEL		D34	DDI1_DDC_AUX_SEL
A35	THRMTRIP#		B35	THRM#		C35	USB4_2_LSTX[1]		D35	USB4_2_LSRX[1]
A36	USB6-		B36	USB7-		C36	DDI3_CTRLCLK_AUX+		D36	DDI1_PAIR3+ /USB4_1_SSRX1+[1]
A37	USB6+		B37	USB7+		C37	DDI3_CTRLDATA_AUX-		D37	DDI1_PAIR3- /USB4_1_SSRX1-[1]
A38	USB_6_7_OC#		B38	USB_4_5_OC#		C38	DDI3_DDC_AUX_SEL		D38	GND
A39	USB4-		B39	USB5-		C39	DDI3_PAIR0+		D39	DDI2_PAIR0+ /USB4_2_SSTX0+[1]
A40	USB4+		B40	USB5+		C40	DDI3_PAIR0-		D40	DDI2_PAIR0- /USB4_2_SSTX0-[1]
A41	GND (FIXED)		B41	GND (FIXED)		C41	GND (FIXED)		D41	GND (FIXED)
A42	USB2-		B42	USB3-		C42	DDI3_PAIR1+		D42	DDI2_PAIR1+ /USB4_2_SSRX0+[1]
A43	USB2+		B43	USB3+		C43	DDI3_PAIR1-		D43	DDI2_PAIR1- /USB4_2_SSRX0-[1]
A44	USB_2_3_OC#		B44	USB_0_1_OC#		C44	DDI3_HPD		D44	DDI2_HPD
A45	USB0-		B45	USB1-		C45	GP_SPI_CS#[2]		D45	GND
A46	USB0+		B46	USB1+		C46	DDI3_PAIR2+		D46	DDI2_PAIR2+ /USB4_2_SSTX1+[1]
A47	VCC_RTC		B47	ESPI_EN#[1]		C47	DDI3_PAIR2-		D47	DDI2_PAIR2- /USB4_2_SSTX1-[1]
A48	~~RSMRST_OUT#~~		B48	~~USB0_HOST_PRSNT~~		C48	RSVD		D48	GND
A49	GBE0_SDP[1]		B49	SYS_RESET#		C49	DDI3_PAIR3+		D49	DDI2_PAIR3+ /USB4_2_SSRX1+[1]
A50	LPC_SERIRQ/ESPI_CS1#[1]		B50	CB_RESET#		C50	DDI3_PAIR3-		D50	DDI2_PAIR3- /USB4_2_SSRX1-[1]
A51	GND (FIXED)		B51	GND (FIXED)		C51	GND (FIXED)		D51	GND (FIXED)
A52	PCIE_TX5+[1]		B52	PCIE_RX5+[1]		C52	PEG_RX0+		D52	PEG_TX0+
A53	PCIE_TX5-[1]		B53	PCIE_RX5-[1]		C53	PEG_RX0-		D53	PEG_TX0-
A54	GPI0		B54	GPO1		C54	TYPE0#		D54	PEG_LANE_RV#
A55	PCIE_TX4+		B55	PCIE_RX4+		C55	PEG_RX1+		D55	PEG_TX1+

Row A			Row B			Row C			Row D	
A56	PCIE_TX4-		B56	PCIE_RX4-		C56	PEG_RX1-		D56	PEG_TX1-
A57	GND		B57	GPO2		C57	TYPE1#		D57	TYPE2#
A58	PCIE_TX3+		B58	PCIE_RX3+		C58	PEG_RX2+		D58	PEG_TX2+
A59	PCIE_TX3-		B59	PCIE_RX3-		C59	PEG_RX2-		D59	PEG_TX2-
A60	GND (FIXED)		B60	GND (FIXED)		C60	GND (FIXED)		D60	GND (FIXED)
A61	PCIE_TX2+		B61	PCIE_RX2+		C61	PEG_RX3+		D61	PEG_TX3+
A62	PCIE_TX2-		B62	PCIE_RX2-		C62	PEG_RX3-		D62	PEG_TX3-
A63	GPI1		B63	GPO3		C63	GND		D63	GND
A64	PCIE_TX1+		B64	PCIE_RX1+		C64	GND		D64	GND
A65	PCIE_TX1-		B65	PCIE_RX1-		C65	PEG_RX4+		D65	PEG_TX4+
A66	GND		B66	WAKE0#		C66	PEG_RX4-		D66	PEG_TX4-
A67	GPI2		B67	WAKE1#		C67	~~RAPID_SHUTDOWN~~		D67	GND
A68	PCIE_TX0+		B68	PCIE_RX0+		C68	PEG_RX5+		D68	PEG_TX5+
A69	PCIE_TX0-		B69	PCIE_RX0-		C69	PEG_RX5-		D69	PEG_TX5-
A70	GND (FIXED)		B70	GND (FIXED)		C70	GND (FIXED)		D70	GND (FIXED)
A71	LVDS_A0+ / eDP_TX2+[1]		B71	LVDS_B0+		C71	PEG_RX6+		D71	PEG_TX6+
A72	LVDS_A0- / eDP_TX2-[1]		B72	LVDS_B0-		C72	PEG_RX6-		D72	PEG_TX6-
A73	LVDS_A1+ / eDP_TX1+[1]		B73	LVDS_B1+		C73	GND		D73	GND
A74	LVDS_A1- / eDP_TX1-[1]		B74	LVDS_B1-		C74	PEG_RX7+		D74	PEG_TX7+
A75	LVDS_A2+ / eDP_TX0+[1]		B75	LVDS_B2+		C75	PEG_RX7-		D75	PEG_TX7-
A76	LVDS_A2- / eDP_TX0-[1]		B76	LVDS_B2-		C76	GND		D76	GND
A77	LVDS_VDD_EN / eDP_VDD_EN[1]		B77	LVDS_B3+		C77	GND		D77	GND
A78	LVDS_A3+		B78	LVDS_B3-		C78	PEG_RX8+		D78	PEG_TX8+
A79	LVDS_A3-		B79	LVDS_BKLT_EN		C79	PEG_RX8-		D79	PEG_TX8-
A80	GND (FIXED)		B80	GND (FIXED)		C80	GND (FIXED)		D80	GND (FIXED)
A81	LVDS_A_CK+ / eDP_TX3+[1]		B81	LVDS_B_CK+		C81	PEG_RX9+		D81	PEG_TX9+
A82	LVDS_A_CK- / eDP_TX3-[1]		B82	LVDS_B_CK-		C82	PEG_RX9-		D82	PEG_TX9-
A83	LVDS_I2C_CK / eDP_AUX+[1]		B83	LVDS_BKLT_CTRL / eDP_BKLT_CTRL[1]		C83	GND		D83	GND
A84	LVDS_I2C_DAT / eDP_AUX-[1]		B84	VCC_5V_SBY		C84	GND		D84	GND
A85	GPI3		B85	VCC_5V_SBY		C85	PEG_RX10+		D85	PEG_TX10+
A86	GP_SPI_MOSI[2]		B86	VCC_5V_SBY		C86	PEG_RX10-		D86	PEG_TX10-
A87	eDP_HPD		B87	VCC_5V_SBY		C87	GND		D87	GND
A88	PCIE_CK_REF+		B88	BIOS_DIS1#		C88	PEG_RX11+		D88	PEG_TX11+
A89	PCIE_CK_REF-		B89	VGA_RED[1]		C89	PEG_RX11-		D89	PEG_TX11-
A90	GND (FIXED)		B90	GND (FIXED)		C90	GND (FIXED)		D90	GND (FIXED)
A91	SPI_POWER		B91	VGA_GRN[1]		C91	PEG_RX12+		D91	PEG_TX12+
A92	SPI_MISO		B92	VGA_BLU[1]		C92	PEG_RX12-		D92	PEG_TX12-

Row A			Row B			Row C			Row D	
A93	GPO0		B93	VGA_HSYNC[1]		C93	GND		D93	GND
A94	SPI_CLK		B94	VGA_VSYNC[1]		C94	PEG_RX13+		D94	PEG_TX13+
A95	SPI_MOSI		B95	VGA_I2C_CK[1]		C95	PEG_RX13-		D95	PEG_TX13-
A96	TPM_PP		B96	VGA_I2C_DAT[1]		C96	GND		D96	GND
A97	TYPE10#		B97	SPI_CS#		C97	GND		D97	GND
A98	SER0_TX		B98	GP_SPI_MISO[2]		C98	PEG_RX14+		D98	PEG_TX14+
A99	SER0_RX		B99	GP_SPI_CK[2]		C99	PEG_RX14-		D99	PEG_TX14-
A100	GND (FIXED)		B100	GND (FIXED)		C100	GND (FIXED)		D100	GND (FIXED)
A101	SER1_TX~~/CAN_TX~~		B101	FAN_PWMOUT		C101	PEG_RX15+		D101	PEG_TX15+
A102	SER1_RX~~/CAN_RX~~		B102	FAN_TACHIN		C102	PEG_RX15-		D102	PEG_TX15-
A103	LID#		B103	SLEEP#		C103	GND		D103	GND
A104	VCC_12V		B104	VCC_12V		C104	VCC_12V		D104	VCC_12V
A105	VCC_12V		B105	VCC_12V		C105	VCC_12V		D105	VCC_12V
A106	VCC_12V		B106	VCC_12V		C106	VCC_12V		D106	VCC_12V[1]
A107	VCC_12V		B107	VCC_12V		C107	VCC_12V		D107	VCC_12V
A108	VCC_12V		B108	VCC_12V		C108	VCC_12V		D108	VCC_12V
A109	VCC_12V		B109	VCC_12V		C109	VCC_12V		D109	VCC_12V
A110	GND (FIXED)		B110	GND (FIXED)		C110	GND (FIXED)		D110	GND (FIXED)

Note: ~~Strike-through~~ entries are not supported functions on this product.

4.2. Signal Terminology Descriptions

Meaning of the terms used for signal description tables

Term	Description
I	Input to the module
O	Output from the module
I/O	Bi-directional Input / Output
OD	Open drain output from the module
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I/O $3.3V_{SB}$	Input or output 3.3V tolerant active in standby state
DDC	Display Data Channel
PCIE	PCI Express compatible differential signal
PEG	PCI Express Graphics
SATA	Serial ATA specification Revision 2.6 and 3
LVDS	Low Voltage Differential Signal - 330 mV nominal; 450 mV maximum differential signal
P	Power Input / Output
REF	Reference voltage output. May be sourced from a Module power plane.
PDS	Pull-down strap. A Module output pin that is either tied to GND or is not connected. Used to signal Module capabilities to the Carrier Board.
PU	PU (pull-up) resistor on module
PD	PD (pull-down) resistor on module

4.3. AB Connector Signal Descriptions

4.3.1. Audio

Name	Pin #	Description	I/O	PU / PD	Comment
AC_RST# / HDA_RST#	A30	Reset output to CODEC, active low.	O 3.3VSB		
AC_SYNC / HDA_SYNC	A29	Sample-synchronization signal to the CODEC(s).	O 3.3VSB		PCH internal PD 20Kohm
AC_BITCLK / HDA_BITCLK	A32	Serial data clock generated by the external CODEC(s).	I/O 3.3VSB		
AC_SDOUT / HDA_SDOUT	A33	Serial TDM data output to the CODEC.	O 3.3VSB		PCH internal PD 20Kohm
AC_SDIN[2:0] / HDA_SDIN[2:0]	~~B28~~ B29 B30	Serial TDM data inputs from up to 3 CODECs.	I/O 3.3VSB		PCH internal PD 20Kohm AC_SDNI2/HDA_SDIN2 not supported

4.3.2. Analog VGA

Name	Pin #	Description	I/O	PU / PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	
VGA_GRN	B91	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3V		
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3V		
VGA_I2C_CK	B95	DDC clock line (I^2C port dedicated to identifying VGA monitor capabilities)	I/O OD 3.3V	PU 2k2 3.3V	
VGA_I2C_DAT	B96	DDC data line.	I/O OD 3.3V	PU 2k2 3.3V	

Note: VGA is BOM option support (in place of DDI 3) by project basis

4.3.3. LVDS or eDP

The module default supports a single- or dual-channel LVDS display panel with up to 24-bit color. A BOM option that removes the eDP-to-LVDS bridge IC and outputs the eDP signals directly is available. eDP vs LVDS pin mapping is shown below.

Pin #	LVDS mode	eDP mode
A71 A72	LVDS_A0+ LVDS_A0-	eDP_TX2+ eDP_TX2-
A73 A74	LVDS_A1+ LVDS_A1-	eDP_TX1+ eDP_TX1-
A75 A76	LVDS_A2+ LVDS_A2-	eDP_TX0+ eDP_TX0-
A78 A79	LVDS_A3+ LVDS_A3-	- -
A81 A82	LVDS_A_CK+ LVDS_A_CK-	eDP_TX3+ eDP_TX3-
B71 B72 B73 B74 B75 B76 B77 B78	LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	- - - - - - - -
B81 B82	LVDS_B_CK+ LVDS_B_CK-	- -
A77	LVDS_VDD_EN	eDP_VDD_EN
B79	LVDS_BKLT_EN	eDP_BKLT_EN
B83	LVDS_BKLT_CTRL	eDP_BKLT_CTRL
A83	LVDS_I2C_CK	eDP_AUX+
A84	LVDS_I2C_DAT	eDP_AUX-
A87	-	eDP_HPD

Note: LVDS is the default mode, and eDP is available as a BOM option.

4.3.3.1. Single/Dual Channel LVDS (default)

Name	Pin #	Description	I/O	PU / PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 100K	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V	PD 100K	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V	PD 100K	
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.	O 3.3V	PU 2k2 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	

4.3.3.2. 4-Lane eDP

Name	Pin #	Description	I/O	PU / PD	Comment
eDP_TX3+ eDP_TX3- eDP_TX2+ eDP_TX2- eDP_TX1+ eDP_TX1- eDP_TX0+ eDP_TX0-	A81 A82 A71 A72 A73 A74 A75 A76	eDP differential pairs	O PCIE		AC coupled off module
eDP_VDD_EN	A77	eDP power enable	O 3.3V	PD 100K	
eDP_BKLT_EN	B79	eDP backlight enable	O 3.3V	PD 100K	
eDP_BKLT_CTRL	B83	eDP backlight brightness control	O 3.3V	PD 100K	
eDP_AUX+	A83	eDP AUX+	I/O PCIE		AC coupled off module
eDP_AUX-	A84	eDP AUX-	I/O PCIE		AC coupled off module
eDP_HPD	A87	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	PD 100K on this pin when eDP is supported

4.3.4. Gigabit Ethernet

Name	Pin #	Description	I/O	PU / PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: **1000 / 100 / 10** MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	I/O Analog		Twisted pair signals for external transformer.
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	OD 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	OD 3.3VSB		
GBE0_LINK100# *	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	OD 3.3VSB		
GBE0_LINK1000# *	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	OD 3.3VSB		
~~GBE0_CTREF~~	~~A14~~	~~Reference voltage for Carrier Board Ethernet channel 1 and 2 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be 250 mA or less.~~	~~REF~~ ~~GND min~~ ~~3.3V max~~		Not supported
GBE0_SDP	A49	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as 1pps signal.	IO 3.3VSB	GBE0_SDP	Depends on the selection of LAN controller. i225-IT support this pin

Note: This product supports up to 2.5GbE. The LAN LED behavior is optimized for a maximum 2.5GbE speed.
GBE0_LINK1000# will be active to indicate a 2.5GbE connection.
GBE0_LINK100# will be active to indicate a 1GbE connection or lower.
GBE0_ACT# and GBE0_LINK# share the same source from the LAN controller.
For 100Mbit/sec and 10Mbit/sec speeds, the LAN LED will be OFF.

4.3.5. SATA

Name	Pin #	Description	I/O	PU / PD	Comment
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		AC coupled on Module
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		AC coupled on Module
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2, Receive Input differential pair.	I SATA		AC coupled on Module
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3, Receive Input differential pair.	I SATA		AC coupled on Module
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	O 3.3V	PU 10K 3.3V	AC coupled on Module

4.3.5.1. PCH HSIO Lane Assignments

Name	HSIO name on SOC	Comment
SATA0	GPP 18/19	Via PCIe to SATA bridge chip
SATA1	GPP 18/19	Via PCIe to SATA bridge chip
SATA2	GPP 18/19	Via PCIe to SATA bridge chip
SATA3	GPP 18/19	Via PCIe to SATA bridge chip

4.3.6. PCI Express

Name	Pin #	Description	I/O	PU / PD	Comment
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		

4.3.6.1. PCH HSIO Lane Assignments

Name	HSIO name on SOC / Switch IC	Comment
PCIE0	GPP 12	
PCIE1	GPP 13	
PCIE2	GPP 14	
PCIE3	GPP 15	
PCIE4	GPP 8	
PCIE5	GPP 9	
PCIE6	GPP 10	
PCIE7	GPP 12	

4.3.7. LPC Bus

Name	Pin #	Description	I/O	PU / PD	Comment
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	B4 B5 B6 B7	LPC multiplexed address, command and data bus	I/O 3.3VSB		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3VSB		
LPC_DRQ0# LPC_DRQ1#	B8 B9	LPC serial DMA request	I 3.3V		Not connected
LPC_SERIRQ	A50	LPC serial interrupt	I/O 3.3VSB	PU 8.2K 3.3VSB	
LPC_CLK	B10	LPC clock output –33MHz nominal	O 3.3VSB		The LPC_CLK frequency is 24MHz on this platform

Note: LPC Bus is supported by an eSPI to LPC bridge IC.

4.3.8. USB

Name	Pin #	Description	I/O	PU / PD	Comment
USB0+ USB0-	A46 A45	USB differential data pairs for Port 0	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB1+ USB1-	B46 B45	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB2+ USB2-	A43 A42	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB3+ USB3-	B43 B42	USB differential data pairs for Port 2	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB4+ USB4-	A40 A39	USB differential data pairs for Port 3	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB5+ USB5-	B40 B39	USB differential data pairs for Port 4	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB6+ USB6-	A37 A36	USB differential data pairs for Port 5	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB7+ USB7-	B37 B37	USB differential data pairs for Port 6	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on the carrier
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on the carrier
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on the carrier
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on the carrier
USB0_HOST_PRSNT	B48	Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present.	I 3.3VSB		Not supported

***Note**: A pull-up for this line shall be present on the module. An open-drain driver from a USB current monitor on the carrier board may drive this line low.

4.3.9. SPI Bus (BIOS only)

Name	Pin #	Description	I/O	PU / PD	Comment
SPI_CS#	B97	Chip select for the Carrier Board SPI BIOS Flash.	O 3.3VSB	PU 10K 3.3VSB	
SPI_MISO	A92	Data in to the module from the carrier board SPI BIOS flash.	I 3.3VSB		
SPI_MOSI	A95	Data out from the module to the carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from the module to the carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power supply for the Carrier Board SPI – sourced from the Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. The carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier.	O P 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I	PU 10K 3.3VSB	The carrier shall pull to GND or leave unconnected.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I	PU 10K 3.3VSB	The carrier shall pull to GND or leave unconnected

4.3.10. Miscellaneous

Name	Pin #	Description	I/O	PU / PD	Comment
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3V		
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V	PU 10K 3.3V	
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3VSB		
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3VSB	PU 100K 3.3VSB	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3V		There shall be PD on carrier board
FAN_TACHIN	B102	Fan tachometer input for a fan with a two-pulse output.	I OD 3.3V	PU 47K 3.3V	
TPM_PP	A96	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V	PD 100K	PD only when TPM on module. Modules implementing a TPM shall pull down

4.3.11. SMBus

Name	Pin #	Description	I/O	PU / PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line. Power sourced through 3.3V standby rail and main power rails.	I/O OD 3.3VSB	PU 4.7K 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line. Power sourced through 3.3V standby rail and main power rails.	I/O OD 3.3VSB	PU 4.7K 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 3.3V standby rail and main power rails.	I 3.3VSB	PU 10K 3.3VSB	

4.3.12. I^2C Bus

Name	Pin #	Description	I/O	PU / PD	Comment
I2C_CK	B33	General purpose I^2C port clock output/input	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Source SEMA BMC as default (chipset by BOM option)
I2C_DAT	B34	General purpose I^2C port data I/O line	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Source SEMA BMC as default (chipset by BOM option)

4.3.13. General Purpose I/O (GPIO)

Name	Pin #	Description	I/O	PU / PD	Comment
GPO[0]	A93	General purpose output pins.	O 3.3V	PD 10K	After hardware RESET output low
GPO[1]	B54	General purpose output pins.	O 3.3V	PD 10K	After hardware RESET output low
GPO[2]	B57	General purpose output pins.	O 3.3V	PD 10K	After hardware RESET output low
GPO[3]	B63	General purpose output pins.	O 3.3V	PD 10K	After hardware RESET output low
GPI[0]	A54	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[1]	A63	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[2]	A67	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[3]	A85	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	

4.3.14. Serial Interface Signals

Name	Pin #	Description	I/O	PU / PD	Comment
SER0_TX	A98	General purpose serial port transmitter	O CMOS 3.3V		Power rail tolerance 5V, 12V There shall be PD on carrier board
SER0_RX	A99	General purpose serial port receiver	I CMOS 3.3V	PU 10K 3.3V	Power rail tolerance 5V, 12V
SER1_TX	A101	General purpose serial port transmitter	O CMOS 3.3V		Power rail tolerance 5V, 12V There shall be PD on carrier board
SER1_RX	A102	General purpose serial port receiver	I CMOS 3.3V	PU 10K 3.3V	Power rail tolerance 5V, 12V

4.3.15. Power and System Management

Name	Pin #	Description	I/O	PU / PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge.	I 3.3VSB	PU 10K 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low request for module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.	I 3.3VSB	PU 10K 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow carrier-based FPGAs or other configurable devices time to be programmed.	I 3.3VSB	PU 10K 3.3VSB	Should have weak pull up.
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON") may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB	PD 100K	
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB	PD 100K	
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB	PD 100K	
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10K 3.3VSB	
WAKE1#	B67	General purpose wake-up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 10K 3.3VSB	Connect to WAKE 0#
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low or may be used to signal some other external power-management event.	I 3.3VSB	PU 10K 3.3VSB	
LID#	A103	LID button. Low active signal used by the ACPI operating system for a LID switch.	I OD 3.3VSB	PU 47K 3.3VSB	Emulated on GPIO (BIOS)
SLEEP#	B103	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I OD 3.3VSB	PU 47K 3.3VSB	Emulated on GPIO (BIOS)
RAPID_ SHUTDOWN	C67	~~Trigger for Rapid Shutdown. Must be driven to 5V though a <=50-ohm source impedance for ≥ 20 µs.~~	I CMOS 5VSB		Not supported

4.3.16. Power and Ground

Name	Pin #	Description	I/O	PU / PD	Comment
VCC_12V	A104, A105, A106, A107, A108, A109, B104, B105, B106, B107, B109	Primary power input supports a wide range input of 5 — 20V. All available VCC_12V pins on the connector(s) shall be used.	P		8.5-20 V
VCC_5V_SBY	B84, B85, B86, B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		5Vsb ±5%
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path.	P		

4.4. CD Connector Signal Descriptions

4.4.1. USB 3.0 Extensions

Name	Pin #	Description	I/O	PU / PD	Comment
USB_SSRX0- USB_SSRX0+	C3 C4	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB0	I PCIE		AC coupled off module
USB_SSTX0- USB_SSTX0+	D3 D4	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB0	O PCIE		AC coupled on module
USB_SSRX1- USB_SSRX1+	C6 C7	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB1	I PCIE		AC coupled off module
USB_SSTX1- USB_SSTX1+	D6 D7	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB1	O PCIE		AC coupled on module
USB_SSRX2- USB_SSRX2+	C9 C10	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB2	I PCIE		AC coupled off module
USB_SSTX2- USB_SSTX2+	D9 D10	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB2	O PCIE		AC coupled on module
USB_SSRX3- USB_SSRX3+	C12 C13	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB3	I PCIE		AC coupled off module
USB_SSTX3- USB_SSTX3+	D12 D13	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB3	O PCIE		AC coupled on module

4.4.1.1. USB Root Segmentation

All USB interfaces are derived from the xHCI controller.

4.4.2. PCI Express

Name	Pin #	Description	I/O	PU / PD	Comment
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair.	I PCIE		AC coupled off Module

4.4.2.1. PCH HSIO Lane Assignments

Refer to Section 4.3.6.1 PCH HSIO Lane Assignments on page 35.

4.4.3. DDI1 Port

Name	Pin #	DisplayPort (DP)	HDMI
DDI1_PAIR0+ DDI1_PAIR0-	D26 D27	DP1_LANE0+ DP1_LANE0-	TMDS1_DATA2+ TMDS1_DATA2-
DDI1_PAIR1+ DDI1_PAIR1-	D29 D30	DP1_LANE1+ DP1_LANE1-	TMDS1_DATA1+ TMDS1_DATA1-
DDI1_PAIR2+ DDI1_PAIR2-	D32 D33	DP1_LANE2+ DP1_LANE2-	TMDS1_DATA0+ TMDS1_DATA0-
DDI1_PAIR3+ DDI1_PAIR3-	D36 D37	DP1_LANE3+ DP1_LANE3-	TMDS1_CLK+ TMDS1_CLK-
DDI1_PAIR4+ DDI1_PAIR4-	C25 C26	-	-
DDI1_PAIR5+ DDI1_PAIR5-	C29 C30	-	-
DDI1_PAIR6+ DDI1_PAIR6-	C15 C16	-	-
DDI1_HPD	C24	DP1_HPD	HDMI1_HPD
DDI1_CTRLCLK_AUX+	D15	DP1_AUX+	HMDI1_CTRLCLK
DDI1_CTRLCLK_AUX-	D16	DP1_AUX-	HMDI1_CTRLDATA
DDI1_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	DDI1_DDC_AUX_SEL

Note: Dual Mode (HDMI and DisplayPort on the same pins) implementations may be realized. This is desirable for SOCs that natively implement this capability. With such SOCs, the primary Dual Mode implementation challenge is that the HDMI_CTRL_DAT and HDMI_CTRL_CK lines are DC coupled, but the DP_AUX+ /- pair must be AC coupled. A set of FET switches is usually used to sort this out. The FET gates can be controlled by the AUX_SEL pin function.

4.4.3.1. DisplayPort (DP) Mode

Name	Pin #	Description	I/O	PU / PD	Comment
DP1_LANE0+ DP1_LANE0- DP1_LANE1+ DP1_LANE1- DP1_LANE2+ DP1_LANE2- DP1_LANE3+ DP1_LANE3-	D26 D27 D29 D30 D32 D33 D36 D37	DP Port 1, differential pair data lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
DP1_HPD	C24	DP Port 1, detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	Module must tolerate high level in stand-by mode. The carrier board shall include a blocking FET on DP1_HPD to prevent back-drive current from damaging the Module.
DP1_AUX+	D15	DP Port 1, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PD 100K	AC coupled on Module
DP1_AUX-	D16	DP Port 1, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PU 100K	AC coupled on Module
DDI1_DDC_AUX_SEL	D34	Strapping Signal to select HDMI or DP output 1M pull-down on the module and floating on the carrier that enables DisplayPort mode	I 3.3V	PD 1M	DP mode enabled

4.4.3.2. HDMI Mode

Name	Pin #	Description	I/O	PU / PD	Comment
TMDS1_DATA2+ TMDS1_DATA2- TMDS1_DATA1+ TMDS1_DATA1- TMDS1_DATA0+ TMDS1_DATA0-	D26 D27 D29 D30 D32 D33	HDMI / DVI Port, Differential Pair Data Lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
TMDS1_CLK+ TMDS1_CLK-	D36 D37	HDMI Port, Differential Pair Clock Lines			
HDMI_HPD	C24	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	
HDMI1_CTRLCLK	D15	I2C_CLK Line for HDMI	I/O PCIE	PU 2.2K	AC couple on Module
HDMI1_CTRLDATA	D16	I2C_DAT Line for HDMI	I/O PCIE	PU 2.2K	AC couple on Module
DDI1_DDC_AUX_SEL	D34	Strapping Signal to select HDMI or DP output 1M pull-down on the module and floating on the carrier that enables DisplayPort mode	I 3.3V	PD 1M	HDMI mode enabled

4.4.4. DDI2 Port

Name	Pin #	DisplayPort (DP)	HDMI
DDI2_PAIR0+ DDI2_PAIR0-	D39 D40	DP2_LANE0+ DP2_LANE0-	TMDS2_DATA2+ TMDS2_DATA2-
DDI2_PAIR1+ DDI2_PAIR1-	D42 D43	DP2_LANE1+ DP2_LANE1-	TMDS2_DATA1+ TMDS2_DATA1-
DDI2_PAIR2+ DDI2_PAIR2-	D46 D47	DP2_LANE2+ DP2_LANE2-	TMDS2_DATA0+ TMDS2_DATA0-
DDI2_PAIR3+ DDI2_PAIR3-	D49 D50	DP2_LANE3+ DP2_LANE3-	TMDS2_CLK+ TMDS2_CLK-
DDI2_HPD	D44	DP2_HPD	HDMI2_HPD
DDI2_CTRLCLK_AUX+	C32	DP2_AUX+	HMDI2_CTRLCLK
DDI2_CTRLCLK_AUX-	C33	DP2_AUX-	HMDI2_CTRLDATA
DDI2_DDC_AUX_SEL	C34	DDI2_DDC_AUX_SEL	DDI2_DDC_AUX_SEL

Note:
Dual Mode (HDMI and DisplayPort on the same pins) implementations may be realized. This is desirable for SOCs that natively implement this capability. With such SOCs, the primary Dual Mode implementation challenge is that the HDMI_CTRL_DAT and HDMI_CTRL_CK lines are DC coupled, but the DP_AUX+ /- pair must be AC coupled. A set of FET switches is usually used to sort this out. The FET gates can be controlled by the AUX_SEL pin function.

4.4.4.1. DisplayPort (DP) Mode

Name	Pin #	Description	I/O	PU / PD	Comment
DP2_LANE0+ DP2_LANE0- DP2_LANE1+ DP2_LANE1- DP2_LANE2+ DP2_LANE2- DP2_LANE3+ DP2_LANE3-	D39 D40 D42 D43 D46 D47 D49 D50	DP Port 2, differential pair data lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
DP2_HPD	D44	DP Port 2, detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	Module must tolerate high level in stand-by mode. The carrier board shall include a blocking FET on DP1_HPD to prevent back-drive current from damaging the Module.
DP2_AUX+	C32	DP Port 2, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PD 100K	AC coupled on Module
DP2_AUX-	C33	DP Port 2, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PU 100K	AC coupled on Module
DDI2_DDC_AUX_SEL	C34	Strapping Signal to select HDMI or DP output 1M pull-down on the module and floating on the carrier that enables DisplayPort mode	I 3.3V	PD 1M	DP mode enabled

4.4.4.2. HDMI Mode

Name	Pin #	Description	I/O	PU / PD	Comment
TMDS2_DATA2+ TMDS2_DATA2- TMDS2_DATA1+ TMDS2_DATA1- TMDS2_DATA0+ TMDS2DATA0-	D39 D40 D42 D43 D46 D47	HDMI / DVI Port, Differential Pair Data Lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
TMDS2_CLK+ TMDS2_CLK-	D49 D50	HDMI Port, Differential Pair Clock Lines			
HDM2_HPD	D44	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	
HDMI2_CTRLCLK	C32	I2C_CLK Line for HDMI	I/O PCIE	PU 2.2K	AC couple on Module
HDMI2_CTRLDATA	C33	I2C_DAT Line for HDMI	I/O PCIE	PU 2.2K	AC couple on Module
DDI2_DDC_AUX_SEL	C34	Strapping Signal to select HDMI or DP output 1M pull-down on the module and floating on the carrier that enables DisplayPort mode	I 3.3V	PD 1M	HDMI mode enabled

4.4.5. DDI3 Port

Name	Pin #	DisplayPort (DP)	HDMI
DDI3_PAIR0+ DDI3_PAIR0-	C39 C40	DP3_LANE0+ DP3_LANE0-	TMDS3_DATA2+ TMDS3_DATA2-
DDI3_PAIR1+ DDI3_PAIR1-	C42 C43	DP3_LANE1+ DP3_LANE1-	TMDS3_DATA1+ TMDS3_DATA1-
DDI3_PAIR2+ DDI3_PAIR2-	C46 C47	DP3_LANE2+ DP3_LANE2-	TMDS3_DATA0+ TMDS3_DATA0-
DDI3_PAIR3+ DDI3_PAIR3-	C49 C50	DP3_LANE3+ DP3_LANE3-	TMDS3_CLK+ TMDS3_CLK-
DDI3_HPD	C44	DP3_HPD	HDMI3_HPD
DDI3_CTRLCLK_AUX+	C36	DP3_AUX+	HMDI3_CTRLCLK
DDI3_CTRLCLK_AUX-	C37	DP3_AUX-	HMDI3_CTRLDATA
DDI3_DDC_AUX_SEL	C38	DDI3_DDC_AUX_SEL	DDI3_DDC_AUX_SEL

Note:
Dual Mode (HDMI and DisplayPort on the same pins) implementations may be realized. This is desirable for SOCs that natively implement this capability. With such SOCs, the primary Dual Mode implementation challenge is that the HDMI_CTRL_DAT and HDMI_CTRL_CK lines are DC coupled, but the DP_AUX+ /- pair must be AC coupled. A set of FET switches is usually used to sort this out. The FET gates can be controlled by the AUX_SEL pin function.

4.4.5.1. DisplayPort (DP) Mode

Name	Pin #	Description	I/O	PU / PD	Comment
DP3_LANE0+ DP3_LANE0- DP3_LANE1+ DP3_LANE1- DP3_LANE2+ DP3_LANE2- DP3_LANE3+ DP3_LANE3-	C39 C40 C42 C43 C46 C47 C49 C50	DP Port 3, differential pair data lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
DP3_HPD	C44	DP Port 3, detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	Module must tolerate high level in stand-by mode. The carrier board shall include a blocking FET on DP1_HPD to prevent back-drive current from damaging the Module.
DP3_AUX+	C36	DP Port 3, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PD 100K	AC coupled on Module
DP3_AUX-	C37	DP Port 3, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PU 100K	AC coupled on Module
DDI3_DDC_AUX_SEL	C38	Strapping Signal to select HDMI or DP output 1M pull-down on the module and floating on the carrier that enables DisplayPort mode	I 3.3V	PD 1M	DP mode enabled

4.4.5.2. HDMI Mode

Name	Pin #	Description	I/O	PU / PD	Comment
TMDS3_DATA2+ TMDS3_DATA2- TMDS3_DATA1+ TMDS3_DATA1- TMDS3_DATA0+ TMDS3_DATA0-	C39 C40 C42 C43 C46 C47	HDMI / DVI Port, Differential Pair Data Lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
TMDS3_CLK+ TMDS3_CLK-	C49 C50	HDMI Port, Differential Pair Clock Lines			
HDM3_HPD	C44	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	
HDMI3_CTRLCLK	C36	I2C_CLK Line for HDMI	I/O PCIE	PU 2.2K	AC couple on Module
HDMI3_CTRLDATA	C37	I2C_DAT Line for HDMI	I/O PCIE	PU 2.2K	AC couple on Module
DDI3_DDC_AUX_SEL	C38	Strapping Signal to select HDMI or DP output 1M pull-down on the module and floating on the carrier that enables DisplayPort mode	I 3.3V	PD 1M	HDMI mode enabled

4.4.6. PCIe Graphics Port (PEG)

Name	Pin #	Description	I/O	PU / PD	Comment
PEG_TX0+ PEG_TX0-	D52 D53	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX0+ PEG_RX0-	C52 C53	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX1+ PEG_TX1-	D55 D56	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX1+ PEG_RX1-	C55 C56	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX2+ PEG_TX2-	D58 D59	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX2+ PEG_RX2-	C58 C59	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX3+ PEG_TX3-	D61 D62	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX3+ PEG_RX3-	C61 C62	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX4+ PEG_TX4-	D65 D66	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX4+ PEG_RX4-	C65 C66	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX5+ PEG_TX5-	D68 D69	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module

Name	Pin #	Description	I/O	PU / PD	Comment
PEG_RX5+ PEG_RX5-	C68 C69	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX6+ PEG_TX6-	D71 D72	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX6+ PEG_RX6-	C71 C72	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX7+ PEG_TX7-	D74 D75	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX7+ PEG_RX7-	C74 C75	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
~~PEG_TX8+ PEG_TX8-~~	~~D78 D79~~	~~PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6~~	~~O PCIE~~		~~AC coupled on Module~~
~~PEG_RX8+ PEG_RX8-~~	~~C78 C79~~	~~PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6~~	~~I PCIE~~		~~AC coupled off Module~~
~~PEG_TX9+ PEG_TX9-~~	~~D81 D82~~	~~PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6~~	~~O PCIE~~		~~AC coupled on Module~~
~~PEG_RX9+ PEG_RX9-~~	~~C81 C82~~	~~PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6~~	~~I PCIE~~		~~AC coupled off Module~~
~~PEG_TX10+ PEG_TX10-~~	~~D85 D86~~	~~PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6~~	~~O PCIE~~		~~AC coupled on Module~~
~~PEG_RX10+ PEG_RX10-~~	~~C85 C86~~	~~PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6~~	~~I PCIE~~		~~AC coupled off Module~~

Name	Pin #	Description	I/O	PU / PD	Comment
~~PEG_TX11+~~ ~~PEG_TX11-~~	~~D88~~ ~~D89~~	~~PCI Express Graphics transmit differential pairs.~~ ~~These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6~~	~~O PCIE~~		~~AC coupled on Module~~
~~PEG_RX11+~~ ~~PEG_RX11-~~	~~C88~~ ~~C89~~	~~PCI Express Graphics receive differential pairs.~~ ~~These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6~~	~~I PCIE~~		~~AC coupled off Module~~
~~PEG_TX12+~~ ~~PEG_TX12-~~	~~D91~~ ~~D92~~	~~PCI Express Graphics transmit differential pairs.~~ ~~These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6~~	~~O PCIE~~		~~AC coupled on Module~~
~~PEG_RX12+~~ ~~PEG_RX12-~~	~~C91~~ ~~C92~~	~~PCI Express Graphics receive differential pairs.~~ ~~These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6~~	~~I PCIE~~		~~AC coupled off Module~~
~~PEG_TX13+~~ ~~PEG_TX13-~~	~~D94~~ ~~D95~~	~~PCI Express Graphics transmit differential pairs.~~ ~~These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6~~	~~O PCIE~~		~~AC coupled on Module~~
~~PEG_RX13+~~ ~~PEG_RX13-~~	~~C94~~ ~~C95~~	~~PCI Express Graphics receive differential pairs.~~ ~~These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6~~	~~I PCIE~~		~~AC coupled off Module~~
~~PEG_TX14+~~ ~~PEG_TX14-~~	~~D98~~ ~~D99~~	~~PCI Express Graphics transmit differential pairs.~~ ~~These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6~~	~~O PCIE~~		~~AC coupled on Module~~
~~PEG_RX14+~~ ~~PEG_RX14-~~	~~C98~~ ~~C99~~	~~PCI Express Graphics receive differential pairs.~~ ~~These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6~~	~~I PCIE~~		~~AC coupled off Module~~
~~PEG_TX15+~~ ~~PEG_TX15-~~	~~D101~~ ~~D102~~	~~PCI Express Graphics transmit differential pairs.~~ ~~These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6~~	~~O PCIE~~		~~AC coupled on Module~~
~~PEG_RX15+~~ ~~PEG_RX15-~~	~~C101~~ ~~C102~~	~~PCI Express Graphics receive differential pairs.~~ ~~These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6~~	~~I PCIE~~		~~AC coupled off Module~~
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the Carrier Board to reverse lane order.	I 3.3V		

Note: PEG slot is suitable for GPU, NVMe SSD.

4.4.7. Module Type Definition

Name	Pin #	Description	I/O	PU / PD	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). For Pin-out Type 1 and Type 10 that lack a CD connector, these pins are not present (X) **TYPE2# TYPE1# TYPE0#** X X X Pinout Type 1 X X X Pinout Type 10 NC NC NC Pinout Type 2 NC NC GND Pinout Type 3 NC GND NC Pinout Type 4 NC GND GND Pinout Type 5 GND NC NC Pinout Type 6 GND NC GND Pinout Type 7 The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g. deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.			Type 6
TYPE10#	A97	In case of a type 10 module this pin signal is tied to GND through a 47K resistor on the module.			No PD

4.4.8. Power and Ground

Name	Pin #	Description	I/O	PU / PD	Comment
VCC_12V	C104, C105, C106, C107, C108, C109, D104, D105, D106, D107, D108, D109	Primary power input supports a wide input range of 5~ 20V. All available VCC_12V pins on the connector(s) shall be used.	P		8.5-20 V
GND	C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70, C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path.	P		

5. Additional Features

This chapter describes connectors, LEDs, switches, and additional items located on the module, which are not necessarily included in the PICMG standard specification. The locations of these items are as below:

5.1. Module Feature Locations (TBD)

Figure 3 – Module feature locations (top side)

5.2. Debug Connector (TBD)

This connector is particularly useful during the carrier design and bring-up phase. It offers access to the following critical parts of the module:

- Test points measurement of internal power rails
- SPI BIOS programming interface
- Embedded Controller programming interface

Figure 4 – cExpress-R8 and debug module

5.3. Status LEDs

The status LEDs are mounted on the module to facilitate easier maintenance.

Name	Color	Connection	Function
LED1	Blue	EC output	Power Sequence Status Code (EC) Power Changes, RESET (see Exception Codes below)
LED2	Green	Power Source 3Vcc	S0 LED ON S3/S4/S5 LED OFF ECO mode LED OFF
LED3	Red	EC output and same signal as WDT (B27) on BtB connector	Module power up WD LED = LED OFF Watchdog counting WD LED = Keep Last State Watchdog timed out WD LED = LED ON Watchdog RESET WD LED = LED ON Rebooted after WD RESET WD LED = LED ON Rebooted after PWRBTN WD LED = LED OFF Rebooted after RESET BTN WD LED = LED OFF Note: only a RESET not initiated by the BMC can clear the WD LED (user action)

5.4. Exception Codes

Exception Code	Error Message
0	NOERROR
3	NO_SLP_S5
4	NO_SLP_S4
5	NO_SLP_S3
6	BIOS_FAIL
7	RESET_FAIL
9	NO_CB_PWROK
10	CRITICAL_TEMP
11	POWER_FAIL
12	VOLTAGE_FAIL
13	RSMRST_FAIL
14	NO_VDDQ_PG
16	NO_VCORE_PG
17	NO_SYS_GD
19	NO_V3P3A
21	NO_PWRSRC_GD

5.5. Fan Connector

Connector type: JVE 24W1125A-04M00

Name	Description
1	FAN_PWMOUT
2	FAN_TACHIN
3	GND
4	12V

5.6. BIOS Default Reset Button

To perform a hardware reset of BIOS default settings, perform the following steps:

1. Shut down the system.
2. Keep the BIOS Setup Defaults Reset Button pressed and boot up the system. You can release the button when the BIOS prompt screen appears
3. The BIOS prompt screen will display a confirmation that BIOS defaults have been reset and request that you reboot the system.

5.7. BIOS Boot Select

The module has two BIOS chips (BOM option) and BIOS operation can be configured to "PICMG" and dual-BIOS "Failsafe" modes using BIOS Select and Mode Configuration Switch, Pin 2.

Setting the module to PICMG mode will configure the BIOS chips on the module as SPI0 and SPI1. In PICMG mode, a BIOS chip cannot be placed in the SPI0 slot on the carrier.

In dual-BIOS Failsafe mode, both BIOS chips on the module are configured as SPI1. Only one of the two is connected to the SPI bus at any given time. In case of failure of the primary SPI1 BIOS, the system will reboot and switch to the secondary SPI1 BIOS on the module. In Failsafe mode, the SPI0 BIOS socket on the carrier can be populated.

In either mode, BIOS Select and Mode Configuration Switch Pin 1 is used to select whether to boot from SPI0 or SPI1.

Mode	Pin 1	Pin 2
Boot from SPI0 (default)	On	-
Boot from SPI1	Off	-
Set BIOS to PICMG mode (default)	-	On
Set BIOS to Failsafe BIOS mode	-	Off

6. System Resources

Note: This section is a preliminary version and is subject to future updates.

6.1. System Memory Map

Address Range (hex)	Description
000A0000-000DFFFF	PCI Express Root Complex
A0000000-DFFFFFFF	PCI Express Root Complex
AC000000-DD0FFFFF	PCI-to-PCI Bridge
DD0FC000-DD0FFFFF	HD Audio Controller
DD200000-DD2FFFFF	AMD Sensor Fusion Hub
DD200000-DD6FFFFF	PCI-to-PCI Bridge
DD300000-DD3FFFFF	AMD USB3 XHC
DD400000-DD4FFFFF	AMD USB3 XHC
DD5F0000-DD5F7FFF	HD Audio Controller
DD5FC000-DD5FDFFF	AMD Sensor Fusion Hub
DD5FE000-DD6FFFFF	AMD PSP Device
DD700000-DD7FFFFF	AMD USB3 XHC
DD700000-DDAFFFFF	PCI-to-PCI Bridge
DD800000-DD8FFFFF	AMD USB3 XHC
DD900000-DD9FFFFF	AMD USB2 XHC
DDA00000-DDA7FFF	AMD USB4 Host Router

Address Range (hex)	Description
DDA80000-DAFFFFFF	AMD USB4 Host Router
DDB00000-DDDFFFFF	PCI-to-PCI Bridge
DDC00000-DDD03FFF	VR7 Onboard Lan Device
DDE00000-DDEFFFFF	PCI-to-PCI Bridge
DDE20000-DDE83FFF	AMD Ethernet Controller
DDE84000-DDE847FF	SATA AHCI Controller
E0000000-EFFFFFFF	System Board
FD000000-FDFFFFFF	Motherboard resources
FEC00000-FEC01FFF	Motherboard resources
FEC10000-FEC10FFF	Motherboard resources
FED00000-FED003FF	High precision event timer
FED40000-FED44FFF	Trusted Platform Module 2.0
FED80000-FED8FFFF	Motherboard resources
FED81500-FED818FF	AMD GPIO Controller
FEDC0000-FEDC0FFF	Motherboard resources
FEDC2000-FEDC2FFF	AMD I2C Controller
FEDC3000-FEDC3FFF	AMD I2C Controller
FEDC9000-FEDC9FFF	AMD UART Controller
FEDC7000-FEDC7FFF	AMD UART Controller
FEE00000-FEE00FFF	Motherboard resources
FF000000-FFFFFFFF	Motherboard resources

6.2. I/O Map

Hex Range	Device
00h - 0Fh	DMA controller
20h - 21h	Programmable Interrupt controller 1
2Eh - 2Fh 4Eh - 4Fh	LPC SIO (W83627DHGSEC / IT5121E) configuration index/data registers
40h - 43h	System Timer
60h & 64h	PS2 Keyboard Mouse
61h	System Speaker
62h/66h, 68h/6Ch	IT5121E
70h - 71h	Real Time Clock Controller
81h - 83h, 87h, 89h - 8Bh, 8Fh	DMA controller
A0h - A1h	Programmable Interrupt controller 2
C0h - DFh	DMA controller
200h - 201h	IT5121E
240h - 247h	Serial port 3 (COM3)
248h - 24Fh	Serial port 4 (COM4)
2F8h – 2FFh	Serial port 2 (COM2)
3F8h - 3FFh	Serial port 1 (COM1)
B00h	SMBUS 0 IO base
B20h	SMBUS 1 IO base
CF9h	Reset Generator

6.3. Interrupt Request (IRQ) Lines

APIC Mode

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
0	High precision even timer/System timer	N/A	No
1	Standard PS/2 Keyboard	IRQ1 via SERIRQ	No
3	Serial Port 2 / AMD chipset UART 1	IRQ3 via SERIRQ	Note (1)
4	Serial Port 1 / AMD chipset UART 0	IRQ4 via SERIRQ	Note (1)
5	Serial Port 3	IRQ5 via SERIRQ	Note (1)
7	Serial Port 4	IRQ7 via SERIRQ	Note (1)
8	High precision even timer	N/A	No
10	AMD I2C Controller	N/A	No
12	Standard PS/2 Mouse	IRQ12 via SERIRQ	No
14	AMD GPIO Controller	N/A	Note (1)
36	High Definition Audio Controller	N/A	Note (1)
37	AMD Sensor Fusion Hub	N/A	Note (1)
39	AMD Audio Coprocessor / High Definition Audio Controller	N/A	Note (1)

Note (1): These IRQs can be used for PCI devices when onboard device is disabled.

6.4. PCI Configuration Space Map

Bus Number	Device Number	Function Number	Routing	Description
00h	00h	00h	Internal	AMD Host Bridge
00h	00h	02h	Internal	AMD Generic System Peripheral
00h	01h	00h	Internal	AMD Host Bridge
00h	02h	00h	Internal	AMD Host Bridge
00h	02h	05h	Internal	AMD Normal Decode PCI Bridge
00h	02h	06h	Internal	AMD Normal Decode PCI Bridge
00h	03h	00h	Internal	AMD Host Bridge
00h	04h	00h	Internal	AMD Host Bridge
00h	08h	00h	Internal	AMD Host Bridge
00h	08h	01h	Internal	AMD Normal Decode PCI Bridge
00h	08h	02h	Internal	AMD Normal Decode PCI Bridge
00h	08h	03h	Internal	AMD Normal Decode PCI Bridge
00h	14h	00h	Internal	AMD SMBus
00h	14h	03h	Internal	AMD ISA Bridge
00h	18h	00h	Internal	AMD Host Bridge
00h	18h	01h	Internal	AMD Host Bridge
00h	18h	02h	Internal	AMD Host Bridge
00h	18h	03h	Internal	AMD Host Bridge
00h	18h	04h	Internal	AMD Host Bridge
00h	18h	05h	Internal	AMD Host Bridge
00h	18h	06h	Internal	AMD Host Bridge

Bus Number	Device Number	Function Number	Routing	Description
00h	18h	07h	Internal	AMD Host Bridge
01h	00h	00h	Internal	AHCI 1.0 SATA Controller (STD BOM)
02h	00h	00h	Internal	Intel Ethernet Controller
03h	00h	00h	Internal	ATI VGA Compatible Controller
03h	00h	01h	Internal	ATI High Definition Audio Controller
03h	00h	02h	Internal	AMD Encryption Controller
03h	00h	03h	Internal	AMD USB Controller
03h	00h	04h	Internal	AMD USB Controller
03h	00h	05h	Internal	AMD Multimedia Controller
03h	00h	06h	Internal	AMD High Definition Audio Controller
03h	00h	07h	Internal	AMD Signal Processing Controller
04h	00h	00h	Internal	Advanced Micro Devices
04h	00h	01h	Internal	AMD Signal Processing Controller
05h	00h	00h	Internal	Advanced Micro Devices
05h	00h	03h	Internal	AMD USB Controller
05h	00h	04h	Internal	AMD USB Controller

6.5. PCI Interrupt Routing Map

INT Line	PEG. Root Port 0	PEG. Root Port 1	Lpc Bridge	HD Audio Controller	SMBus	SATA Controller
Int0	INTA:24	INTE:28	INTA:16	INTC:34	INTA:16	INTG:30
Int1	INTB:25	INTF:29	INTB:17	INTD:35	INTB:17	INTH:31
Int2	INTC:26	INTG:30	INTC:18	INTA:32	INTC:18	INTE:28
Int3	INTD:27	INTH:31	INTD:19	INTB:33	INTD:19	INTF:29

INT Line	XHCI Controller 1	XHCI Controller2	XHCI Controller3	XHCI Controller4	XHCI Controller5
Int0	INTC:34	INTC:34	INTC:26	INTC:26	INTC:26
Int1	INTD:35	INTD:35	INTD:27	INTD:27	INTD:27
Int2	INTA:32	INTA:32	INTA:24	INTA:24	INTA:24
Int3	INTB:33	INTB:33	INTB:25	INTB:25	INTB:25

INT Line	PCIE Port1	PCIE Port 2	PCIE Port 3	PCIE Port 4	PCIE Port 5	PCIE Port 6	PCIE Port 7	PCIE Port 8
Int0	INTE:44	INTE:44	INTG:46	INTG:46	INTC:42	INTC:42	N/A	N/A
Int1	INTF:45	INTF:45	INTH:47	INTH:47	INTD:43	INTD:43	N/A	N/A
Int2	INTG:46	INTG:46	INTE:44	INTE:44	INTA:40	INTA:40	N/A	N/A
Int3	INTH:47	INTH:47	INTF:45	INTF:45	INTB:41	INTB:41	N/A	N/A

6.6. SMBus Address Table

Device	Address
DDR5 Channel A(SO-DIMM1)	A0h
DDR5 Channel B(SO-DIMM2)	A2h

7. BIOS Settings

Note: This section is a preliminary version and is subject to future updates.

7.1. Menu Structure

This section presents the six primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. The subsections in this section describe the submenus and setting options for each menu item. The default setting options are presented in **bold**, and the function of each setting is described in the right-hand column of the respective table.

Main	Advanced	Chipset	Security	Boot	Save & Exit
BIOS Information System Information System Date System Time	CPU Configuration ► Graphics Configuration ► SATA Configuration ► Power Management ► System Management ► Thermal Management ► Watchdog Timer ► Super IO Configuration ► Miscellaneous ► Serial Port Console Redirection ► Trusted Computing ► AMD fTPM configuration ► Network Stack Configuration ► PCI Subsystem Settings► USB Configuration ► PCI/PCIe Configuration ►	South Bridge► GFX Configuration► North Bridge►	Password Description Secure Boot Menu ►	Boot Configuration	Save Options Default Options Boot Override

Main	Advanced	Chipset	Security	Boot	Save & Exit
	AMD CBS► AMD PBS► Asmedia AHCI Controller► Intel Ethernet Controller►				

Note: Indicates a submenu, and gray text indicates info only. Asmedia AHCI Controller► is STD BOM only

7.1.1. BIOS Information

Feature	Options	Description
BIOS Vender	Info only	American Megatrends
BIOSVersion	Info only	Display Core version
Build Date	Info only	Display compliancy information
AGESA Version	Info only	Display compliancy information
GOP Driver Version	Info only	ADLINK BIOS version.

7.1.2. System Information

Feature	Options	Description
Project Name	Info only	Display Project Name.
CPU Board Version	Info only	Display CPU Signature.
CPU Brand String	Info only	Display CPU Brand Name.
CPU Frequency	Info only	Display CPU Frequency
Total Memory	Info only	Display installed memory size.
Memory Frequency	Info only	Display memory frequency.

7.1.3. System Date and Time

Feature	Options	Description
System Date	Weekday, MM/DD/YYYY	Requires the alpha-numeric entry of the day of the week, day of the month, calendar month, and all 4 digits of the year, indicating the century and year (Fri XX/XX/20XX)
System Time	HH/MM/SS	Presented as a 24-hour clock setting in hours, minutes, and seconds
Access Level	Info only	

7.2. Advanced

This menu contains the settings for most of the user interfaces in the system

7.2.1. CPU Configuration

Feature	Options	Description
PSS support	Disabled **Enabled**	Enable/disable the generation of ACPI _PPC, _PSS, and _PCT objects.
PPC Adjustment	**PState 0** PState 1 PState 2	Provide to adjust _PPC object.
NX Mode	Disabled **Enabled**	Enable/disable No-execute page protection Function.
Node 0 Information	Info only	Display the information of process.

7.2.2. Graphics Configuration

Feature	Options	Description
NXP configuration	Info only	
eDP/LVDS	**Disabled** Enabled	Enables/Disables eDP/LVDS
DDI Port 1	Disabled **Display Port** HDMI	SOC DDI port 1 fuction choose to Display port or HDMI
DDI Port 2	Disabled **Display Port** HDMI	SOC DDI port 2 fuction choose to Display port or HDMI
DDI Port 3	Disabled **Display Port** HDMI	SOC DDI port 3 fuction choose to Display port or HDMI

7.2.3. SATA Configuration

ASMedia SATA Configuration

Feature	Options	Description
SATA Controller Speed	Gen1 Gen2 **Gen3**	Indicates the maximum speed the SATA controller can support.
Port 1 Hot Plug	Disabled **Enabled**	AsMedia SATA Port 1 Hot Plug Enable/Disable.
SATA Controller Speed	Gen1 Gen2 **Gen3**	Indicates the maximum speed the SATA controller can support.
Port 2 Hot Plug	Disabled **Enabled**	AsMedia SATA Port 2 Hot Plug Enable/Disable.
SATA Controller Speed	Gen1 Gen2 **Gen3**	Indicates the maximum speed the SATA controller can support.
Port 3 Hot Plug	Disabled **Enabled**	AsMedia SATA Port 3 Hot Plug Enable/Disable.
SATA Controller Speed	Gen1 Gen2 **Gen3**	Indicates the maximum speed the SATA controller can support.
Port 4 Hot Plug	Disabled **Enabled**	AsMedia SATA Port 4 Hot Plug Enable/Disable.

7.2.4. Power Management

Feature	Options	Description
Power Management	Info only	
Enable ACPI Auto Configuration	**Disabled** Enabled	Enables or Disables BIOS ACPI Auto Configuration.
~~Enable Hibernation~~	~~Disabled~~ ~~**Enabled**~~	~~Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may not be effective with some operating systems.~~
~~ACPI Sleep State~~	~~Suspend Disabled~~ ~~**S3 (Suspend to RAM)**~~	~~Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.~~
~~LID Function~~	~~**Disabled**~~ ~~Enabled~~	~~Enable/Disable LID Function~~
~~Sleep Function~~	~~Disabled~~ ~~**Enabled**~~	~~Enable/Disable Sleep Button Function~~
ECO Mode	**Disabled** Enabled	Reduces the power consumption of the system, but after a shut down, you have to wait at least 5 seconds before you can restart the system.
Power-Up Mode	**Turn On** Remain Off Last State	Turn On: The machine starts automatically when the power supply is turned on. Remain Off: To start the machine the power button has to be pressed. Last State: The machine will power up to last power state

7.2.4.1. Power Management > Power Consumption

Feature	Options	Description
Power Consumption	Info only	
Main Current	Read only	Display input current.
Current Input Power	Read only	Display input power.
RTC	Read only	Display actual voltage of the RTC.
5VSB	Read only	Display actual voltage of the 5VSB.
VIN	Read only	Display actual voltage of the VIN.
3.3V	Read only	Display actual voltage of the 3.3V.
VMEM	Read only	Display actual voltage of the VMEM.
3.3VSB	Read only	Display actual voltage of the 3.3VSB.
VCORE	Read only	Display actual voltage of the VCORE.

7.2.5. System Management

Feature	Options	Description
System Management	Info only	
SEMA BIOS Specification Version	Info only	
SEMA Firmware Version	Info only	
SEMA Flags	Submenu	
SEMA Features	Info only	
Uptime & Power Cycles Counter	Read only	
System Restart Event	Read only	
4096 Bytes User-Flash	Read only	

Feature	Options	Description
Runtime Watchdog	Read only	
Temperatures	Read only	
Voltage Monitor	Read only	
Display Backlight Control	Read only	
Power-up Watchdog	Read only	
Power Monitor (Current Sense)	Read only	
Boot Counter	Read only	
Dual-BIOS	Read only	
I2C Bus 1	Read only	
I2C Bus 2	Read only	
CPU Fan	Read only	
System Fan 1	Read only	
AT/ATX Mode	Read only	
ACPI Thermal Trigger	Read only	
Power-up to Last State	Read only	
Backlight Restore	Read only	
Ext - GPIO	Read only	
I2C Bus 3	Read only	
Other BMC	Read only	
Error Log	Read only	
Wake-by-BMC	Read only	
Soft Fan	Read only	

Feature	Options	Description
Parameter Memory	Read only	
Ext-GPIO Input Interrupt Support	Read only	

7.2.5.1. System Management > SEMA Flags

Feature	Options	Description
SEMA Flags	Info only	
BMC Flags	Read only	
BIOS Select	Read only	
ATX/AT-Mode	Read only	

7.2.6. Thermal Management

Feature	Options	Description
Active Cooling Trip Point	40 C 50 C 60 C 70 C **Refer to BMC**	This value is the temperature threshold of the active cooling trip point.
Passive Cooling Trip Point	**Disable** 100 C	This value is the temperature threshold of the passive cooling trip point.
Critical Trip Point	**Disable** 105 C	This value is the temperature threshold of the critical trip point.
Watchdog ACPI Event Shutdown	**Disabled** Enabled	Watchdog ACPI Event Shutdown Enabled/Disabled

Feature	Options	Description
Temperatures and Fan Speed	Info only	
CPU Temperature	Info only	
Current	Read only	
Startup	Read only	
Min	Read only	
Max	Read only	
Board Temperatures	Info only	
Current	Read only	
Startup	Read only	
Min	Read only	
Max	Read only	
CPU Fan Speed	Read only	
Smart Fan	Submenu	

7.2.6.1. Thermal Management > Smart Fan

Feature	Options	Description
Smart Fan	Info only	
CPU Smart FanTemperature Source	**CPU Sensor** Board Sensor	CPU Smart FanTemperature Source.
CPU Fan Mode	**AUTO (Smart Fan)** Off On Soft	CPU Fan Mode

Feature	Options	Description
Trigger Point 1	Info only	
Trigger Temperature	40	Trigger Temperature
PWM Level	30	PWM Level
Trigger Point 2	Info only	
Trigger Temperature	50	Trigger Temperature
PWM Level	40	PWM Level
Trigger Point 3	Info only	
Trigger Temperature	60	Trigger Temperature
PWM Level	63	PWM Level
Trigger Point 4	Info only	
Trigger Temperature	70	Trigger Temperature
PWM Level	100	PWM Level

7.2.7. Watchdog Timer

Feature	Options	Description
Watchdog Timer	**Info only**	
Power-Up watchdog	**Disabled** Enabled	The Power Up Watchdog resets the system after a certain amount of time after power up. Press F12 during start uo disable the Power Up Watchdog.
ATTENTION: Pressing F12 during start up disables the Power Up Watchdog.	Info only	
RunTime Watchdog	**Disabled** Enabled	The RunTime Watchdog resets the system after a certain amount of time after power up.

7.2.8. Super IO Configuration

Feature	Options	Description
Super IO Configuration	Info only	
~~ITE5121 Super IO Configuration~~	~~submenu~~	
Nct6126dSec Super IO Configuration	submenu	

~~7.2.8.1. Super IO Configuration> ITE5121 Super IO Configuration~~

Feature	Options	Description
~~IT5121E Super IO Configuration~~	~~Info only~~	
~~Super IO Chip~~	~~Info only~~	
~~Serial Port 1 Configuration~~	~~submenu~~	
~~Serial Port 2 Configuration~~	~~submenu~~	

7.2.8.2. Super IO Configuration> Nct6126dSec Super IO Configuration

Feature	Options	Description
Nct6126dSec Super IO Configuration	Info only	
Super IO Chip	Info only	
Serial Port 1 Configuration	submenu	
Serial Port 2 Configuration	submenu	

7.2.8.3. Super IO Configuration >ITE5121 Super IO Configuration > Serial Port 1 Configuration

Feature	Options	Description
Serial Port 1 Configuration	Info only	
Serial Port 1 Configuration	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	IO=3F8h; IRQ=4	Fixed configuration of serial port.
Change Settings	**Auto** IO=3F8h; IRQ=4 IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12	Select an optimal setting for Super IO device.
Change Settings	**Normal** High Speed	Select an optimal settings for Super IO Device.

7.2.8.4. Super IO Configuration >ITE5121 Super IO Configuration > Serial Port 2 Configuration

Feature	Options	Description
Serial Port 2 Configuration	Info only	
Serial Port 2 Configuration	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	IO=2F8h; IRQ=3	Fixed configuration of serial port.

~~Feature~~	~~Options~~	~~Description~~
~~Change Settings~~	~~**Auto**~~ ~~IO=2F8h; IRQ=3~~ ~~IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12~~ ~~IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12~~ ~~IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12~~ ~~IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12~~	~~Select an optimal setting for Super IO device.~~

7.2.8.5. Super IO Configuration > Nct6126dSec Super IO Configuration > Serial Port 1 Configuration

Feature	Options	Description
Serial Port 1 Configuration	Info only	
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	IO=240h; IRQ=5	Fixed configuration of serial port.
Change Settings	**Auto** IO=240h; IRQ=10 IO=240h; IRQ=3,4,5,6,7,10,11,12 IO=248h; IRQ=3,4,5,6,7,10,11,12 IO=250h; IRQ=3,4,5,6,7,10,11,12 IO=258h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for Super IO device.

Feature	Options	Description
	IO=260h; IRQ=3,4,5,6,7,10,11,12 IO=268h; IRQ=3,4,5,6,7,10,11,12	

7.2.8.6. Super IO Configuration > Nct6126dSec Super IO Configuration > Serial Port 2 Configuration

Feature	Options	Description
Serial Port 2 Configuration	Info only	
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	IO=248h; IRQ=7	Fixed configuration of serial port.
Change Settings	**Auto** IO=248h; IRQ=10 IO=240h; IRQ=3,4,5,6,7,10,11,12 IO=248h; IRQ=3,4,5,6,7,10,11,12 IO=250h; IRQ=3,4,5,6,7,10,11,12 IO=258h; IRQ=3,4,5,6,7,10,11,12 IO=260h; IRQ=3,4,5,6,7,10,11,12 IO=268h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for Super IO device.

Feature	Options	Description
Device Mode	**Standard Serial Port Mode** IrDA Active pulse 1.6 uS IrDA Active pulse 3/16 bit time ASKIR Mode	Change the Serial Port mode.

7.2.9. Miscellaneous

Feature	Options	Description
Miscellaneous	Info only	
I2C Speed Control	**100 Kbps** 400 Kbps	I2C Speed Control
WOL From S5	OFF **ON**	This Config to control power on/off LAN in S5 State by SEMA(EC).
Smart Battery Function	**Disabled** Enabled Auto	Enable/Disable Smart Battery function. Auto: disable Smart Battery function if charger IC not be detected.

7.2.10. Serial Console Redirection

Feature	Options	Description
COM0	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	
COM1	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	
COM2(Pci Bus0,Dev0,Func0,Port0)	Info only	
Console Redirection	**Enabled** Disabled	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	
COM3(Pci Bus0,Dev0,Func0,Port1)	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	
Serial Port for Out-of-Band Management/	Info only	
Windows Emergency Management Services (EMS)	Info only	
Console Redirection EMS	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	

7.2.10.1. Serial Port Console > Console Redirection Settings

Feature	Options	Description
COM2	Info only	
Console Redirection Settings	Info only	
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits.
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection..
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.

Feature	Options	Description
VT-UTF8 Combo Key Support	Disabled **Enable**	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.
Recorder Mode	**Disabled** Enable	With this mode enabled only text will be sent. This is to capture Terminal data.
Resolution 100x31	Disabled **Enable**	Enables or disables extended terminal resolution
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.

7.2.10.2. Serial Port Console > Console Redirection Settings

Feature	Options	Description
Out-of-Band Mgmt Port	**COM0** COM1 COM2 COM3	Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.
Terminal Type EMS	VT100 VT100+ **VT-UTF8** ANSI	VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation.
Bits per second	9600 19200 38400 57600	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.

Feature	Options	Description
	115200	
Flow Control	**None** Hardware RTS/CTS Software Xon/Xoff	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
Data Bits EMS	**8**	
Parity EMS	**None**	
Stop Bits EMS	**1**	

7.2.11. Trusted Computing

Feature	Options	Description
TPM 2.0 Device Found	Info only	
Firmware Version	Info only	
Vendor	Info only	
Security Device Support	Disabled **Enabled**	Security Device Support
Active PCR banks	Info only	
Available PCR banks	Info only	
Pending operation	**None** TPM Clear	Pending operation
Platform Hierarchy	Disabled **Enabled**	Enable or Disable Platform Hierarchy
Storage Hierarchy	Disabled	Enable or Disable Storage Hierarchy

Feature	Options	Description
	Enabled	
Endorsement Hierarchy	Disabled **Enabled**	Enable or Disable Endorsement Hierarchy
Physical Presence Spec Version	1.2 **1.3**	Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.
TPM 2.0 InterfaceType	Info only	Select the Communication Interface to TPM 20 Device.
PH Randomization	Disabled **Enabled**	Enables or Disables Platform Hierarchy randomization. DO NOT ENABLE THIS QUESTION IN PRODUCTION PLATFORMS. THIS IS FOR DEVELOPMENT TESTING. OVERRIDE ChangePlatformAuth ELINK for production platforms supporting TXT.
Device Select	TPM 1.2 TPM 2.0 **Auto**	TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated

7.2.12. AMD fTPM Configuration

Feature	Options	Description
Erase fTPM NV for factory reset	Disabled **Enabled**	When New CPU is installed, Select \"Enabled\" to reset fTPM, if you have BitLocker or encryption-enabled system, the system will not boot without a recovery key. Select \"Disabled\" to keep previous fTPM record and continue system boot, fTPM will NOT be enabled with new CPU unless fTPM is reset (reinitialized), you could swap back to the old CPU to recover TPM related keys and data.

7.2.13. Network Stack Configuration

Feature	Options	Description
Network Stack	**Disabled** Enabled	Enable/Disable UEFI network stack.
Ipv4 PXE Support	**Disabled** Enabled	Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.
IPv4 HTTP Support	**Disabled** Enabled	Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.
Ipv6 PXE Support	**Disabled** Enabled	Enable/Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.
IPv6 HTTP Support	**Disabled** Enabled	Enable/Disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.
PXE boot wait time	**0**	Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.
Media detect count	**1**	Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

7.2.14. PCI Subsystem Settings

Feature	Options	Description
AMI PCI Driver Version:	Info only	
PCI Settings Devices Common for all Deviceds:	Info only	
Above 4G Decoding	Disabled **Enabled**	Enables or Disables 64bit capable Devices to be Decoded in Above 4G Address Space (Only if System Supports 64 bit PCI Decoding).

Feature	Options	Description
Re-Size BAR Support	**Disabled** Enabled	If system has Resizable BAR capable PCIe Devices, this option Enables or Disables Resizable BAR Support.
SR-IOV Support	**Disabled** Enabled	If system has SR-IOV capable PCIe Devices, this option Enables or Disables Single Root IO Virtualization Support.
BME DMA Mitigation	**Disabled** Enabled	Re-enable Bus Master Attribute disabled during Pci enumeration for PCI Bridges after SMM Locked
Hot-Plug Support	Disabled **Enabled**	Globally Enables or Disables Hot-Plug support for the entire System. If System has Hot-Plug capable Slots and this option set to Enabled, it provides a Setup screen for selecting PCI resource padding for Hot-Plug.

7.2.15. USB Configuration

Feature	Options	Description
USB Configuration	Info only	
USB Module Version	Info only	
USB Controllers:	Info only	
USB Devices:	Info only	
Legacy USB Support	**Enabled** Disabled Auto	Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
XHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Device	Disabled	Enable/Disable USB Mass Storage Driver Support.

Feature	Options	Description
Configuration	**Enabled**	
USB hardware delays and time-outs	Info only	
USB transfer time-out	1 sec 5 sec 10 sec **20 sec**	The time-out value for Control, Bulk, and Interrupt transfers.
Device reset time-out	10 sec **20 sec** 30 sec 40 sec	USB mass storage device Start Unit command time-out.
Device power-up delay	**Auto** Manual	Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.
Mass Storage Devices	Info only	

7.2.16. PCI/PCIe Configuration

Feature	Options	Description
PCI/PCIe Configuration	Info only	
GPP0-7 Configuration(PEG)	**1X8** 2X4	To set the GFX Configuration
GPP12-15 Configuration(Lane 0-3)	**1X4 Port** 4X1 Port 2X1 1X2 Port 1X2 2X1 Port 2X2 Port	To set GPP12-15 Configuration (PCIe Lane 0-3).

Feature	Options	Description
GPP8-11 Configuration(Lane4-7)	**1X4 Port** 4X1 Port 2X1 1X2 Port 1X2 2X1 Port 2X2 Port	To set GPP8-11 Configuration (PCIe Lane 4-7).
GPP0-7 Gen Speed(PEG)	**Auto** Gen4 Gen3 Gen2 Gen1	Select GPP0-7(PEG) Gen speed.
GPP8-19 Gen Speed(PCIe)	**Auto** Gen4 Gen3 Gen2 Gen1	Select GPP8-19(PCIe) Gen speed
~~GPP~~	~~**Auto**~~ ~~Gen 4~~ ~~Gen 3~~ ~~Gen 2~~ ~~Gen 1~~	~~Select PCI Express slot Gen speed~~
GPP0-7 (PEG Port)	Disabled **Enabled**	Enable/Disable PCI Express root port (SOC GPP0-7)
GPP12 (Lane0)	Disabled **Enabled**	Enable/Disable GPP12 (Lane0)
GPP13 (Lane1)	Disabled **Enabled**	Enable/Disable GPP13 (Lane1)
GPP14 (Lane2)	Disabled **Enabled**	Enable/Disable GPP14 (Lane2)

Feature	Options	Description
GPP15 (Lane3)	Disabled **Enabled**	Enable/Disable GPP15 (Lane3)
GPP8 (Lane4)	Disabled **Enabled**	Enable/Disable GPP8 (Lane4)
GPP9 (Lane5)	Disabled **Enabled**	Enable/Disable GPP9 (Lane5)
GPP10 (Lane6)	Disabled **Enabled**	Enable/Disable GPP10 (Lane6)
GPP11 (Lane7)	Disabled **Enabled**	Enable/Disable GPP11 (Lane7)

7.2.17. AMD PBS

Feature	Options	Description
AMD Firmware Version	submenu	Show all of AMD Firmware Version
PCI Express Configurations	submenu	
Power Saving Configurations	submenu	
Graphics Configurations	submenu	
Display Configurations	submenu	
Above 4GB MMIO Limit	35bit (32GB) 36bit (64GB) 37bit (128GB) 38bit (256GB) 39bit (512GB) **40bit (1TB)**	ASelect Above 4GB MMIO Limit to 35~48bits limit.

Feature	Options	Description
	41bit (2TB) 42bit (4TB) 43bit (8TB) 44bit (16TB) 45bit (32TB) 46bit (64TB) 47bit (128TB) 48bit (256TB)	
5V_S5 voltage.	**5v_ALW(default)** 5v_ALW +60mv 5v_ALW +100mv	S5V_S5 voltage setting for 3ANPEC PSA
Processor Aggregator Device	**Disabled** Enabled	Enable/Disable Processor Aggregator Device
APIC Software Enable	Disabled **Enabled**	Enable/Disable APIC Software Enable
Dynamic P3T limit	**Enable for DC-only case (include fake DC)**	Set PEAK_PACKAGE_POWER_LIMIT dynamically at runtime by considering system overall power limit
HDMI 3.0G TX SLEW	**Disabled** Enabled	HDMI 3.0G TX SLEW

7.2.17.1.AMD PBS > AMD Firmware Version

Feature	Options	Description
AMD Firmware Version	Info only	
AGESA Version	Info only	
PSP BootLoader Version	Info only	
PSP SecureOS Version	Info only	
ABL Version	Info only	
APCB Version	Info only	
APOB Version	Info only	
Ucode Patch Version	Info only	
SMU FW Version	Info only	
ZSC FW Version	Info only	
MPIO FW Version	Info only	
MP2 FW Version	Info only	
XHCI FW Version	Info only	
VBIOS FW Version	Info only	
GOP Driver Version	Info only	

7.2.17.2.AMD PBS > PCI Express Configurations

Feature	Options	Description
PCI Express Configurations	Info only	
Pcie Dxio Timing ControlEnable	**Auto** Enabled	Pcie Dxio Timing Control Enable Custom: Customize timing

Feature	Options	Description
	Disabled	Disabled: DXIO default
NVMe RAID mode	**Disabled** Enabled	Enable or disable NVMe RAID mode. Please setting the 'PCIe/GFX Lanes Configuration' item according to the RAID configuration

7.2.17.3.AMD PBS > Power Saving Configurations

Feature	Options	Description
Power Saving Configurations	Info only	
S3/Modern Standby Support	Modern Standby Enable	
~~Modern Standby Type~~	~~Modern Standby + S0i~~ ~~**Modern Standby + S0i3**~~ ~~S0i3 with workaround~~ ~~Modern Standby + S0i2 + S0i3~~	~~Select S0I2 or S0I3 type for Modern Standby.~~
~~MS Resource~~	~~Disabled~~ ~~**Enabled**~~	~~Enable: Enable USB current resource for MS; Disable: Disable USB current resource for MS.~~
~~NVMe D3Cold~~	~~Disabled~~ ~~**NVMe D3 for single NVMe**~~ ~~NVMe D3 for multiple NVMe~~	~~Option for NVMe D3Cold.~~
~~M.2 NVME Tpvperl~~	~~**50**~~	~~Minimum time from powerrails within specifiedtoleranceto PERST# inactive. Default is 50ms~~
~~M.2 NVME Trst-cfg~~	~~**100**~~	~~Minimum period following the end of a Conventional Reset of device before it is permitted to issue Configuration Requests to the device. Default is 0ms~~
~~WLAN D3Cold~~	~~**Disabled**~~	~~Enabled/Disabled WLAN D3Cold.~~

Feature	Options	Description
	~~Enabled~~	
Wake on PME	Disabled **Enabled**	Determines the action taken when the system power is off and a PCI Power Management Enable wake up event occurs.
Internal PCIe GPP 0 D3	**Disabled** Enabled	Enabled Internal PCIe GPP Bridge 0 D3
SOC GPU D3	Disabled **Enabled**	Not support
SOC HD Audio D3	Disabled **Enabled**	Not support
SOC USB3.1 D3	Disabled **Enabled**	Enabled ISOC USB3.1 0 D3
SOC ACP D3	Disabled **Enabled**	Enabled ISOC ACP D3
SOC Azalia D3	Disabled **Enabled**	Not support
Internal PCIe GPP 2 D3	**Disabled** Enabled	Enabled IInternal PCIe GPP Bridge 2 D3
SOC USB2.0 D3	Disabled **Enabled**	Enabled ISOC USB2.0 D3
SOC USB3.1 for USB4 D3	Disabled **Enabled**	Not support
SOC USB4 D3	Disabled **Enabled**	Not support
Internal USB4 PCIe Tunneling D3	Disabled **Enabled**	Not support

Feature	Options	Description
SOC USB4 PCIe Endpoint D3	**Disabled** Enabled	Not support
Unused GPP Clocks Off	**Disabled** Enabled	Not support, fixed by HW design
Clock PM: CLK_REQ0	Enabled	Not support, fixed by HW design
Clock PM: CLK_REQ1	Enabled	Not support, fixed by HW design
Clock PM: CLK_REQ2	Enabled	Not support, fixed by HW design
Clock PM: CLK_REQ3	Enabled	Not support, fixed by HW design
Clock PM: CLK_REQ4	Enabled	Not support, fixed by HW design
Clock PM: CLK_REQ5	Enabled	Not support, fixed by HW design
Clock PM: CLK_REQ6	Enabled	Not support, fixed by HW design
PCIe x4 Slot D3 Cold	**Disabled** Enabled	

7.2.17.4. AMD PBS > Graphics Configurations

Feature	Options	Description
Graphics Configurations	Info only	
EVAL Slot Power Enable	Enabled	CRB design, Not support
EVAL CARD T-Diode Routing Select	EC	CRB design, Not support
Special Display Features	HybridGraphics	CRB design, Not support
D3Cold Support	Disabled	CRB design, Not support
NVIDIA DGPU Power Enable	Disabled	CRB design, Not support
Discrete GPU _DSM Function A	Disabled	CRB design, Not support

Feature	Options	Description
Discrete GPU _DSM Function B	Disabled	CRB design, Not support
Non-Eval Discrete GPU Support	Disabled	CRB design, Not support
Discrete GPU HPD Circuitry	OR Circuitry	CRB design, Not support
Discrete GPU's Audio	Keep ROM Strap Setting	CRB design, Not support
Discrete GPU's USB Port	Keep Default Setting	CRB design, Not support
Discrete GPU's SSID/SVID	Program by Vendor	CRB design, Not support
Discrete GPU's VGA SSID/SVID	0	CRB design, Not support
Discrete GPU's AUDIO SSID/SVID	0	CRB design, Not support
Discrete GPU BOMACO Support	Disabled	CRB design, Not support
BLINK LED	Enabled	CRB design, Not support
ATIF Notify Command Code	Notify VGA 0x81	CRB design, Not support
ATIF Function 21 Support	Disabled	CRB design, Not support
ATIF Function 22 Support	Disabled	CRB design, Not support
ATIF Function 23 Support	Disabled	CRB design, Not support
ATIF Function 24 Support	Disabled	CRB design, Not support
Primary Video Adaptor	Int Graphics (IGD)	R8000 support PEG only
Smart Mux Acpi Control	Disabled	CRB design, Not support
Display Panel Multiplexer	0	CRB design, Not support
Smart Mux _HID Selection	SMUX1234	CRB design, Not support
Smart Mux MDM Support Level	No Support	CRB design, Not support
Smart Mux First Connected GPU	Discrete Graphics	CRB design, Not support
Smart Mux ACPI Method Location	Under dGPU	CRB design, Not support

7.2.17.5. AMD PBS > Display Configurations (Do Not Modify, Fixed by HW Design)

Feature	Options	Description
Display Configurations	Info only	

7.2.18. AMD CBS

Feature	Options	Description
AMD CBS	Info only	
CPU Common Options	submenu	CPU Common Options
DF Common Options	submenu	DF Common Options
UMC Common Options	submenu	UMC Common Options
NBIO Common Options	submenu	NBIO Common Options
FCH Common Options	submenu	FCH Common Options
SMU Common Options	submenu	SMU Common Options
Soc Miscellaneous Control	submenu	Soc Miscellaneous Control

7.2.18.1. AMD CBS > CPU Common Options

Feature	Options	Description
Performance	Info	Performance
REP-MOV/STOS Streaming	Disabled **Enabled**	Allow REP-MOVS/STOS to use non-caching streaming stores for large sizes
Prefetcher settings	submenu	
Core Watchdog	submenu	Core Watchdog

Feature	Options	Description
RedirectForReturnDis	**Auto** 0 1	From a workaround for GCC/C000005 issue for XV Core on CZ A0, setting MSRC001_1029 Decode Configuration (DE_CFG) bit 14 [DecfgNoRdrctForReturns] to 1
Platform First Error Handling	Enabled Disabled **Auto**	Enable/disable PFEH, cloak individual banks, and mask deferred error interrupts from each bank.
Core Performance Boost	Disabled **Auto**	Disable CPB
Global C-state Control	Disabled Enabled **Auto**	Controls IO based C-state generation and DF C-states.\nThere is another DF Cstate option which will be synchronized with this option if DF Cstate option is auto.
Opcache Control	Enable Disable **Auto**	Enables or disables the Opcache
SEV ASID Count	253 ASIDs 509 ASIDs **Auto**	This fields specifies the maximum valid ASID, which affects the maximum system physical address space. 16TB of physical address space is available for systems that support 253 ASIDs, while 8TB of physical address space is available for systems that support 509 ASIDs.
SEV-ES ASID Space Limit Control	**Auto** Manual	No help string
Streaming Stores Control	Enabled Disabled **Auto**	Enables or disables the streaming stores functionality
Local APIC Mode	xAPIC x2APIC **Auto**	No help string

Feature	Options	Description
ACPI _CST C1 Declaration	Enabled Disabled **Auto**	Determines whether or not to declare the C1 state to the OS.
MCA error thresh enable	False **True**	Enable MCA error thresholding.
SMU and PSP Debug Mode	Enabled Disabled **Auto**	When this option is enabled, specific uncorrected errors detected by the PSP FW or SMU FW will hang and not reset the system
SVM Lock	Enabled Disabled **Auto**	Enable or Disable VM_CR[Lock]
SVM Enable	Enabled Disabled **Auto**	Enable or Disable VM_CR[SvmeDisable]
Log Transparent Errors	**Auto** Disabled Enabled	Log transparent errors in MCA in addition to debug registers.
AVX512	Disable Enable **Auto**	Enable/Disable AVX512.
MONITOR and MWAIT disable	Enabled Disabled **Auto**	The MONITOR, MWAIT, MONITORX, and MWAITX opcodes become invalid, when Enabled.

7.2.18.1.1 AMD CBS > CPU Common Options > Prefetcher Settings

Feature	Options	Description
L1 Stream HW Prefetcher	Disable Enable **Auto**	Option to Enable | Disable L1 Stream HW Prefetcher
L1 Stride Prefetcher	Disable Enable **Auto**	Uses memory access history of individual instructions to fetch additional lines when each access is a constant distance from the previous.
L1 Region Prefetcher	Disable Enable **Auto**	Uses memory access history to fetch additional lines when the data access for a given instruction tends to be followed by other data accesses.
L2 Stream HW Prefetcher	Disable Enable **Auto**	Option to Enable | Disable L2 Stream HW Prefetcher
L2 Up/Down Prefetcher	Disable Enable **Auto**	Uses memory access history to determine whether to fetch the next or previous line for all memory accesses.

7.2.18.1.2 AMD CBS > CPU Common Options > Core Watchdog

Feature	Options	Description
Core Watchdog Timer Enable	Enable Disable **Auto**	Enable or disable CPU Watchdog Timer

7.2.18.2. AMD CBS > DF Common Options

Feature	Options	Description
Memory Addressing	submenu	
DF Watchdog Timer Interval	**Auto** 41 ms 166 ms 334 ms 669ms 1.34 seconds 2.68 seconds 5.36 seconds	Configure the Data Fabric watchdog timer interval.
Disable DF to external downstream IP SyncFloodPropagation	Sync flood disabled Sync flood Enabled **Auto**	Disables Error propagation to UMC or any downstream slaves eg. FCH. Use this to avoid reset in failure scenario
Sync Flood Propagation to DF Components	Sync flood disabled Sync flood Enabled **Auto**	Control DF::PIEConfig[DisSyncFloodProp].
Freeze DF module queues on error	Disabled Enabled **Auto**	Disabling this option sets DF:DfGlobalCtrl[DisImmSyncFloodOnFatalError] Enables freezing of all DF queues on error and also forces a sync flood on HWA even if MCAs are disabled
CC6 memory region encryption	Disnabled Enabled **Auto**	Control whether or not the CC6 save/restore memory is encrypted
System probe filter	Disnabled Enabled **Auto**	Controls whether or not the probe filter is enabled. Has no effect on parts where the probe filter is fuse disabled.
Disable DF sync flood propagation	Sync flood disabled Sync flood enabled **Auto**	Control DF::PIEConfig[DisSyncFloodProp]\nDisables propagation from PIE to other DF components and eventually to SDP ports

Feature	Options	Description
DF Cstates	Disnabled Enabled **Auto**	When DF Cstate feature is enabled, FW programs the registers required to enable this feature is the DF HW. (For auto option, it means this option will synchronized with Global C State.)

7.2.18.2.1 AMD CBS > DF Common Options > Memory Addressing

Feature	Options	Description
Memory Addressing	Disabled **Auto**	Allows for disabling memory channel interleaving.
Memory interleaving size	256 Bytes 512 Bytes 1 KB 2 KB **Auto**	Controls the memory interleaving size. The valid values are AUTO, 256 bytes, 512 bytes, 1 Kbytes or 2Kbytes. This determines the starting address of the interleave (bit 8, 9, 10 or 11).
DRAM map inversion	Disabled Enabled **Auto**	Inverting the map will cause the highest memory channels to get assigned the lowest addresses in the system.
Location of private memory regions	Distributed Consolidated Consolidated to 1st DRAM pair **Auto**	Controls whether or not the private memory regions (PSP, SMU and CC6) are at the top of DRAM, at the top of 1st DRAM pair or distributed. Note that distributed requires memory on all dies. Note that it will always be at the top of DRAM if some dies don't have memory regardless of this option's setting.

7.2.18.3. AMD CBS > UMC Common Options

Feature	Options	Description
UMC Common Options	Info only	
DDR Options	submenu	DDR Options

7.2.18.3.1 AMD CBS > UMC Common Options > DDR Options

Feature	Options	Description
DDR Options	Info only	
DDR Timing Configuration	submenu	DDR Timing Configuration
DDR Bus Configuration	submenu	DDR Bus Configuration
DDR Controller Configuration	submenu	DDR Controller Configuration
DDR RAS	submenu	DDR RAS
DDR Security	submenu	DDR Security
DDR Addressing Options	submenu	DDR Addressing Options
DDR Training Options	submenu	DDR Training Options
DDR Memory MBIST	submenu	DDR Memory MBIST

13.2.18.3.1.1 AMD CBS > UMC Common Options > DDR Options > DDR Timing Configuration

Feature	Options	Description
DRAM Timing Configuration	Info only	

7.2.18.3.2 AMD CBS > UMC Common Options > DDR Options > DDR Bus Configuration

Feature	Options	Description
Processor CA drive strengt	**Auto** High Impedance 120.0 Ohm 60.0 Ohm 40.0 Ohm 30.0 Ohm	Select the drive strength for all CA0-13 IOs
Processor CK drive strengths	**Auto** High Impedance 120.0 Ohm 60.0 Ohm 40.0 Ohm 30.0 Ohm	Select the drive strength for all CK{T,C} IOs
Processor DQ drive strengths	**Auto** High Impedance 120.0 Ohm 60.0 Ohm 40.0 Ohm 30.0 Ohm	Select the drive strength for all DQ and DMI IOs
Processor DQS drive strengths	**Auto** High Impedance 120.0 Ohm 60.0 Ohm 40.0 Ohm 30.0 Ohm	Select the drive strength for all DQS IOs
Processor CA ODT impedance	**Auto** 120.0 Ohm 60.0 Ohm 40.0 Ohm 30.0 Ohm	Select the ODT impedance for ACHAN CA IOs

Feature	Options	Description
	Disable	
Processor CK ODT impedance	**Auto** 120.0 Ohm 60.0 Ohm 40.0 Ohm 30.0 Ohm Disable	Select the ODT impedance for ACHAN CK IOs
Processor CS ODT impedance	**Auto** 120.0 Ohm 60.0 Ohm 40.0 Ohm 30.0 Ohm Disable	Select the ODT impedance for ACHAN CS IOs
Processor DQ ODT impedance	**Auto** 120.0 Ohm 60.0 Ohm 40.0 Ohm 30.0 Ohm Disable	Select the ODT impedance for ACHAN DQ IOs
Processor DQS ODT impedance	**Auto** 120.0 Ohm 60.0 Ohm 40.0 Ohm 30.0 Ohm Disable	Select the ODT impedance for ACHAN DQS IOs
Dram DQ drive strengths	**Auto** 34 Ohm 40 Ohm 48 Ohm	Selects the Dram Pull-up and Pull-Down Output Driver Impedance for all DQ and DMI IOs

Feature	Options	Description
Dram ODT impedance RTT_NOM_WR	**Auto** RTT_OFF RZQ (240) RZQ/2 (120) RZQ/3 (80) RZQ/4 (60) RZQ/5 (48) RZQ/6 (40) RZQ/7 (34)	Select the DRAMs On-die Termination impedance for RTT_NOM_WR
Dram ODT impedance RTT_NOM_RD	**Auto** RTT_OFF RZQ (240) RZQ/2 (120) RZQ/3 (80) RZQ/4 (60) RZQ/5 (48) RZQ/6 (40) RZQ/7 (34)	Select the DRAMs On-die Termination impedance for RTT_NOM_RD
Dram ODT impedance RTT_WR	Auto RTT_OFF RZQ (240) RZQ/2 (120) RZQ/3 (80) RZQ/4 (60) RZQ/5 (48) RZQ/6 (40) RZQ/7 (34)	Select the DRAMs On-die Termination impedance for RTT_WR
Dram ODT impedance RTT_PARK	**Auto** RTT_OFF RZQ (240)	Select the DRAMs On-die Termination impedance for RTT_PARK

Feature	Options	Description
	RZQ/2 (120) RZQ/3 (80) RZQ/4 (60) RZQ/5 (48) RZQ/6 (40) RZQ/7 (34)	
Dram ODT impedance DQS_RTT_PARK	**Auto** RTT_OFF RZQ (240) RZQ/2 (120) RZQ/3 (80) RZQ/4 (60) RZQ/5 (48) RZQ/6 (40) RZQ/7 (34)	Select the DRAMs On-die Termination impedance for DQS_RTT_PARK

7.2.18.3.2.1 AMD CBS > UMC Common Options > DDR Options > DDR Controller Configuration

Feature	Options	Description
DDR Controller Configuration	Info only	
DDR Power Options	submenu	DDR Power Options

7.2.18.3.2.1.1 AMD CBS > UMC Common Options > DDR Options > DDR Controller Configuration > DDR Power Options

Feature	Options	Description
DDR Power Options	Info only	
Power Down Enable	Disabled Enabled	Enable or disble DDR Power down mode

Feature	Options	Description
	Auto	

13.2.18.3.3.1 AMD CBS > UMC Common Options > DDR Options > DDR RAS

Feature	Options	Description
DDR RAS	Info only	
Disable Memory Error Injection	False True **Auto**	True: UMC::CH:MiscCfg[DisErrInj]=1
DDR ECC Configuration	submenu	DDR ECC Configuration

13.2.18.3.3.1.1 AMD CBS > UMC Common Options > DDR Options > DDR RAS > DDR ECC Configuration

Feature	Options	Description
DDR ECC Configuration	Info only	
ECC	Disabled Enabled **Auto**	Use this option to enable / disable ECC. Auto will set ECC to enable.
Memory Clear	**Auto** Enabled Disabled	Clear/Zero out Dram range [DramScrubBaseAddr: DramScrubLimitAddr]. When this option is disabled, Memory is not cleared after training. ECC Dimms have memory clear enabled always. Non-ECC DIMMs can choose to disable/enable using this option. Default = Memclear disabled

13.2.18.3.3.2 AMD CBS > UMC Common Options > DDR Options > DDR Security

Feature	Options	Description
DDR Security	Info only	
TSME	**Auto** Enabled Disabled	No help string
Data Scramble	Enabled Disabled **Auto**	Data scrambling: DataScrambleEn

13.2.18.3.3.3 AMD CBS > UMC Common Options > DDR Options > DDR Addressing Options

Feature	Options	Description
DDR Addressing Options	Info only	
Chipselect Interleaving	Disable **Auto**	Interleave memory blocks across the DRAM chip selects for node 0.
Address Hash Bank	Disabled Enabled **Auto**	Enable or disable bank address hashing
Address Hash CS	**Auto** Enabled Disabled	Enable or disable CS address hashing
BankSwapMode	**Auto** Disabled Swap APU	BankSwapMode value: 0=Disabled, 2=SwapAPU

13.2.18.3.3.4 AMD CBS > UMC Common Options > DDR Options > DDR Training Options

Feature	Options	Description
DDR Training Options	Info only	
DFE Read Training	**Auto** Enabled Disabled	Perform 2D Read Training with FFE on.
DRAM PDA Enumerate ID Programming Mode	**Auto** Enabled Disabled	Specify PDA enumeration mode\nAuto : default\n0 : Continuous DQS toggling PDA enumeration mode (default)\n1 : Legacy PDA enumeration mode

13.2.18.3.3.5 AMD CBS > UMC Common Options > DDR Options > DDR Memory MBIST

Feature	Options	Description
DDR Memory MBIST	Info only	
MBIST Enable	**Disabled** Enabled	Enable or disable Memory MBIST
MBIST Test Mode	Interface Mode Data Eye Mode Both **Auto**	Select MBIST Test Mode -Interface Mode (Tests Single and Multiple CS transactions and Basic Connectivity) or Data Eye Mode (Measures Voltage vs. Timing)
MBIST Aggressors	Disabled Enabled **Auto**	Enable or disable MBIST Aggressor test
MBIST Per Bit Slave Die Reporting	Disabled Enabled **Auto**	Reports 2D Data Eye Results in ABL Log for each DQ, Chipselect, and Channel
DDR Data Eye	submenu	Data Eye

13.2.18.3.3.6 AMD CBS > UMC Common Options > DDR Options > DDR Memory MBIST > DDR Data Eye

Feature	Options	Description
DDR Data Eye	Info only	
Pattern Select	PRBS SSO **Both**	No help string
Pattern Length	**6**	This token helps to determine the pattern length. The possible options are N=3...12
Aggressor Channel	Disable **1 Aggressor Channel** 3 Aggressor Channels 7 Aggressor Channels	This helps read the aggressors channels. If it is enabled, you can read from one or more than one aggressor channel. The default is set to disabled.

7.2.18.4. AMD CBS > NBIO Common Options

Feature	Options	Description
NBIO Common Options	Info only	
IOMMU	Disabled **Enabled** Auto	Enable/Disable IOMMU
DMAr Support	Auto Enabled **Disabled**	Enable DMAr system protection during POST.
DMA Protection	**Auto** Enabled Disable	Enable DMA remap support in IVRS IVinfo Field.
PCIe ARI Support	Disabled Enabled	Enable/Disable ARI

Feature	Options	Description
	Auto	
PCIe ARI Enumeration	Disabled Enabled **Auto**	ARI Forwarding Enable for each downstream port
PSPP Policy	Disabled Enabled **Auto**	No Help string
GFX Configuration	submenu	GFX Configuration
Audio Configuration	submenu	Audio Configuration
PCIe loopback Mode	Disabled Enabled **Auto**	Enable/Disable PcieLoopbackMode.

13.2.18.3.4 AMD CBS > NBIO Common Options > GFX Configuration

Feature	Options	Description
GFX Configuration	Info only	
iGPU Configuration	**Auto** iGPU Disabled UMA_SPECIFIED UMA_AUTO UMA_GAME_OPTIMIZED UMA_WORKSTATION_OPTIMIZED	UMA Mode
UMA Version	Legacy Non-Legacy **Auto**	UMA Legacy Version\nUMA Non Legacy Version\nHybrid Secure
GPU Host Translation Cache	Disabled	Option to disable GPU Host Translation Cache

Feature	Options	Description
	Enabled **Auto**	
TCON INSTANT ON LOGO	Disabled Enabled **Auto**	Option to enable/disable TCON Instant on LOGO
UMA Carveout Index Max Control	**Auto** Manual	Control of indicates maximum index selectable for carveout options.

13.2.18.3.5 AMD CBS > NBIO Common Options > Audio Configuration

Feature	Options	Description
Audio Configuration	Info only	
NB Azalia	Disabled Enabled **Auto**	Enable Integrate HD Audio controller Auto=Enable
Audio IOs	**Auto** HDA(3SDI) + PDM(2CH), HDA(1SDI) + PDM(6CH), HDA(1SDI) + SDW0(1MDATA) + PDM(2CH), SDW0(4MDATA) + PDM(6CH), SDW0(4MDATA) + SDW1(1MDATA) + PDM(2CH), 3I2S PORTS + 1 REFCLK + 1 INTR, HDA(3SDI) + PDM(6CH) +I2S,	Audio IOs control

Feature	Options	Description
	HDA(3SDI) + PDM(8CH), HDA(1SDI) + SDW0(1MDATA) + PDM(6CH) + I2S, SDW0(4MDATA)+ SDW1(1MDATA) + PDM(6CH) + I2S, SDW0(4MDATA) + SDW1(1MDATA)+ PDM(8CH)	

7.2.18.5. AMD CBS > FCH Common Options

Feature	Options	Description
FCH Common Options	Info only	
I3C/I2C Configuration Options	submenu	I3C/I2C Configuration Options
USB Configuration Options	submenu	USB Configuration Options
Ac Power Loss Options	submenu	Ac Power Loss Options
Uart Configuration Options	submenu	Uart Configuration Options

13.2.18.3.6 AMD CBS > FCH Common Options > I3C/I2C Configuration Options

Feature	Options	Description
I3C/I2C Configuration Options	Info only	
I3C/I2C 0 Enable	Both Disabled I3C Enabled **I2C Enabled** Auto	No help string

Feature	Options	Description
I3C/I2C 1 Enable	Both Disabled I3C Enabled **I2C Enabled** Auto	No help string
I3C/I2C 2 Enable	**Both Disabled** I3C Enabled I2C Enabled Auto	No help string
I3C/I2C 3 Enable	**Both Disabled** I3C Enabled I2C Enabled Auto	No help string

13.2.18.3.7 AMD CBS > FCH Common Options > USB Configuration Options

Feature	Options	Description
USB Configuration Options	Info only	
USB0 controller enable	Enabled Disabled **Auto**	Enable or disable USB3 controller.
USB1 controller enable	Enabled Disabled **Auto**	Enable or disable USB3 controller.
USB0 2.0 port enable	submenu	USB0 2.0 port enable
USB1 2.0 port enable	submenu	USB1 2.0 port enable
USB2 2.0 port enable	submenu	USB2 2.0 port enable
USB3 2.0 port enable	submenu	USB3 2.0 port enable

Feature	Options	Description
USB0 3.1 port enable	submenu	USB0 3.1 port enable
USB1 3.1 port enable	submenu	USB1 3.1 port enable
USB3 3.1 port enable	submenu	USB3 3.1 port enable

13.2.18.3.7.1 AMD CBS > FCH Common Options > USB Configuration Options > USB0 2.0 port enable

Feature	Options	Description
USB0 2.0 port enable	Info only	
USB0 2.0 port 0	Disabled Enabled **Auto**	Disable or Enable USB0 2.0 port 0
USB0 2.0 port 1	Disabled Enabled **Auto**	Disable or Enable USB0 2.0 port 1
USB0 2.0 port 2	Disabled Enabled **Auto**	Disable or Enable USB0 2.0 port 2
USB0 2.0 port 3	Disabled Enabled **Auto**	Disable or Enable USB0 2.0 port 3
USB0 2.0 port 4	Disabled Enabled **Auto**	Disable or Enable USB0 2.0 port 4

13.2.18.3.7.2 AMD CBS > FCH Common Options > USB Configuration Options > USB1 2.0 port enable

Feature	Options	Description
USB1 2.0 port enable	Info only	
USB1 2.0 port 0	Disabled Enabled **Auto**	Disable or Enable USB1 2.0 port 0

13.2.18.3.7.3 AMD CBS > FCH Common Options > USB Configuration Options > USB2 2.0 port enable

Feature	Options	Description
USB2 2.0 port enable	Info only	
USB2 2.0 port 0	Disabled Enabled **Auto**	Disable or Enable USB2 2.0 port 0

13.2.18.3.7.4 AMD CBS > FCH Common Options > USB Configuration Options > USB3 2.0 port enable

Feature	Options	Description
USB3 2.0 port enable	Info only	
USB3 2.0 port 0	Disabled Enabled **Auto**	Disable or Enable USB3 2.0 port 0

13.2.18.3.7.5 AMD CBS > FCH Common Options > USB Configuration Options > USB0 3.1 port enable

Feature	Options	Description
USB0 3.1 port enable	Info only	
USB0 3.1 port 0	Disabled	Disable or Enable USB0 3.1 port 0

Feature	Options	Description
	Enabled **Auto**	
USB0 3.1 port 1	Disabled Enabled **Auto**	Disable or Enable USB0 3.1 port 1

13.2.18.3.7.6 AMD CBS > FCH Common Options > USB Configuration Options > USB1 3.1 port enable

Feature	Options	Description
USB1 3.1 port enable	Info only	
USB1 3.1 port 0	Disabled Enabled **Auto**	Disable or Enable USB1 3.1 port 0

13.2.18.3.7.7 AMD CBS > FCH Common Options > USB Configuration Options > USB2 3.1 port enable

Feature	Options	Description
USB1 3.1 port enable	Info only	
USB1 3.1 port 0	Disabled Enabled **Auto**	Disable or Enable USB1 3.1 port 0

13.2.18.3.7.8 AMD CBS > FCH Common Options > USB Configuration Options > USB3 3.1 port enable

Feature	Options	Description
USB3 3.1 port enable	Info only	
USB3 3.1 port 0	Disabled	Disable or Enable USB3 3.1 port 0

Feature	Options	Description
	Enabled **Auto**	

13.2.18.3.8 AMD CBS > FCH Common Options > Ac Power Loss Options

Feature	Options	Description
Ac Power Loss Options	Info only	
Ac Loss Control	**Always Off** Always On Reserved Previous Auto	Select Ac Loss Control Method

13.2.18.3.9 AMD CBS > FCH Common Options > UART Configuration Options

Feature	Options	Description
Uart Configuration Options	Info only	
Uart 0 Enable	Disabled **Enabled**	Uart 0 enabled
Uart 0 Resource Options	MMIO 0x2E8 0x2F8 0x3E8 **0x3F8**	MMIO: Enable for HSUART; 0x3F8/0x2F8/0x3E8/0x2E8: Legacy IO for Windows inbox driver and Linux.
Uart 1 Enable	Disabled **Enabled**	Uart 1 enabled
Uart 3 Enable (no HW FC)	MMIO 0x2E8	MMIO: Enable for HSUART; 0x3F8/0x2F8/0x3E8/0x2E8: Legacy IO for Windows

Feature	Options	Description
	0x2F8 0x3E8 **0x3F8**	inbox driver and Linux.

7.2.18.6. AMD CBS > SMU Common Options

Feature	Options	Description
SMU Common Options	Info only	
System Configuration	**Auto** 15W 20W 28W 30W 35W 45W 54W	Warning: Select System Configuration may cause the system to hang, as some System Configuration may not be supported by your OPN.
SPL Control	Manual **Auto**	Auto = Use the default Sustained Power Limit\nManual = User can set customized Sustained Power Limit
PPT Control	Manual **Auto**	Auto = Use the default PPT Limits\nManual = User can set customized PPT Limits
STAPM Control	Manual **Auto**	Auto = Use the default STAPM settings Manual = User can set customized STAPM settings
Thermal Control	Manual **Auto**	Auto = Use the default TctlMax Manual = User can set customized TctlMax
TDC Control	Manual **Auto**	Auto = Use the default TDC limits Manual = User can set customized TDC limits
EDC Control	Manual	Auto = Use the default EDC limits

Feature	Options	Description
	Auto	Manual = User can set customized EDC limits
PSI3 Control	Manual **Auto**	Auto = Use the default PSI3 limits Manual = User can set customized PSI3 limits
PROCHOT Control	Manual **Auto**	Auto = Use the default PROCHOT deassertion ramp time Manual = User can set customized PROCHOT deassertion ramp time
STT Control	Manual **Auto**	Auto = Use the default STT controller settings Manual = User can set customized STT controller settings
Fan Control	Manual **Auto**	Auto = Use the default fan controller settings\nManual = User can set customized fan controller settings
SmartShift Control	submenu	SmartShift Control
ECO Mode	**Auto** H Series OPNs System Config 4 (35W)	H Series OPNs System Config 4 (35W)

13.2.18.3.10 AMD CBS > SMU Common Options > SmartShift Control

Feature	Options	Description
SmartShift Control	Info only	
SmartShift Control	**Auto** Manual	No help string

7.2.18.7. AMD CBS > Soc Miscellaneous Control

Feature	Options	Description
Soc Miscellaneous Control	Info only	
Trusted Platform Module	Auto **Disabled** Enable dTPM Enable ASP fTPM Enable Pluton fTPM	Enable/Disable TPM physical presence.
Pluton Security Processor	**Auto** Disabled Enabled	This option is used to enable/disable Pluton Security Processor
Microsoft Security Levels	**Customized** dTPM Level 1 without Pluton Security Processor dTPM Level 2 without Pluton Security Processor dTPM Level 3 without Pluton Security Processor Pluton fTPM Level 1 Pluton fTPM Level 2 Pluton fTPM Level 3 dTPM Level 1 with Pluton Security Processor dTPM Level 2 with Pluton Security Processor dTPM Level 3 with Pluton Security Processor ASP fTPM Level 0 ASP fTPM Level 1 ASP fTPM Level 2	This option provide one stop configuration for SCPC (Note: Firmware Anti-rollback is excluded). \nFor Level 1, it will configure TPM, SVM, IOMMU, SecureBoot; \nFor Level 2, it will configure TPM, SVM, IOMMU, DMAr, SecureBIO, SecureBoot; \nFor Level 3, it will configure TPM, SMM Isolation, SVM, IOMMU, DMAr, TSME, SecureBIO, SecureBoot, Modern Standby. \nRegard TPM configuration, dTPM refers to discrete TPM. Pluton fTPM refers to Pluton firmware TPM. ASP fTPM refers to ASP firmware TPM. \nNOTE: FAR is required for Level3 and please enable it manually in CBS-> SOC Miscellaneous Control / Firmware Anti-rollback (FAR) / FAR Switch.\n dTPM with Pluton security processor is recommend configuration for Level1/2/3
Secured-core Auto enablement	**Auto**	If set to Disable, AGESA will delete EFI variable "BuiltAsSecuredCorePC" if detected

Feature	Options	Description
	Enabled Disabled	If set to Enable, AGESA will set EFI variable "BuiltAs-SecuredCorePC" to non-zero value If "BuiltAsSecuredCorePC" set to non-zero, it will iden-tify a device as Secure-core PC More detials refer to "Secured-Core PC Identifier" in MSFT document. If set to Auto, ignore, AGESA will do nothing
DRTM Support	**Auto** Enabled Disabled	Enable DRTM
SMM Isolation Support	**Auto** Enabled Disabled	Enable SMM Isolation (as known as SMM Supervisor)
Pluton Options	submenu	Pluton Options
Firmware Anti-rollback (FAR)	submenu	Firmware Anti-rollback (FAR)
GFX workstation support	**Auto** Enabled Disabled	Enable/disable GFX workstation feature
AIM-T Options	submenu	AIM-T Options
Intrusion Detection	submenu	Intrusion Detection
SecureBio	submenu	SecureBio
ABL Console Out Control	**Auto** Enabled Disabled	Enable : Enable ConsoleOut Function for ABL Disable : Disable ConsoleOut Function for ABL Auto : Keep default behavior
PSP RPMC Switch"	**Auto** Disabled Enabled	Control RPMC usage. Enable : Enable RMPC function Disable : Disable RMPC function Auto : Keep default behavior

Feature	Options	Description
		This option is for test purpose only, NOT FOR PRODUCTION!!!
Mixed DIMM config extended NUMA domain	Disabled Enabled **Auto**	Mixed DIMM config extended NUMA domain in SRAT that contain only non-interleaving memory region but no processor.

13.2.18.3.11 AMD CBS > Soc Miscellaneous Control > Pluton Options

Feature	Options	Description
Pluton (HSP) Options	Info only	
Pluton UART	Disabled Enabled **Auto**	HSP Firmware will print debug information to FCH UART, select to enable/disable this function, By default it will be disabled.
Pluton FIPS	Disabled Enabled **Auto**	Enable FIPS mode for HSP

13.2.18.3.12 AMD CBS > Soc Miscellaneous Control > Firmware Anti-rollback (FAR)

Feature	Options	Description
Firmware Anti-rollback (FAR)	Info only	
FAR Switch	**Auto** Enabled Disabled	Enabled = if initial SPL value is 0, and FAR is NOT enforced, BIOS will enforce FAR and set SPL fuse to SPL value in the SPL table. if initial SPL value is 0, and FAR is enforced, BIOS will update SPL fuse to SPL value in the SPL table. if initial SPL value is not 0, and FAR is NOT enforced, BIOS will enforce FAR and set SPL

Feature	Options	Description
		fuse to initial SPL value. if initial SPL value is not 0, and FAR is enforced, BIOS will keep SPL fuse as it is. Disabled = BIOS will NOT change FAR enforcement state and NOT set SPL fuse.

13.2.18.3.13 AMD CBS > Soc Miscellaneous Control > AIM-T Options

Feature	Options	Description
AIM-T Options	Info only	
AIM-T Support	**AIM-T Disabled** AIM-T Enabled Auto	Only works on the platform which is AIM-T capable. AIM-T disable: turn off all MPM related feature for both wired KVM and wireless manageability

13.2.18.3.14 AMD CBS > Soc Miscellaneous Control > Intrusion Detection

Feature	Options	Description
Intrusion Detection	Info only	
Intrusion Detection Control	**0**	Intrusion Detection settings should be configured by system administrator only, please input correct password.to show related settings

13.2.18.3.15 AMD CBS > Soc Miscellaneous Control > SecureBIO

Feature	Options	Description
SecureBio Support	**Auto** Enabled Disabled	Switch to turn off Secure BIO, when set to FALSE, it will turn off Secure BIO, Enable: Enable Secure Bio

Feature	Options	Description
		Disable : Disable Secure Bio Auto : Keep default behavior

7.2.19. Asmedia ACHI Controller

Feature	Options	Description
SATA Port 0	Info only	
SATA Port 1	Info only	
SATA Port 2	Info only	
SATA Port 3s	Info only	

7.2.20. Intel(R) Ethernet Controller

Feature	Options	Description
UEFI Driver	Info only	
PCI Device ID	Info only	
PCI Address	Info only	
MAC Address	Info only	
Link Status	Info only	
Link auto-negotiation Timeout	**8**	How long the UEFI PXE driver should wait for link

7.3. Chipset

Feature	Options	Description
South Bridge	submenu	
GFX Configuration	submenu	
North Bridge	submenu	

7.3.1. Chipset > South Bridge

Feature	Options	Description
SB USB Configuration	submenu	

7.3.1.1. Chipset > SB USB Configuration

Feature	Options	Description
> USB0 Ports	submenu	
> USB1 Ports	submenu	
> USB3 Ports	submenu	
> USB4 Ports	submenu	

13.2.18.3.16 Chipset > SB USB Configuration > USB0 Ports

Feature	Options	Description
XHCI0 Port 0	Disabled **Enabled**	Enabled/Disabled XHCI0 Port 0
XHCI0 Port 1	Disabled	Enabled/Disabled XHCI0 Port 1

Feature	Options	Description
	Enabled	
XHCI0 2.0 Port 0	Disabled **Enabled**	Enabled/Disabled XHCI0 2.0 Port 0
XHCI0 2.0 Port 1	Disabled **Enabled**	Enabled/Disabled XHCI0 2.0 Port 1
XHCI0 2.0 Port 2	Disabled **Enabled**	Enabled/Disabled XHCI0 2.0 Port 2
XHCI0 2.0 Port 3	Disabled **Enabled**	Enabled/Disabled XHCI0 2.0 Port 3

13.2.18.3.17 Chipset > SB USB Configuration > USB1 Ports

Feature	Options	Description
XHCI1 Port 0	Disabled **Enabled**	Enabled/Disabled XHCI1 Port 0
XHCI1 Port 1	Disabled **Enabled**	Enabled/Disabled XHCI1 Port 1

13.2.18.3.18 Chipset > SB USB Configuration > USB3 Ports

Feature	Options	Description
XHCI3 Port 0	Disabled **Enabled**	Enabled/Disabled XHCI3 Port 0
XHCI3 2.0 Port 0	Disabled **Enabled**	Enabled/Disabled XHCI3 2.0 Port 0

13.2.18.3.19 Chipset > SB USB Configuration > USB4 Ports

Feature	Options	Description
XHCI4 Port 0	Disabled **Enabled**	Enabled/Disabled XHCI4 Port 0
XHCI4 2.0 Port 0	Disabled **Enabled**	Enabled/Disabled XHCI4 2.0 Port 0

7.3.2. Chipset > GFX Configuration

Feature	Options	Description
IGD - AmdGop Output Priority	**Default** Manually	Sample Code
IGD - AmdGop Bootup Brightness Level	**255**	Lcd Only, Range 0 - 255

7.3.3. Chipset > North Bridge

Feature	Options	Description
North Bridge Configuration	Info only	
Memory Information	Info only	
Total Memory	Info only	
Socket 0 Information	submenu	

7.3.3.1. Chipset > North Bridge > Socket 0 Information

Feature	Options	Description
Socket 0 Information	Info only	
Starting address	Info only	
Ending Address	Info only	
ChannelA	Info only	
Dimm0	Info only	
Current speed	Info only	
MAX speed	Info only	
ChannelB	Info only	
Dimm0	Info only	
Current speed	Info only	
MAX speed	Info only	

7.4. Security

Feature	Options	Description
Administrator Password	Enter password	Set Admonistrator Password
User Password	Enter password	Set User Password
Secure Boot	submenu	

7.4.1. Security > Secure Boot Menu

Feature	Options	Description
Secure Mode	Info only	
Secure Boot	**Disabled** Enabled	Secure Boot feature is Active if Secure Boot is Enabled,platform Key(PK) is enrolled and the System is in User mode, The mode change requires platform reset
Secure Boot Mode	**Standard** Custom	Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full
Restore Factory Keys	Info only	Force System to User Mode. Install factory default Secure Boot key databases
Reset To Setup Mode	Info only	
Key Management		Enables expert users to modify Secure Boot Policy variables without full authentication

7.5. Boot

7.5.1. Boot Configuration

Feature	Options	Description
Boot Configuration	Info only	
Setup Prompt Timeout	**0**	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
Bootup NumLock State	**On** Off	Select the keyboard NumLock state
Quiet Boot	Disabled **Enabled**	Enables or disables Quiet Boot option
Fast Boot	Disabled **Enabled**	Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.
SATA Support	**Last Boot SATA Devices Only** All Sata Devices	If Last Boot SATA Devices Only, Only last boot SATA device will be available in Post. If All Sata Devices, all SATA devices will be available in OS and Post.
NVME Support	Disabled **Enabled**	If Disabled, NVMe device will be skipped.
VGA Support	Auto **EFI Driver**	If Auto, only install Legacy OpRom with Legacy OS and logo would NOT be shown during post. Efi driver will still be installed with EFI OS.
USB Support	Disabled **Full Initial** Partial Initial	If Disabled, all USB devices will NOT be available until after OS boot. If Partial Initial, USB Mass Storage and specific USB port/device will NOT be available before OS boot. If Enabled, all USB devices will be available in OS and Post.
PS2 Devices Support	Disabled	If Disabled, PS2 devices will be skipped.

Feature	Options	Description
	Enabled	
NetWork Stack Driver Support	**Disabled** Enabled	If Disabled, NetWork Stack Driver will be skipped.
Redirection Support	**Disabled** Enabled	If disable, Redirection function will be disabled.

7.6. Save & Exit

7.6.1. Save Options

Feature	Options	Description
Save Option	Info only	
Save Changes and Exit		Exit system setup after saving the changes.
Discard Changes and Exit		Exit system setup without saving any changes.

8. BIOS Checkpoints, Beep Codes

This document section lists checkpoints and beep codes generated by AMI Aptio BIOS. The checkpoints defined in this document are inherent to the AMIBIOS generic core, and do not include any chipset or board-specific checkpoint definitions.

Checkpoints and Beep Codes Definition

A checkpoint is either a byte or word value output to I/O port 80h. The BIOS outputs checkpoints throughout the boot block and Power-On Self-Test (POST) to indicate the task the system is currently executing. Checkpoints are very useful for debugging problems that occur during the preboot process.

Beep codes are used by the BIOS to indicate a serious or fatal error. They are used when an error occurs before the system video has been initialized, and generated by the system board speaker.

Aptio Boot Flow

While performing the functions of the traditional BIOS, Aptio 5.x core follows the firmware model described by the Intel Platform Innovation Framework for EFI ("the Framework"). The Framework refers the following "boot phases", which may apply to various status code & checkpoint descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization[1]
- Driver Execution Environment (DXE) – main hardware initialization[2]
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, …)

Viewing BIOS Checkpoints

Viewing all checkpoints generated by the BIOS requires a checkpoint card, also referred to as a POST Card or POST Diagnostic Card. These are PCI add-in cards that show the value of I/O port 80h on a LED display.

Some computers display checkpoints in the bottom right corner of the screen during POST. This display method is limited, since it only displays checkpoints that occur after the video card has been activated.

Keep in mind that not all computers using AMI Aptio BIOS enable this feature. In most cases, a checkpoint card is the best tool for viewing AMI Aptio BIOS checkpoints.

[1]Analogous to "boot block" functionality of legacy BIOS
[2]Analogous to "POST" functionality in legacy BIOS

Aptio V Checkpoint and Beep Codes

Download the Aptio V Checkpoint and Beep Codes from the AMI website at: www.ami.com/download/aptio-v-checkpoint-and-beep-codes

8.1. Status Code Ranges

Status Code Range	Description
0x01 – 0x0F	SEC execution
0x10 – 0x2F	PEI CAR execution
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0xCF	DXE execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)
0x01 – 0x0F	SEC execution
0x10 – 0x2F	PEI CAR execution

8.2. Standard Status Codes

8.2.1. SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization

SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

8.2.2. SEC Beep Codes

None

8.2.3. PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12 – 0x14	Reserved for CPU
0x15	Pre-memory North Bridge initialization is started
0x16 – 0x18	Reserved for North Bridge
0x19	Pre-memory South Bridge initialization is started
0x1A – 0x1C	Reserved for South Bridge
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization

Status Code	Description
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38 – 0x3A	Reserved for North Bridge initialization
0x3B	Post-Memory South Bridge initialization is started
0x3C -0x3E	Reserved for South Bridge
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error

Status Code	Description
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes

Status Code	Description
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

8.2.4. PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

8.2.5. DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64 – 0x67	Reserved for CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B – 0x6F	Reserved for North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73 – 0x77	Reserved for South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization

Status Code	Description
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)

Status Code	Description
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM

Status Code	Description
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

8.2.6. DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met (out of resource)

8.2.7. ACPI/ASL Checkpoint

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

8.3. OEM-Reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

9. Software Support

9.1. Windows 11 IoT Enterprise LTSC 2024 64-Bit

9.2. Yocto Linux 64-bit

https://github.com/ADLINK/meta-adlink-x86-64bit (TBC)

10. Mechanical and Thermal

10.1. Module Dimensions

Figure 5 – Module mechanical dimensions

10.2. Thermal Solutions

Note: The images will be updated later or are TBD.

10.2.1. Heatspreader: HTS

Dimensions: mm

Figure 6 – Heatspreader: HTS

10.2.2. Heatsink: THS

Dimensions: mm

Figure 7 – Heatsink: THS

10.2.3. Heatsink High Profile: THSH

Dimensions: mm

Figure 8 – Heatsink high profile: THSH

10.2.4. Heatsink with Fan: THSF

Dimensions: mm

Figure 9 – Heatsink with fan: THSF