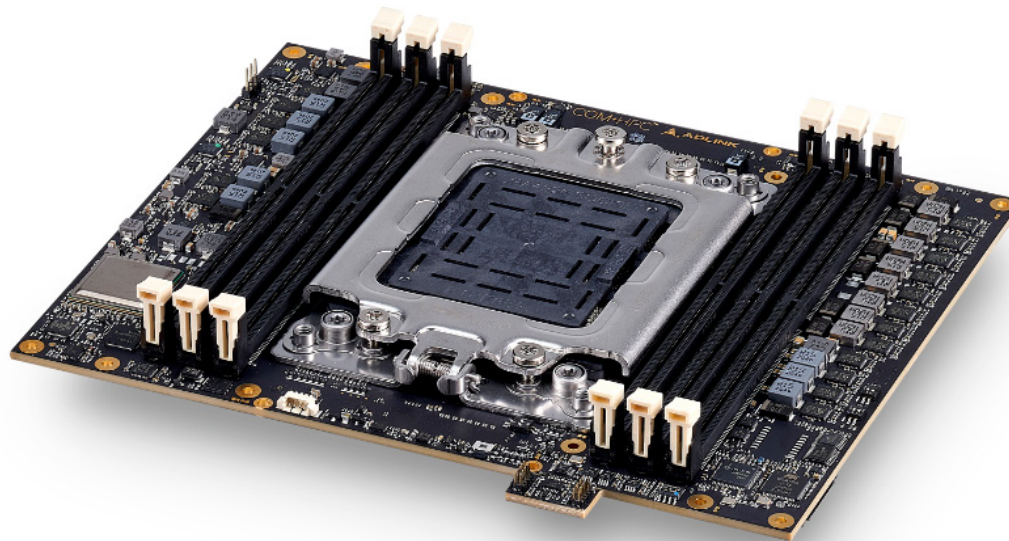


# COM-HPC-ALT

User's Guide



COM+HPC™

Revision: Rev. 1.1  
Date: 2025-07-30  
Part Number: 50M-00115-1010



## Revision History

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| Revision | Description                                                             | Date       | Author |
|----------|-------------------------------------------------------------------------|------------|--------|
| 1.0      | Initial release                                                         | 2023-01-10 | CC     |
| 1.1      | Pinout and signal descriptions and BIOS checkpoints, beep codes updated | 2025-07-30 | AL     |

## Preface

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For user safety, please read and follow all Instructions, **WARNINGS**, **CAUTIONS**, and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

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## Conventions

The following conventions may be used throughout this manual, denoting special levels of information



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**Note:** This information adds clarity or specifics to text and illustrations.

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**Caution:** This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

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**Warning:** This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

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# 1. Introduction

---



**Caution:** This is an EA (early available) engineering manual. The contents may not accurately reflect the actual or final version of this product.

---

ADLINK COM-HPC-ALT is a COM-HPC® Server Type Size E compliance module featuring Ampere® Altra® Series SoC. It supports up to 128 cores and boosts up to 2.6GHz based on 190W TDP while providing up to 384GB of RDIMM, UDIMM, LRDIMM DDR4 six-channel memory at up to 3200 MT/s in 6 DIMM sockets. These combined features make the COM-HPC-ALT well suited to customers who need uncompromising system performance and responsiveness embedded solutions with extended product life.

The COM-HPC-ALT features 4x 110G SFP+ interfaces by Broadcom BCM57502 (PCIex8 input, 4x 10G-KR output) and a single on-board Gigabit Ethernet port by Intel i210/i211 series. It features 64x PCIe Gen4 physical lanes, 4x USB 3.x upgrade signals, and 4x USB 2.0 ports

The COM-HPC-ALT features 1x GPP\_SPI and 1x Boot\_SPI, 1x SMBus, 2x I2C, 2x UART and 12x GPIO. No eSPI offered

The COM-HPC-ALT based discrete circuit and MMC (ATMEGA128), instead of CLPD, are supported by the module for power sequence control

The COM-HPC-ALT supports IPMB, which supports an MMC (module management controller, ATMEGA) and its firmware on the module. Combined with a dedicate 1x PCIe lane (it is called PCIe\_BMC), IPMB can enable Carrier BMC (for example, AST2500 or equivalent) and access necessary message (for example, voltage information and CPU temperature on module) between MMC and Carrier BMC. In addition, an EEPROM is located on I2C\_0 bus as a traditional COMe EEPROM usage and also as a FRU for Carrier BMC

One security chip is supported on the module. The traditional TPM 2.0, SPI based (same as Ampere Altra reference design) (it is on GP\_SPI bus)

The module is equipped with EDK2 (bootloader, open source) BIOS with CMOS backup, supporting embedded features such as remote console, hardware monitor, and watchdog timer.

No EC on this product.

## 2. Specifications

---

### 2.1 Core System

#### SoC

Ampere Computing, Ampere® Altra® Series Processors

- M128-26 128 cores, 2.6GHz, 190W TDP
- Q80-26 80 cores, 2.6GHz, 150W TDP
- Q64-22 64 cores, 2.2GHz, 95W TDP
- Q32-17 32 cores, 1.7GHz, 65W TDP

## Memory

Up to 384GB 3200 MT/s DDR4 in 6 DIMM sockets, Maximum 64GB per socket

Supports RDIMM, UDIMM and LRDIMM and 3DS

3 DIMM on the right side, the other 3 DIMMs on the left side

## Cache

1 MB L2 cache per core

32 MB system level cache

## Embedded BIOS

EDK2 UEFI with CMOS backup in 32 (or 16, TBC) MB SPI BIOS

## 2.2 Expansion Busses

### PCI Express

#### 64x PCIe lanes with 5x PCIe\_REFCLK / 5x PCIe\_CLKREQ

- Up to Gen4 speed
- PCIe 0-7      1 x4 or 2 x2 config at 0-3,    1 x4 or 2 x2 config at 4-7,      1 x8 config at 0-7      (from Root Complex B)
- PCIe 8-15    1 x4 or 2 x2 config at 8-11, 1 x4 or 2 x2 config at 12-15, 1 x8 config at 8-15      (from Root Complex B)
- PCIe 16-31   1 x16 or 2 x8 or 4 x4 config at 16-31,      (from Root Complex A)
- PCIe 32-47   1 x16 or 2 x8 or 4 x4 config at 32-47,      (from Root Complex A)
- PCIe 48-63   1 x16 or 2 x8 or 4 x4 config at 48-63,      (from Root Complex A)
- Lane polarity inversion

- 5x PCIe\_REFCLK/PCIe\_CLKREQ  
PCIe\_REFCLK0\_LO & PCIe\_CLKREQ0\_LO# : for PCIe lanes [0:7] and PCIe\_BMC  
PCIe\_REFCLK0\_HI & PCIe\_CLKREQ0\_HI# : for PCIe lanes [8:15]  
PCIe\_REFCLK1 & PCIe\_CLKREQ1# : for PCIe lanes [16:31]  
PCIe\_REFCLK2 & PCIe\_CLKREQ2# : for PCIe lanes [32:47]  
PCIe\_REFCLK3 & PCIe\_CLKREQ3# : for PCIe lanes [48:63]

---

 **Note:** Due to SoC orientation, the trace of PCIe 48-63 lanes over the PICMG specification marginally and may require re-driver on carrier.

---

### PCI Express Dedicated for Carrier BMC

1x PCIe lane (called PCIe\_BMC)

They can be used to connect the Carrier BMC (located on carrier) and combined with MMC (Module Management Controller, build option feature), such as voltage monitoring, power on/off, in the server applications.

### Boot SPI

1x Boot\_SPI, 2x Boot\_SPI\_CS dedicated for boot BIOS flash usage

SPI clock is either 20 MHz, 25 MHz, 33 MHz (Ampere Altra SOC only support up to 30MHz)

Support 3.3V of VCC\_BOOT\_SPI pin, if SPI flash on carrier is implemented, it shall be powered by VCC\_BOOT\_SPI pin

### BIOS Boot Selection

BIOS flash can be boot up at SPI bus, can be located at module or carrier or combined

## I2C

2x I2C, I2C 0 and I2C 1

I2C 0 additional offer ALERT# input and 3.3V power rail

(source from Ampere Altra SoC)

I2C 1 is 1.8V power rail

(source from Ampere Altra SoC)

Supports software programmable clock of 100 KHz (standard mode) and 400 KHz operation (fast mode)

Supports multi-master, allowing carrier to read the module's EEPROM before powering up the module

Support 7-bit and 10-bit address mode

An EEPROM is located on I2C 0, which can be used as Module EEPROM and IPMI FRU, combined together

## USB\_PD\_I2C

COM-HPC Module should support exporting Port 80 information over the USB\_PD I2C bus (signals USB\_OD\_I2C\_DAT and USB\_PD\_I2C\_CLK) to Carrier hardware that implements a pair of 7-segment displays to show the codes

The USB\_PD\_I2C comes from MMC ATMEGA128 and USB\_PD\_I2C, MMC and SOC connect to the same bus

## IPMB

1x IPMB comes from MMC. Please refer to section **2.9 Module Management Controller** for further details

IPMB is used with a Carrier BMC.

[MMC is ATMEGA solution that communicate with Ampere Altra SOC through UART](#)

Several monitored voltage (for example, memory voltage, CPU voltage) and temperature (for example, CPU temperature) can be communicated between MMC and Carrier BMC through IPMB.

A dedicated PCIe x1 lane is also available on the Carrier BMC, allowing the Carrier BMC to generate a VGA or other format video output, for management functions.

**General Purpose SPI**

1x GP\_SPI, 2x GP\_SPI\_CS

A TPM is located on GP\_SPI bus

**SM Bus**

1x SMBus comes from SoC I2C\_9 bus

## 2.3 Ethernet

**NBASE-T Ethernet**

Intel® Ethernet Controller i210/i211, connected to the SoC through PCIe lane

Supports 10/100/1000 Mbps data transfer rates, both full-duplex and half-duplex

Supports NBASET\_SDP, Software-Defined Pin. Can also be used for IEEE 1588 support such as 1pps signal

Supports Wake on LAN at S3/S4/S5

Supports PXE boot

**Ethernet KR/KX Interfaces**

Broadcom® Ethernet Controller BCM57502, connected to the SoC through PCIe x8 lane

4x 10GBASE-KR and its sideband signals

Supports both full-duplex and half-duplex

## 2.4 Multi I/O and Storage

### USB

Up to 4x USB 3.2 Gen1/2.0 (USB 0,1,2,3; via PCIe to USB IC) (the IC is Renesas uPD720201)  
SuperSpeedPlus, SuperSpeed, High-Speed, Full-Speed and Low-Speed USB signalling

### Asynchronous Serial Port

Two UART interfaces UART0 and UART1. UART0 supports TX RX RTS CTS. UART1 supports TX/RX  
Console Redirection UART0 or UART1 selectable in BIOS

Up to 2 serial ports are supported in standard BIOS including Super I/O on the carrier

| COM Port | Description                                    | IRQ | Address | Console Redirection Support |
|----------|------------------------------------------------|-----|---------|-----------------------------|
| COM 1    | Supported by module (SER0, A98/A99), via SOC   | 4   | 0x3F8   | Yes                         |
| COM 2    | Supported by module (SER1, A101/A102), via SOC | 3   | 0x2F8   | Yes                         |



**Note:** UART0, 1 both source from SOC. UART0 offers TX, RX, RTS#, CTS#. UART1 only offers TX and RX; its RTS#, CTS# are simulated by 2 GPIO from SOC.

### GPIO

12x GPIO

Supports GPI with interrupt

## 2.5 Others

### FAN Control

Control source is from MMC

FAN control is offered

### Health Monitoring

CPU temperature (through I2C3 of SOC) and board temperature are monitored by MMC.

8-10 voltage are monitored by EC, customer can get voltage information on BIOS menu and also shown in SEMA GUI and access it through SEMA API

1. CPU core
2. GFX core
3. Memory power
4. 5VSB (ROW AB/CD)
5. Main power (ROW AB/CD, 8.5V~20V or 5V~xxV)
6. 5VDUAL (CPU board)
7. 3.3VS (CPU board)
8. 3.3VSTBY (CPU board)
9. RTC battery (ROW AB/CD)
10. MAINPWRSENSE(For BMC calculate power consumption of the main power)

## 2.6 Security

This module offers one security-related chip on the module.

### Trusted Platform Module (TPM)

Chipset: Infineon solution

Type: TPM 2.0 (SPI bus based) (located on GP\_SPI)

## 2.7 Module Management Controller (MMC)

A Module Management Controller (MMC) is supported by default, which offers power sequence management and IPMB that can be connected to Carrier BMC for voltage, current, temperature, and other system information through IPMI protocol

The selected MMC is ATMEGA128A-MU (Microchip) (-40 to 85°C) solution.

MMC connects to SOC through UART interface

MMC connects to a HW monitor through I2C bus to monitor module's voltage, current and temperature

MMC only offers two I2C, one is used for USB\_PD\_I2C, the other used for IPMB.

### Overview

COM-HPC Module and Carrier boards **may** support out-of-band (OOB) management features. These features **may** be implemented on COM-HPC Server or Client systems. Traditionally OOB management is more of a server class feature, but the option is there for both COM-HPC Clients and Servers. There is a separate PICMG document that describes COM-HPC OOB management features in details — **PICMG COM-HPC Platform Management Interface Specification**. The management architecture is divided into BMC (Board Management Controller) and MMC (Module Management Controller), which are explained in the following sections.

**BMC (Board Management Controller)** (Located on Carrier board if deployed)

This is a microcontroller subsystem, usually based on the Carrier, that performs system out-of-band management functions such as firmware updates, power and reset control, performance monitoring and more. For COM-HPC module, which are hosted on the carrier, it **may** be a full subsystem with CPU / SOC, DRAM memory, an internal display controller and more. It **may** be ARM based. It **may** run a Linux or other OS. A popular vendor for this sort of BMC part is Aspeed, and in particular the Aspeed AST2510 and successor parts. Many other vendors and parts are possible.

It is anticipated that in most situations the BMC, if deployed, will be on the Carrier. Implementation of OOB management and a BMC on the Carrier is entirely optional. A Carrier based BMC is intended to work in conjunction with a Module based microcontroller referred to as the MMC (described below).

A Carrier BMC, if deployed, **shall** implement an IPMB interface to the COM-HPC Module. This is the channel for IPMI support. The Carrier BMC **may** also make use of the COM-HPC I2C0, USB, eSPI, NBASET0, UARTx and / or the PCIe\_BMC interfaces, as well as controlling the module power signals like PWRBTN, ...).

Any COM-HPC USB host port may be used to interface to a Carrier BMC USB client port. The Module USB port is usually a Module chipset or SOC host port, and not a MMC USB port. Designers **should** avoid using COM-HPC USB0, as it has special privileges allowing it to be used as a host or client. Designers **may want to** avoid using COM-HPC USB0, 1, 2, 3 as they are defined to allow USB SuperSpeed capability and BMC devices do not typically have USB SuperSpeed capability. USB4, 5, 6 or 7 **should** be used for the BMC interface if available.

Of the two COM-HPC UART interfaces that **may** be used to interface to a Carrier BMC, UART1 **should** be selected as UART0 is often used for functions such as Console Redirect.

#### **MMC (Module Management Controller)** (Located on COM-HPC Module, optional)

The MMC is a Module based microcontroller that **may** work in conjunction with a Carrier based BMC. If there is no Carrier BMC, then the MMC **shall** fall back to a mode that does not depend on the Carrier BMC, allowing the Module to function without external OOB management. The MMC **shall** be powered by the VCC\_5V\_SBY supply to allow for OOB functionality even when the main supply is not available, however, it **should** also use the main VCC rail, if available.

In most implementations, the MMC will be a relatively small low cost and low power device, in order to keep Module costs down for customers that do not require OOB management features. It **may** serve as a sensor aggregator. It **may** serve as host for nonvolatile Module parameter storage.

The MMC, if implemented, **shall** include an IPMB slave interface. It **may** additionally interface to the Carrier BMC over any of several other COM-HPC interfaces, including the I2C0 and or UART0 ports.

## Carrier and Module BMC and MMC Combinations

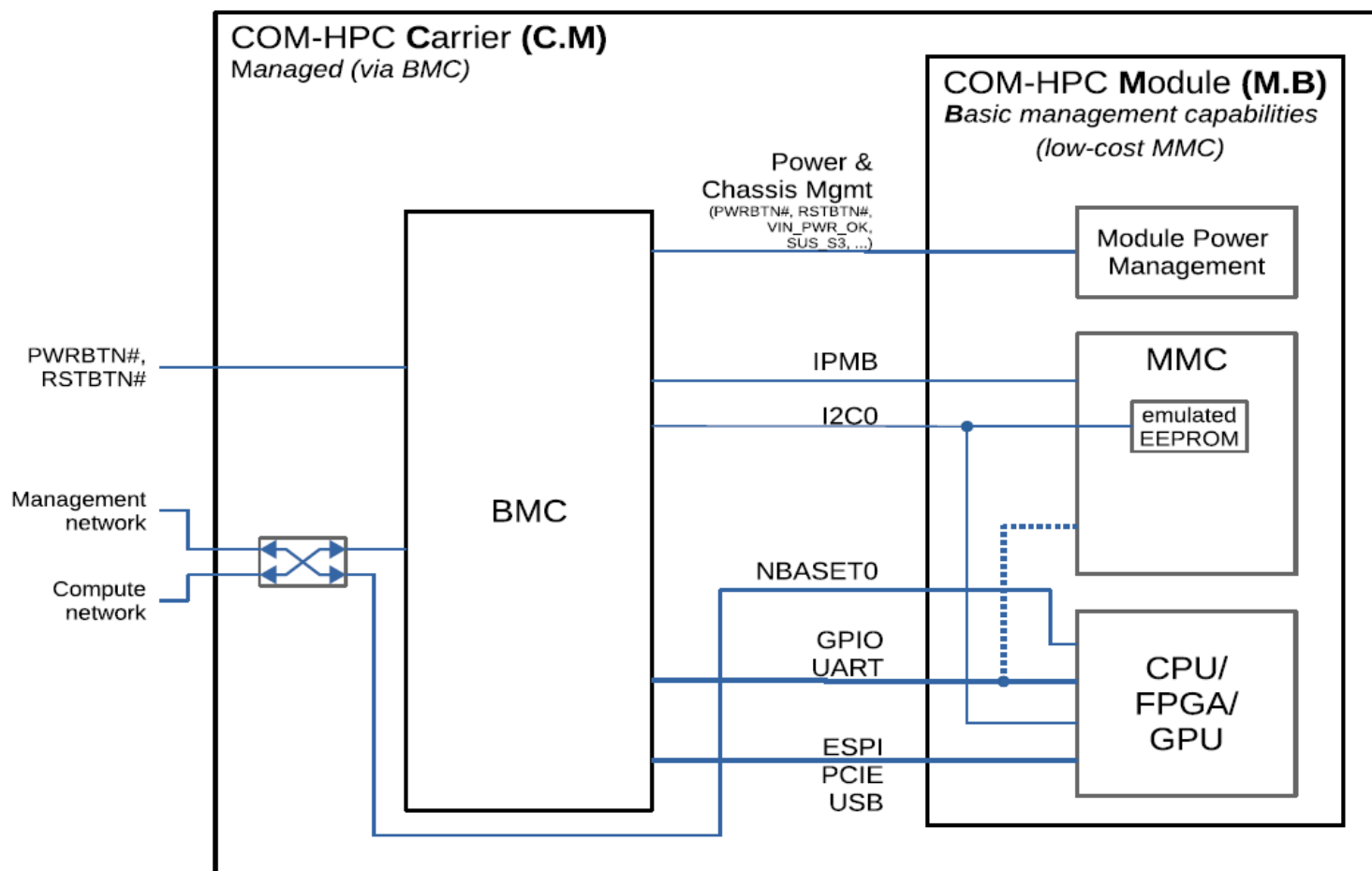
The **PICMG COM-HPC Platform Management Interface Specification** defines a number of different carrier and module options, which differ based on their management capabilities. Table 45 below lays out the options and defines a shorthand notation for the options. Full details are in the **PICMG COM-HPC Platform Management Interface Specification**.

Table 45: Carrier and Module BMC and MMC Combinations and Shorthand Notation

|         | Shorthand Notation | Description                                                                                                                                                                                                                                                                                                                                                                                            |
|---------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Carrier | C.U                | <ul style="list-style-type: none"> <li>Unmanaged</li> <li>The carrier has no BMC. Power and chassis management is typically done via a small microcontroller</li> <li>Management depends on the Module's capabilities</li> </ul>                                                                                                                                                                       |
|         | C.M                | <ul style="list-style-type: none"> <li>Managed via Carrier based BMC</li> <li>An IPMB communication channel to the MMC <b>shall</b> be implemented</li> <li>The BMC <b>may</b> also make use of the NBASET0, eSPI, USB, I2C0, UART0, PCIe_BMC, and / or the GPIO interfaces</li> <li>Provides Redfish to the outside (or IPMI for legacy)</li> <li>iKVM for the module via PCIe_BMC/USB</li> </ul>     |
| Module  | M.U                | <ul style="list-style-type: none"> <li>Unmanaged (No MMC)</li> <li><b>Should</b> implement a dedicated EEPROM (EeeP) for module identification</li> <li>CPU management possible via I2C0, NBASET0, eSPI, USB, UART0, GPIO, PCIe_BMC (all except IPMB), depending on the Carrier capabilities</li> </ul>                                                                                                |
|         | M.B                | <ul style="list-style-type: none"> <li>Basic Management capabilities via low cost MMC</li> <li>An IPMB interface to Carrier BMC <b>shall</b> be implemented</li> <li>Management via external interfaces (IPMB, I2C0, NBASET0, eSPI, USB, UART0, GPIO, PCIe_BMC)</li> </ul>                                                                                                                             |
|         | M.F                | <ul style="list-style-type: none"> <li>Full Management capabilities (typically via ARM-based OS)</li> <li>NBASET0 is shared by MMC and CPU (switched on Module), providing a high-speed OOB communication channel</li> <li>An IPMB interface to Carrier BMC <b>shall</b> be implemented</li> <li>Additional interfaces <b>may</b> be used (I2C0, NBASET0, eSPI, USB, UART0, GPIO, PCIe_BMC)</li> </ul> |

Assuming that the Types of the Carrier and Module match up (Server with Server, Client with Client) and the board sizes / connector positions match up (size A, B, C or size D,E) then a C.U or C.M Carrier shall be basically operable with a M.U or M.B or M.F Module. The OOB management features may be missing, depending on what is matched with what. Additionally, there will likely be some vendor specific aspects to OOB management options.

**M.B Module and C.M Carrier will be implemented at ADLINK COM-HPC Server Module and COM-HPC Server Carrier as first wave.**



## IPMI on COM-HPC

The COM-HPC management platform **shall** use an IPMI (Intelligent Platform Management Interface) for communication between the Carrier BMC and MMC, over the COM-HPC IPMB port. The interface from the BMC to the user is independent from this, and **may** be realized using Redfish, it **may** support IPMI for legacy support. The interface used for IPMI between BMC and MMC **shall** be IPMB (an I2C bus specifically for IPMI use).

A set of IPMI commands for communication between MMC and BMC have been defined in the **PICMG COM-HPC Platform Management Interface Specification**. Most of those commands are not specific to COM-HPC, but defined in the IPMI specification and related specifications. However, also some COM-HPC specific commands have been developed. Specifically, the following command sets are covered:

- IPM Device Global Commands: Initialization and module discovery
- BMC Watchdog and Device and Messaging Commands: System interface and BMC interaction.
- Chassis Device Commands: Power control and boot options
- Event Commands: IPMI event handling
- PEF and Alerting Commands: Alerting and trigger support
- Sensor Device Commands: Sensor monitoring and housekeeping
- FRU Device Commands: Inventory data
- SDR Device Commands: Sensor information
- SEL Device Commands: System event logging
- LAN Device Commands and HPM.2: Support for Ethernet
- Serial/Modem Device Commands: For UART and SOL support
- AdvancedTCA subset: For Fan Management
- HPM.1: For Firmware update
- HPM.2: For managing BMC-MMC Ethernet communication
- COM-HPC specific Commands: For fast sensors and JTAG support

The inventory data available via IPMI FRU also includes information present in the COM-HPC EEPROM (see Section **Error! Bookmark not defined.**). The COM-HPC EEPROM content is defined in the **PICMG Embedded EEPROM for COM-HPC** document, a companion document to the **PICMG COM-HPC Platform Management Interface Specification**. The information available in the COM-HPC EEPROM area will be converted from EeeP format into IPMI FRU data structures by the MMC. In order to accomplish this, the MMC reads the data from the EEPROM during start of the system, and buffers the data internally to service incoming IPMI FRU accesses.

The EEPROM area for storing EeeP data **may** be implemented as a physical EEPROM on the board, on the I2C0 bus. Alternatively, it **may** be realized within the MMC. This is illustrated in Figure 10 above. In that figure, it is labeled as an “emulated EEPROM”. An I2C slave interface on the MMC is connected to the I2C0 bus of the COM-HPC module. This eases implementation, as the MMC does not need to fetch information from the physical COM-HPC EEPROM, and also prevents potential access conflicts between the MMC and other I2C agents on the Baseboard or Carrier. The MMC implemented this way does not need I2C Master or Multi-Master capability.

### COM-HPC EEPROM

Modules and Carriers for COM-HPC **should** implement an EEPROM which allows the identification of Module or Carrier features via I2C. This feature is similar to the COM Express EEPROM defined in the PICMG COM Express specification. Some Module vendors will find a benefit in software reuse with test scripts and software infrastructure developed for COM Express use. The COM-HPC EEPROM content is defined in the **EeeP for COM-HPC** (Embedded EEPROM for COM-HPC) document, a companion document to the **PICMG COM-HPC Platform Management Interface Specification**. The **EeeP for COM-HPC** specification is derived from the **EeeP for COM-Express** document and introduces new data structures specific to COM-HPC modules and carriers, while the data structures for COM Express modules and carriers remain untouched. A new revision has been assigned to distinguish between COM Express and COM-HPC EEPROMs.

### EEPROM Device Information

If the COM Express Module and / or Carrier EEPROMs are implemented on COM-HPC, then the COM-HPC I2C0 port **shall** be used to interface to the EEPROMs. The EEPROM devices **shall** have a capacity of at least 32 Kbits, and **shall** have three address inputs. Suitable devices include the Atmel AT24C32C, the ST M24C32 and other compatible devices. Larger capacity devices may be used if they are compatible with the base 32 Kbit part referenced above.

### COM-HPC Module EEPROM

The Module **should** implement a serial EEPROM that identifies the Module using the EeeP defined Unique Device ID. In addition this EEPROM **should** describe the available module interfaces and capabilities as described in the **EeeP for COM-HPC** specification. The EEPROM **may** be implemented as a physical EEPROM on the board, or may be realized within the MMC (see Section **Error! Bookmark not defined.**).

The Module EEPROM allows the Carrier Board to set up any software configurable Carrier Board features in a way that is appropriate for the Module board. The Module EEPROM I2C device address lines, A2, A1 and A0 **shall** be pulled to a logic low, placing the device at address 0x50 (7 bit I2C addressing) and address 0xA0 (8 bit I2C addressing). **Note:** I2C address A6-A3 are fixed at 1010b for I2C EEPROM devices per the I2C specification.

## COM-HPC Carrier Board EEPROM

The Carrier Board **should** implement a serial EEPROM that identifies the Carrier using the Unique Device Id and describes the expected PCI Express link configuration. In addition this EEPROM **may** describe the expected link presence for SATA, USB, DDI, VGA, LAN, audio, and the expected presence of miscellaneous I/O signals. The EEPROM **may** be implemented as a physical EEPROM on the board, or **may** be realized within the BMC (see Section **Error! Bookmark not defined.**).

The Carrier EEPROM allows the Module firmware to set up any software configurable Module features in a way that is appropriate for the Carrier Board. If there is an incompatibility between the expected Carrier Board configuration and the Module capabilities, an error message **may** be generated. The error messaging is Module vendor specific and is not defined by this standard.

The Carrier EEPROM device address lines, A2, A1 and A0 **shall** be pulled to a logic high, placing the device at address 0x57 (7 bit addressing) and 0xAE (8 bit addressing). I2C addresses A6-A3 are fixed at 1010b for I2C EEPROM devices.

## 2.8 Debug

40 pin flat cable connector to be used with DB40 HPC debug module

Supports BIOS POST code LED, BMC access, SPI BIOS flashing, internal power rail test points, debug LEDs

## 2.9 Power

Power Modes: AT and ATX mode

Standard Voltage Input: ATX 12V±5% / 5Vsb ±5% or AT 12V±5%

Power Management: ACPI 5.0 compliant, Smart Battery support

Power States: C1-C6, S0, S1, S5, S5 ECO mode (Wake-on-USB, WoL S5)

ECO Mode support for deep S5 for 5Vsb power saving

## 2.10 Mechanical and Environmental

### Form Factor and Specification

PICMG COM-HPC Rev 1.0, Server Type, Size D 200 x 160 mm

### Operating Temperature

|            |                      |                        |
|------------|----------------------|------------------------|
| Standard   | 0°C to 60°C at 12V   | Storage: -20°C to 80°C |
| Industrial | -20°C to 70°C at 12V | Storage: -20°C to 80°C |

Operate at -40°C to 85°C at 12V is by project basis discussion

### Humidity

5-90% RH operating, non-condensing, 5-95% RH storage (and operating with conformal coating)

### Shock and Vibration

IEC 60068-2-64 and IEC-60068-2-27

MIL-STD-202F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D

### HALT tested

Thermal Stress, Vibration Stress, Thermal Shock and Combined Test

### EMI

EN55032 Class B inside an enclosure

Ultrasound equipment will typically be sensitive to noise in the 1MHz to 20MHz band, we shall handle it well during these bands

**De-rating**

De-rating file is provided by RD (delta temperature of some of components is based on the experience of previous products) and reviewed/approved by RRC team before each Gerber Out

Once we have real sample on-hand, the temperature of critical components shall be measured and feedback to the De-rating file to see if it still in specification.

**MTBF**

200,000 hrs commercial 40°C ambient (according MIL calculation) based on actual calculated de-rating

120,000 hrs ETT -20°C~70°C ambient (according MIL calculation) based on actual calculated de-rating (excludes the BCM57504 LAN controller)



## 4. Pinout and Signal Descriptions

### 4.1 Pin Summary

The below table is a comprehensive list of all signal pins supported on the dual 400-pin COM-HPC connectors (J1 and J2) as defined for Server Type in the PICMG COM-HPC Rev 1.0 specification. Signals described in the specification but not supported on the COM-HPC-ALT are marked by ~~strikethrough~~ ROW A/B/C/D on J1 connector, ROW E/F/G/H on J2 connector

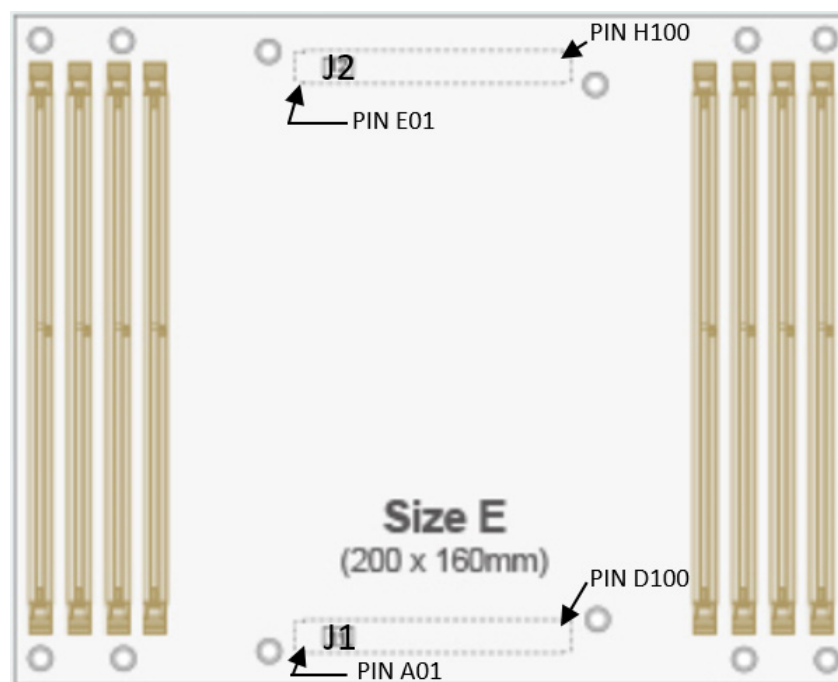


Figure 2 – Rear side row

| Row A |          | Row B |                | Row C |              | Row D |            |
|-------|----------|-------|----------------|-------|--------------|-------|------------|
| A1    | VCC      | B1    | VCC            | C1    | VCC          | D1    | VCC        |
| A2    | VCC      | B2    | PWRBTN#        | C2    | RSTBTN#      | D2    | VCC        |
| A3    | VCC      | B3    | VCC            | C3    | VCC          | D3    | VCC        |
| A4    | VCC      | B4    | THERMTRIP#     | C4    | CARRIER_HOT# | D4    | VCC        |
| A5    | VCC      | B5    | VCC            | C5    | VCC          | D5    | VCC        |
| A6    | VCC      | B6    | TAMPER#        | C6    | VIN_PWR_OK   | D6    | VCC        |
| A7    | VCC      | B7    | VCC            | C7    | VCC          | D7    | VCC        |
| A8    | VCC      | B8    | SUS_S3#        | C8    | SUS_S4_S5#   | D8    | VCC        |
| A9    | VCC      | B9    | VCC            | C9    | VCC          | D9    | VCC        |
| A10   | GND      | B10   | WD_STROBE#     | C10   | GND          | D10   | WAKE0#     |
| A11   | BATLOW#  | B11   | WD_OUT         | C11   | FAN_PWMOUT   | D11   | WAKE1#     |
| A12   | PLTRST#  | B12   | GND            | C12   | FAN_TACHIN   | D12   | GND        |
| A13   | GND      | B13   | USB5-          | C13   | GND          | D13   | USB1-      |
| A14   | USB7-    | B14   | USB5+          | C14   | USB3-        | D14   | USB1+      |
| A15   | USB7+    | B15   | GND            | C15   | USB3+        | D15   | GND        |
| A16   | GND      | B16   | USB4-          | C16   | GND          | D16   | USB0-      |
| A17   | USB6-    | B17   | USB4+          | C17   | USB2-        | D17   | USB0+      |
| A18   | USB6+    | B18   | GND            | C18   | USB2+        | D18   | GND        |
| A19   | GND      | B19   | RSVD           | C19   | GND          | D19   | ETH0_RX-   |
| A20   | ETH4_RX- | B20   | RSVD           | C20   | ETH0_TX-     | D20   | ETH0_RX+   |
| A21   | ETH4_RX+ | B21   | RSVD           | C21   | ETH0_TX+     | D21   | GND        |
| A22   | GND      | B22   | RSVD           | C22   | GND          | D22   | ETH1_RX-   |
| A23   | ETH5_RX- | B23   | RSVD           | C23   | ETH1_TX-     | D23   | ETH1_RX+   |
| A24   | ETH5_RX+ | B24   | VCC_5V_SBY     | C24   | ETH1_TX+     | D24   | GND        |
| A25   | GND      | B25   | USB67_OC#      | C25   | GND          | D25   | ETH2_RX-   |
| A26   | ETH6_RX- | B26   | USB45_OC#      | C26   | ETH2_TX-     | D26   | ETH2_RX+   |
| A27   | ETH6_RX+ | B27   | USB23_OC#      | C27   | ETH2_TX+     | D27   | GND        |
| A28   | GND      | B28   | USB01_OC#      | C28   | GND          | D28   | ETH3_RX-   |
| A29   | ETH7_RX- | B29   | SML1_CLK       | C29   | ETH3_TX-     | D29   | ETH3_RX+   |
| A30   | ETH7_RX+ | B30   | SML1_DAT       | C30   | ETH3_TX+     | D30   | GND        |
| A31   | GND      | B31   | PMCALERT#      | C31   | GND          | D31   | USB3_SSTX- |
| A32   | RSVD     | B32   | SML0_CLK       | C32   | USB3_SSRX-   | D32   | USB3_SSTX+ |
| A33   | RSVD     | B33   | SML0_DAT       | C33   | USB3_SSRX+   | D33   | GND        |
| A34   | GND      | B34   | USB_PD_ALERT#  | C34   | GND          | D34   | USB2_SSTX- |
| A35   | ETH4_TX- | B35   | USB_PD_I2C_CLK | C35   | USB2_SSRX-   | D35   | USB2_SSTX+ |
| A36   | ETH4_TX+ | B36   | USB_PD_I2C_DAT | C36   | USB2_SSRX+   | D36   | GND        |

| Row A |                  | Row B |              | Row C |                  | Row D |             |
|-------|------------------|-------|--------------|-------|------------------|-------|-------------|
| A37   | GND              | B37   | USB_RT_ENA   | C37   | GND              | D37   | USB1_SSTX0- |
| A38   | ETH5_TX-         | B38   | USB1_LSRX    | C38   | USB1_SSRX0-      | D38   | USB1_SSTX0+ |
| A39   | ETH5_TX+         | B39   | USB1_LSTX    | C39   | USB1_SSRX0+      | D39   | GND         |
| A40   | GND              | B40   | USB0_LSRX    | C40   | GND              | D40   | USB1_SSTX1- |
| A41   | ETH6_TX-         | B41   | USB0_LSTX    | C41   | USB1_SSRX1-      | D41   | USB1_SSTX1+ |
| A42   | ETH6_TX+         | B42   | GND          | C42   | USB1_SSRX1+      | D42   | GND         |
| A43   | GND              | B43   | USB0_AUX-    | C43   | GND              | D43   | USB0_SSTX0- |
| A44   | ETH7_TX-         | B44   | USB0_AUX+    | C44   | USB0_SSRX0-      | D44   | USB0_SSTX0+ |
| A45   | ETH7_TX+         | B45   | RSVD         | C45   | USB0_SSRX0+      | D45   | GND         |
| A46   | GND              | B46   | RSVD         | C46   | GND              | D46   | USB0_SSTX1- |
| A47   | USB1_AUX-        | B47   | VCC_BOOT_SPI | C47   | USB0_SSRX1-      | D47   | USB0_SSTX1+ |
| A48   | USB1_AUX+        | B48   | BOOT_SPI_CS# | C48   | USB0_SSRX1+      | D48   | GND         |
| A49   | GND              | B49   | BSEL0        | C49   | GND              | D49   | SATA0_RX-   |
| A50   | eSPI_IO0         | B50   | BSEL1        | C50   | BOOT_SPI_IO0     | D50   | SATA0_RX+   |
| A51   | eSPI_IO1         | B51   | BSEL2        | C51   | BOOT_SPI_IO1     | D51   | GND         |
| A52   | eSPI_IO2         | B52   | eSPI_ALERT0# | C52   | BOOT_SPI_IO2     | D52   | SATA0_TX-   |
| A53   | eSPI_IO3         | B53   | eSPI_ALERT1# | C53   | BOOT_SPI_IO3     | D53   | SATA0_TX+   |
| A54   | eSPI_CLK         | B54   | eSPI_CS0#    | C54   | BOOT_SPI_CLK     | D54   | GND         |
| A55   | GND              | B55   | eSPI_CS1#    | C55   | GND              | D55   | SATA1_RX-   |
| A56   | PCIe_CLKREQ0_LO# | B56   | eSPI_RST#    | C56   | PCIe_REFCLK0_HI- | D56   | SATA1_RX+   |
| A57   | PCIe_CLKREQ0_HI# | B57   | GND          | C57   | PCIe_REFCLK0_HI+ | D57   | GND         |
| A58   | GND              | B58   | PCIe_BMC_RX- | C58   | GND              | D58   | SATA1_TX-   |
| A59   | PCIe_BMC_TX-     | B59   | PCIe_BMC_RX+ | C59   | PCIe_REFCLK0_LO- | D59   | SATA1_TX+   |
| A60   | PCIe_BMC_TX+     | B60   | GND          | C60   | PCIe_REFCLK0_LO+ | D60   | GND         |
| A61   | GND              | B61   | PCIe08_RX-   | C61   | GND              | D61   | PCIe00_TX-  |
| A62   | PCIe08_TX-       | B62   | PCIe08_RX+   | C62   | PCIe00_RX-       | D62   | PCIe00_TX+  |
| A63   | PCIe08_TX+       | B63   | GND          | C63   | PCIe00_RX+       | D63   | GND         |
| A64   | GND              | B64   | PCIe09_RX-   | C64   | GND              | D64   | PCIe01_TX-  |
| A65   | PCIe09_TX-       | B65   | PCIe09_RX+   | C65   | PCIe01_RX-       | D65   | PCIe01_TX+  |
| A66   | PCIe09_TX+       | B66   | GND          | C66   | PCIe01_RX+       | D66   | GND         |
| A67   | GND              | B67   | PCIe10_RX-   | C67   | GND              | D67   | PCIe02_TX-  |
| A68   | PCIe10_TX-       | B68   | PCIe10_RX+   | C68   | PCIe02_RX-       | D68   | PCIe02_TX+  |
| A69   | PCIe10_TX+       | B69   | GND          | C69   | PCIe02_RX+       | D69   | GND         |
| A70   | GND              | B70   | PCIe11_RX-   | C70   | GND              | D70   | PCIe03_TX-  |
| A71   | PCIe11_TX-       | B71   | PCIe11_RX+   | C71   | PCIe03_RX-       | D71   | PCIe03_TX+  |
| A72   | PCIe11_TX+       | B72   | GND          | C72   | PCIe03_RX+       | D72   | GND         |

| Row A |                    | Row B |                       | Row C |                          | Row D |                   |
|-------|--------------------|-------|-----------------------|-------|--------------------------|-------|-------------------|
| A73   | GND                | B73   | PCIe12_RX-            | C73   | GND                      | D73   | PCIe04_TX-        |
| A74   | PCIe12_TX-         | B74   | PCIe12_RX+            | C74   | PCIe04_RX-               | D74   | PCIe04_TX+        |
| A75   | PCIe12_TX+         | B75   | GND                   | C75   | PCIe04_RX+               | D75   | GND               |
| A76   | GND                | B76   | PCIe13_RX-            | C76   | GND                      | D76   | PCIe05_TX-        |
| A77   | PCIe13_TX-         | B77   | PCIe13_RX+            | C77   | PCIe05_RX-               | D77   | PCIe05_TX+        |
| A78   | PCIe13_TX+         | B78   | GND                   | C78   | PCIe05_RX+               | D78   | GND               |
| A79   | GND                | B79   | PCIe14_RX-            | C79   | GND                      | D79   | PCIe06_TX-        |
| A80   | PCIe14_TX-         | B80   | PCIe14_RX+            | C80   | PCIe06_RX-               | D80   | PCIe06_TX+        |
| A81   | PCIe14_TX+         | B81   | GND                   | C81   | PCIe06_RX+               | D81   | GND               |
| A82   | GND                | B82   | PCIe15_RX-            | C82   | GND                      | D82   | PCIe07_TX-        |
| A83   | PCIe15_TX-         | B83   | PCIe15_RX+            | C83   | PCIe07_RX-               | D83   | PCIe07_TX+        |
| A84   | PCIe15_TX+         | B84   | GND                   | C84   | PCIe07_RX+               | D84   | GND               |
| A85   | GND                | B85   | RSVD                  | C85   | GND                      | D85   | NBASET0_MDI0-     |
| A86   | VCC_RTC            | B86   | RSMRST_OUT#           | C86   | SMB_CLK                  | D86   | NBASET0_MDI0+     |
| A87   | <del>SUS_CLK</del> | B87   | UART1_TX              | C87   | SMB_DAT                  | D87   | GND               |
| A88   | GPIO_00            | B88   | UART1_RX              | C88   | SMB_ALERT#               | D88   | NBASET0_MDI1-     |
| A89   | GPIO_01            | B89   | UART1_RTS#            | C89   | UART0_TX                 | D89   | NBASET0_MDI1+     |
| A90   | GPIO_02            | B90   | UART1_CTS#            | C90   | UART0_RX                 | D90   | GND               |
| A91   | GPIO_03            | B91   | IPMB_CLK              | C91   | UART0_RTS#               | D91   | NBASET0_MDI2-     |
| A92   | GPIO_04            | B92   | IPMB_DAT              | C92   | UART0_CTS#               | D92   | NBASET0_MDI2+     |
| A93   | GPIO_05            | B93   | GPSPI_MOSI            | C93   | I2C0_CLK                 | D93   | GND               |
| A94   | GPIO_06            | B94   | GPSPI_MISO            | C94   | I2C0_DAT                 | D94   | NBASET0_MDI3-     |
| A95   | GPIO_07            | B95   | GPSPI_CS0#            | C95   | I2C0_ALERT#              | D95   | NBASET0_MDI3+     |
| A96   | GPIO_08            | B96   | GPSPI_CS1#            | C96   | I2C1_CLK                 | D96   | GND               |
| A97   | GPIO_09            | B97   | <del>GPSPI_CS2#</del> | C97   | I2C1_DAT                 | D97   | NBASET0_LINK_MAX# |
| A98   | GPIO_10            | B98   | <del>GPSPI_CS3#</del> | C98   | NBASET0_SDP              | D98   | NBASET0_LINK_MID# |
| A99   | GPIO_11            | B99   | GPSPI_CLK             | C99   | <del>NBASET0_CTREF</del> | D99   | NBASET0_LINK_ACT# |
| A100  | TYPE0              | B100  | GPSPI_ALERT#          | C100  | TYPE1                    | D100  | TYPE2             |

| Row E |                | Row F |                 | Row G |            | Row H |            |
|-------|----------------|-------|-----------------|-------|------------|-------|------------|
| E1    | RAPID_SHUTDOWN | F1    | ETH2_SDP        | G1    | RSVD       | H1    | RSVD       |
| E2    | GND            | F2    | ETH3_SDP        | G2    | RSVD       | H2    | RSVD       |
| E3    | RSVD           | F3    | ETH4_SDP        | G3    | RSVD       | H3    | RSVD       |
| E4    | RSVD           | F4    | ETH5_SDP        | G4    | RSVD       | H4    | RSVD       |
| E5    | GND            | F5    | ETH6_SDP        | G5    | RSVD       | H5    | RSVD       |
| E6    | RSVD           | F6    | ETH7_SDP        | G6    | RSVD       | H6    | RSVD       |
| E7    | RSVD           | F7    | ETH4_7_I2C_CLK  | G7    | RSVD       | H7    | RSVD       |
| E8    | GND            | F8    | ETH4_7_I2C_DAT  | G8    | RSVD       | H8    | RSVD       |
| E9    | RSVD           | F9    | ETH4_7_INT#     | G9    | RSVD       | H9    | RSVD       |
| E10   | RSVD           | F10   | ETH4_7_MDIO_CLK | G10   | RSVD       | H10   | RSVD       |
| E11   | GND            | F11   | ETH4_7_MDIO_DAT | G11   | RSVD       | H11   | RSVD       |
| E12   | RSVD           | F12   | ETH4_7_PHY_INT# | G12   | RSVD       | H12   | RSVD       |
| E13   | RSVD           | F13   | ETH4_7_PHY_RST# | G13   | RSVD       | H13   | RSVD       |
| E14   | GND            | F14   | ETH4_7_PRSNT#   | G14   | GND        | H14   | RSVD       |
| E15   | RSVD           | F15   | RSVD            | G15   | RSVD       | H15   | RSVD       |
| E16   | RSVD           | F16   | RSVD            | G16   | RSVD       | H16   | RSVD       |
| E17   | GND            | F17   | RSVD            | G17   | RSVD       | H17   | RSVD       |
| E18   | RSVD           | F18   | RSVD            | G18   | RSVD       | H18   | RSVD       |
| E19   | RSVD           | F19   | GND             | G19   | RSVD       | H19   | GND        |
| E20   | GND            | F20   | PCIe32_RX-      | G20   | GND        | H20   | PCIe40_TX- |
| E21   | PCIe32_TX-     | F21   | PCIe32_RX+      | G21   | PCIe40_RX- | H21   | PCIe40_TX+ |
| E22   | PCIe32_TX+     | F22   | GND             | G22   | PCIe40_RX+ | H22   | GND        |
| E23   | GND            | F23   | PCIe33_RX-      | G23   | GND        | H23   | PCIe41_TX- |
| E24   | PCIe33_TX-     | F24   | PCIe33_RX+      | G24   | PCIe41_RX- | H24   | PCIe41_TX+ |
| E25   | PCIe33_TX+     | F25   | GND             | G25   | PCIe41_RX+ | H25   | GND        |
| E26   | GND            | F26   | PCIe34_RX-      | G26   | GND        | H26   | PCIe42_TX- |
| E27   | PCIe34_TX-     | F27   | PCIe34_RX+      | G27   | PCIe42_RX- | H27   | PCIe42_TX+ |
| E28   | PCIe34_TX+     | F28   | GND             | G28   | PCIe42_RX+ | H28   | GND        |
| E29   | GND            | F29   | PCIe35_RX-      | G29   | GND        | H29   | PCIe43_TX- |
| E30   | PCIe35_TX-     | F30   | PCIe35_RX+      | G30   | PCIe43_RX- | H30   | PCIe43_TX+ |
| E31   | PCIe35_TX+     | F31   | GND             | G31   | PCIe43_RX+ | H31   | GND        |
| E32   | GND            | F32   | PCIe36_RX-      | G32   | GND        | H32   | PCIe44_TX- |
| E33   | PCIe36_TX-     | F33   | PCIe36_RX+      | G33   | PCIe44_RX- | H33   | PCIe44_TX+ |
| E34   | PCIe36_TX+     | F34   | GND             | G34   | PCIe44_RX+ | H34   | GND        |
| E35   | GND            | F35   | PCIe37_RX-      | G35   | GND        | H35   | PCIe45_TX- |
| E36   | PCIe37_TX-     | F36   | PCIe37_RX+      | G36   | PCIe45_RX- | H36   | PCIe45_TX+ |

| Row E |            | Row F |            | Row G |            | Row H |            |
|-------|------------|-------|------------|-------|------------|-------|------------|
| E37   | PCle37_TX+ | F37   | GND        | G37   | PCle45_RX+ | H37   | GND        |
| E38   | GND        | F38   | PCle38_RX- | G38   | GND        | H38   | PCle46_TX- |
| E39   | PCle38_TX- | F39   | PCle38_RX+ | G39   | PCle46_RX- | H39   | PCle46_TX+ |
| E40   | PCle38_TX+ | F40   | GND        | G40   | PCle46_RX+ | H40   | GND        |
| E41   | GND        | F41   | PCle39_RX- | G41   | GND        | H41   | PCle47_TX- |
| E42   | PCle39_TX- | F42   | PCle39_RX+ | G42   | PCle47_RX- | H42   | PCle47_TX+ |
| E43   | PCle39_TX+ | F43   | GND        | G43   | PCle47_RX+ | H43   | GND        |
| E44   | GND        | F44   | PCle16_RX- | G44   | GND        | H44   | PCle24_TX- |
| E45   | PCle16_TX- | F45   | PCle16_RX+ | G45   | PCle24_RX- | H45   | PCle24_TX+ |
| E46   | PCle16_TX+ | F46   | GND        | G46   | PCle24_RX+ | H46   | GND        |
| E47   | GND        | F47   | PCle17_RX- | G47   | GND        | H47   | PCle25_TX- |
| E48   | PCle17_TX- | F48   | PCle17_RX+ | G48   | PCle25_RX- | H48   | PCle25_TX+ |
| E49   | PCle17_TX+ | F49   | GND        | G49   | PCle25_RX+ | H49   | GND        |
| E50   | GND        | F50   | PCle18_RX- | G50   | GND        | H50   | PCle26_TX- |
| E51   | PCle18_TX- | F51   | PCle18_RX+ | G51   | PCle26_RX- | H51   | PCle26_TX+ |
| E52   | PCle18_TX+ | F52   | GND        | G52   | PCle26_RX+ | H52   | GND        |
| E53   | GND        | F53   | PCle19_RX- | G53   | GND        | H53   | PCle27_TX- |
| E54   | PCle19_TX- | F54   | PCle19_RX+ | G54   | PCle27_RX- | H54   | PCle27_TX+ |
| E55   | PCle19_TX+ | F55   | GND        | G55   | PCle27_RX+ | H55   | GND        |
| E56   | GND        | F56   | PCle20_RX- | G56   | GND        | H56   | PCle28_TX- |
| E57   | PCle20_TX- | F57   | PCle20_RX+ | G57   | PCle28_RX- | H57   | PCle28_TX+ |
| E58   | PCle20_TX+ | F58   | GND        | G58   | PCle28_RX+ | H58   | GND        |
| E59   | GND        | F59   | PCle21_RX- | G59   | GND        | H59   | PCle29_TX- |
| E60   | PCle21_TX- | F60   | PCle21_RX+ | G60   | PCle29_RX- | H60   | PCle29_TX+ |
| E61   | PCle21_TX+ | F61   | GND        | G61   | PCle29_RX+ | H61   | GND        |
| E62   | GND        | F62   | PCle22_RX- | G62   | GND        | H62   | PCle30_TX- |
| E63   | PCle22_TX- | F63   | PCle22_RX+ | G63   | PCle30_RX- | H63   | PCle30_TX+ |
| E64   | PCle22_TX+ | F64   | GND        | G64   | PCle30_RX+ | H64   | GND        |
| E65   | GND        | F65   | PCle23_RX- | G65   | GND        | H65   | PCle31_TX- |
| E66   | PCle23_TX- | F66   | PCle23_RX+ | G66   | PCle31_RX- | H66   | PCle31_TX+ |
| E67   | PCle23_TX+ | F67   | GND        | G67   | PCle31_RX+ | H67   | GND        |
| E68   | GND        | F68   | PCle48_RX- | G68   | GND        | H68   | PCle56_TX- |
| E69   | PCle48_TX- | F69   | PCle48_RX+ | G69   | PCle56_RX- | H69   | PCle56_TX+ |
| E70   | PCle48_TX+ | F70   | GND        | G70   | PCle56_RX+ | H70   | GND        |
| E71   | GND        | F71   | PCle49_RX- | G71   | GND        | H71   | PCle57_TX- |
| E72   | PCle49_TX- | F72   | PCle49_RX+ | G72   | PCle57_RX- | H72   | PCle57_TX+ |

| Row E |                              | Row F |                     | Row G |                           | Row H |                            |
|-------|------------------------------|-------|---------------------|-------|---------------------------|-------|----------------------------|
| E73   | PCle49_TX+                   | F73   | GND                 | G73   | PCle57_RX+                | H73   | GND                        |
| E74   | GND                          | F74   | PCle50_RX-          | G74   | GND                       | H74   | PCle58_TX-                 |
| E75   | PCle50_TX-                   | F75   | PCle50_RX+          | G75   | PCle58_RX-                | H75   | PCle58_TX+                 |
| E76   | PCle50_TX+                   | F76   | GND                 | G76   | PCle58_RX+                | H76   | GND                        |
| E77   | GND                          | F77   | PCle51_RX-          | G77   | GND                       | H77   | PCle59_TX-                 |
| E78   | PCle51_TX-                   | F78   | PCle51_RX+          | G78   | PCle59_RX-                | H78   | PCle59_TX+                 |
| E79   | PCle51_TX+                   | F79   | GND                 | G79   | PCle59_RX+                | H79   | GND                        |
| E80   | GND                          | F80   | PCle52_RX-          | G80   | GND                       | H80   | PCle60_TX-                 |
| E81   | PCle52_TX-                   | F81   | PCle52_RX+          | G81   | PCle60_RX-                | H81   | PCle60_TX+                 |
| E82   | PCle52_TX+                   | F82   | GND                 | G82   | PCle60_RX+                | H82   | GND                        |
| E83   | GND                          | F83   | PCle53_RX-          | G83   | GND                       | H83   | PCle61_TX-                 |
| E84   | PCle53_TX-                   | F84   | PCle53_RX+          | G84   | PCle61_RX-                | H84   | PCle61_TX+                 |
| E85   | PCle53_TX+                   | F85   | GND                 | G85   | PCle61_RX+                | H85   | GND                        |
| E86   | GND                          | F86   | PCle54_RX-          | G86   | GND                       | H86   | PCle62_TX-                 |
| E87   | PCle54_TX-                   | F87   | PCle54_RX+          | G87   | PCle62_RX-                | H87   | PCle62_TX+                 |
| E88   | PCle54_TX+                   | F88   | GND                 | G88   | PCle62_RX+                | H88   | GND                        |
| E89   | GND                          | F89   | PCle55_RX-          | G89   | GND                       | H89   | PCle63_TX-                 |
| E90   | PCle55_TX-                   | F90   | PCle55_RX+          | G90   | PCle63_RX-                | H90   | PCle63_TX+                 |
| E91   | PCle55_TX+                   | F91   | GND                 | G91   | PCle63_RX+                | H91   | GND                        |
| E92   | GND                          | F92   | PCle_REFCLK2-       | G92   | GND                       | H92   | <del>PCle_REFCLKIN0-</del> |
| E93   | PCle_REFCLK1-                | F93   | PCle_REFCLK2+       | G93   | PCle_REFCLK3-             | H93   | <del>PCle_REFCLKIN0+</del> |
| E94   | PCle_REFCLK1+                | F94   | GND                 | G94   | PCle_REFCLK3+             | H94   | GND                        |
| E95   | GND                          | F95   | PCle_CLKREQ3#       | G95   | GND                       | H95   | <del>PCle_REFCLKIN1-</del> |
| E96   | PCle_CLKREQ1#                | F96   | ETH0-3_PRST#        | G96   | <del>ETH0-3_I2C_CLK</del> | H96   | <del>PCle_REFCLKIN1+</del> |
| E97   | PCle_CLKREQ2#                | F97   | ETH0-3_PHY_RST#     | G97   | <del>ETH0-3_I2C_DAT</del> | H97   | GND                        |
| E98   | <del>PCle_CLKREQ_OUT0#</del> | F98   | <del>ETH0_SDP</del> | G98   | ETH0-3_PHY_INT#           | H98   | ETH0-3_MDIO_CLK            |
| E99   | <del>PCle_CLKREQ_OUT1#</del> | F99   | <del>ETH1_SDP</del> | G99   | ETH0-3_INT#               | H99   | ETH0-3_MDIO_DAT            |
| E100  | PCle_PERST_IN0#              | F100  | PCle_PERST_IN1#     | G100  | PCle_WAKE_OUT0#           | H100  | PCle_WAKE_OUT1#            |



**Note:** Strikethrough entries are functions not supported by this product.

IPMB is supported if there's MMC on module. No eSPI support on this platform

## 4.2 Signal Terminology Descriptions

Definitions of the terms used for signal description tables

| Term                   | Description                                                                                                                                      |
|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| I                      | Input to the module                                                                                                                              |
| O                      | Output from the module                                                                                                                           |
| I/O                    | Bi-directional Input / Output                                                                                                                    |
| OD                     | Open drain output from the module                                                                                                                |
|                        |                                                                                                                                                  |
| I 3.3V                 | Input 3.3V tolerant                                                                                                                              |
| I 5V                   | Input 5V tolerant                                                                                                                                |
| O 3.3V                 | Output 3.3V signal level                                                                                                                         |
| O 5V                   | Output 5V signal level                                                                                                                           |
| I/O 3.3V               | Bi-directional signal 3.3V tolerant                                                                                                              |
| I/O 5V                 | Bi-directional signal 5V tolerant                                                                                                                |
| I/O 3.3V <sub>SB</sub> | Input or output 3.3V tolerant active in standby state                                                                                            |
|                        |                                                                                                                                                  |
| DDC                    | Display Data Channel                                                                                                                             |
| PCIE                   | PCI Express compatible differential signal                                                                                                       |
| PEG                    | PCI Express Graphics                                                                                                                             |
| SATA                   | Serial ATA specification Revision 2.6 and 3                                                                                                      |
| LVDS                   | Low Voltage Differential Signal - 330 mV nominal; 450 mV maximum differential signal                                                             |
|                        |                                                                                                                                                  |
| P                      | Power Input / Output                                                                                                                             |
| REF                    | Reference voltage output. May be sourced from a Module power plane.                                                                              |
| PDS                    | Pull-down strap. A Module output pin that is either tied to GND or is not connected.<br>Used to signal Module capabilities to the Carrier Board. |
|                        |                                                                                                                                                  |
| PU                     | PU (pull-up) resistor on module                                                                                                                  |
| PD                     | PD (pull-down) resistor on module                                                                                                                |

## 4.3 Signal Descriptions on J1/J2 Connectors

### 4.3.1 Ethernet KR/KX

Ethernet KR interface are defined for COM-HPC. For these ports, the Ethernet MACs are located on COM-HPC module. PHYs (if used) are on the Carrier. In some cases, no PHY is required, for short cable ("Direct Attach" cables) or Carrier runs.

COM-HPC support both of MDIO and I2C control interfaces for the PHYs. The MDIO and I2C control interfaces are grouped into quads, for KR ports 0:3 and ports 4:7

| Name                                                                                         | Pin #                                                | Description                                                                                                                                         | I/O           | PU / PD | Comment               |
|----------------------------------------------------------------------------------------------|------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|-----------------------|
| ETH0_TX-<br>ETH0_TX+<br>ETH1_TX-<br>ETH1_TX+<br>ETH2_TX-<br>ETH2_TX+<br>ETH3_TX-<br>ETH3_TX+ | C20<br>C21<br>C23<br>C24<br>C26<br>C27<br>C29<br>C30 | Ethernet KR ports, transmit output differential pairs.                                                                                              | O<br>KR       |         | AC coupled Off Module |
| ETH0_RX-<br>ETH0_RX+<br>ETH1_RX-<br>ETH1_RX+<br>ETH2_RX-<br>ETH2_RX+<br>ETH3_RX-<br>ETH3_RX+ | D19<br>D20<br>D22<br>D23<br>D25<br>D26<br>D28<br>D29 | Ethernet KR ports, receive input differential pairs.                                                                                                | I<br>KR       |         | AC coupled Off Module |
| ETH0-3_MDIO_DAT                                                                              | H99                                                  | Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 0 to 3                  | I/O<br>3.3VSB | PU 2K2  | Not Supported         |
| ETH0-3_MDIO_CLK                                                                              | H98                                                  | Clock signal for Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 0 to 3 | Ø<br>3.3VSB   |         | Not Supported         |
| ETH0-3_INT#                                                                                  | G99                                                  | Active low interrupt signal from IO Port expanders for ETH ports 0 to 3                                                                             | I<br>3.3VSB   | PU 4K7  |                       |

|                                                                                          |                                                                    |                                                                                                                                                                                                                                                                    |                                     |        |               |
|------------------------------------------------------------------------------------------|--------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------|--------|---------------|
| ETH0-3_PHY_INT#                                                                          | G98                                                                | Active low PHY interrupt signal from ETH ports 0 to 3                                                                                                                                                                                                              | I<br>3.3VSB                         | PU 4K7 |               |
| ETH0-3_PHY_RST#                                                                          | F97                                                                | Active low output PHY reset signal for ETH ports 0 to 3.                                                                                                                                                                                                           | O<br>3.3VSB                         |        |               |
| ETH0-3_I2C_DAT                                                                           | G97                                                                | I2C data signal of the 2-wire management interface used by the Ethernet KR controller to access the management registers of an external SFP Module or to configure the Carrier PHY for ETHx ports 0 to 3 and for serialized status information (e.g. LED states).. | I/O OD<br>3.3VSB                    | PU 1K  |               |
| ETH0-3_I2C_CLK                                                                           | G96                                                                | The I2C clock signals associated with ETH0-3 I2C data lines in the row above.                                                                                                                                                                                      | I/O OD<br>3.3VSB                    | PU 1K  |               |
| <del>ETH0_SDP</del><br><del>ETH1_SDP</del><br><del>ETH2_SDP</del><br><del>ETH3_SDP</del> | <del>F98</del><br><del>F99</del><br><del>F1</del><br><del>F2</del> | <del>Software-Definable Pins. Can also be used for IEEE1588 support such as a PPS signal.</del>                                                                                                                                                                    | <del>I/O</del><br><del>3.3VSB</del> |        | Not Supported |
| ETH0-3_PRSENT#                                                                           | F96                                                                | Carrier pulls this line to GND if there is Carrier hardware present to support Ethernet KR signalling on ETH0 through ETH3. If the entire KR quad is not supported it should pull from ETH0 on up.                                                                 | I<br>3.3VSB                         | PU 4K7 |               |



**Note:** The Ethernet KR support is 10GBASE-KR

### 4.3.2 NBASE-T Ethernet

The port may operate in 10Gbps, 5Gbps, 2.5Gbps, 1Gbps, 100Mbps, or 10Mbps modes. Magnetics are to be on the Carrier board. The COM-HPC module shall be capable of 1000BASE-T mode.

| Name                                                                                                                                 | Pin #                                                | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | I/O      | PU / PD                   | Comment                             |          |           |          |       |       |           |          |       |       |           |          |  |  |           |          |  |  |            |  |                                                |
|--------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|---------------------------|-------------------------------------|----------|-----------|----------|-------|-------|-----------|----------|-------|-------|-----------|----------|--|--|-----------|----------|--|--|------------|--|------------------------------------------------|
| NBASET0_MDI0-<br>NBASET0_MDI0+<br>NBASET0_MDI1-<br>NBASET0_MDI1+<br>NBASET0_MDI2-<br>NBASET0_MDI2+<br>NBASET0_MDI3-<br>NBASET0_MDI3+ | D85<br>D86<br>D88<br>D89<br>D91<br>D92<br>D93<br>D94 | Ethernet Controller 1: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 10Gbps, 1Gbps, 100Mbps and 10 Mbps modes. Some pairs are unused in some modes, per the following: <table><tr><td></td><td>10000BASE-T<br/>1000BASE-T</td><td>100BASE-TX</td><td>10BASE-T</td></tr><tr><td>MDI[0]+/-</td><td>B1_DA+/-</td><td>TX+/-</td><td>TX+/-</td></tr><tr><td>MDI[1]+/-</td><td>B1_DB+/-</td><td>RX+/-</td><td>RX+/-</td></tr><tr><td>MDI[2]+/-</td><td>B1_DC+/-</td><td></td><td></td></tr><tr><td>MDI[3]+/-</td><td>B1_DD+/-</td><td></td><td></td></tr></table> |          | 10000BASE-T<br>1000BASE-T | 100BASE-TX                          | 10BASE-T | MDI[0]+/- | B1_DA+/- | TX+/- | TX+/- | MDI[1]+/- | B1_DB+/- | RX+/- | RX+/- | MDI[2]+/- | B1_DC+/- |  |  | MDI[3]+/- | B1_DD+/- |  |  | I/O Analog |  | Twisted pair signals for external transformer. |
|                                                                                                                                      | 10000BASE-T<br>1000BASE-T                            | 100BASE-TX                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 10BASE-T |                           |                                     |          |           |          |       |       |           |          |       |       |           |          |  |  |           |          |  |  |            |  |                                                |
| MDI[0]+/-                                                                                                                            | B1_DA+/-                                             | TX+/-                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | TX+/-    |                           |                                     |          |           |          |       |       |           |          |       |       |           |          |  |  |           |          |  |  |            |  |                                                |
| MDI[1]+/-                                                                                                                            | B1_DB+/-                                             | RX+/-                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | RX+/-    |                           |                                     |          |           |          |       |       |           |          |       |       |           |          |  |  |           |          |  |  |            |  |                                                |
| MDI[2]+/-                                                                                                                            | B1_DC+/-                                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |          |                           |                                     |          |           |          |       |       |           |          |       |       |           |          |  |  |           |          |  |  |            |  |                                                |
| MDI[3]+/-                                                                                                                            | B1_DD+/-                                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |          |                           |                                     |          |           |          |       |       |           |          |       |       |           |          |  |  |           |          |  |  |            |  |                                                |
| NBASET0_LINK_ACT#                                                                                                                    | D99                                                  | NBASE-T Ethernet Controller activity indicator, active low.<br>20 mA or more current sink capability at VOL of 0.4V max.<br>20 mA or more current source capability at VOH of 2.4V min.                                                                                                                                                                                                                                                                                                                                                                                                    | O 3.3VSB |                           | Need add pull-high on carrier board |          |           |          |       |       |           |          |       |       |           |          |  |  |           |          |  |  |            |  |                                                |
| NBASET0_LINK_MAX#                                                                                                                    | D97                                                  | NBASE-T Ethernet Controller MAX Speed Link indicator, active low. If active, the link is established at the maximum speed that the Ethernet controller is capable of (which may be 10G, 5G, 2.5G etc).<br>20 mA or more current sink capability at VOL of 0.4V max.<br>20 mA or more current source capability at VOH of 2.4V min.                                                                                                                                                                                                                                                         | O 3.3VSB |                           |                                     |          |           |          |       |       |           |          |       |       |           |          |  |  |           |          |  |  |            |  |                                                |
| NBASET0_LINK_MID#                                                                                                                    | D98                                                  | NBASE-T Ethernet Controller MID Speed Link indicator, active low. If active, the link is established but at a speed lower than what the maximum speed that the Ethernet controller is capable of.<br>20 mA or more current sink capability at VOL of 0.4V max.<br>20 mA or more current source capability at VOH of 2.4V min.                                                                                                                                                                                                                                                              | O 3.3VSB |                           |                                     |          |           |          |       |       |           |          |       |       |           |          |  |  |           |          |  |  |            |  |                                                |

|               |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                            |  |               |
|---------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|--|---------------|
| NBASET0_CTREF | C99 | Reference voltage for Carrier Board NBASET Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. If not needed, these pins may be left open on the Carrier. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less. | REF<br>GND min<br>3.3V max |  | Not Supported |
| NBASET0_SDP   | C98 | NBASE-T Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal.                                                                                                                                                                                                                                                                                                                                  | IO 3.3VSB                  |  |               |

### 4.3.3 PCI Express

| Name       | Pin # | Description                                                       | I/O    | PU / PD | Comment               |
|------------|-------|-------------------------------------------------------------------|--------|---------|-----------------------|
| PCle00_TX+ | D62   | PCI Express Differential Transmit Pairs 0-7<br>PCIe Group 0 Low   | O PCIe |         | AC coupled on Module  |
| PCle00_TX- | D61   |                                                                   |        |         |                       |
| PCle01_TX+ | D65   |                                                                   |        |         |                       |
| PCle01_TX- | D64   |                                                                   |        |         |                       |
| PCle02_TX+ | D68   |                                                                   |        |         |                       |
| PCle03_TX- | D67   |                                                                   |        |         |                       |
| PCle03_TX+ | D71   |                                                                   |        |         |                       |
| PCle03_TX- | D70   |                                                                   |        |         |                       |
| PCle04_TX+ | D74   |                                                                   |        |         |                       |
| PCle04_TX- | D73   |                                                                   |        |         |                       |
| PCle05_TX+ | D77   |                                                                   |        |         |                       |
| PCle05_TX- | D76   |                                                                   |        |         |                       |
| PCle06_TX+ | D80   |                                                                   |        |         |                       |
| PCle06_TX- | D79   |                                                                   |        |         |                       |
| PCle07_TX+ | D83   |                                                                   |        |         |                       |
| PCle07_TX- | D82   |                                                                   |        |         |                       |
| PCle00_RX+ | C63   | PCI Express Differential Receive Pairs 0-7<br>PCIe Group 0 Low    | I PCIe |         | AC coupled off Module |
| PCle00_RX- | C62   |                                                                   |        |         |                       |
| PCle01_RX+ | C66   |                                                                   |        |         |                       |
| PCle01_RX- | C65   |                                                                   |        |         |                       |
| PCle02_RX+ | C69   |                                                                   |        |         |                       |
| PCle02_RX- | C68   |                                                                   |        |         |                       |
| PCle03_RX+ | C72   |                                                                   |        |         |                       |
| PCle03_RX- | C71   |                                                                   |        |         |                       |
| PCle04_RX+ | C75   |                                                                   |        |         |                       |
| PCle04_RX- | C74   |                                                                   |        |         |                       |
| PCle05_RX+ | C78   |                                                                   |        |         |                       |
| PCle05_RX- | C77   |                                                                   |        |         |                       |
| PCle06_RX+ | C81   |                                                                   |        |         |                       |
| PCle06_RX- | C80   |                                                                   |        |         |                       |
| PCle07_RX+ | C84   |                                                                   |        |         |                       |
| PCle07_RX- | C83   |                                                                   |        |         |                       |
| PCle08_TX+ | A63   | PCI Express Differential Transmit Pairs 8-15<br>PCIe Group 0 High | O PCIe |         | AC coupled on Module  |
| PCle08_TX- | A62   |                                                                   |        |         |                       |

|            |     |                                                                                                                                                 |        |  |                       |
|------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------|--------|--|-----------------------|
| PCle09_TX+ | A66 | A Server Module may map up to 8 higher bandwidth PCIe lanes to Group 0 High                                                                     |        |  |                       |
| PCle09_TX- | A65 |                                                                                                                                                 |        |  |                       |
| PCle10_TX+ | A69 |                                                                                                                                                 |        |  |                       |
| PCle10_TX- | A68 |                                                                                                                                                 |        |  |                       |
| PCle11_TX+ | A72 |                                                                                                                                                 |        |  |                       |
| PCle11_TX- | A71 |                                                                                                                                                 |        |  |                       |
| PCle12_TX+ | A75 |                                                                                                                                                 |        |  |                       |
| PCle12_TX- | A74 |                                                                                                                                                 |        |  |                       |
| PCle13_TX+ | A78 |                                                                                                                                                 |        |  |                       |
| PCle13_TX- | A77 |                                                                                                                                                 |        |  |                       |
| PCle14_TX+ | A81 |                                                                                                                                                 |        |  |                       |
| PCle14_TX- | A80 |                                                                                                                                                 |        |  |                       |
| PCle15_TX+ | A84 |                                                                                                                                                 |        |  |                       |
| PCle15_TX- | A83 |                                                                                                                                                 |        |  |                       |
| PCle08_RX+ | B62 | PCI Express Differential Receive Pairs 8-15<br>PCIe Group 0 High<br>A Server Module may map up to 8 higher bandwidth PCIe lanes to Group 0 High | I PCIe |  | AC coupled off Module |
| PCle08_RX- | B61 |                                                                                                                                                 |        |  |                       |
| PCle09_RX+ | B65 |                                                                                                                                                 |        |  |                       |
| PCle09_RX- | B64 |                                                                                                                                                 |        |  |                       |
| PCle10_RX+ | B68 |                                                                                                                                                 |        |  |                       |
| PCle10_RX- | B67 |                                                                                                                                                 |        |  |                       |
| PCle11_RX+ | B71 |                                                                                                                                                 |        |  |                       |
| PCle11_RX- | B70 |                                                                                                                                                 |        |  |                       |
| PCle12_RX+ | B74 |                                                                                                                                                 |        |  |                       |
| PCle12_RX- | B73 |                                                                                                                                                 |        |  |                       |
| PCle13_RX+ | B77 |                                                                                                                                                 |        |  |                       |
| PCle13_RX- | B76 |                                                                                                                                                 |        |  |                       |
| PCle14_RX+ | B80 |                                                                                                                                                 |        |  |                       |
| PCle14_RX- | B79 |                                                                                                                                                 |        |  |                       |
| PCle15_RX+ | B83 |                                                                                                                                                 |        |  |                       |
| PCle15_RX- | B82 |                                                                                                                                                 |        |  |                       |
| PCle16_TX+ | E46 | PCI Express Differential Transmit Pairs 16-31<br>PCIe Group 1                                                                                   | O PCIe |  | AC coupled on Module  |
| PCle16_TX- | E46 |                                                                                                                                                 |        |  |                       |
| PCle17_TX+ | E49 |                                                                                                                                                 |        |  |                       |
| PCle17_TX- | E48 |                                                                                                                                                 |        |  |                       |
| PCle18_TX+ | E52 |                                                                                                                                                 |        |  |                       |
| PCle18_TX- | E51 |                                                                                                                                                 |        |  |                       |
| PCle19_TX+ | E55 |                                                                                                                                                 |        |  |                       |
| PCle19_TX- | E54 |                                                                                                                                                 |        |  |                       |
| PCle20_TX+ | E58 |                                                                                                                                                 |        |  |                       |

|            |     |                                                              |        |  |                       |
|------------|-----|--------------------------------------------------------------|--------|--|-----------------------|
| PCle20_TX- | E57 |                                                              |        |  |                       |
| PCle21_TX+ | E61 |                                                              |        |  |                       |
| PCle21_TX- | E60 |                                                              |        |  |                       |
| PCle22_TX+ | E64 |                                                              |        |  |                       |
| PCle22_TX- | E63 |                                                              |        |  |                       |
| PCle23_TX+ | E67 |                                                              |        |  |                       |
| PCle23_TX- | E66 |                                                              |        |  |                       |
| PCle24_TX+ | H45 |                                                              |        |  |                       |
| PCle24_TX- | H44 |                                                              |        |  |                       |
| PCle25_TX+ | H48 |                                                              |        |  |                       |
| PCle25_TX- | H47 |                                                              |        |  |                       |
| PCle26_TX+ | H51 |                                                              |        |  |                       |
| PCle26_TX- | H50 |                                                              |        |  |                       |
| PCle27_TX+ | H54 |                                                              |        |  |                       |
| PCle27_TX- | H53 |                                                              |        |  |                       |
| PCle28_TX+ | H57 |                                                              |        |  |                       |
| PCle28_TX- | H56 |                                                              |        |  |                       |
| PCle29_TX+ | H60 |                                                              |        |  |                       |
| PCle29_TX- | H59 |                                                              |        |  |                       |
| PCle30_TX+ | H63 |                                                              |        |  |                       |
| PCle30_TX- | H62 |                                                              |        |  |                       |
| PCle31_TX+ | H66 |                                                              |        |  |                       |
| PCle31_TX- | H65 |                                                              |        |  |                       |
| PCle16_RX+ | F45 | PCI Express Differential Receive Pairs 16-31<br>PCIe Group 1 | 1 PCIe |  | AC coupled off Module |
| PCle16_RX- | F44 |                                                              |        |  |                       |
| PCle17_RX+ | F48 |                                                              |        |  |                       |
| PCle17_RX- | F47 |                                                              |        |  |                       |
| PCle18_RX+ | F51 |                                                              |        |  |                       |
| PCle18_RX- | F50 |                                                              |        |  |                       |
| PCle19_RX+ | F54 |                                                              |        |  |                       |
| PCle19_RX- | F53 |                                                              |        |  |                       |
| PCle20_RX+ | F57 |                                                              |        |  |                       |
| PCle20_RX- | F56 |                                                              |        |  |                       |
| PCle21_RX+ | F60 |                                                              |        |  |                       |
| PCle21_RX- | F59 |                                                              |        |  |                       |
| PCle22_RX+ | F63 |                                                              |        |  |                       |
| PCle22_RX- | F62 |                                                              |        |  |                       |
| PCle23_RX+ | F66 |                                                              |        |  |                       |
| PCle23_RX- | F65 |                                                              |        |  |                       |

|            |     |                                                               |        |  |                      |
|------------|-----|---------------------------------------------------------------|--------|--|----------------------|
| PCle24_RX+ | G46 |                                                               |        |  |                      |
| PCle24_RX- | G45 |                                                               |        |  |                      |
| PCle25_RX+ | G49 |                                                               |        |  |                      |
| PCle25_RX- | G48 |                                                               |        |  |                      |
| PCle26_RX+ | G52 |                                                               |        |  |                      |
| PCle26_RX- | G51 |                                                               |        |  |                      |
| PCle27_RX+ | G55 |                                                               |        |  |                      |
| PCle27_RX- | G54 |                                                               |        |  |                      |
| PCle28_RX+ | G58 |                                                               |        |  |                      |
| PCle28_RX- | G57 |                                                               |        |  |                      |
| PCle29_RX+ | G61 |                                                               |        |  |                      |
| PCle29_RX- | G60 |                                                               |        |  |                      |
| PCle30_RX+ | G64 |                                                               |        |  |                      |
| PCle30_RX- | G63 |                                                               |        |  |                      |
| PCle31_RX+ | G67 |                                                               |        |  |                      |
| PCle31_RX- | G66 |                                                               |        |  |                      |
| PCle32_TX+ | E22 | PCI Express Differential Transmit Pairs 32-47<br>PCle Group 2 | O PCle |  | AC coupled on Module |
| PCle32_TX- | E21 |                                                               |        |  |                      |
| PCle33_TX+ | E25 |                                                               |        |  |                      |
| PCle33_TX- | E24 |                                                               |        |  |                      |
| PCle34_TX+ | E28 |                                                               |        |  |                      |
| PCle34_TX- | E27 |                                                               |        |  |                      |
| PCle35_TX+ | E31 |                                                               |        |  |                      |
| PCle35_TX- | E30 |                                                               |        |  |                      |
| PCle36_TX+ | E34 |                                                               |        |  |                      |
| PCle36_TX- | E33 |                                                               |        |  |                      |
| PCle37_TX+ | E37 |                                                               |        |  |                      |
| PCle37_TX- | E36 |                                                               |        |  |                      |
| PCle38_TX+ | E40 |                                                               |        |  |                      |
| PCle38_TX- | E39 |                                                               |        |  |                      |
| PCle39_TX+ | E43 |                                                               |        |  |                      |
| PCle39_TX- | E42 |                                                               |        |  |                      |
| PCle40_TX+ | H22 |                                                               |        |  |                      |
| PCle40_TX- | H21 |                                                               |        |  |                      |
| PCle41_TX+ | H24 |                                                               |        |  |                      |
| PCle41_TX- | H23 |                                                               |        |  |                      |
| PCle42_TX+ | H27 |                                                               |        |  |                      |
| PCle42_TX- | H26 |                                                               |        |  |                      |
| PCle43_TX+ | H30 |                                                               |        |  |                      |

|            |     |                                                              |        |  |                       |
|------------|-----|--------------------------------------------------------------|--------|--|-----------------------|
| PCle43_TX- | H29 |                                                              |        |  |                       |
| PCle44_TX+ | H33 |                                                              |        |  |                       |
| PCle44_TX- | H32 |                                                              |        |  |                       |
| PCle45_TX+ | H36 |                                                              |        |  |                       |
| PCle45_TX- | H35 |                                                              |        |  |                       |
| PCle46_TX+ | H39 |                                                              |        |  |                       |
| PCle46_TX- | H38 |                                                              |        |  |                       |
| PCle47_TX+ | H42 |                                                              |        |  |                       |
| PCle47_TX- | H41 |                                                              |        |  |                       |
| PCle32_RX+ | F21 | PCI Express Differential Receive Pairs 32-47<br>PCle Group 2 | 1 PCle |  | AC coupled off Module |
| PCle32_RX- | F20 |                                                              |        |  |                       |
| PCle33_RX+ | F24 |                                                              |        |  |                       |
| PCle33_RX- | F23 |                                                              |        |  |                       |
| PCle34_RX+ | F27 |                                                              |        |  |                       |
| PCle34_RX- | F26 |                                                              |        |  |                       |
| PCle35_RX+ | F30 |                                                              |        |  |                       |
| PCle35_RX- | F29 |                                                              |        |  |                       |
| PCle36_RX+ | F33 |                                                              |        |  |                       |
| PCle36_RX- | F32 |                                                              |        |  |                       |
| PCle37_RX+ | F36 |                                                              |        |  |                       |
| PCle37_RX- | F35 |                                                              |        |  |                       |
| PCle38_RX+ | F39 |                                                              |        |  |                       |
| PCle38_RX- | F38 |                                                              |        |  |                       |
| PCle39_RX+ | F42 |                                                              |        |  |                       |
| PCle39_RX- | F41 |                                                              |        |  |                       |
| PCle40_RX+ | G22 |                                                              |        |  |                       |
| PCle40_RX- | G21 |                                                              |        |  |                       |
| PCle41_RX+ | G25 |                                                              |        |  |                       |
| PCle41_RX- | G24 |                                                              |        |  |                       |
| PCle42_RX+ | G28 |                                                              |        |  |                       |
| PCle42_RX- | G27 |                                                              |        |  |                       |
| PCle43_RX+ | G31 |                                                              |        |  |                       |
| PCle43_RX- | G30 |                                                              |        |  |                       |
| PCle44_RX+ | G34 |                                                              |        |  |                       |
| PCle44_RX- | G33 |                                                              |        |  |                       |
| PCle45_RX+ | G37 |                                                              |        |  |                       |
| PCle45_RX- | G36 |                                                              |        |  |                       |
| PCle46_RX+ | G40 |                                                              |        |  |                       |
| PCle46_RX- | G39 |                                                              |        |  |                       |

|            |     |                                                               |        |  |                       |
|------------|-----|---------------------------------------------------------------|--------|--|-----------------------|
| PCIe47_RX+ | G43 |                                                               |        |  |                       |
| PCIe47_RX- | G42 |                                                               |        |  |                       |
| PCIe48_TX+ | E70 | PCI Express Differential Transmit Pairs 48-63<br>PCIe Group 3 | O PCIe |  | AC coupled on Module  |
| PCIe48_TX- | E69 |                                                               |        |  |                       |
| PCIe49_TX+ | E73 |                                                               |        |  |                       |
| PCIe49_TX- | E72 |                                                               |        |  |                       |
| PCIe50_TX+ | E76 |                                                               |        |  |                       |
| PCIe50_TX- | E75 |                                                               |        |  |                       |
| PCIe51_TX+ | E79 |                                                               |        |  |                       |
| PCIe51_TX- | E78 |                                                               |        |  |                       |
| PCIe52_TX+ | E82 |                                                               |        |  |                       |
| PCIe52_TX- | E81 |                                                               |        |  |                       |
| PCIe53_TX+ | E85 |                                                               |        |  |                       |
| PCIe53_TX- | E84 |                                                               |        |  |                       |
| PCIe54_TX+ | E88 |                                                               |        |  |                       |
| PCIe54_TX- | E87 |                                                               |        |  |                       |
| PCIe55_TX+ | E91 |                                                               |        |  |                       |
| PCIe55_TX- | E90 |                                                               |        |  |                       |
| PCIe56_TX+ | H69 |                                                               |        |  |                       |
| PCIe56_TX- | H68 |                                                               |        |  |                       |
| PCIe57_TX+ | H72 |                                                               |        |  |                       |
| PCIe57_TX- | H71 |                                                               |        |  |                       |
| PCIe58_TX+ | H75 |                                                               |        |  |                       |
| PCIe58_TX- | H74 |                                                               |        |  |                       |
| PCIe59_TX+ | H78 |                                                               |        |  |                       |
| PCIe59_TX- | H77 |                                                               |        |  |                       |
| PCIe60_TX+ | H81 |                                                               |        |  |                       |
| PCIe60_TX- | H80 |                                                               |        |  |                       |
| PCIe61_TX+ | H84 |                                                               |        |  |                       |
| PCIe61_TX- | H83 |                                                               |        |  |                       |
| PCIe62_TX+ | H87 |                                                               |        |  |                       |
| PCIe62_TX- | H86 |                                                               |        |  |                       |
| PCIe63_TX+ | H91 |                                                               |        |  |                       |
| PCIe63_TX- | H90 |                                                               |        |  |                       |
| PCIe48_RX+ | F69 | PCI Express Differential Receive Pairs 48-63<br>PCIe Group 3  | I PCIe |  | AC coupled off Module |
| PCIe48_RX- | F68 |                                                               |        |  |                       |
| PCIe49_RX+ | F72 |                                                               |        |  |                       |
| PCIe49_RX- | F71 |                                                               |        |  |                       |

|                                      |            |                                                                                                           |        |  |                       |
|--------------------------------------|------------|-----------------------------------------------------------------------------------------------------------|--------|--|-----------------------|
| PCle50_RX+                           | F75        |                                                                                                           |        |  |                       |
| PCle50_RX-                           | F74        |                                                                                                           |        |  |                       |
| PCle51_RX+                           | F78        |                                                                                                           |        |  |                       |
| PCle51_RX-                           | F77        |                                                                                                           |        |  |                       |
| PCle52_RX+                           | F81        |                                                                                                           |        |  |                       |
| PCle52_RX-                           | F80        |                                                                                                           |        |  |                       |
| PCle53_RX+                           | F84        |                                                                                                           |        |  |                       |
| PCle53_RX-                           | F83        |                                                                                                           |        |  |                       |
| PCle54_RX+                           | F87        |                                                                                                           |        |  |                       |
| PCle54_RX-                           | F86        |                                                                                                           |        |  |                       |
| PCle55_RX+                           | F90        |                                                                                                           |        |  |                       |
| PCle55_RX-                           | F89        |                                                                                                           |        |  |                       |
| PCle56_RX+                           | G70        |                                                                                                           |        |  |                       |
| PCle56_RX-                           | G69        |                                                                                                           |        |  |                       |
| PCle57_RX+                           | G73        |                                                                                                           |        |  |                       |
| PCle57_RX-                           | G72        |                                                                                                           |        |  |                       |
| PCle58_RX+                           | G76        |                                                                                                           |        |  |                       |
| PCle58_RX-                           | G75        |                                                                                                           |        |  |                       |
| PCle59_RX+                           | G79        |                                                                                                           |        |  |                       |
| PCle59_RX-                           | G78        |                                                                                                           |        |  |                       |
| PCle60_RX+                           | G82        |                                                                                                           |        |  |                       |
| PCle60_RX-                           | G81        |                                                                                                           |        |  |                       |
| PCle61_RX+                           | G85        |                                                                                                           |        |  |                       |
| PCle61_RX-                           | G84        |                                                                                                           |        |  |                       |
| PCle62_RX+                           | G88        |                                                                                                           |        |  |                       |
| PCle62_RX-                           | G87        |                                                                                                           |        |  |                       |
| PCle63_RX+                           | G91        |                                                                                                           |        |  |                       |
| PCle63_RX-                           | G90        |                                                                                                           |        |  |                       |
| PCle_BMC_TX-<br>PCle_BMC_TX+         | A59<br>A60 | PCI Express Differential Transmit Pair for Carrier BMC<br>(Board Management Controller)                   | O PCIe |  | AC coupled on Module  |
| PCle_BMC_RX-<br>PCle_BMC_RX+         | B58<br>B59 | PCI Express Differential Transmit Pair for Carrier BMC<br>(Board Management Controller)                   | I PCIe |  | AC coupled off Module |
| PCle_REFCLK0_LO-<br>PCle_REFCLK0_LO+ | C59<br>C60 | Reference clock pair for PCIe lanes [0:7], also referred<br>to PCIe Group 0 Low and for the PCIe_BMC link | O PCIe |  |                       |
| PCle_REFCLK0_HI-<br>PCle_REFCLK0_HI+ | C57<br>C56 | Reference clock pair for PCIe lanes [8:15], also<br>referred to PCIe Group 0 High                         | O PCIe |  |                       |

|                                |            |                                                                                          |                |        |  |
|--------------------------------|------------|------------------------------------------------------------------------------------------|----------------|--------|--|
| PCIe_REFCLK1-<br>PCIe_REFCLK1+ | E93<br>E94 | Reference clock pair for PCIe lanes [16:31], also referred to PCIe Group 1               | O PCIe         |        |  |
| PCIe_REFCLK2-<br>PCIe_REFCLK2+ | F92<br>F93 | Reference clock pair for PCIe lanes [32:47], also referred to PCIe Group 2               | O PCIe         |        |  |
| PCIe_REFCLK3-<br>PCIe_REFCLK3+ | G93<br>G94 | Reference clock pair for PCIe lanes [48:63], also referred to PCIe Group 2               | O PCIe         |        |  |
| PCIe_CLKREQ0_LO#               | A56        | PCIe reference clock request signals from Carrier devices for PCIe_REFCLK0_LO clock pair | I/O OD<br>3.3V | PU 10K |  |
| PCIe_CLKREQ0_HI#               | A57        | PCIe reference clock request signals from Carrier devices for PCIe_REFCLK0_HI clock pair | I/O OD<br>3.3V | PU 10K |  |
| PCIe_CLKREQ0_1#                | E96        | PCIe reference clock request signals from Carrier devices for PCIe_REFCLK1 clock pair    | I/O OD<br>3.3V | PU 10K |  |
| PCIe_CLKREQ0_2#                | E97        | PCIe reference clock request signals from Carrier devices for PCIe_REFCLK2 clock pair    | I/O OD<br>3.3V | PU 10K |  |
| PCIe_CLKREQ0_3#                | F95        | PCIe reference clock request signals from Carrier devices for PCIe_REFCLK3 clock pair    | I/O OD<br>3.3V | PU 10K |  |

### 4.3.4 USB

The COM-HPC Server Module supports up to eight USB 2.0 ports, up to two USB 3.2 Gen1 or Gen2 ports and up to two USB 3.2 Gen2x2 ports or USB4 ports. A USB 3.2 Gen2x2 may be used as USB 3.2 Gen1 or Gen2 port as well.

To realize a COM-HPC USB 3.2 Gen1, Gen2, Gen2x2 or USB4 port, one of the four available USB 2.0 ports from the USB[0:3] pool must be used along with the SuperSpeed pins. The specific pairings noted in table below need to be made.

| Name                                                                 | Pin #                                                | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                            | I/O           | PU / PD | Comment                                                                                                     |
|----------------------------------------------------------------------|------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|-------------------------------------------------------------------------------------------------------------|
| USB0+<br>USB0-<br>USB1+<br>USB1-<br>USB2+<br>USB2-<br>USB3+<br>USB3- | D17<br>D16<br>D14<br>D13<br>C18<br>C17<br>C15<br>C14 | USB 2.0 differential pairs, channels 0 through 7.<br><br>USB0 may be configured as a USB client or as a host, or both at the Module designer's discretion. All other USB ports, if implemented, shall be host ports.<br><br>If any SuperSpeed ports are implemented, then they must be supported by a USB 2.0 port, using one of the USB[0:3] ports from this pool.                                                                                                    | I/O<br>3.3VSB |         | USB 1.1/2.0 compliant<br><br>This product only support USB0-3 through a PCIe to USB IC                      |
| USB0_SSTX0+<br>USB0_SSTX0-<br><br>USB1_SSTX0+<br>USB1_SSTX0-         | D44<br>D43<br><br>D38<br>D37                         | Four sets of SuperSpeed transmit pairs, used to realize the transmit side of two USB 3.2 Gen 2x2 ports.<br><br>Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface.<br><br>These ports shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB0_SSxxx+/- shall be used with the USB0 USB 2.0 pair and so on, USB1_SSxxx+/- with the USB1 USB 2.0 pair). | O PCIe        |         | AC coupled on Module<br><br>This product only support USB0-3 (up to USB 3.2 Gen1) through a PCIe to USB IC  |
| USB0_SSRX0+<br>USB0_SSRX0-<br><br>USB1_SSRX0+<br>USB1_SSRX0-         | C45<br>C44<br><br>C39<br>C38                         | Four sets of SuperSpeed receive pairs, used to realize the transmit side of two USB 3.2 Gen 2x2 ports.<br><br>Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface.                                                                                                                                                                                                              | I PCIe        |         | AC coupled off Module<br><br>This product only support USB0-3 (up to USB 3.2 Gen1) through a PCIe to USB IC |

|                                                             |                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |          |                  |                                                                                                             |
|-------------------------------------------------------------|-------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|------------------|-------------------------------------------------------------------------------------------------------------|
|                                                             |                                     | These ports shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB0_SSxxx+/- shall be used with the USB0 USB 2.0 pair and so on, USB1_SSxxx+/- with the USB1 USB 2.0 pair).                                                                                                                                                                                                                                                                                                   |          |                  |                                                                                                             |
| USB2_SSTX+<br>USB2_SSTX-<br>USB3_SSTX+<br>USB3_SSTX-        | D35<br>D34<br>D32<br>D31            | Two sets of high speed transmit pairs, to realize two USB 3.2 Gen 1 or Gen 2 implementations.<br><br>These ports shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB2_SSxxx+/- shall be used with the USB2 USB 2.0 pair and USB3_SSxxx+/- with the USB3 USB 2.0 pair).                                                                                                                                                                                                     | O PCIe   |                  | AC coupled on Module<br><br>This product only support USB0-3 (up to USB 3.2 Gen1) through a PCIe to USB IC  |
| USB2_SSRX+<br>USB2_SSRX-<br>USB3_SSRX+<br>USB3_SSRX-        | C36<br>C35<br>C33<br>C32            | Two sets of high speed receive pairs, to realize two USB 3.2 Gen 1 or Gen 2 implementations.<br><br>These ports shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB2_SSxxx+/- shall be used with the USB2 USB 2.0 pair and USB3_SSxxx+/- with the USB3 USB 2.0 pair).                                                                                                                                                                                                      | I PCIe   |                  | AC coupled off Module<br><br>This product only support USB0-3 (up to USB 3.2 Gen1) through a PCIe to USB IC |
| USB01_OC#<br>USB23_OC#<br><del>USB45_OC#</del><br>USB67_OC# | B28<br>B27<br><del>B26</del><br>B25 | USB over-current sense, USB channels 0,1; channels 2,3; channels 4,5 and channels 6,7 respectively.<br>A pull-up for each of these lines to the 3.3V Suspend rail shall be present on the Module.<br>The pull-up should be 10K. An open drain driver from USB current monitors on the Carrier Board may drive this line low. The Carrier Board shall not pull these lines up.<br>Note that the over-current limits for USB 2.0 and USB 3.0 are different; this is a Carrier board implementation item. | I 3.3VSB | PU 10K<br>3.3VSB | Do not pull high on carrier                                                                                 |
| RSMRST_OUT#                                                 | B86                                 | USB devices that are to be powered in the S5 / S4 / S3 Suspend states should not have their 5V VBUS power enabled before RSMRST_OUT# transitions to the hi state.<br><br>RSMRST_OUT# is also described in Power and System Management section                                                                                                                                                                                                                                                          | O 3.3VSB |                  |                                                                                                             |

This platform doesn't support USB4, thus additional signals required by USB4 are not shown here.

### 4.3.5 Asynchronous Serial Port

Two logic level Module "5 wire" (TX, RX, RTS#, CTS#, GND) asynchronous serial ports are provided for general purpose use and for use with debugging software that make use of the "console redirect" features available in many BIOS and operating systems. The Module BIOS should support "console redirect" to the UART0 port.

It is preferred that if the Module is based on an Intel x86 architecture, the Module serial ports be I/O mapped and be register compatible with the National Semiconductor 16550 UARTs that were used in the PC AT architecture.

The Module asynchronous serial ports *should not* be implemented as USB peripherals, as such implementations are generally not useful for low level debug purposes.

The COM-HPC UART signals are "logic level" signals and are the logic inverse of what is on an RS-232 line. The "Mark" (logic 1) voltage level is nominally 3.3V on the COM-HPC line and the "Space" (logic 0) is nominally 0V. RS-232 transceivers (on the Carrier) invert the signals and change the levels – so that a "Mark" is between -3V and -25V, and a "Space" is between +3V and +25V

In some situations, the UARTx\_RTS# line can be used alternatively as an RS485 transmit enable line.

| Name                     | Pin #      | Description                                                             | I/O    | PU / PD | Comment |
|--------------------------|------------|-------------------------------------------------------------------------|--------|---------|---------|
| UART0_TX<br>UART1_TX     | C89<br>B87 | Logic level asynchronous serial port transmit signal                    | O 3.3V |         |         |
| UART0_RX<br>UART1_RX     | C90<br>B88 | Logic level asynchronous serial port receive signal                     | I 3.3V | PU 10K  |         |
| UART0_RTS#<br>UART1_RTS# | C91<br>B89 | Logic level asynchronous serial port Request to Send signal, active low | O 3.3V |         |         |
| UART0_CTS#<br>UART1_CTS# | C92<br>B90 | Logic level asynchronous serial port Clear to Send input, active low    | I 3.3V |         |         |

### 4.3.6 I2C

Two general purpose I2C ports are defined for COM-HPC. The first of the two supports an ALERT# input. The ports shall support 100KHz operation and should 400KHz operation. The ports should be multi-master capable. I2C0 is defined to operate from a 3.3V rail and I2C1 from a 1.8V rail. The I2C1 port may be I3C capable.

I2C source from Ampere Altra SOC supports multi-master

| Name        | Pin # | Description                                      | I/O              | PU / PD          | Comment           |
|-------------|-------|--------------------------------------------------|------------------|------------------|-------------------|
| I2C0_CLK    | C93   | Clock I/O line for the general purpose I2C0 port | I/O OD<br>3.3VSB | PU 2K2<br>3.3VSB |                   |
| I2C0_DAT    | C94   | Data I/O line for the general purpose I2C0 port  | I/O OD<br>3.3VSB | PU 2K2<br>3.3VSB |                   |
| I2C0_ALERT# | C95   | Alert input / interrupt for I2C0                 | I 3.3V           | PU 2K2<br>3.3VSB |                   |
| I2C1_CLK    | C96   | Clock I/O line for the general purpose I2C1 port | I/O OD<br>1.8VSB | PU 4K7<br>1.8VSB | I3C Not supported |
| I2C1_DAT    | C97   | Data I/O line for the general purpose I2C1 port  | I/O OD<br>1.8VSB | PU 4K7<br>1.8VSB | I3C Not supported |



**Note:** multi-master support is I2C0 and I2C1

Supports 100KHz, 400KHz, and 1MHz

### 4.3.7 Port 80 Support on USB\_PD I2C Bus

COM-HPC Module should support exporting Port 80 information over the USB\_PD I2C bus (signals USB\_PD\_I2C\_DAT and USB\_PD\_I2C\_CLK) (pin B36 and B35) to Carrier hardware that implements a pair of 7-segment displays to show the codes.

### 4.3.8 IPMB

An IPMB (Intelligent Platform Management Bus) port is defined for both the Client and Server pinout types for platform management functions. The IPMB is used (optionally) with a Carrier based BMC (Board Management Controller) Master. On the Module, the IPMB should be routed to and used with a MMC (Module Management Controller). The Module IPMB is a slave port. See Section **Error! Bookmark not defined.** below for more details on platform management topics.

| Name     | Pin # | Description                                   | I/O              | PU / PD          | Comment |
|----------|-------|-----------------------------------------------|------------------|------------------|---------|
| IPMB_CLK | B91   | Clock I/O line for the multi-master IPMB port | I/O OD<br>3.3VSB | PU 2K2<br>3.3VSB |         |
| IPMB_DAT | B92   | Data I/O line for the multi-master IPMB port  | I/O OD<br>3.3VSB | PU 2K2<br>3.3VSB |         |



**Note:** Weak pull-up values are shown for the IPMB CLK and DAT lines in Table above. These are merely to prevent the lines from floating if no Carrier BMC is present. Stiffer pull-ups should be implemented on the Carrier with values appropriate to the situation at hand if the Carrier implements a BMC and an IPMB master.

### 4.3.9 General Purpose SPI

| Name                                                                           | Pin #                    | Description                                                                                | I/O    | PU / PD | Comment                               |
|--------------------------------------------------------------------------------|--------------------------|--------------------------------------------------------------------------------------------|--------|---------|---------------------------------------|
| GP_SPI_MISO                                                                    | B94                      | Serial data into the COM-HPC Module from the Carrier GP_SPI device ("Master In Slave Out") | I 3.3V |         |                                       |
| GP_SPI_MOSI                                                                    | B93                      | Serial data from the COM-HPC Module to the Carrier GP_SPI device ("Master Out Slave In")   | O 3.3V |         |                                       |
| GP_SPI_CLK                                                                     | B99                      | Clock from the Module to Carrier GP_SPI device                                             | O 3.3V |         |                                       |
| GP_SPI_CS0#<br>GP_SPI_CS1#<br><del>GP_SPI_CS2#</del><br><del>GP_SPI_CS3#</del> | B95<br>B96<br>B97<br>B98 | GP_SPI chip selects, active low                                                            | O 3.3V |         | GP_SPI CS2 and CS3 are not supported. |
| GP_SPI_ALERT#                                                                  | B100                     | Alert (interrupt) from a Carrier GP_SPI device to the Module                               | I 3.3V | PU 10K  |                                       |

### 4.3.10 Power & System Management

VIN\_PWR\_OK indicates that all the power to the Module is stable within the specified range and can be used to enable Module internal power supplies.

| Name    | Pin # | Description                                                                                                                                                                                                                         | I/O      | PU / PD | Comment |
|---------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|---------|---------|
| PWRBTN# | B02   | A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down.                                                    | I 3.3VSB | PU 10K  |         |
| RSTBTN# | C02   | Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when RSTBTN# is not able to reestablish control of the system, VIN_PWR_OK or a power cycle <b>may</b> be used. | I 3.3VSB | PU 90K  |         |
| PLTRST# | A12   | Platform Reset: output from Module to Carrier Board. Active low. Issued by Module chipset and <b>may</b> result from a low RSTBTN# input, a low VIN_PWR_OK input, a VCC power input that falls below the                            | O 3.3VSB |         |         |

|             |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                     |        |               |
|-------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|--------|---------------|
|             |     | minimum specification, a watchdog timeout, or <b>may</b> be initiated by the Module software..                                                                                                                                                                                                                                                                                                                                                                                               |                     |        |               |
| VIN_PWR_OK  | C06 | Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed.                                                                                                                                                                                                                                                                         | I 3.3V              | PU 10K |               |
| SUS_S3#     | B08 | <del>Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board <b>should</b> be used to enable the non-standby power on a typical ATX supply.</del><br><br>Even in single input supply system implementations (AT mode, no standby input), the SUS_S3# Module output should be used to disable any Carrier voltage regulators when SUS_S3# is low, to prevent bleed leakage from Carrier circuits into the Module.                    | <del>O 3.3VSB</del> |        | Not Supported |
| SUS_S4_S5#  | C08 | Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.                                                                                                                                                                                                                                                                                                                                                                                                       | O 3.3VSB            |        |               |
| SUS_CLK     | A87 | 32.768 kHz +/- 100 ppm clock used by Carrier peripherals such as M.2 cards in their low power modes.                                                                                                                                                                                                                                                                                                                                                                                         | O 3.3VSB            |        |               |
| WAKE0#      | D10 | PCI Express wake up signal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | I/O 3.3VSB          | PU 10K |               |
| WAKE1#      | D11 | General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.                                                                                                                                                                                                                                                                                                                                                                                          | I 3.3VSB            | PU 10K |               |
| BATLOW#     | A11 | Indicates that external battery is low.<br>This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.                                                                                                                                                                                                                                                                                                                      | I 3.3VSB            | PU 10K |               |
| TAMPER#     | B06 | <del>Tamper or Intrusion detection line on VCC_RTC power well. Carrier hardware pulls this low on a Tamper event.</del>                                                                                                                                                                                                                                                                                                                                                                      |                     |        | Not Supported |
| RSMRST_OUT# | B86 | This is a buffered copy of the internal Module RSMRST# (Resume Reset, active low) signal. The internal Module RSMRST# signal is an input to the chipset or SOC and when it transitions from low to high it indicates that the suspend well power rails are stable.<br><br>USB devices on the Carrier that are to be active in S5 / S3 / S0 should not have their 5V supply applied before RSMRST_OUT# goes high. RSMRST_OUT# shall be a 3.3V CMOS Module output, active in all power states. | O 3.3VSB            |        |               |

### 4.3.11 Thermal Protection

| Name         | Pin # | Description                                                             | I/O    | PU / PD | Comment |
|--------------|-------|-------------------------------------------------------------------------|--------|---------|---------|
| CARRIER_HOT# | C04   | Input from off-Module temp sensor indicating an over-temp situation.    | I 3.3V | PU 4.7K |         |
| THERMTRIP#   | B04   | Active low output indicating that the CPU has entered thermal shutdown. | O 3.3V |         |         |

### 4.3.12 SMBus

| Name       | Pin # | Description                                                                                                                         | I/O           | PU / PD | Comment                                                             |
|------------|-------|-------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|---------------------------------------------------------------------|
| SMB_CLK    | C86   | System Management Bus bidirectional clock line.                                                                                     | I/O OD 3.3VSB | PU 2.2K | The maximum capacitance on the Carrier Board shall not exceed 100pF |
| SMB_DAT    | C87   | System Management Bus bidirectional data line.                                                                                      | I/O OD 3.3VSB | PU 2.2K | The maximum capacitance on the Carrier Board shall not exceed 100pF |
| SMB_ALERT# | C88   | System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. | I 3.3VSB      | PU 10K  | The maximum capacitance on the Carrier Board shall not exceed 100pF |

### 4.3.13 General Purpose Input Outputs

| Name    | Pin # | Description                                                                                                                                                                                     | I/O        | PU / PD        | Comment |
|---------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|----------------|---------|
| GPIO_00 | A88   | General purpose input / output pins. Upon a hardware reset, these pins should be configured as inputs.<br><br>As inputs, these pins should be able to generate an interrupt to the Module host. | I/O 3.3VSB | PU 100K 3.3VSB |         |
| GPIO_01 | A89   |                                                                                                                                                                                                 |            |                |         |
| GPIO_02 | A90   |                                                                                                                                                                                                 |            |                |         |
| GPIO_03 | A91   |                                                                                                                                                                                                 |            |                |         |
| GPIO_04 | A92   |                                                                                                                                                                                                 |            |                |         |
| GPIO_05 | A93   |                                                                                                                                                                                                 |            |                |         |
| GPIO_06 | A94   |                                                                                                                                                                                                 |            |                |         |
| GPIO_07 | A95   |                                                                                                                                                                                                 |            |                |         |
| GPIO_08 | A96   |                                                                                                                                                                                                 |            |                |         |

|         |     |  |  |  |  |
|---------|-----|--|--|--|--|
| GPIO_09 | A97 |  |  |  |  |
| GPIO_10 | A98 |  |  |  |  |
| GPIO_11 | A99 |  |  |  |  |

### 4.3.14 Module Type Definition

| Name                    | Pin #                | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | I/O                | Comment                                    |  |  |         |     |       |       |       |  |   |    |    |    |          |   |    |    |     |          |   |    |     |    |          |   |    |     |     |                                 |   |     |    |    |          |   |     |    |     |          |   |     |     |    |                                            |   |     |     |     |                                 |  |                                 |
|-------------------------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|--------------------------------------------|--|--|---------|-----|-------|-------|-------|--|---|----|----|----|----------|---|----|----|-----|----------|---|----|-----|----|----------|---|----|-----|-----|---------------------------------|---|-----|----|----|----------|---|-----|----|-----|----------|---|-----|-----|----|--------------------------------------------|---|-----|-----|-----|---------------------------------|--|---------------------------------|
| TYPE0<br>TYPE1<br>TYPE2 | A100<br>C100<br>D100 | <p>The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). These pins shall be pulled up on the Carrier, to Carrier standby voltage rail of 5V or less. Carrier hardware reads the level on these straps.</p> <table> <tr> <th colspan="4">Module Connections</th><th>Meaning</th></tr> <tr> <th>Ref</th><th>TYPE2</th><th>TYPE1</th><th>TYPE0</th><th></th></tr> <tr> <td>7</td><td>NC</td><td>NC</td><td>NC</td><td>Reserved</td></tr> <tr> <td>6</td><td>NC</td><td>NC</td><td>GND</td><td>Reserved</td></tr> <tr> <td>5</td><td>NC</td><td>GND</td><td>NC</td><td>Reserved</td></tr> <tr> <td>4</td><td>NC</td><td>GND</td><td>GND</td><td>Server Module – Fixed 12V input</td></tr> <tr> <td>3</td><td>GND</td><td>NC</td><td>NC</td><td>Reserved</td></tr> <tr> <td>2</td><td>GND</td><td>NC</td><td>GND</td><td>Reserved</td></tr> <tr> <td>1</td><td>GND</td><td>GND</td><td>NC</td><td>Client Module - Wide Range 8V to 20V input</td></tr> <tr> <td>0</td><td>GND</td><td>GND</td><td>GND</td><td>Client Module – Fixed 12V input</td></tr> </table> <p>The Module shall implement all three TYPE[x] pins per the table above.</p> <p>The Carrier Board should implement combinatorial logic that monitors the Module TYPE pins and keeps power off (e.g deactivates the ATX PS_ON# signal to an ATX power supply or otherwise deactivates VCC to the COM-HPC Module) if an incompatible Module pin-out type is detected. All three TYPE[x] pins should be monitored by the Carrier. The Carrier Board logic may also implement a fault indicator such as an LED.</p> | Module Connections |                                            |  |  | Meaning | Ref | TYPE2 | TYPE1 | TYPE0 |  | 7 | NC | NC | NC | Reserved | 6 | NC | NC | GND | Reserved | 5 | NC | GND | NC | Reserved | 4 | NC | GND | GND | Server Module – Fixed 12V input | 3 | GND | NC | NC | Reserved | 2 | GND | NC | GND | Reserved | 1 | GND | GND | NC | Client Module - Wide Range 8V to 20V input | 0 | GND | GND | GND | Client Module – Fixed 12V input |  | Server Module – Fixed 12V input |
| Module Connections      |                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                    | Meaning                                    |  |  |         |     |       |       |       |  |   |    |    |    |          |   |    |    |     |          |   |    |     |    |          |   |    |     |     |                                 |   |     |    |    |          |   |     |    |     |          |   |     |     |    |                                            |   |     |     |     |                                 |  |                                 |
| Ref                     | TYPE2                | TYPE1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | TYPE0              |                                            |  |  |         |     |       |       |       |  |   |    |    |    |          |   |    |    |     |          |   |    |     |    |          |   |    |     |     |                                 |   |     |    |    |          |   |     |    |     |          |   |     |     |    |                                            |   |     |     |     |                                 |  |                                 |
| 7                       | NC                   | NC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | NC                 | Reserved                                   |  |  |         |     |       |       |       |  |   |    |    |    |          |   |    |    |     |          |   |    |     |    |          |   |    |     |     |                                 |   |     |    |    |          |   |     |    |     |          |   |     |     |    |                                            |   |     |     |     |                                 |  |                                 |
| 6                       | NC                   | NC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | GND                | Reserved                                   |  |  |         |     |       |       |       |  |   |    |    |    |          |   |    |    |     |          |   |    |     |    |          |   |    |     |     |                                 |   |     |    |    |          |   |     |    |     |          |   |     |     |    |                                            |   |     |     |     |                                 |  |                                 |
| 5                       | NC                   | GND                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | NC                 | Reserved                                   |  |  |         |     |       |       |       |  |   |    |    |    |          |   |    |    |     |          |   |    |     |    |          |   |    |     |     |                                 |   |     |    |    |          |   |     |    |     |          |   |     |     |    |                                            |   |     |     |     |                                 |  |                                 |
| 4                       | NC                   | GND                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | GND                | Server Module – Fixed 12V input            |  |  |         |     |       |       |       |  |   |    |    |    |          |   |    |    |     |          |   |    |     |    |          |   |    |     |     |                                 |   |     |    |    |          |   |     |    |     |          |   |     |     |    |                                            |   |     |     |     |                                 |  |                                 |
| 3                       | GND                  | NC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | NC                 | Reserved                                   |  |  |         |     |       |       |       |  |   |    |    |    |          |   |    |    |     |          |   |    |     |    |          |   |    |     |     |                                 |   |     |    |    |          |   |     |    |     |          |   |     |     |    |                                            |   |     |     |     |                                 |  |                                 |
| 2                       | GND                  | NC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | GND                | Reserved                                   |  |  |         |     |       |       |       |  |   |    |    |    |          |   |    |    |     |          |   |    |     |    |          |   |    |     |     |                                 |   |     |    |    |          |   |     |    |     |          |   |     |     |    |                                            |   |     |     |     |                                 |  |                                 |
| 1                       | GND                  | GND                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | NC                 | Client Module - Wide Range 8V to 20V input |  |  |         |     |       |       |       |  |   |    |    |    |          |   |    |    |     |          |   |    |     |    |          |   |    |     |     |                                 |   |     |    |    |          |   |     |    |     |          |   |     |     |    |                                            |   |     |     |     |                                 |  |                                 |
| 0                       | GND                  | GND                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | GND                | Client Module – Fixed 12V input            |  |  |         |     |       |       |       |  |   |    |    |    |          |   |    |    |     |          |   |    |     |    |          |   |    |     |     |                                 |   |     |    |    |          |   |     |    |     |          |   |     |     |    |                                            |   |     |     |     |                                 |  |                                 |

### 4.3.15 Miscellaneous Signals

| Name       | Pin # | Description                                                                                                                                                                                                                                                                                                                                                                                           | I/O       | PU / PD | Comment |
|------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|---------|---------|
| WD_OUT     | B11   | Output indicating that a watchdog time-out event has occurred. Refer to Section 5.3 for details.                                                                                                                                                                                                                                                                                                      | O 3.3V    |         |         |
| WD_STROBE# | B10   | Strobe input to watchdog timer. Periodic strobing prevents the watchdog, if enabled, from timing out.                                                                                                                                                                                                                                                                                                 | I 3.3V    |         |         |
| FAN_PWMOUT | C11   | <p>Fan speed control for a secondary system fan. The primary fan control signals for CPU thermal management are on the Module, along with a vendor specific connector.</p> <p>Fan controls use the Pulse Width Modulation (PWM) technique to control the fan's RPM. CMOS output; Carrier designers should buffer this signal with an open drain FET and pullup or other robust Carrier device(s).</p> | O 3.3V    |         |         |
| FAN_TACHIN | C12   | Fan tachometer input for a fan with a two pulse output for the secondary fan.                                                                                                                                                                                                                                                                                                                         | I OD 3.3V | PU 10K  |         |
| RSVD       |       | Reserved pins. These may be assigned functions in future versions of this specification. Reserved pins shall not be connected to anything, and shall not be connected to each other.                                                                                                                                                                                                                  |           |         |         |

#### WD\_OUT

If a Module supports a watchdog timer it shall minimally support output mode 1 and may also support output modes 2 or 3 as defined in the table below. The selection of the output modes may be realized by software configurable hardware or by Module build options.

| WD Mode | Description                                                                                                                           | Comment |
|---------|---------------------------------------------------------------------------------------------------------------------------------------|---------|
| 1       | The Module generates an internal reset. Module output pin PLTRST# is driven low. The WD_OUT pin is driven high until the unit resets. |         |
| 2       | The Module only drives WD_OUT pin high until cleared by Module software.                                                              |         |
| 3       | The Module generates an NMI. The WD_OUT pin is driven high until cleared by Module software.                                          |         |

The watchdog output shall come up as a logic low and shall be disabled upon power-on-reset (VCC power cycle) or external system reset (when RSTBTN# pin is toggled low by external hardware). The watchdog may be enabled by BIOS or system software.

#### **WD\_STROBE#**

Typically, the watchdog parameters (output options, enabling, enable delay, timeout delay) are managed by the Module BIOS, often via a BIOS setup screen. The regular watchdog software strobes to prevent a watchdog timeout are typically handled by the Module's application software. There may be API abstractions to isolate the application software from the watchdog hardware.

In COM-HPC (unlike COM-Express), there is a hardware strobe option. Carrier board hardware may periodically drive ("strobe") the Module WD\_STROBE# input pin low to keep the watchdog from timing out.

The software and hardware strobes should be implemented as a logical OR by the Module design, so that either method may be used, or both, to keep the watchdog from timing out.

The software programmable Watchdog Enable Delay is the time between when the watchdog is enabled by firmware and when the first watchdog strobe is needed to prevent a watchdog time out. The enable delay allows time for the operating system to boot and the application to load and initialize. This feature is sometimes referred to as a "two stage" watchdog. After the initial Enable Delay, the enabled watchdog must be periodically strobed by software to prevent a watchdog timeout. The Strobe Interval shall be software programmable. Recommended ranges in enable delay and max strobe periods are given in the following table.

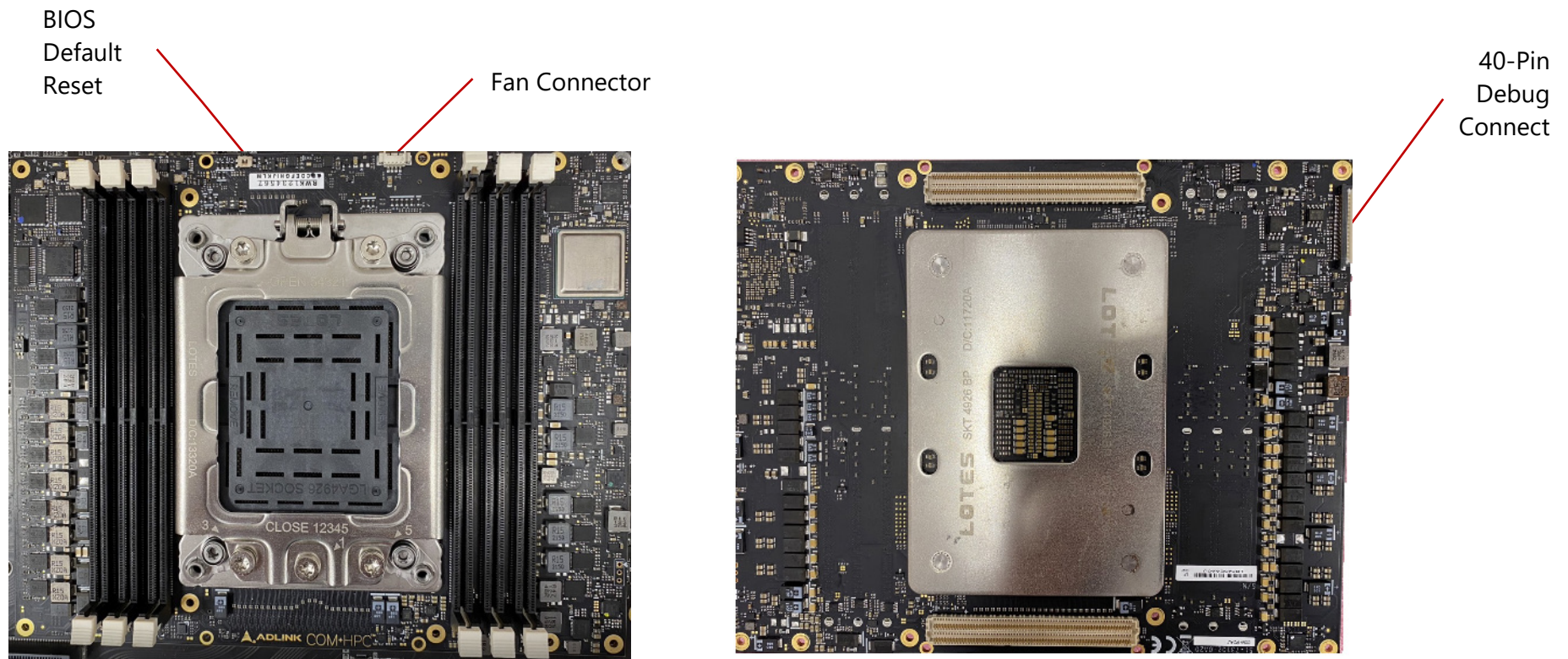
|                 | Min Value  | Max Value  |
|-----------------|------------|------------|
| Enable Delay    | 1 second   | 10 minutes |
| Strobe Interval | 0.1 second | 10 minutes |

### 4.3.16 Power and Ground

| Name       | Pin #                                                                                    | Description                                                                                                                                                                                  | I/O | PU / PD | Comment     |
|------------|------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---------|-------------|
| VCC        | A01-A09<br>B01<br>B03<br>B05<br>B07<br>B09<br>C01<br>C03<br>C05<br>C07<br>C09<br>D01-D09 | Primary power input:<br>fixed +12V on the Client Type 0; wide range +8V to +20V on the Client Type 1;<br>fixed +12V on the Server.<br>All available VCC pins on the connector shall be used. | P   |         | 12V +/- 5%  |
| VCC_5V_SBY | B24                                                                                      | Standby power input: +5.0V nominal.<br>Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.                            | P   |         | 5VSB +/- 5% |
| VCC_RTC    | A86                                                                                      | Real-time clock circuit-power input. Nominally +3.0V.                                                                                                                                        | P   |         |             |
| GND        |                                                                                          | Ground - DC power and signal and AC signal return path.<br>All available GND connector pins shall be used and tied to Carrier Board GND plane(s).                                            | P   |         |             |

## 5. Additional Features

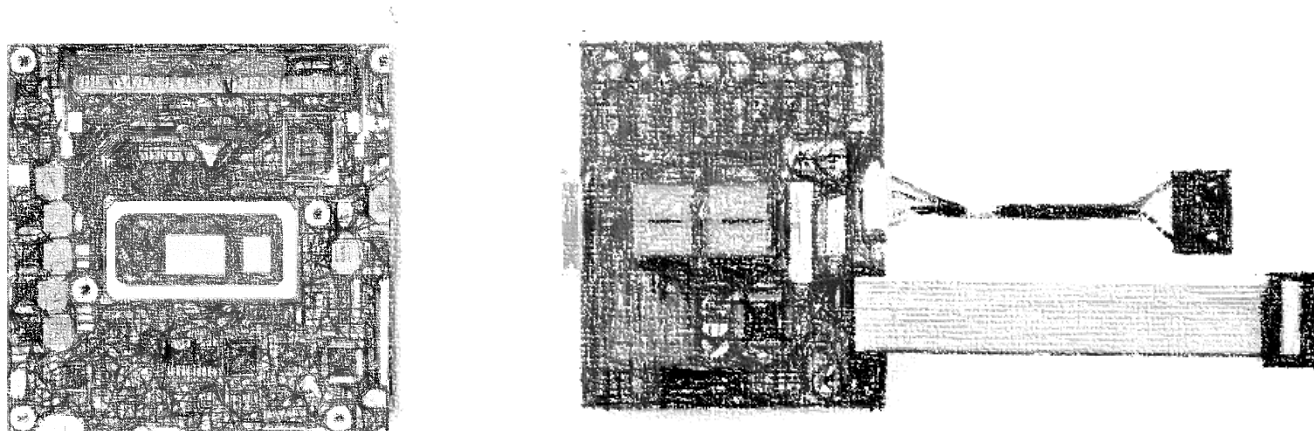
This chapter describes the connectors, LEDs, and switches, located on the module and are not necessarily included in the PICMG standard specification. The locations of these parts are as shown below:



## 5.1 Debug Connector (40-pin connector)

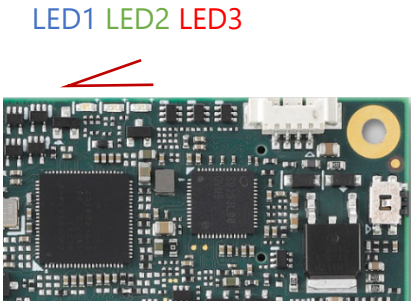
This connector is particularly useful during carrier design and bring up phase. It offers access to the following critical parts of the module:

- Test points for measurement of internal power rails
- SPI BIOS programming interface
- I2C bus for BIOS POST code readout
- BMC programming interface



5.2 Status LEDs

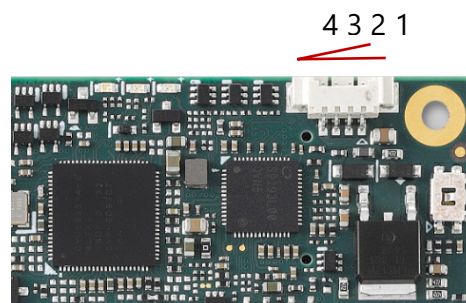
Status LEDs are mounted on the module as below



| Name | Color | Connection                                               | Function                                                                                                                                                                                                                                                                                                                                                                   |
|------|-------|----------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LED1 | Blue  | BMC output                                               | Power Sequence Status Code (BMC) Power Changes, Reset (see Exception Codes Table below)                                                                                                                                                                                                                                                                                    |
| LED2 | Green | Power Source 3Vcc                                        | S0 LED ON<br>S3/S4/S5 LED OFF<br>ECO mode LED OFF                                                                                                                                                                                                                                                                                                                          |
| LED3 | Red   | BMC output and same signal as WDT (B27) on BtB connector | Module power up WD LED = LED OFF<br>Watchdog counting WD LED = Keep Last State<br>Watchdog timed out WD LED = LED ON<br>Watchdog RESET WD LED = LED ON<br>Rebooted after WD RESET WD LED = LED ON<br>Rebooted after PWRBTN WD LED = LED OFF<br>Rebooted after RESET BTN WD LED = LED OFF<br>Note: only a Reset not initiated by the BMC can clear the WD LED (user action) |

## 5.3 Fan Connector

Connector Type: JVE 24W1125A-04M00

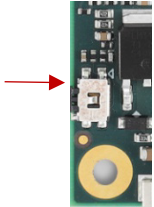


| Name | Description |
|------|-------------|
| 1    | FAN_PWMOUT  |
| 2    | FAN_TACHIN  |
| 3    | GND         |
| 4    | 12V*        |

The supply voltage and maximum current of the fan connector is dependent on the module's input voltage (VCC\_12V pins)

- If the module's input voltage is 12V or lower, the supply voltage will be equal to the module's input voltage and the maximum supply current of the fan connector will be TBC mA.
- If the module's input voltage is from 12V to 20V, the supply voltage will be 12V ( $\pm 5\%$ ) and the maximum supply current of the fan connector will be TBC mA..

## 5.4 BIOS Default Reset (update later)



To perform a hardware reset of the default BIOS settings, follow the steps below:

1. Shut down the system.
2. Hold down the BIOS Setup Defaults Reset Button continuously and boot up the system. You can release the button when the BIOS prompt screen appears.
3. The BIOS prompt screen will display a confirmation that BIOS defaults have been reset and request that you reboot the system.



## 5.5 BIOS Boot Select (update later)

The module has two BIOS chips (BOM option) and BIOS operation can be configured to "PICMG" and dual-BIOS "Failsafe" modes using the BIOS Select and Mode Configuration Switch, Pin 2.

Setting the module to PICMG mode will configure the BIOS chips on the module as SPI0 and SPI1. In PICMG mode, a BIOS chip cannot be placed in the SPI0 slot on the carrier.

In dual-BIOS Failsafe mode, both BIOS chips on the module are configured as SPI1. Only one of the two is connected to the SPI bus at any given time. In case of failure of the primary SPI1 BIOS, the system will reboot and switch to the secondary SPI1 BIOS on the module. In Failsafe mode, the SPI0 BIOS socket on the carrier can be populated.

In either mode, BIOS Select and Mode Configuration Switch, Pin 1 is used to select whether to boot from SPI0 or SPI1.

| Mode                                  | Pin 1 | Pin 2 |
|---------------------------------------|-------|-------|
| Boot from SPI0 (default)              | On    | -     |
| Boot from SPI1                        | Off   | -     |
| Set BIOS to PICMG mode (default, TBC) | -     | On    |
| Set BIOS to Failsafe BIOS mode        | -     | Off   |

## 6. BIOS Checkpoints, Beep Codes

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This document section lists checkpoints and beep codes generated by AMI Aptio BIOS. The checkpoints defined in this document are inherent to the AMIBIOS generic core, and do not include any chipset or board-specific checkpoint definitions.

### Checkpoints and Beep Codes Definition

A checkpoint is either a byte or word value output to I/O port 80h. The BIOS outputs checkpoints throughout the boot block and Power-On Self-Test (POST) to indicate the task the system is currently executing. Checkpoints are very useful for debugging problems that occur during the preboot process.

Beep codes are used by the BIOS to indicate a serious or fatal error. They are used when an error occurs before the system video has been initialized, and generated by the system board speaker.

### Aptio Boot Flow

While performing the functions of the traditional BIOS, Aptio 5.x core follows the firmware model described by the Intel Platform Innovation Framework for EFI ("the Framework"). The Framework refers the following "boot phases", which may apply to various status code & checkpoint descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization<sup>1</sup>
- Driver Execution Environment (DXE) – main hardware initialization<sup>2</sup>
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, ...)

### Viewing BIOS Checkpoints

Viewing all checkpoints generated by the BIOS requires a checkpoint card, also referred to as a POST Card or POST Diagnostic Card. These are PCI add-in cards that show the value of I/O port 80h on a LED display.

Some computers display checkpoints in the bottom right corner of the screen during POST. This display method is limited, since it only displays checkpoints that occur after the video card has been activated.

Keep in mind that not all computers using AMI Aptio BIOS enable this feature. In most cases, a checkpoint card is the best tool for viewing AMI Aptio BIOS checkpoints.

<sup>1</sup>Analogous to "boot block" functionality of legacy BIOS

<sup>2</sup>Analogous to "POST" functionality in legacy BIOS

### Aptio V Checkpoint and Beep Codes

Download the Aptio V Checkpoint and Beep Codes from the AMI website at: [www.ami.com](http://www.ami.com)

## Viewing Checkpoints

Checkpoints generated by Aptio firmware can be viewed using a PCI checkpoint card, also referred to as a "POST Card" or "POST Diagnostic Card". These PCI add-in cards show the value of I/O port 80h on a LED display. Checkpoint cards are available through a variety of computer mail-order outlets.

Newer systems feature support for AMI Debug Rx, a USB connected alternative to the PCI POST Card. AMI Debug Rx is a low-cost debug tool built around the debug port feature common to today's USB 2.0 EHCI controllers. AMI Debug Rx is designed as replacement for the PCI POST Checkpoint Card as newer systems omit PCI expansion slots. Along with checkpoints, AMI Debug Rx has several features specifically designed for BIOS developers.

## 6.1 Status Code Ranges

| Code Range  | Description                                        |
|-------------|----------------------------------------------------|
| 0x01 – 0x0B | SEC execution                                      |
| 0x0C – 0x0F | SEC errors                                         |
| 0x10 – 0x2F | PEI execution up to and including memory detection |
| 0x30 – 0x4F | PEI execution after memory detection               |
| 0x50 – 0x5F | PEI errors                                         |
| 0x60 – 0x8F | DXE execution up to BDS                            |
| 0x90 – 0xCF | BDS execution                                      |
| 0xD0 – 0xDF | DXE errors                                         |
| 0xE0 – 0xE8 | S3 Resume (PEI)                                    |
| 0xE9 – 0xEF | S3 Resume errors (PEI)                             |
| 0xF0 – 0xF8 | Recovery (PEI)                                     |
| 0xF9 – 0xFF | Recovery errors (PEI)                              |

**Note:** Table above is subject to future updates.

## 7. Mechanical and Thermal

### 7.1 Module Dimensions

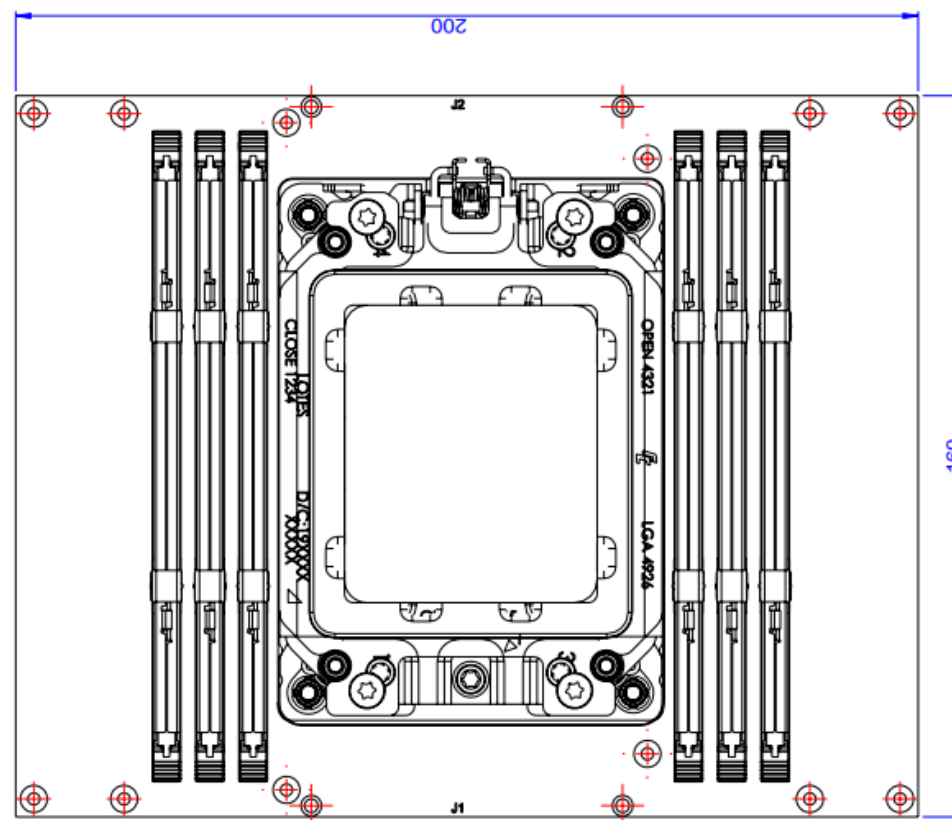


Figure 3 – Module dimensions (mm)

## 7.2 Thermal Solutions

### 7.2.1 Heatsink : THS-ALT-BL

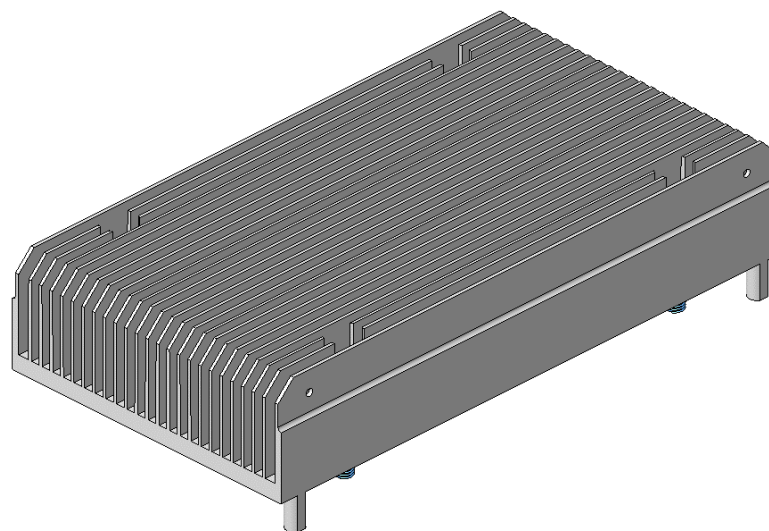


Figure 4 – Heatsink THS-ALT-BL

### 7.2.2 Low Profile Active Cooler: THSF-ALT-BL-S

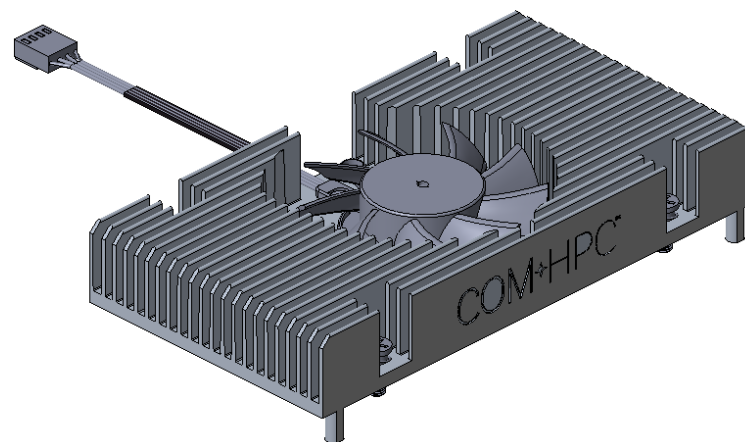


Figure 5 – THSF-ALT-BL-S

### 7.2.3 High Profile Passive Heatsink: THSH-ALT-VC

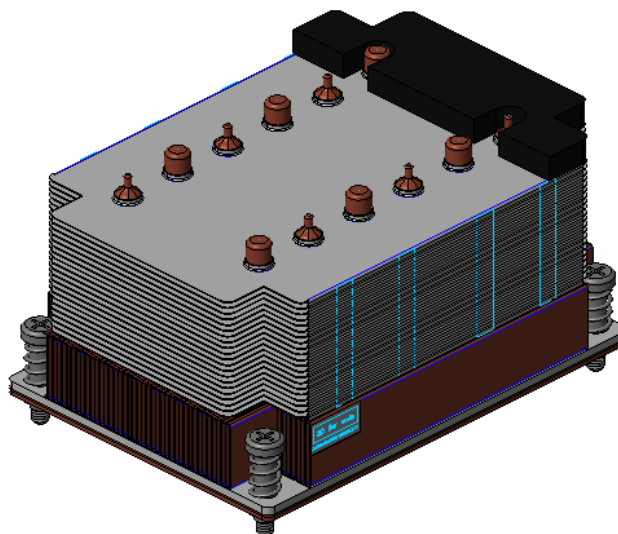


Figure 6 – High profile passive heatsink THSH-ALT-VC

## 7.2.4 Active Cooling: THSF-ALT-BL

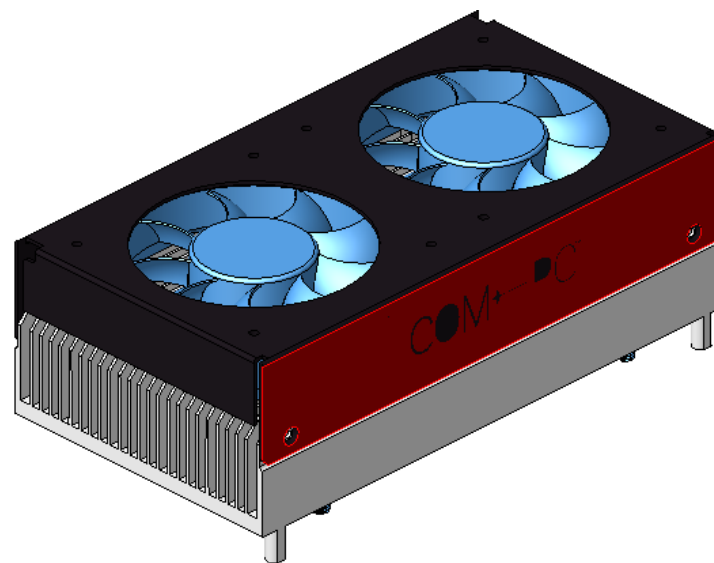


Figure 7 – Cooler THSF-ALT-BL