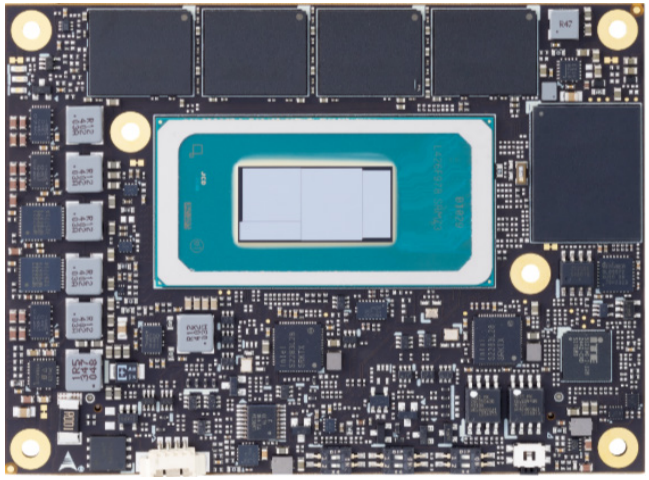
COM-HPC-mMTL

User's Guide

intel



COM-HPC™

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ADLINK
LEADING EDGE COMPUTING

Revision History

Revision	Description	Date	Author
0.1	Preliminary release	2025-06-18	AL
0.2	Installation updated	2025-06-26	AL
0.3	Mechanical and thermal updated	2025-07-08	AL

Preface

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Safety Instructions

For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

Read these safety instructions carefully.

- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

Conventions

The following conventions may be used throughout this manual, denoting special levels of information

Note: This information adds clarity or specifics to text and illustrations.

Caution: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

Warning: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

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1. Introduction

The COM-HPC-mMTL is the **smallest COM module that delivers powerful computing performance and rich interfaces**. It integrates Intel® Core™ Ultra processors (formerly "Meteor Lake-H/U") in a compact 95x70mm dimension Mini Type COM-HPC form factor. With up to16 CPU cores (Six P-cores + Eight E-cores + Two Low Power E-cores) and a nominal **TDP of just 28W**, it is well-suited for space-constrained edge computing and battery-powered applications.

Moreover, COM-HPC-mMTL features powerful integrated Intel Arc graphics with 8 Xe-cores and a neural processing unit (NPU) to efficiently handle varioustypes of workloads and AI models. Combined with high bandwidth LPDDR5 soldered memory, it is ideal for edge AI applications.

The integrated Intel® Iris® ARC Low Power Graphics includes features such as OpenGL 4.5, DirectX 12, OpenCL 2.1/2.0/1.2, Intel® Clear Video HD Technology, and DirectX Video Acceleration (DXVA), supporting full H.265/HEVC 10-bit and VP9 hardware codecs. In addition, High Dynamic Range is supported for enhanced color and image quality, and digital content protection has been upgraded to HDCP 2.3. Graphics outputs include eDP and up to two DDI ports supporting HDMI/DVI/DisplayPort, with up tof four 4K displays supported. Additionally, USB4 Alt Mode is available as an alternative for display output. USB4, which can transfer media and data through single tunnel, is a build option—available on a **per-project basis**—in place of DDI port 0, 1, or even USB 3.x port 2.

Inputs/outputs provided include 2x PCIe Gen4 x4 lane, a default 7x PCIe Gen4 lanes, and 2x 2.5GbE Ethernet. Up to 8x PCIe Gen4 lanes are available if only 1x 2.5GbE Ethernet configured. The default includes 3x USB3.x/2.0 ports and 5x USB 2.0 ports. Low speed interfaces, such as 12x GPIO pins and 2x UART interfaces, are supported. A TPM chip is equipped for security-related purposes. In addition, onboard PCIe Gen4 NVMe SSD and 2x SATA 6Gb/s are build options supported by project basis.

Support for SMBus and 2x I2C is also available, and the module is equipped with an SPI AMI EFI BIOS with CMOS backup, supporting embedded features such as remote console, hardware monitor, and watchdog timer.

2. Specifications

2.1 Core System

CPU

1st Gen Core™ Ultra Processor (formerly "Meteor Lake-H/U")

- Intel® Core Ultra 7 155H 4.8/1.4GHz, 28W with 20-65W cTDP (6P+8E+2LP-E/22T and additional 2 NPU)
- Intel® Core Ultra 5 135H 4.6/1.7GHz, 28W with 20-65W cTDP (4P+8E+2LP-E/18T and additional 2 NPU)
- Intel® Core Ultra 5 125H 4.5/1.2GHz, 28W with 20-65W cTDP (4P+8E+2LP-E/18T and additional 2 NPU)
- Intel® Core Ultra 5 135U 4.4/1.6GHz, 15W with 12-28W cTDP (2P+8E+2LP-E/14T and additional 2 NPU)
- Intel® Core Ultra 5 125U 4.3/1.3GHz, 15W with 12-28W cTDP (2P+8E+2LP-E /14T and additional 2 NPU)

NPU

Up to 8.2 TOPS, integrated

Memory

Up to 64GB (4x 16GB) LPDDR5 soldered down memory

4GB/8GB/16GB/32GB/64GB capacity ranged. Some of configuration will be supported by project basis

Embedded BIOS

AMI UEFI with CMOS backup in 32MB SPI BIOS (dual BIOS by build option)

Cache

- Ultra 7 155H 24MB
- Ultra 5 135H/125H 18MB
- Ultra 5 135U/125U 12MB

2.2 Video

GPU

Intel® Xe Graphics architecture with up to 128 execution units

Display Interface

4 independent and simultaneous combinations of DisplayPort/HDMI/eDP and USB4 DP Alt Mode (4x 4K @60Hz). Playback of high-definition content including Blu-ray Disc and Blu-ray Disc 3D content using HDMI (1.4a spec compliant with 3D)

Graphics Acceleration

DirectX 12 Video Acceleration (DXVA)/Open GL 4.6/Vulkan 1.2 and one VPL support for accelerated video processing.

Video Decode or Encode

HEVC, VP9, AV1

Note:The availability of features depends on the operating system used (Windows 10/11 64-bit, Linux 64-bit).

2.2.1 Display Interface Support

DDI: Up to two DDI are supported, with options for DisplayPort 1.4a, HDMI 2.1 or DVI at port 0, port 1. DDI port 0 is enabled by default.

eDP: Supports eDP 1.4b with up to 4 lane, resolutions up to 4096x2304@60Hz bpp with DSC.

Optional USB4: Up to three USB4 ports are available via DP Alt Mode. This is a build option (HW and BIOS) by project basis. USB4 support also requires a re-timer and PD on the carrier.

USB4 port 0 in place of DDI port 1, USB4 port 1 replaces USB3.x port 2-3. USB4 port 2 replaces DDI port 0. USB4 port 0, port 1 are enabled by default

Pin Sharing Mechanism

The COM-HPC Mini form factor offers only one highspeed COM-HPC 400-pin connector. To optimize the pin, certain DDI/USB4/USB3.x share the same pins. A maximum of Eight Super Speed lanes (SS), SS Lane 0 to SS Lane 7, are defined in the COM-HPC specification for this shared usage.. Each SS consist of TX-/+ and RX-/+

For example: SS lane 0 and SS lane 1 can be implemented as either DDI port 0 or USB4 port 2.

Table below indicates the mapping between SS lanes and DDI/USB4/USB3.x functionality for this product

- DDI_0 indicates DDI port 0, USB4_2 indicates USB4 port 2. USB3_0 indicates USB3.x port 0
- For example, SS lane 4 and SS lane 5 can be either used as USB4 port 1 (based on SS lane 4 and lane 5) or USB3.x port 3 (based on SS lane 4).

Based on the combination of the COM-HPC-mMTL module and ADLINK's COM-HPC Mini Base, the default supported configuration is Config 3

All other configurations are subject to discussion and supported on a project basis.

SS Lanes	Config 1	Config 2	Config 3	Config 4	Config 5
SS Lane 0	DDI_0	DDI_0	**DDI_0**	USB4_2	USB4_2
SS Lane 1					
SS Lane 2	DDI_1	USB4_0	**USB4_0**	USB4_0	USB4_0
SS Lane 3					
SS Lane 4	USB3_3	USB3_3	**USB4_1**	USB4_1	USB4_1
SS Lane 5	-	-			
SS Lane 6	USB3_1	USB3_1	**USB3_1**	USB3_1	USB4_3
SS Lane 7	USB3_0	USB3_0	**USB3_0**	USB3_0	(TBC, project basis)

2.3 Audio

A maximum of one HDA, maximum one I2S, four SNDW, two DMIC are defined in the PICMG specification for pin sharing configurations (HDA/I2S/SNDW/DMIC).

HDA

Default support is HDA

Intel® HD Audio integrated

Located on carrier COM-HPC-mini base (ALC888 standard support)

Note: I2S, SNDW, and DMIC support depends on driver readiness and is to be confirmed (TBC).

2.4 Expansion Buses

Maximum 16 PCIe Gen4 lanes

1x PCI Express x4: Lane 8-11 (configurable to 1 x4)

1x PCI Express x4: Lane 12-15 (configurable to 1 x4)

4x PCI Express x1: Lane 0-3 (4 x1, 2 x2, 1 x4 configurable)

Up to 4x PCI Express x1: Lane 4-7 (4 x1, 2 x2, 1 x4 configurable)

In addition, PCIe lane 6 is muxed with SATA port 1, and PCIe lane 7 is muxed with SATA port 0 and NBASE-T port 1. By default, PCIe lane 6 and NBASE-T port 1 are enabled. A maximum of **9** PCIe Root Ports (or devices) can be enabled at the same time. (On-board LAN controllers are PCIe based devices and must also be counted. The optional on-board NMVe SSD is a PCIe based device and also need be counted.)

Note: Gen4 support is also dependent on the carrier design.

2 PCI Express Reference Clocks: PCIe_REFCLK0_LO, PCIe_REFCLK0_HI. PCIe_REFCLK0_LO is recommended as the reference clock pair for PCIe lanes [0:7], while PCIe_REFCLK0_HI is recommended for PCIe lanes [8:15].

Others: SMBus (system), 2x I2C (user), eSPI bus, GP_SPI (project basis discussion), Boot_SPI (only for system BIOS)

Note: eSPI_CS1 is disabled by default. eSPI_CS1 should be enabled if there's an eSPI based chip on the carrier board—for example, a Super I/O chip. eSPI_CS1 can be enabled in the BIOS menu.

2.5 Ethernet NBASE-T

Up to 2x NBASE-T (port 0, 1)

Onboard Intel® i226 series Ethernet Controller, 2pcs

2.5Gbps, 1Gbps, and 100/10Mbps connections, 1000BASE-T mode support

Note: NBASE-T port 1 is muxed with PCIe lane 7/SATA port 0. NBASE-T port 1 is a default feature.

2.6 Multi I/O and Storage

USB

USB3.x/2.0 (Ports 0, 1, 2). Up to three ports supported. USB3.x supports speeds up to 10Gb/s speed and is also dependent on the carrier board design. USB3.x port 0, port 1 are enabled as default.

4x USB 2.0 (Ports 4, 5, 6, 7)

Optional USB4 (Ports 0, 1, 2). Up to three interfaces supported. These are available In place of DDI port 0, 1, and USB3x. port 2. USB4 requires a re-timer and PD on the carrier. USB4 port 0, port 1 are enabled by default.

Note: Capable of TBT4. Contact your local ADLINK representative for details (TBC).

SATA

Optional 2x SATA 6Gb/s (SATA 0, 1). Maximum two interfaces

SATA_1 muxed with PCIe_6. SATA_0 muxed with NBASE-T port 1 / PCIe_7. SATA interfaces are available as a build option, supported on a project basis support

NVMe SSD

Optional on-board NVMe SSD PCIe x4. Build option by project basis. Only available for 28W CPU SKU (155H, 135H, 125H CPU)

UART

2x UART on module (UART_0, UART_1)

Console Redirection COM1 or COM2 selectable by BIOS

SER0, SER1 from CPU UART are supported by BOM option and project basis

Up to 4 serial ports supported by standard BIOS, including Super I/O on carrier board

COM Port	Description	IRQ	Address	Console Redirection Support
COM 1	Supported by module (UART 0), via embedded controller	4	0x3F8	Yes
COM 2	Supported by module (UART 1), via embedded controller	3	0x2F8	Yes
COM 3	Supported by Super I/O (NCT6126D) on carrier	5	0x240	Yes
COM 4	Supported by Super I/O (NCT6126D) on carrier	7	0x248	Yes

Note: eSPI_CS1 is disabled by default. eSPI_CS1 should be enabled if there's an eSPI based chip on the carrier board, for example, a Super I/O chip. eSPI_CS1 can be enabled in the BIOS menu.

GPIO

12x GPIO (GPI with interrupt)

GPI and GPO from SoC GPIO are supported by BOM option and project basis

MIPI-CSI

Optional 2x MIPI-CSI 4-lanes (the readiness of driver and supported camera module is TBC)

2.7 Trusted Platform Module (TPM)

Chipset: Infineon solution

Type: TPM 2.0 (SPI bus based)

2.8 SEMA Board Controller

Supports voltage/current monitoring, power sequence debug, logistics and forensic information, general purpose I2C, failsafe BIOS (dual BIOS, build, optional support), watchdog Timer, and fan control.

2.9 Debug

40-pin flat cable connector for DB40-HPC debug module.

Supports BIOS POST code LED, SEMA Board Controller access, Module Management Controller access, SPI BIOS flashing, Internal power rail test points, and Debug LEDs.

2.10 Power

Power Modes: single power rail input

Standard Voltage Input: single power rail input, 12V±5%

Wide Voltage Input: single power rail input, 8-20V

Power Management: ACPI 5.0 compliant

Power States: C0-C6, S0, S3, S5, ECO mode (Wake-on-USB S3/S4, WoL S3/S4/S5)

Power Consumption

Please contact our ADLINK representative for the document-"COM-HPC Mini Module Power Consumption."

2.11 Mechanical and Environmental

Form Factor and Specification

PICMG COM-HPC Revision 1.2, mini Type, Size is 95 x 70 mm

Operating Temperature

Standard	0°C to 60°C (Wide Voltage Input)	Storage: -20°C to 80°C

Humidity

5-90% RH operating, non-condensing, 5-95% RH storage (and operating with conformal coating)

Shock and Vibration

HALT tested

Thermal Stress, Vibration Stress, Thermal Shock, and Combined Test

3. Block Diagram

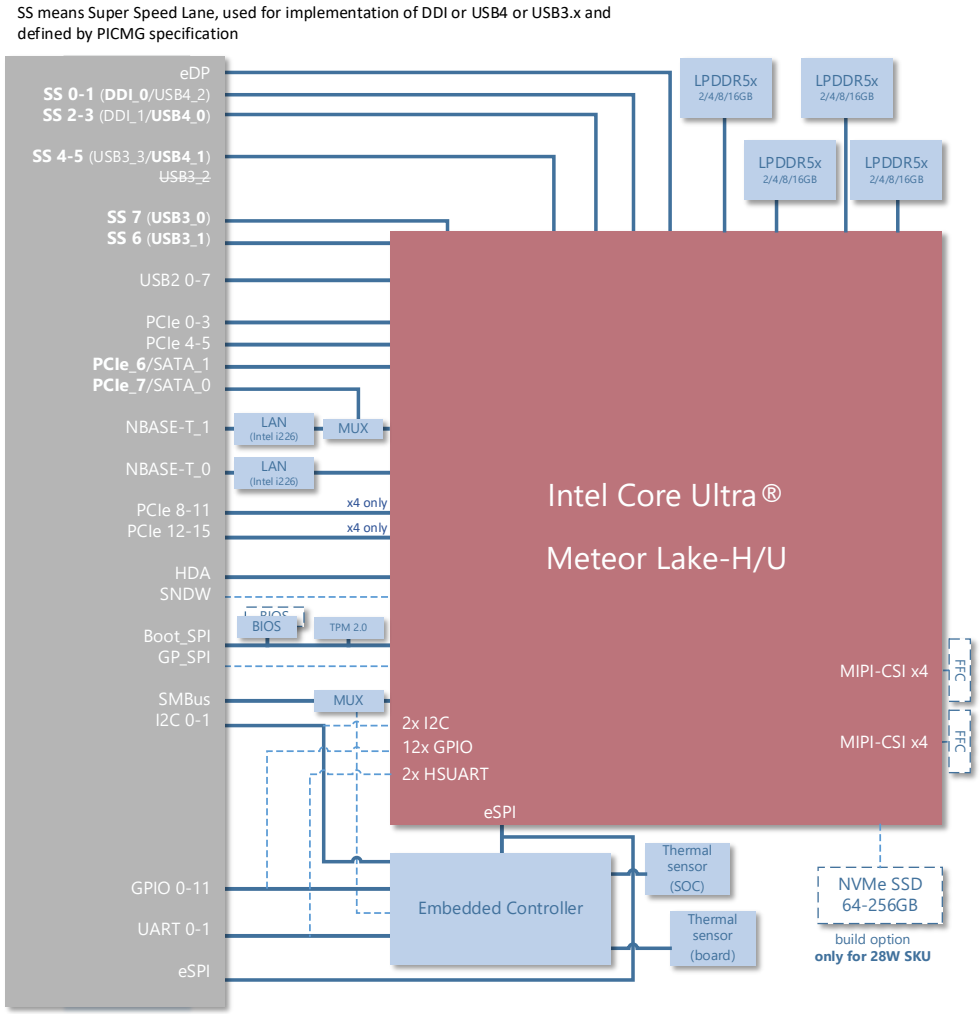


Figure 1 – Module function diagram

4. Pinout and Signal Descriptions

4.1 Pin Summary

The table below is a comprehensive list of all signal pins supported on the single 400-pin COM-HPC connectors as defined for Mini Type in the PICMG COM-HPC R1.2 specification. Signals described in the specification but not supported on the COM-HPC-mMTL are marked by ~~STRIKETHROUGH.~~

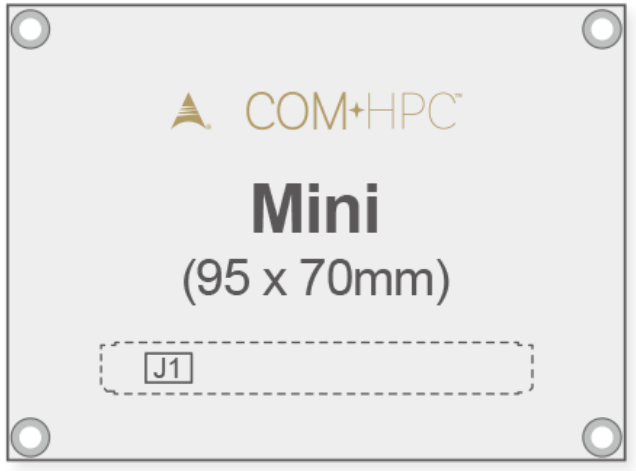


Figure 2 – Module rear side row and pin numbering

Row A			Row B			Row C			Row D	
A1	VCC		B1	VCC		C1	VCC		D1	VCC
A2	VCC		B2	PWRBTN#		C2	RSTBTN#		D2	VCC
A3	VCC		B3	VCC		C3	VCC		D3	VCC
A4	VCC		B4	THERMTRIP#		C4	CARRIER_HOT#		D4	VCC
A5	~~RAPID_SHUTDOWN~~		B5	~~CAN_TX~~		C5	~~CAN_RX~~		D5	PLTRST#
A6	~~FUSA_SPI_ALERT~~		B6	TAMPER#		C6	VIN_PWR_OK		D6	~~FUSA_SPI_CS#~~
A7	~~FUSA_STATUS0~~		B7	PROCHOT#		C7	CATERR#		D7	~~FUSA_SPI_CLK~~
A8	~~FUSA_STATUS1~~		B8	SUS_S3#		C8	SUS_S4_S5#		D8	~~FUSA_SPI_MISO~~
A9	~~PCIe_PERST_IN0#~~		B9	~~FUSA_VOLTAGE_ERR#~~		C9	~~FUSA_ALERT#~~		D9	~~FUSA_SPI_MOSI~~
A10	GND		B10	WD_STROBE#		C10	BATLOW#		D10	WAKE0#
A11	~~PCIe_REFCLKIN0-~~		B11	WD_OUT		C11	FAN_PWMOUT		D11	WAKE1#
A12	~~PCIe_REFCLKIN0+~~		B12	GND		C12	FAN_TACHIN		D12	GND
A13	GND		B13	USB5-		C13	GND		D13	USB1-
A14	USB7-		B14	USB5+		C14	USB3-		D14	USB1+
A15	USB7+		B15	GND		C15	USB3+		D15	GND
A16	GND		B16	USB4-		C16	GND		D16	USB0-
A17	USB6-		B17	USB4+		C17	USB2-		D17	USB0+
A18	USB6+		B18	GND		C18	USB2+		D18	GND
A19	GND		B19	~~I2S_LRCLK/SNDW_CLK3~~/HDA_SYNC		C19	GND		D19	SS01_SDA_AUX-
A20	SS23_SDA_AUX-		B20	~~I2S_DOUT/SNDW_DAT3~~/HDA_SDO		C20	~~SNDW_DMIC_CLK1~~		D20	SS01_SCL_AUX+
A21	SS23_SCL_AUX+		B21	~~I2S_MCLK~~/HDA_RST#		C21	~~SNDW_DMIC_DAT1~~		D21	GND
A22	GND		B22	~~I2S_DIN/SNDW_DAT2~~/HDA_SDI		C22	GND		D22	SS0_TX-
A23	SS2_TX-		B23	~~I2S_CLK/SNDW_CLK2~~/HDA_BCLK		C23	~~SNDW_DMIC_CLK0~~		D23	SS0_TX+
A24	SS2_TX+		B24	RSVD		C24	~~SNDW_DMIC_DAT0~~		D24	GND
A25	GND		B25	USB67_OC#		C25	GND		D25	SS0_RX-
A26	SS2_RX-		B26	USB45_OC#		C26	USB0_LSRX/DDI1_DDC_AUX_SEL		D26	SS0_RX+
A27	SS2_RX+		B27	USB23_OC#		C27	USB1_LSRX		D27	GND
A28	GND		B28	USB01_OC#		C28	USB0_LSTX/DDI1_HPD		D28	SS1_TX-
A29	SS3_TX-		B29	SML1_CLK		C29	USB1_LSTX		D29	SS1_TX+
A30	SS3_TX+		B30	SML1_DAT		C30	eDP_HPD		D30	GND
A31	GND		B31	PMCALERT#		C31	eDP_VDD_EN		D31	SS1_RX1
A32	SS3_RX-		B32	SML0_CLK		C32	eDP_BKLT_EN		D32	SS1_RX+
A33	SS3_RX+		B33	SML0_DAT		C33	eDP_BKLTCTL		D33	GND
A34	GND		B34	USB_PD_ALERT#		C34	GND		D34	ACPRESENT
A35	eDP_AUX-		B35	USB_PD_I2C_CLK		C35	USB3_AUX-		D35	NBASET1_SDP
A36	eDP_AUX+		B36	USB_PD_I2C_DAT		C36	USB3_AUX+		D36	GND

Row A			Row B			Row C			Row D	
A37	GND		B37	USB_RT_ENA		C37	GND		D37	SS6_TX-
A38	eDP_TX0-		B38	USB3_LSRX		C38	SS6_RX-		D38	SS6_TX+
A39	eDP_TX0+		B39	USB3_LSTX		C39	SS6_RX+		D39	GND
A40	GND		B40	USB2_LSRX/DDI0_DDC_AUX_SEL		C40	GND		D40	SS7_TX-
A41	eDP_TX1-		B41	USB2_LSTX/DDI0_HPD		C41	SS7_RX-		D41	SS7_TX+
A42	eDP_TX1+		B42	GND		C42	SS7_RX+		D42	GND
A43	GND		B43	USB1_AUX-		C43	GND		D43	SS4_TX-
A44	eDP_TX2-		B44	USB1_AUX+		C44	SS4_RX-		D44	SS4_TX+
A45	eDP_TX2+		B45	LID#		C45	SS4_RX+		D45	GND
A46	GND		B46	SLEEP#		C46	GND		D46	SS5_TX-
A47	eDP_TX3-		B47	VCC_BOOT_SPI		C47	SS5_RX-		D47	SS5_TX+
A48	eDP_TX3+		B48	BOOT_SPI_CS#		C48	SS5_RX+		D48	GND
A49	GND		B49	BSEL0		C49	GND		D49	NBASET1_MDI0-
A50	eSPI_IO0		B50	BSEL1		C50	BOOT_SPI_IO0		D50	NBASET1_MDI0+
A51	eSPI_IO1		B51	BSEL2		C51	BOOT_SPI_IO1		D51	GND
A52	eSPI_IO2		B52	eSPI_ALERT0#		C52	BOOT_SPI_IO2		D52	NBASET1_MDI1-
A53	eSPI_IO3		B53	eSPI_ALERT1#		C53	BOOT_SPI_IO3		D53	NBASET1_MDI1+
A54	eSPI_CLK		B54	eSPI_CS0#		C54	BOOT_SPI_CLK		D54	GND
A55	GND		B55	eSPI_CS1#		C55	GND		D55	NBASET1_MDI2-
A56	PCIe_CLKREQ0_LO#		B56	eSPI_RST#		C56	PCIe_REFCLK0_HI-		D56	NBASET1_MDI2+
A57	PCIe_CLKREQ0_HI#		B57	~~PCIe_WAKE_OUT0#~~		C57	PCIe_REFCLK0_HI+		D57	GND
A58	~~PCIe_CLKREQ_OUT0#~~		B58	NBASET1_LINK_MID#		C58	GND		D58	NBASET1_MDI3-
A59	NBASET1_LINK_MAX#		B59	NBASET1LINK_ACT#		C59	PCIe_REFCLK0_LO-		D59	NBASET1_MDI3+
A60	NBASET1_CTREF		B60	GND		C60	PCIe_REFCLK0_LO+		D60	GND
A61	GND		B61	PCIe08_RX-		C61	GND		D61	PCIe00_TX-
A62	PCIe08_TX-		B62	PCIe08_RX+		C62	PCIe00_RX-		D62	PCIe00_TX+
A63	PCIe08_TX+		B63	GND		C63	PCIe00_RX+		D63	GND
A64	GND		B64	PCIe09_RX-		C64	GND		D64	PCIe01_TX-
A65	PCIe09_TX-		B65	PCIe09_RX+		C65	PCIe01_RX-		D65	PCIe01_TX+
A66	PCIe09_TX+		B66	GND		C66	PCIe01_RX+		D66	GND
A67	GND		B67	PCIe10_RX-		C67	GND		D67	PCIe02_TX-~~/SGMII1_TX-~~
A68	PCIe10_TX-		B68	PCIe10_RX+		C68	PCIe02_RX-~~/SGMII1_RX-~~		D68	PCIe02_TX+~~/SGMII1_TX+~~
A69	PCIe10_TX+		B69	GND		C69	PCIe02_RX+~~/SGMII1_RX+~~		D69	GND
A70	GND		B70	PCIe11_RX-		C70	GND		D70	PCIe03_TX-~~/SGMII0_TX-~~
A71	PCIe11_TX-		B71	PCIe11_RX+		C71	PCIe03_RX-~~/SGMII0_RX-~~		D71	PCIe03_TX+~~/SGMII0_TX+~~
A72	PCIe11_TX+		B72	GND		C72	PCIe03_RX+~~/SGMII0_RX+~~		D72	GND

Row A			Row B			Row C			Row D	
A73	GND		B73	PCIe12_RX-		C73	GND		D73	PCIe04_TX-
A74	PCIe12_TX-		B74	PCIe12_RX+		C74	PCIe04_RX-		D74	PCIe04_TX+
A75	PCIe12_TX+		B75	GND		C75	PCIe04_RX+		D75	GND
A76	GND		B76	PCIe13_RX-		C76	GND		D76	PCIe05_TX-
A77	PCIe13_TX-		B77	PCIe13_RX+		C77	PCIe05_RX-		D77	PCIe05_TX+
A78	PCIe13_TX+		B78	GND		C78	PCIe05_RX+		D78	GND
A79	GND		B79	PCIe14_RX-		C79	GND		D79	PCIe06_TX-/SATA1_TX-
A80	PCIe14_TX-		B80	PCIe14_RX+		C80	PCIe06_RX-/SATA1_RX-		D80	PCIe06_TX+/SATA1_TX+
A81	PCIe14_TX+		B81	GND		C81	PCIe06_RX+/SATA1_RX+		D81	GND
A82	GND		B82	PCIe15_RX-		C82	GND		D82	PCIe07_TX-/SATA0_TX-
A83	PCIe15_TX-		B83	PCIe15_RX+		C83	PCIe07_RX-/SATA0_RX-		D83	PCIe07_TX+/SATA0_TX+
A84	PCIe15_TX+		B84	GND		C84	PCIe07_RX+/SATA0_RX+		D84	GND
A85	GND		B85	~~TEST#~~		C85	GND		D85	NBASET0_MDI0-
A86	VCC_RTC		B86	RSMRST_OUT#		C86	SMB_CLK		D86	NBASET0_MDI0+
A87	SUS_CLK		B87	UART1_TX		C87	SMB_DAT		D87	GND
A88	GPIO_00		B88	UART1_RX		C88	SMB_ALERT#		D88	NBASET0_MDI1-
A89	GPIO_01		B89	UART1_RTS#		C89	UART0_TX		D89	NBASET0_MDI1+
A90	GPIO_02		B90	UART1_CTS#		C90	UART0_RX		D90	GND
A91	GPIO_03		B91	~~I2C2_CLK/ETH_MDIO_CLK~~		C91	UART0_RTS#		D91	NBASET0_MDI2-
A92	GPIO_04		B92	~~I2C2_DAT/ETH_MDIO_DAT~~		C92	UART0_CTS#		D92	NBASET0_MDI2+
A93	GPIO_05		B93	~~GP_SPI_MOSI~~		C93	I2C0_CLK		D93	GND
A94	GPIO_06		B94	~~GP_SPI_MISO~~		C94	I2C0_DAT		D94	NBASET0_MDI3-
A95	GPIO_07		B95	~~GP_SPI_CS0#~~		C95	I2C0_ALERT#		D95	NBASET0_MDI3+
A96	GPIO_08		B96	~~GP_SPI_CS1#~~		C96	I2C1_CLK		D96	GND
A97	GPIO_09		B97	~~GP_SPI_CS2#~~		C97	I2C1_DAT		D97	NBASET0_LINK_MAX#
A98	GPIO_10		B98	~~GP_SPI_CS3#~~		C98	NBASET0_SDP		D98	NBASET0_LINK_MID#
A99	GPIO_11		B99	~~GP_SPI_CLK~~		C99	NBASET0_CTREF		D99	NBASET0_LINK_ACT#
A100	PINOUT_TYPE0		B100	~~GP_SPI_ALERT#~~		C100	PINOUT_TYPE1		D100	PINOUT_TYPE2

Note: USB4/DDI/USB3.x are pin sharing. PCIe_6/SATA_1 are muxed. PCIe_7/SATA_0/NBASE-T_1 are muxed. Please check Chapter.2 for identifying default setting

Note: SS lane 5 pairs will be used if the USB4_1 enabled. SATA ports are build option by project basis

Note: GP_SPI by project basis discussion, also depends on device type

4.2 Signal Terminology Descriptions

Definition of terms used in signal description tables

Term	Description
I	Input to the module
O	Output from the module
I/O	Bi-directional Input / Output
OD	Open drain output from the module
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I/O $3.3V_{SB}$	Input or output 3.3V tolerant, active in standby state
DDC	Display Data Channel
PCIE	PCI Express compatible differential signal
PEG	PCI Express Graphics
SATA	Serial ATA specification Revision 2.6 and 3
LVDS	Low Voltage Differential Signal - 330 mV nominal; 450 mV maximum differential signal
P	Power Input / Output
REF	Reference voltage output, may be sourced from a Module power plane.
PDS	Pull-down strap. A Module output pin that is either tied to GND or is not connected. Used to signal Module capabilities to the Carrier Board.
PU	PU (pull-up) resistor on module
PD	PD (pull-down) resistor on module

Note: The I/O voltage for most I/O pins is 1.8V. Sidebands of PCIe, USB3.x, USB4, DDI, eDP and Asynch Serial at either 1.8V or 1.8VSB. In addition, I2C, GP_SPI, Thermal Protection, SMBUs, GPIOs, FuSa, Miscellaneous Signals, New Added Signals, Power and Sys Mgmt at either 1.8V or 1.8VSB.

Note: There is no VCC_5V_SBY input on the Mini –VCC pins are used for all power states.

Note: Certain interfaces on the COM-HPC Mini move AC coupling caps **off-module,** which differs from the other COM-HPC types. Off-module placement applies to PCIe lane 0-7 (both of TX and RX), PCIe lane 8-15 (only RX), SATA, DDI and USB4 AUX channels, as well as high-speed data signals for USB3.x and USB4.

Note: AC coupling caps for PCI Express TX lanes 8 through 15 are **on-Module** according to the COM-HPC Mini specification.

4.3 Signal Descriptions on J1 Connectors

4.3.1 NBASE-T Ethernet

2x NBASE-T Ethernet ports, designated NBASET0 and NBASET1, are defined for the Mini.

Magnetics are located on the carrier board.

NBASE-T_0

Name	Pin #	Description	I/O	PU / PD	Comment
NBASET0_MDI0- NBASET0_MDI0+ NBASET0_MDI1- NBASET0_MDI1+ NBASET0_MDI2- NBASET0_MDI2+ NBASET0_MDI3- NBASET0_MDI3+	D85 D86 D88 D89 D91 D92 D94 D95	Ethernet Controller : Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 10Gbps, 1Gbps, 100Mbps and 10 Mbps modes. Some pairs are unused in some modes, per the following: 10000BASE-T / 1000BASE-T: MDI[0]+/- B1_DA+/-; MDI[1]+/- B1_DB+/-; MDI[2]+/- B1_DC+/-; MDI[3]+/- B1_DD+/- 100BASE-TX: TX+/-; RX+/- 10BASE-T: TX+/-; RX+/-	I/O Analog		Twisted pair signals for external transformer.
NBASET0_LINK_ACT#	D99	NBASE-T Ethernet Controller activity indicator, active low. 20 mA or more current sink capability at VOL of 0.4V max. 20 mA or more current source capability at VOH of 2.4V min.	O 3.3VSB		
NBASET0_LINK_MAX#	D97	NBASE-T Ethernet Controller MAX Speed Link indicator, active low. If active, the link is at the maximum speed that the Ethernet controller is capable of (which may be 10G, 5G, 2.5G, etc). 20 mA or more current sink capability at VOL of 0.4V max. 20 mA or more current source capability at VOH of 2.4V min.	O 3.3VSB		
NBASET0_LINK_MID#	D98	NBASE-T Ethernet Controller MID Speed Link indicator, active low. If active, the link is established but at a speed lower than what the maximum speed that the Ethernet controller is capable of.	O 3.3VSB		

		20 mA or more current sink capability at VOL of 0.4V max. 20 mA or more current source capability at VOH of 2.4V min.			
NBASET0_CTREF	C99	Reference voltage for Carrier Board NBASET Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. If not needed, these pins may be left open on the Carrier. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.	REF GND min 3.3V max		
~~NBASET0_SDP~~	~~C98~~	~~NBASE-T Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal.~~	~~IO 3.3VSB~~		Not Supported

NBASE-T_1 (Optional)

Name	Pin #	Description	I/O	PU / PD	Comment
NBASET1_MDI0- NBASET1_MDI0+ NBASET1_MDI1- NBASET1_MDI1+ NBASET1_MDI2- NBASET1_MDI2+ NBASET1_MDI3- NBASET1_MDI3+	D49 D50 D52 D53 D55 D56 D58 D59	Ethernet Controller : Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 10Gbps, 1Gbps, 100Mbps and 10 Mbps modes. Some pairs are unused in some modes, per the following:	I/O Analog		Twisted pair signals for external transformer.
NBASET1_LINK_ACT#	B59	NBASE-T Ethernet Controller activity indicator, active low. 20 mA or more current sink capability at VOL of 0.4V max. 20 mA or more current source capability at VOH of 2.4V min.	O 3.3VSB		
NBASET1_LINK_MAX#	A59	NBASE-T Ethernet Controller MAX Speed Link indicator, active low. If active, the link is at the maximum speed that the Ethernet controller is capable of (which may be 10G, 5G, 2.5G, etc). 20 mA or more current sink capability at VOL of 0.4V max. 20 mA or more current source capability at VOH of 2.4V min.	O 3.3VSB		

	10000BASE-T 1000BASE-T	100BASE-TX	10BASE-T
MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-
MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-
MDI[2]+/-	B1_DC+/-		
MDI[3]+/-	B1_DD+/-		

NBASET1_LINK_MID#	B58	NBASE-T Ethernet Controller MID Speed Link indicator, active low. If active, the link is established but at a speed lower than what the maximum speed that the Ethernet controller is capable of. 20 mA or more current sink capability at VOL of 0.4V max. 20 mA or more current source capability at VOH of 2.4V min.	O 3.3VSB		
NBASET1_CTREF	A60	Reference voltage for Carrier Board NBASET Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. If not needed, these pins may be left open on the Carrier. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.	REF GND min 3.3V max		
~~NBASET1_SDP~~	~~D35~~	~~NBASE-T Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal.~~	~~IO 3.3VSB~~		Not Supported

Note: NBASE-T port 1 is a build option on a project basis.

4.3.2 Super Speed Lanes for DDI/USB4/USB3.x and Sidebands

COM-HPC mini form-factor only offers only one high-speed COM-HPC 400-pin connector. To utilize the pin effectively, some of the DDI/USB4/USB3.x signals share pins.

DDI/USB4/USB3.x all require differential data and high-speed pairs, such as TX+/TX- pair and RX+/RX- pair. These are called Super Speed Lane

One Super Speed Lane (SS) consists of TX+, TX-, and RX+, RX-

A maximum of **Eight** Super Speed lanes (SS) are definedin COM-HPC for that pin sharing usage, numbered from SS lane 0 to 7.

For example: SS lane 0 and SS lane 1 can be implemented either as DDI port 0 or USB4 port 2.

Please note that to get USB4, USB3.x work, USB2.0 signals are also required.

The table below indicates the usage between SS lanes and DDI/USB4/USB3.x for this product.

The default configuration (HW/BIOS) is Config 3. The other usage can be discussed by project basis.

SS Lanes	Config 1	Config 2	Config 3	Config 4	Config 5
SS Lane 0	DDI_0	DDI_0	**DDI_0**	USB4_2	USB4_2
SS Lane 1					
SS Lane 2	DDI_1	USB4_0	**USB4_0**	USB4_0	USB4_0
SS Lane 3					
SS Lane 4	USB3_3	USB3_3	**USB4_1**	USB4_1	USB4_1
SS Lane 5	-	-			
SS Lane 6	USB3_1	USB3_1	**USB3_1**	USB3_1	USB4_3 (TBC, project basis)
SS Lane 7	USB3_0	USB3_0	**USB3_0**	USB3_0	

DDI_0 indicates DDI port 0, USB4_2 indicates USB4 port 2. USB3_0 indicates USB3.x port 0.

For example, SS lane 4 and SS lane 5 can be used either as USB4 port 1 (based on SS lane 4 and lane 5) or as USB3.x port 3 (based on SS lane 4).

Super Speed [0-3] and its Sideband for DDI/USB4

Name	Pin #	Description	I/O	PU / PD	Comment
SS0_TX+ SS0_TX- SS1_TX+ SS1_TX-	D23 D22 D29 D28	Differential data pair			AC coupled off Module SS 0-1 lanes for **DDI_0** (default) or USB4_2
SS2_TX+ SS2_TX- SS3_TX+ SS3_TX-	A24 A23 A30 A29	Differential data pair			AC coupled off Module SS 2-3 lanes for DDI_1 or **USB4_0** (default)
SS0_RX+ SS0_RX- SS1_RX+ SS1_RX-	D26 D25 D32 D31	Differential data pair			AC coupled off Module SS 0-1 lanes for **DDI_0** (default) or USB4_2
SS2_RX+ SS2_RX- SS3_RX+ SS3_RX-	A27 A26 A33 A32	Differential data pair			AC coupled off Module SS 2-3 lanes for DDI_1 or **USB4_0** (default)
SS01_SCL_AUX+ SS23_SCL_AUX+	D20 A21	**As DDI** DP AUX+ function if DDI[0:1]_DDC_AUX_SEL is a no connect or driven to GND on the Carrier. HDMI/DVI I2C clock if DDI[0:1]_DDC_AUX_SEL is pulled or driven high on the Carrier. **As USB4** DisplayPort Aux channel for USB4_0, USB4_2 DP modes High speed differential pair. SS01_SCL_AUX+/- for USB4_2	1.8V	PD 100K	AC coupled off Module for DP SS01_SCL_AUX+/- for **DDI_0** (default) SS23_SCL_AUX+/- for **USB4_0** (default)
SS01_SDA_AUX- SS23_SDA_AUX-	C19 A20	**As DDI** DP AUX- function if DDI[0:1]_DDC_AUX_SEL is no connect HDMI/DVI I2C data if DDI[0:1]_DDC_AUX_SEL is pulled high **As USB4**	1.8V	PU 100K	AC coupled off Module for DP SS01_SCL_AUX+/- for **DDI_0** (default) SS23_SCL_AUX+/- for **USB4_0** (default)

		DisplayPort Aux channel for USB4_0, USB4_2 DP modes High speed differential pair. SS01_SCL_AUX+/- for USB4_2			
USB2_LSRX/DDI0_DDC_AUX_SEL USB0_LSRX/DDI1_DDC_AUX_SEL	B40 C26	**As DDI** Selects the function of DDI[0:1]_SCL_AUX+ and DDI[0:2]_SDA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is unconnected on the Carrier, the AUX pair is used for the DP AUX+/- signals. If pulled or driven high on the Carrier, the AUX pair contains the HDMI[0:2] I2C CRTL_CLK and CTRL_DAT signals. **As USB4** Sideband RX interface for USB4 Alternate modes "Low Speed" asynchronous serial RX line	I 1.8V	PD 100K	DDI0_DDC_AUX_SEL for **DDI_0** (default) USB0_LSRX for **USB4_0** (default)
USB2_LSTX/DDI0_HPD USB0_LSTX/DDI1_HPD	B41 C28	**As DDI** DDIP0:1] Hot-Plug Detect **As USB4** Sideband TX interface for USB4 Alternate modes "Low Speed" asynchronous serial TX line	O 1.8V	PD 100K	DDI0_HPD for **DDI_0** (default) USB0_LSTX for **USB4_0** (default)
SML0_DAT	B33	**Only for USB4** USB4 / TBT Re-timer Setup (from SOC). For all USB4	OD 1.8VSB	PU 2.2K 1.8VSB	
SML0_CLK	B32		OD 1.8VSB	PU 2.2K 1.8VSB	
USB_RT_ENA	B37		O 1.8V		
SML1_DAT	B30	**Only for USB4** USB-C PD Controller Setup (from SOC). For all USB4	OD 1.8VSB	PU 2.2K 1.8VSB	
SML1_CLK	B29		OD 1.8VSB	PU 2.2K 1.8VSB	
PMCALERT#	B31		I 1.8V	PU 10K 1.8V	
USB_PD_I2C_DAT	B36	**Only for USB4** Alternative USB-C PD Controller Setup (from EC).	OD 1.8VSB	PU 2.2K 1.8VSB	

USB_PD_I2C_CLK	B35	For all USB4	OD 1.8VSB	PU 2.2K 1.8VSB	
USB_PD_ALERT#	B34		I 1.8VSB	PU 10K 1.8VSB	

Note: The COM-HPC module should support exporting Port 80 information over the USB_PD_I2C bus (signals USB_PD_I2C_DAT and USB_PD_I2C_CLK) to the carrier hardware that implements a pair of 7-segment displays to show the codes.

DDI / USB4 Signal Mapping

Name	DDI Use	USB4 Use	Note
SS0_TX-	DDI0_PAIR0-	USB4_2_SSTX0-	**DDI_0** (default) or USB4_2
SS0_TX+	DDI0_PAIR0+	USB4_2_SSTX0+	
SS0_RX-	DDI0_PAIR1-	USB4_2_SSRX0-	
SS0_RX+	DDI0_PAIR1+	USB4_2_SSRX0+	
SS1_TX-	DDI0_PAIR2-	USB4_2_SSTX1-	
SS1_TX+	DDI0_PAIR2+	USB4_2_SSTX1+	
SS1_RX-	DDI0_PAIR3-	USB4_2_SSRX1-	
SS1_RX+	DDI0_PAIR3+	USB4_2_SSRX1+	
SS01_SDA_AUX-	DDI0_SDA_AUX-	USB2_AUX-	
SS01_SCL_AUX+	DDI0_SCL_AUX+	USB2_AUX+	
USB2_LSRX/DDI0_DDC_AUX_SEL	DDI0_DDC_AUX_SEL	USB2_LSRX	
USB2_LSTX/DDI0_HPD	DDI0_HPD	USB2_LSTX	
SS2_TX-	DDI1_PAIR0-	USB4_0_SSTX0-	DDI_1 or **USB4_0** (default)
SS2_TX+	DDI1_PAIR0+	USB4_0_SSTX0+	
SS2_RX-	DDI1_PAIR1-	USB4_0_SSRX0-	
SS2_RX+	DDI1_PAIR1+	USB4_0_SSRX0+	
SS3_TX-	DDI1_PAIR2-	USB4_0_SSTX1-	
SS3_TX+	DDI1_PAIR2+	USB4_0_SSTX1+	
SS3_RX-	DDI1_PAIR3-	USB4_0_SSRX1-	
SS3_RX+	DDI1_PAIR3+	USB4_0_SSRX1+	
SS23_SDA_AUX-	DDI1_SDA_AUX-	USB0_AUX-	
SS23_SCL_AUX+	DDI1_SCL_AUX+	USB0_AUX+	
USB0_LSRX/DDI1_DDC_AUX_SEL	DDI1_DDC_AUX_SEL	USB0_LSRX	

USB0_LSTX/DDI1_HPD	DDI1_HPD	USB0_LSTX	

Super Speed [4-7] and its Sideband for USB4/USB3.x

Name	Pin #	Description	I/O	PU / PD	Comment
SS4_TX+ SS4_TX- SS5_TX+ SS5_TX-	D44 D43 D47 D46	Differential data pair			AC coupled off Module SS 4-5 lanes for **USB4_1** (default) or SS 4 lanes for USB3_3 (port 3)
SS6_TX+ SS6_TX- SS7_TX+ SS7_TX-	D38 D37 D41 D40	Differential data pair			AC coupled off Module SS 6 lanes for USB3_1 (port 1) SS 7 lanes for USB3_0 (port 0)
SS4_RX+ SS4_RX- SS5_RX+ SS5_RX-	C45 C44 C48 C47				AC coupled off Module SS 4-5 lanes for **USB4_1** (default) or SS 4 lanes for USB3_3 (port 3)
SS6_RX+ SS6_RX- SS7_RX+ SS7_RX-	C39 C38 C42 C41				AC coupled off Module SS 6 lanes for USB3_1 (port 1) SS 7 lanes for USB3_0 (port 0)
USB1_AUX+ ~~USB3_AUX+~~	B44 ~~C36~~	**As USB4** DisplayPort Aux channel for USB4_1, USB4_3 DP modes High speed differential pair. USB1_AUX+/- for USB4_1 (port 1)		PD 100K	AC coupled off Module for DP USB3_AUX+/- : not supported
USB1_AUX- ~~USB3_AUX-~~	B43 ~~C35~~	**As USB4** DisplayPort Aux channel for USB4_1, USB4_3 DP modes High speed differential pair. USB1_AUX+/- for USB4_1 (port 1)		PU 100K	AC coupled off Module for DP USB3_AUX+/- : not supported
USB1_LSRX ~~USB3_LSRX~~	C27 ~~B38~~	**As USB4** Sideband RX interface for USB4 Alternate modes "Low Speed" asynchronous serial RX line	I 1.8V	PD 100K	USB3_LSRX/LSTX : not supported
USB1_LSTX ~~USB3_LSTX~~	C29 ~~B39~~	**As USB4** Sideband TX interface for USB4 Alternate modes "Low Speed" asynchronous serial TX line	O 1.8V	PD 100K	USB3_LSRX/LSTX : not supported

Note: SML0, SML1, USB_PD_I2C, USB_RT_ENA, PMCALERT#, USB_PD_ALERT# shared with the signals for USB4_0, USB4_2. Shownin table above.

Signal Mapping

Name	USB4 Use	Note
SS4_TX-	USB4_1_SSTX0-	**USB4_1** (port 1) (default)
SS4_TX+	USB4_1_SSTX0+	
SS4_RX-	USB4_1_SSRX0-	
SS4_RX+	USB4_1_SSRX0+	
SS5_TX-	USB4_1_SSTX1-	
SS5_TX+	USB4_1_SSTX1+	
SS5_RX-	USB4_1_SSRX1-	
SS5_RX+	USB4_1_SSRX1+	
USB1_AUX-	USB1_AUX-	
USB1_AUX+	USB1_AUX+	
USB1_LSRX	USB1_LSRX	
USB1_LSTX	USB1_LSTX	
SS6_TX-	USB4_3_SSTX0-	USB4_3 (port 3), if it supported Note: USB4_3 by project basis discussion
SS6_TX+	USB4_3_SSTX0+	
SS6_RX-	USB4_3_SSRX0-	
SS6_RX+	USB4_3_SSRX0+	
SS7_TX-	USB4_3_SSTX1-	
SS7_TX+	USB4_3_SSTX1+	
SS7_RX-	USB4_3_SSRX1-	
SS7_RX+	USB4_3_SSRX1+	
USB3_AUX-	USB3_AUX-	
USB3_AUX+	USB3_AUX+	
USB3_LSRX	USB3_LSRX	
USB3_LSTX	USB3_LSTX	

4.3.3 USB2.0 and Sidebands

Each COM-HPC Mini USB4 or USB 3.2 port implementation needs a USB 2.0 pair for support functions.

Name	Pin #	Description	I/O	PU / PD	Comment
USB0+ USB0- USB1+ USB1- USB2+ USB2- USB3+ USB3-	D17 D16 D14 D13 C18 C17 C15 C14	USB 2.0 differential pairs, channels 0 through 7. USB0 may be configured as a USB client or as a host, or both at the Module designer's discretion. All other USB ports, if implemented, shall be host ports. If any SuperSpeed or USB4 ports are implemented, then they shall be supported by a specific USB 2.0 port			USB 1.1/2.0 compliant USB Client mode – Not supported
USB4+ USB4- USB5+ USB5- USB6+ USB6- USB7+ USB7-	B17 B16 B14 B13 A18 A17 A15 A14	USB 2.0 differential pairs, channels 0 through 7. USB0 may be configured as a USB client or as a host, or both at the Module designer's discretion. All other USB ports, if implemented, shall be host ports. If any SuperSpeed or USB4 ports are implemented, then they shall be supported by a specific USB 2.0 port			USB 1.1/2.0 compliant USB Client mode – Not supported
USB01_OC# USB23_OC# USB45_OC# USB67_OC#	B28 B27 B26 B25	USB over-current sense, USB 2.0 channels 0,1; channels 2,3; channels 4,5 and channels 6,7 respectively. A pull-up for each of these lines to the 1.8V Suspend rail shall be present on the Mini Module. The pull-up should be 10K. An open drain driver from USB current monitors on the Carrier Board may drive this line low. The Carrier Board shall not pull these lines up. Note that the over-current limits for USB 2.0 and USB 3.0 are different; this is a Carrier board implementation item.	I 1.8VSB	PU 10K 1.8VSB	Do not pull high on carrier **Assignment of USB_OC defined by specification** USB01_OC# for USB4 port 0 and 1 and USB3.x port 3 USB23_OC# for USB4 port 2 and 3 and USB3.x port 1 USB45_OC# for USB3.x port 0 and 2 USB67_OC# for USB2.0 port 6 and 7
RSMRST_OUT#	B86	USB devices that are to be powered in the S5 / S4 / S3 Suspend states should not have their 5V VBUS power enabled before RSMRST_OUT# transitions to the hi state. RSMRST_OUT# is also described in Power and System Management section	O 1.8VSB	PD 100K	

Preferred USB2 and USB3.x/USB4 Signals Assignment

The usage in **bold front** is based on the combination of the COM-HPC-mMTL module and ADLINK's COM-HPC mini base.

SS Lanes	Config 1	Config 2	Config 3	Config 4	Config 5	USB2.0 Support for USB4	USB2.0 Support for USB3.x
SS Lane 0	DDI_0	DDI_0	**DDI_0**	USB4_2	USB4_2	**USB2**	-
SS Lane 1							
SS Lane 2	DDI_1	USB4_0	**USB4_0**	USB4_0	USB4_0	**USB0**	-
SS Lane 3							
SS Lane 4	USB3_3	USB3_3	**USB4_1**	USB4_1	USB4_1	**USB1**	USB1
SS Lane 5	~~USB3_2~~	~~USB3_2~~					-
SS Lane 6	USB3_1	USB3_1	**USB3_1**	USB3_1	~~USB4_3~~ (TBC, project basis)	~~USB3~~	**USB3**
SS Lane 7	USB3_0	USB3_0	**USB3_0**	USB3_0			**USB5**

USB2 indicates USB 2.0 signalport 2, USB4_2 indicates USB4 SS signals port 2, USB3_1 indicates USB3.x SS signals port 1

For example, the USB4_2 pair with USB2 and other sidebands is recommended for USB4 port 2 at Type C connector implementation.

Similarly, the USB3_0 pair with USB5 is recommended for USB3.x port 0 at a Type-A connector implementation.

Note: USB2.0 ports 6 and 7 (pin names USB6 and USB7) may be used as general purpose ports, they are not needed for USB4 or USB3.2 support.

Note: If a USB 2.0 resource is not needed for USB4 or USB 3.2 support, that USB 2.0 may be used elsewhere by the carrier designer – for example, in Config 1 in the Table above, USB2 and USB0 are not needed and may be used elsewhere (as the DDI interfaces do not need a USB support).

4.3.4 Embedded Display Port (eDP)

Embedded DisplayPort or eDP is derived from DisplayPort, but is intended to support internal flat panel eDP screens.

Name	Pin #	Description	I/O	PU / PD	Comment
eDP_TX0+ eDP_TX0-	A39 A38	eDP / DSI differential data pairs	O PCIE		AC coupled off Module (eDP only)
eDP_TX1+ eDP_TX1-	A42 A41	eDP / DSI differential data pairs	O PCIE		
eDP_TX2+ eDP_TX2-	A45 A44	eDP differential data pairs or DSI differential clock pairs	O PCIE		
eDP_TX3+ eDP_TX3-	A47 A48	eDP / DSI differential data pairs	O PCIE		
eDP_AUX+ eDP_AUX-	A36 A35	eDP AUX channel differential pair or DSI differential data pair	I/O PCIE		
eDP_VDD_EN	C31	eDP / DSI power enable	O 1.8V	PD 100K	Follow silicon platform design guide
eDP_BKLT_EN	C32	eDP / DSI backlight enable	O 1.8V	PD 100K	
eDP_BKLTCTL	C33	EDP / DSI backlight brightness control	O 1.8V		
eDP_HPD	C30	eDP: Detection of Hot Plug / Unplug and notification of the link layer DSI: Tearing Effect Input: this is an optional signal from the DSI display (that has it's own display controller and frame buffer) coordinating with the host display controller	I 1.8V	PD 100K	

Note: This platform does not support MIPI-DSI interface, thus the mapping table between eDP and DSI is not mentioned here.

4.3.5 Serial Audio Interface

HD Audio / I2S / Soundwire

Name	Pin #	Description	I/O	PU / PD	Comment
~~I2S_CLK/SNDW_CLK2/~~HDA_BCLK	B23	I2S Clock Alternative use as Soundwire 2 clock or HDA serial data clock	O 1.8VSB		**HDA** is default support I2S/Soundwire : Not supported. The driver readiness limitation
~~I2S_DIN/SNDW_DAT2/~~HDA_SDI	B22	I2S Data In This pin is an input in I2S mode Alternative use as bi-directional Soundwire 2 data lane or HDA serial TDM data input	I/O 1.8VSB		
~~I2S_DOUT/SNDW_DAT3/~~HDA_SDO	B20	I2S Data Out This pin is an output in I2S mode Alternative use as bi-directional Soundwire 3 data lane or HDA serial TDM data output	I/O 1.8VSB		
~~I2S_LRCLK/SNDW_CLK3/~~HDA_SYNC	B19	I2S L/R Clock Alternative use as Soundwire 3 clock or HDA sample synchronization signal	O 1.8VSB		
~~I2S_MCLK/~~HDA_RST#	B21	I2S Master Clock Alternative use as HDA reset output	O 1.8VSB	PD 100K	

Soundwrie / DMIC Audio

Not supported

Name	Pin #	Description	I/O	PU / PD	Comment
~~SNDW_DMIC_DAT0~~ ~~SNDW_DMIC_DAT1~~	~~C24~~ ~~C21~~	~~Bi-directional PCM audio data~~	~~I/O 1.8VSB~~	~~PU 10K~~	
~~SNDW_DMIC_CLK0~~ ~~SNDW_DMIC_CLK1~~	~~C23~~ ~~C20~~	~~Clock for Soundwire transactions~~	~~O 1.8VSB~~	~~PU 10K~~	

4.3.6 PCI Express

Name	Pin #	Description	I/O	PU / PD	Comment
PCIe00_TX+	D62	PCI Express Differential Transmit Pairs 0-7	O PCIe		AC coupled off Module
PCIe00_TX-	D61	PCIe Group 0 Low			
PCIe01_TX+	D65				
PCIe01_TX-	D64				
PCIe02_TX+/SGMII1_TX+	D68				SGMII not supported
PCIe02_TX-/SGMII1_TX-	D67				
PCIe03_TX+/SGMII0_TX+	D71				
PCIe03_TX-/SGMII0_TX-	D70				
PCIe04_TX+	D74				
PCIe04_TX-	D73				
PCIe05_TX+	D77				
PCIe05_TX-	D76				
PCIe06_TX+/SATA1_TX+	D80				PCIe06 is default feature
PCIe06_TX-/SATA1_TX-	D79				
PCIe07_TX+/SATA0_TX+	D83				PCIe07/SATA0 are muxed with NBASE-T_1 at module
PCIe07_TX-/SATA0_TX-	D82				design, NBAE-T_1 is default feature. Check function diagram
PCIe00_RX+	C63	PCI Express Differential Receive Pairs 0-7	I PCIe		AC coupled off Module
PCIe00_RX-	C62	PCIe Group 0 Low			
PCIe01_RX+	C66				
PCIe01_RX-	C65				
PCIe02_RX+/SGMII1_RX+	C69				SGMII not supported
PCIe02_RX-/SGMII1_RX-	C68				
PCIe03_RX+/SGMII0_RX+	C72				
PCIe03_RX-/SGMII0_RX-	C71				
PCIe04_RX+	C75				
PCIe04_RX-	C74				
PCIe05_RX+	C78				
PCIe05_RX-	C77				
PCIe06_RX+/SATA1_RX+	C81				PCIe06 is default feature
PCIe06_RX-/SATA1_RX-	C80				
PCIe07_RX+/SATA0_RX+	C84				PCIe07/SATA0 are muxed with NBASE-T_1 at module
PCIe07_RX-/SATA0_RX-	C83				design, NBAE-T_1 is default feature. Check function diagram
PCIe08_TX+	A63	PCI Express Differential Transmit Pairs 8-15	O PCIe		AC coupled on Module
PCIe08_TX-	A62	PCIe Group 0 High			
PCIe09_TX+	A66				
PCIe09_TX-	A65				

PCIe10_TX+ PCIe10_TX- PCIe11_TX+ PCIe11_TX- PCIe12_TX+ PCIe12_TX- PCIe13_TX+ PCIe13_TX- PCIe14_TX+ PCIe14_TX- PCIe15_TX+ PCIe15_TX-	A69 A68 A72 A71 A75 A74 A78 A77 A81 A80 A84 A83				
PCIe08_RX+ PCIe08_RX- PCIe09_RX+ PCIe09_RX- PCIe10_RX+ PCIe10_RX- PCIe11_RX+ PCIe11_RX- PCIe12_RX+ PCIe12_RX- PCIe13_RX+ PCIe13_RX- PCIe14_RX+ PCIe14_RX- PCIe15_RX+ PCIe15_RX-	B62 B61 B65 B64 B68 B67 B71 B70 B74 B73 B77 B76 B80 B79 B83 B82	PCI Express Differential Receive Pairs 8-15 PCIe Group 0 High	I PCIe		AC coupled off Module
PCIe_REFCLK0_LO- PCIe_REFCLK0_LO+	C59 C60	Reference clock pair for PCIe lanes [0:7], also referred to PCIe Group 0 Low	O PCIe		
PCIe_REFCLK0_HI- PCIe_REFCLK0_HI+	C56 C57	Reference clock pair for PCIe lanes [8:15], also referred to PCIe Group 0 High	O PCIe		
PCIe_CLKREQ0_LO#	A56	PCIe reference clock request signal from Carrier target devices for PCIe_REFCLK0_LO clock pair	I/O OD 1.8V	PU 10K 1.8V	
PCIe_CLKREQ0_HI#	A57	PCIe reference clock request signal from Carrier target devices for PCIe_REFCLK0_HI clock pair	I/O OD 1.8V	PU 10K 1.8V	

Note: Some pins are defined to allow a COM-HPC Module to host PCIe Target devices, such as an FPGA, GPU, or PCIe bridge. However, this product doesn't offer this kind of usage; therefore, the related pins are not shown here.

4.3.6.1 HSIO Lane Assignments

Name	HSIO name on PCH	Comment
PCIE 0-3	HSIO 6-9	
PCIE 4-5	HSIO 2-5	SATA 0/1 and NBASE-T_1 (port 1) are muxed with PCIE lane 6/7
PCIE 8-11	HSIO 14-17	
PCIE 12-15	HSIO 18-21	
NVMe SSD	HSIO 22-25	Optional on-board NVMe SSD utilize the HSIO 22-25.
NBASE-T_0	HSIO 10	NBASE-T port 0 is implemented by Intel LAN controller and utilize HSIO lane 10

4.3.7 SATA

SATA 0 and PCIe lane 7 share pins. SATA 1 and PCIe lane 6 also share pins. The mapping and the default setting are described in Section 4.3.6.

SATA 0/1 are optional feature and will be supported on a project basis

4.3.8 Asynchronous Serial Port

Name	Pin #	Description	I/O	PU / PD	Comment
UART0_TX UART1_TX	C89 B87	Logic level asynchronous serial port transmit signal	O 1.8V	PU 10K 1.8V	
UART0_RX UART1_RX	C90 B88	Logic level asynchronous serial port receive signal	I 1.8V	PU 470ohm 1.8V	
UART0_RTS# UART1_RTS#	C91 B89	Logic level asynchronous serial port Request to Send signal, active low	O 1.8V		UART 0, 1_CTS#, RTS# only available if routed from PCH and by project basis
UART0_CTS# UART1_CTS#	C92 B90	Logic level asynchronous serial port Clear to Send input, active low	I 1.8V		

UART default come from EC (embedded controller). UART from SoC will be supported by project basis

4.3.9 I2C

2x general-purpose I2C ports are defined for COM-HPC. The first of the two supports an ALERT# input. I2C0, I2C1 are defined to operate from a 1.8V rail.

Name	Pin #	Description	I/O	PU / PD	Comment
I2C0_CLK	C93	Clock I/O line for the general purpose I2C0 port	I/O OD 1.8VSB	PU 2.2K 1.8VSB	
I2C0_DAT	C94	Data I/O line for the general purpose I2C0 port	I/O OD 1.8VSB	PU 2.2K 1.8VSB	
I2C0_ALERT#	C95	Alert input / interrupt for I2C0	I 1.8VSB	PU 10K 1.8VSB	

I2C1_CLK	C96	Clock I/O line for the general purpose I2C1 port	I/O OD 1.8VSB	PU 2.2K 1.8VSB	
I2C1_DAT	C97	Data I/O line for the general purpose I2C1 port	I/O OD 1.8VSB	PU 2.2K 1.8VSB	

I2C default come from EC (embedded controller). I2C from SoC will be supported by project basis

4.3.10 General Purpose SPI (GP_SPI)

No supported by default. Available through project-based discussion and dependent on device type.

Name	Pin #	Description	I/O	PU / PD	Comment
GP_SPI_MISO	B94	Serial data into the COM-HPC Module from the Carrier GP_SPI device ("Master In Slave Out")	I 1.8V		
GP_SPI_MOSI	B93	Serial data from the COM-HPC Module to the Carrier GP_SPI device ("Master Out Slave In")	O 1.8V		
GP_SPI_CLK	B99	Clock from the Module to Carrier GP_SPI device	O 1.8V		
GP_SPI_CS0# GP_SPI_CS1# GP_SPI_CS2# GP_SPI_CS3#	B95 B96 B97 B98	GP_SPI chip selects, active low	O 1.8V		
GP_SPI_ALERT#	B100	Alert (interrupt) from a Carrier GP_SPI device to the Module	I V	PU 10K	

4.3.11 SMBus

Name	Pin #	Description	I/O	PU / PD	Comment
SMB_CLK	C86	System Management Bus bidirectional clock line.	I/O OD 1.8VSB	PU 2.2K 1.8VSB	The maximum capacitance on the Carrier Board shall not exceed 100pF
SMB_DAT	C87	System Management Bus bidirectional data line.	I/O OD 1.8VSB	PU 2.2K 1.8VSB	The maximum capacitance on the Carrier Board shall not exceed 100Pf
SMB_ALERT#	C88	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 1.8VSB	PU 10K 1.8VSB	The maximum capacitance on the Carrier Board shall not exceed 100pF

The SMB default comes from the SoC. SMB from EC (embedded controller) is supported on a project basis.

4.3.12 General Purpose Input Outputs

Name	Pin #	Description	I/O	PU / PD	Comment
GPIO_00 GPIO_01 GPIO_02 GPIO_03 GPIO_04 GPIO_05 GPIO_06 GPIO_07 GPIO_08 GPIO_09 GPIO_10 GPIO_11	A88 A89 A90 A91 A92 A93 A94 A95 A96 A97 A98 A99	General-purpose input / output pins. Upon a hardware reset, these pins should be configured as inputs. As inputs, these pins should be able to generate an interrupt to the Module host.	I/O 1.8V	PU 100K 1.8V	

GPIO default come from EC (embedded controller). GPIO from SoC will be supported by project basis

4.3.13 Thermal Protection & Thermal Management

Name	Pin #	Description	I/O	PU / PD	Comment
CARRIER_HOT#	C04	Input from off-Module temp sensor indicating an over-temp situation.	I 1.8V	PU 10K 1.8V	
THERMTRIP#	B04	Active low output indicating that the CPU has entered thermal shutdown.	O 1.8V	PU 10K 1.8V	
FAN_PWMOUT	C11	Fan controllers use the Pulse Width Modulation (PWM) technique to control the fan speed, via the FAN_PWMOUT signal. Carrier designers should buffer this signal with an open drain FET and pullup or other robust Carrier device(s).	O 1.8V		
FAN_TACHIN	C12	Fan tachometer input for a fan with a two pulse per revolution output	I 1.8V		

4.3.14 eSPI

Name	Pin #	Description	I/O	PU / PD	Comment
eSPI_IO0 eSPI_IO1 eSPI_IO2 eSPI_IO3	A50 A51 A52 A53	eSPI Master Data Input / Outputs. These are bi directional input/output pins used to transfer data between master and slaves.	I/O CMOS 1.8VSB		
eSPI_CS0# eSPI_CS1#	B54 B55	eSPI Master Chip Select Outputs. A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Select pin. If an eSPI_CSx# pins is not in use, it shall be either pulled high or actively driven high.	O COMS 1.8VSB	PU 20K 1.8VSB	PU 20K based on the SOC's internal PU value
eSPI_CLK	A54	eSPI Master Clock Output. This pin provides the reference timing for all the serial input and output operations.	O CMOS 1.8VSB		
eSPI_ALERT0# eSPI_ALERT1#	B52 B53	eSPI pins used by eSPI slave to request service from the eSPI master.	I COMS 1.8VSB	TBC	
eSPI_RST#	B56	eSPI Reset - resets the eSPI interface for both master and slaves. eSPI_RST# is typically driven from the eSPI master to eSPI slaves.	O CMOS 1.8VSB	PD 75K	Refer to Intel platform design guidance

Note: eSPI_CS1 is disabled by default. eSPI_CS1 should be enabled if there's an eSPI based chip on the carrier board, such as a Super I/O chip. eSPI_CS1 can be enabled in the BIOS menu.

4.3.15 Boot SPI (BIOS ONLY) and Boot Select

Name	Pin #	Description	I/O	PU / PD	Comment
BOOT_SPI_CS#	B48	Chip select for Carrier Board SPI. See Table 20 "BIOS Select Options: Module eSPI and SPI Chip Select Routing" for implementation details. If the BOOT_SPI_CS# pin is not in use, it shall be either pulled high or actively driven high.	O VCC_BOOT_SPI	PU 10K	
BOOT_SPI_IO0 BOOT_SPI_IO1 BOOT_SPI_IO2 BOOT_SPI_IO3	C50 C51 C52 C53	Bidirectional 4 bit data path out of and into a Carrier SPI flash operating in Serial Quad Interface (SQI) mode. If the flash memory device is operating in traditional Serial Peripheral Interface (SPI) mode, then signal BOOT_SPI_IO0 is used for getting serial data into the flash device (referred to as SI or MOSI in SPI Flash data sheets) and signal BOOT_SPI_IO1 is used to get serial data from the flash device (referred to as SO or MISO in flash data sheets)	I/O CMOS VCC_BOOT_SPI		
BOOT_SPI_CLK	C54	Clock from Module chipset to Carrier SPI	O VCC_BOOT_SPI		Clock support is 50MHz, can be adjusted by project basis
VCC_BOOT_SPI	B47	Power supply for Carrier Board SPI – sourced from Module – nominally either 1.8V or 3.3V. The Module shall provide a minimum of 100mA on VCC_BOOT_SPI. Carriers shall use less than 100mA from this power source. VCC_BOOT_SPI shall only be used to power SPI devices on the Carrier Board. The Module vendor may choose what power domains the BOOT_SPI is active in.	O 1.8VSB		
BSEL2 BSEL1 BSEL0	B51 B50 B49	Boot Select pins. These pins distinguish between a SPI or eSPI BIOS boot and between an on—Module or off-Module BIOS. Details are in Table 20: BIOS Select Options: Module eSPI and SPI Chip Select Routing. Pulled up on Module to vendor specific power rail	I VCC_BOOT_SPI	PU 10K	

4.3.16 Power & System Management

Name	Pin #	Description	I/O	PU / PD	Comment
PWRBTN#	B02	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down.	I 1,8VSB	PU 10K 1.8VSB	
RSTBTN#	C02	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when RSTBTN# is not able to reestablish control of the system, VIN_PWR_OK or a power cycle *may* be used.	I 1.8VSB	PU 10K 1.8VSB	
PLTRST#	D05	Platform Reset: output from Module to Carrier Board. Active low. Issued by Module chipset and *may* result from a low RSTBTN# input, a low VIN_PWR_OK input, a VCC power input that falls below the minimum specification, a watchdog timeout, or *may* be initiated by the Module software.	O 1.8VSB		
VIN_PWR_OK	C06	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed.	I 1.8V	PU 10K 1.8VSB	
SUS_S3#	B08	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board *should* be used to enable the non-standby power on a typical ATX supply. Even in single input supply system implementations (AT mode, no standby input), the SUS_S3# Module output should be used disable any Carrier voltage regulators when SUS_S3# is low, to prevent bleed leakage from Carrier circuits into the Module.	O 1.8VSB		
SUS_S4_S5#	C08	Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.	O 1.8VSB		
SUS_CLK	A87	32.768 kHz +/- 100 ppm clock used by Carrier peripherals such as M.2 cards in their low power modes.	O 1.8VSB		
WAKE0#	D10	PCI Express wake up signal.	I/O 1.8VSB	PU 1K 1.8VSB	
WAKE1#	D11	General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.	I 1.8VSB	PU 1K 1.8VSB	
BATLOW#	C10	Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly	I 1.8VSB	PU 10K 1.8VSB	

		transitioning to power saving or power cut-off ACPI modes.			
LID#	B45	LID switch. Low active signal used by the ACPI operating system for a LID switch.	I 1.8VSB	PU 47K 1.8VSB	
SLEEP#	B46	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I 1.8VSB	PU 47K 1.8VSB	
TAMPER#	B06	Tamper or Intrusion detection line on VCC_RTC power well. Carrier hardware pulls this low on a Tamper event.	VCC_RTC	PU 1M RTC	
ACPRESENT	D34	Driven hard low on Carrier if system AC power is not present	I 1.8VSB	PU 100K 1.8VSB	
RSMRST_OUT#	B86	This is a buffered copy of the internal Module RSMRST# (Resume Reset, active low) signal. The internal Module RSMRST# signal is an input to the chipset or SOC and when it transitions from low to high it indicates that the suspend well power rails are stable. USB devices on the Carrier that are to be active in S5 / S3 / S0 should not have their 5V supply applied before RSMRST_OUT# goes high. RSMRST_OUT# shall be a 3.3V CMOS Module output, active in all power states.	O 1.8VSB	PD 100K	

4.3.17 Rapid Shutdown

Not supported

Name	Pin #	Description	I/O	PU / PD	Comment
~~RAPID_SHUTDOWN~~	~~A05~~	~~Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 µs. Pull-down / disable on Module if RAPID_SHUTDOWN pin is not asserted.~~	~~I 5VSB~~		

4.3.18 FuSa – Functional Safety

Not supported. So, the related pins are not shown here

4.3.19 CAN Bus

Not supported, therefore, the related pins are not shown here

4.3.20 Module Type Definition

<table>
<tr><th>Name</th><th>Pin #</th><th>Description</th><th>I/O</th><th>Comment</th></tr>
<tr><td>PINOUT_TYPE0
PINOUT_TYPE1
PINOUT_TYPE2</td><td>A100
C100
D100</td><td>The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). These pins shall be pulled up on the Carrier, to Carrier standby voltage rail of 5V or less. Carrier hardware reads the level on these straps.

<table>
<tr><th></th><th colspan="3">Module Connections</th><th>Meaning</th></tr>
<tr><th>Ref</th><th>TYPE2</th><th>TYPE1</th><th>TYPE0</th><th></th></tr>
<tr><td>7</td><td>NC</td><td>NC</td><td>NC</td><td>Mini Module – Wide Range 8V to 20V input</td></tr>
<tr><td>6</td><td>NC</td><td>NC</td><td>GND</td><td>Reserved</td></tr>
<tr><td>5</td><td>NC</td><td>GND</td><td>NC</td><td>Reserved</td></tr>
<tr><td>4</td><td>NC</td><td>GND</td><td>GND</td><td>Server Module – Fixed 12V input</td></tr>
<tr><td>3</td><td>GND</td><td>NC</td><td>NC</td><td>Reserved</td></tr>
<tr><td>2</td><td>GND</td><td>NC</td><td>GND</td><td>Reserved</td></tr>
<tr><td>1</td><td>GND</td><td>GND</td><td>NC</td><td>Client Module - Wide Range 8V to 20V input</td></tr>
<tr><td>0</td><td>GND</td><td>GND</td><td>GND</td><td>Client Module – Fixed 12V input</td></tr>
</table>

The Module shall implement all three TYPE[x] pins per the table above.

The Carrier Board should implement combinatorial logic that monitors the Module TYPE pins and keeps power off (e.g deactivates the ATX PS_ON# signal to an ATX power supply or otherwise deactivates VCC to the COM-HPC Module) if an incompatible Module pin-out type is detected. All three TYPE[x] pins should be monitored by the Carrier. The Carrier Board logic may also implement a fault indicator such as an LED.</td><td></td><td>Mini Module – Wide Range 8V to 20V input</td></tr>
</table>

4.3.21 Miscellaneous Signals

Name	Pin #	Description	I/O	PU / PD	Comment
WD_OUT	B11	Output indicating that a watchdog time-out event has occurred. Refer to Section 5.3 for details.	O 1.8V	PU 10K 1.8V	
WD_STROBE#	B10	Strobe input to watchdog timer. Periodic strobing prevents the watchdog, if enabled, from timing out.	I 1.8V	PU 100K 1.8V	
~~TEST#~~	~~B85~~	~~Module input to allow vendor specific Module test mode(s). Carrier designers should leave this pin open on the Carrier. Designers involved in the design of specialty Carriers for Module test may pull this line to GND or possibly to a Module specific analog voltage between GND and 3.3V to select a test mode.~~			Not Supported
RSVD		Reserved pins. These may be assigned functions in future versions of this specification. Reserved pins shall not be connected to anything, and shall not be connected to each other.			

4.3.22 Power and Ground

Name	Pin #	Description	I/O	PU / PD	Comment
VCC	A01-A04 B01 B03 C01 C03 D01-D04	Primary power input: fixed +12V on the Client Type 0; wide range +8V to +20V on the Client Type 1; fixed +12V on the Server. All available VCC pins on the connector shall be used.	P		8-20V
VCC_RTC	A86	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND		Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane(s).	P		

Note: There is no VCC_5V_SBY input on the Mini – the VCC pins are used for all power states, as defined by the PICMG specification.

5. Additional Features

This chapter describes the connectors, LEDs, and switches located on the module, which are not necessarily included in the PICMG standard specification. The locations of these parts are shown below:

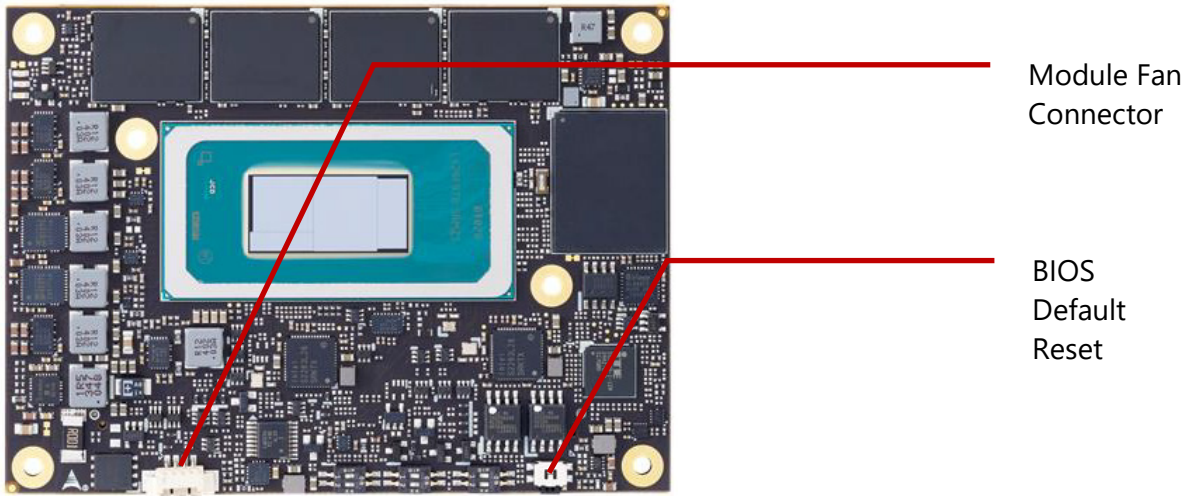


Figure 3 – Module feature locations (front)

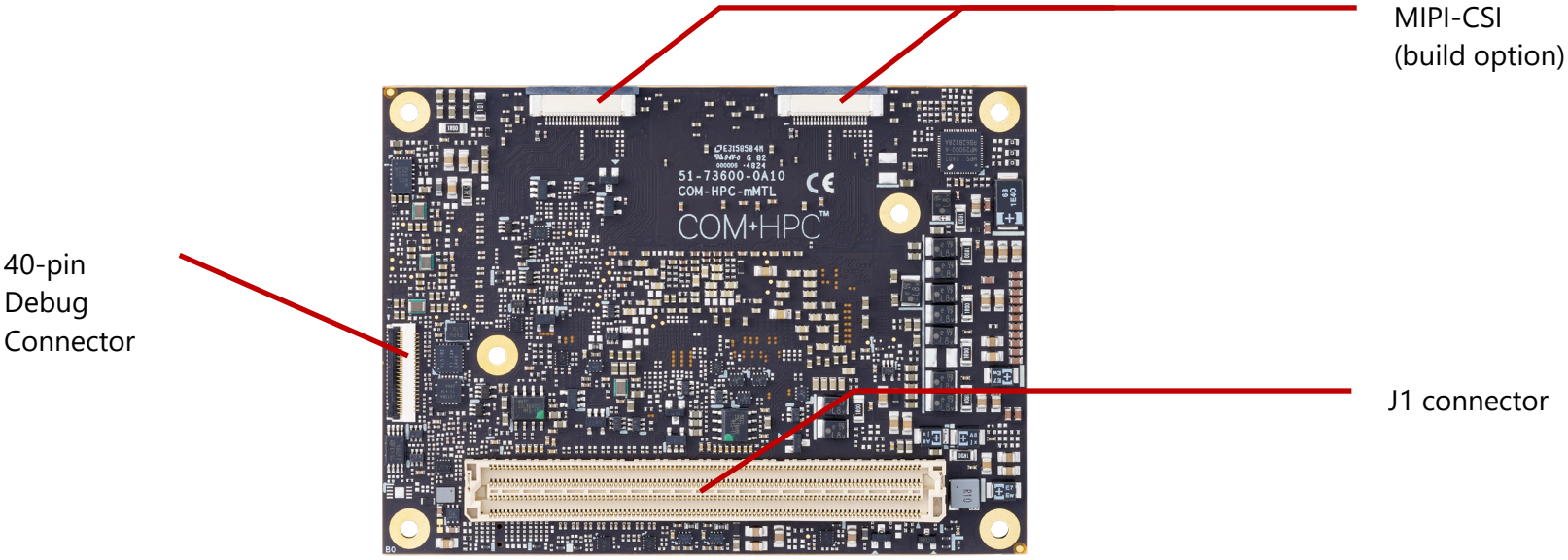


Figure 4 – Module feature locations (back)

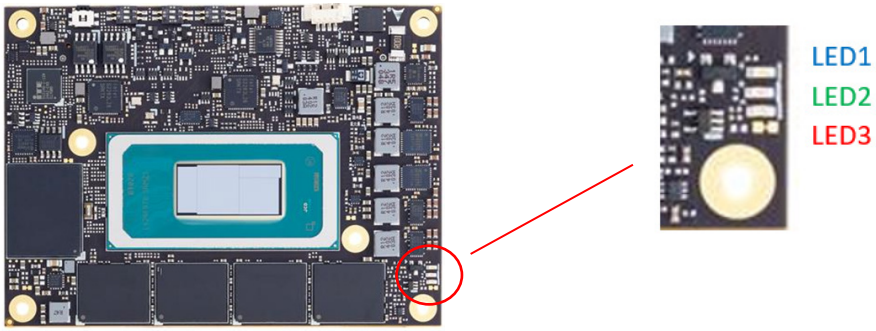
5.1 Debug Connector (40-pin connector)

The picture will be updated later.

This connector is particularly useful during the carrier design and bring-up phase. It offers access to the following critical parts of the module:

- Test points for measurement of internal power rails
- SPI BIOS programming interface
- I2C bus for BIOS POST code readout
- Module EC and MMC programming interface

5.2 Status LEDs



Status LEDs are mounted on the module as illustrated above.

LED behavior are described in the table below.

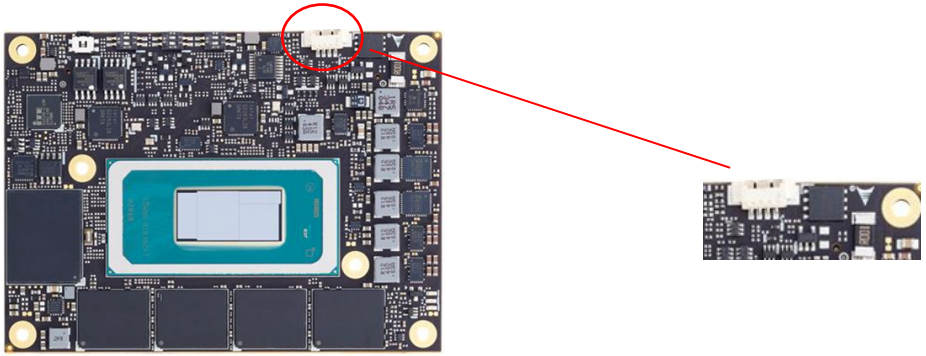
Name	Color	Connection	Function
LED1	Blue	BMC output	Power Sequence Status Code (BMC) Power Changes, Reset (see Exception Codes below)
LED2	Green	Power Source 3Vcc	S0 LED ON S3/S4/S5 LED OFF (S3 also depends on BIOS configuration) ECO mode LED OFF
LED3	Red	BMC output and same signal as WD_OUT (pin B11) on B-to-B connector	Module power up WD LED = LED OFF Watchdog counting WD LED = Keep Last State Watchdog timed out WD LED = LED ON Watchdog reset WD LED = LED ON Rebooted after WD reset WD LED = LED ON Rebooted by power button WD LED = LED OFF Rebooted by reset button WD LED = LED OFF Note: only a Reset not initiated by the BMC can clear the WD LED (user action)

5.3 Exception Codes

Exception Code	Error Message
0	NOERROR
3	NO_SLP_S5
4	NO_SLP_S4
5	NO_SLP_S3
6	BIOS_FAIL
7	RESET_FAIL
9	NO_CB_PWROK
10	CRITICAL_TEMP
11	POWER_FAIL
12	VOLTAGE_FAIL
13	RSMRST_FAIL
16	NO_VCORE_PG
17	NO_SYS_GD
21	NO_PWRSRC_GD

Note: The S3/S4 behavior also depends on the BIOS configuration.

5.4 Fan Connector

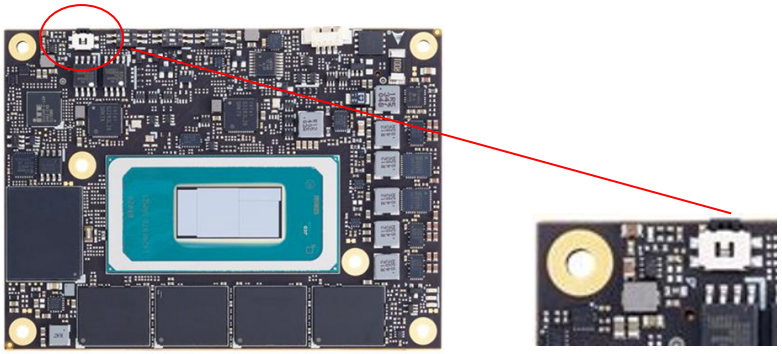


Connector Type: JVE 24W1125A-04M00

Name	Description
1	FAN_PWMOUT
2	FAN_TACHIN
3	GND
4	12V*

The supply voltage and maximum current of the fan connector is dependent on the module's input voltage (VCC_12V pins).

5.5 BIOS Default Reset



To perform a hardware reset to revert BIOS settings back to default, follow the steps below.

1. Shut down the system.
2. Press and hold the BIOS Setup Default Reset Button and boot up the system. Release the button when the BIOS prompt screen appears.
3. Once the BIOS settings have been reset to default, you will be prompted to reboot the system.

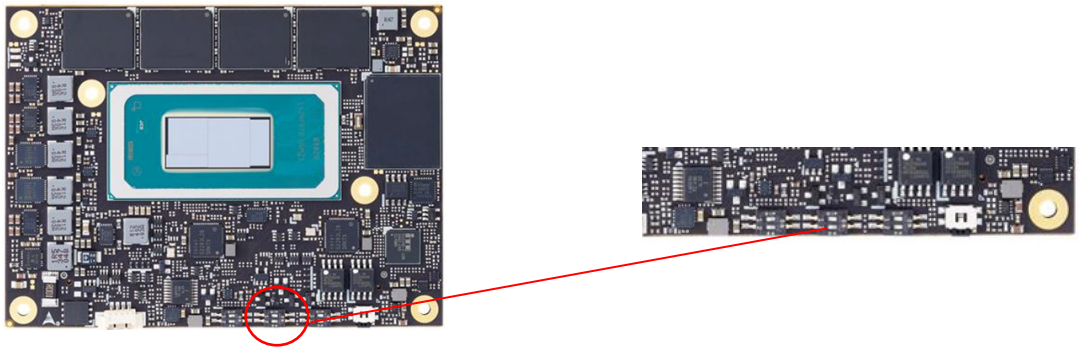
5.6 BIOS Boot Select

The module has two BIOS chips (BOM option), allowing you to configure its BIOS operation to "PICMG" and/or "Dual-BIOS Failsafe" modes using the BIOS Select and Mode Configuration Switch, Pin 2.

Setting the module to PICMG mode will configure the BIOS chips on the module as SPI0 and SPI1. In PICMG mode, a BIOS chip cannot be placed in the SPI0 slot on the carrier.

In Dual-BIOS Failsafe mode, both BIOS chips on the module are configured as SPI1. Only one of the two is connected to the SPI bus at any given time. In case of failure of the primary SPI1 BIOS, the system will reboot and switch to the secondary SPI1 BIOS on the module. In Failsafe mode, the SPI0 BIOS socket on the carrier can be populated.

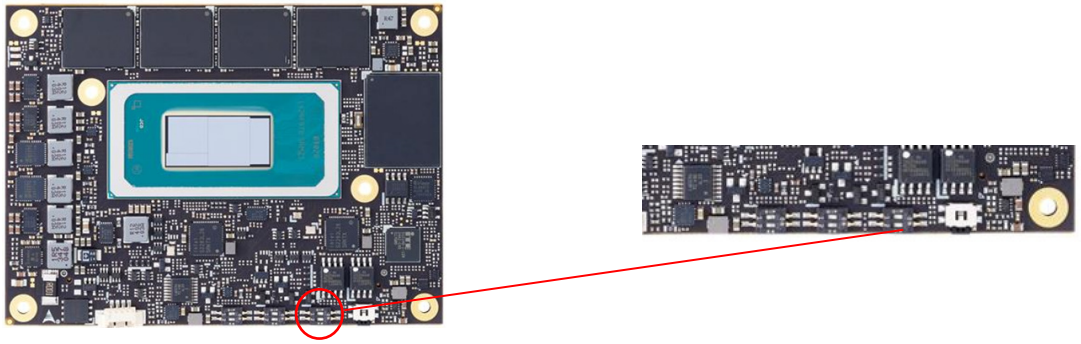
In either mode, BIOS Select and Mode Configuration Switch, Pin 1 is used to select whether to boot from SPI0 or SPI1.



Mode	Pin 1	Pin 2
Boot from SPI0 (default)	On	-
Boot from SPI1	Off	-
Set BIOS to PICMG mode (default)	-	On
Set BIOS to Failsafe BIOS mode	-	Off

5.7 NBASE-T_1 Select

NBASE-T_1 and PCIe_7/SATA_0 are multiplex design. the switch below allows to switch to NBASE-T_1 (NBASE-T port 0) to PCIe_7/SATA_0. The default setting is NBASE-T_1 enabled.



6. System Resources

Will be updated later.

7. BIOS Configurations

Will be updated later.

8. BIOS Checkpoints, Beep Codes

A status code is a data value used to provide diagnostic information about the boot process. Progress codes are status codes that signify successful progression to an initialization step. Error codes signify error conditions encountered in the process of system initialization. The Aptio 5.x core can be configured to send status codes to a variety of sources. The two most commonly used types of status codes are checkpoint codes and beep codes. Checkpoint codes are byte length data values. Checkpoints are typically output to I/O port 80h, but the Aptio 5.x core can be configured to send checkpoints to a variety of sources. The Aptio 5.x core outputs checkpoints throughout the boot process to indicate the task the system is currently executing. Checkpoints are very useful in aiding software developers or technicians in debugging problems that occur during the pre-boot process on production hardware. A beep code is a series of short sound signals. Beep codes are typically error codes that do not occur during normal boot process.

Note: Beep codes are not just sounds generated during the boot process. Some firmware components may use sounds to notify the user about other events such as detection of a hot-pluggable device. These sounds are typically generated using a frequency that is different from the frequency of the beep codes.

Viewing Checkpoints

Checkpoints generated by the Aptio firmware can be viewed using a PCI checkpoint card, also referred to as a "POST Card" or "POST Diagnostic Card". These PCI add-on cards show the value of I/O port 80h on an LED display.

Aptio V Checkpoint and Beep Codes

You can download the Aptio V Checkpoint and Beep Codes from the AMI website at: www.ami.com/download/aptio-v-checkpoint-and-beep-codes

8.1 Status Code Ranges

Status Code Range	Description
0x01 – 0x0F	SEC execution
0x10 – 0x2F	PEI CAR execution
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0xCF	DXE execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

8.2 Standard Status Codes

8.2.1 SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization

SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

8.2.2 PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12 – 0x14	Reserved for CPU
0x15	Pre-memory North Bridge initialization is started
0x16 – 0x18	Reserved for North Bridge
0x19	Pre-memory South Bridge initialization is started
0x1A – 0x1C	Reserved for South Bridge
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM)

Status Code	Description
	initialization
0x37	Post-Memory North Bridge initialization is started
0x38 – 0x3A	Reserved for North Bridge initialization
0x3B	Post-Memory South Bridge initialization is started
0x3C -0x3E	Reserved for South Bridge
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes

Status Code	Description
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes

Status Code	Description
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available

Status Code	Description
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

8.2.2.1 PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

8.2.3 DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64 – 0x67	Reserved for CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B – 0x6F	Reserved for North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73 – 0x77	Reserved for South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization

Status Code	Description
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)

Status Code	Description
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM

Status Code	Description
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

8.2.4 DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met (out of resource)

8.2.5 ACPI/ASL Checkpoint

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

8.3 OEM-reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

9. Software Support

Microsoft

Windows 10 IoT Enterprise 2021 LTSC 64-bit

Windows 11 IoT Enterprise LTSC 64-bit

Canonical

Ubuntu 24.04 LTSC

Others

Yocto Project BSP tool-based embedded Linux distribution (TBC)

VxWorks (TBC)

10. Mechanical and Thermal

The mounting hole positions for the Mini Type Module are in deliberately different positions from those of the COM-HPC Client and Server sizes due to connector pin-out differences. All dimensions are shown in mm with a tolerance of +/- 0.25mm unless otherwise noted.

10.1 Module Dimensions – Top View

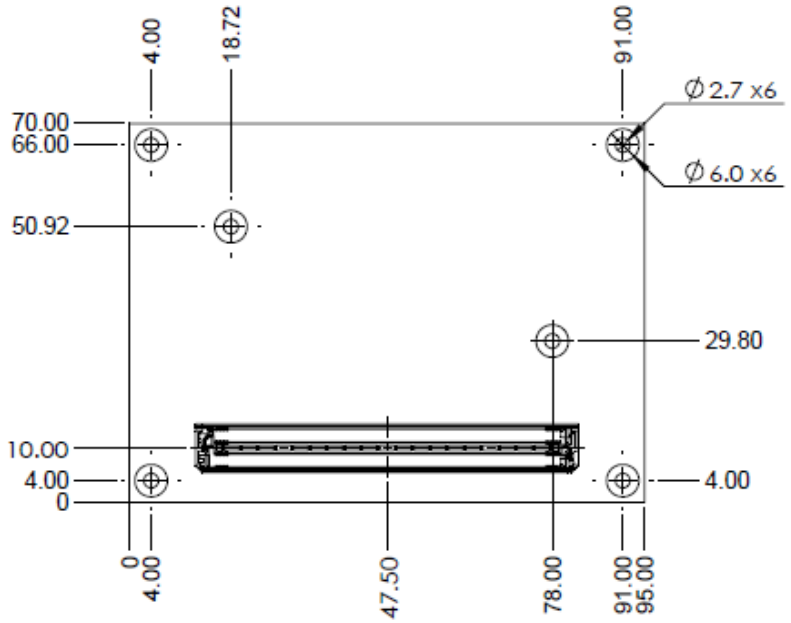


Figure 5 – Module mechanical dimensions (top view)

10.2 Module Dimensions – Side View

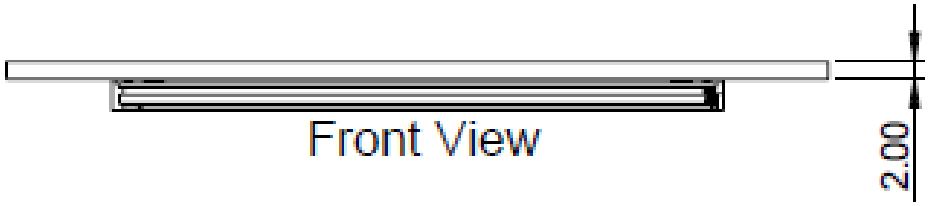
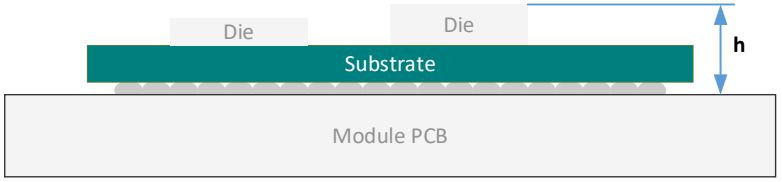


Figure 6 – Module mechanical dimensions (front view)

10.3 Height of Processor and Static Compressive Load

Processor Height Tolerance

The tolerance of the processor height is one of the key factors to consider when designing your thermal solution, as illustrated below. Please contact our ADLINK representative for further details.



	Typical	Tolerance
h	1.25 mm	+/- 0.1mm

Static Compressive Load

Another key factor to consider is the static compressive load. The module exhibits a processor maximum pressure die of 40 lbf.

10.4 Thermal Solutions

10.4.1 Heatspreader: HTS

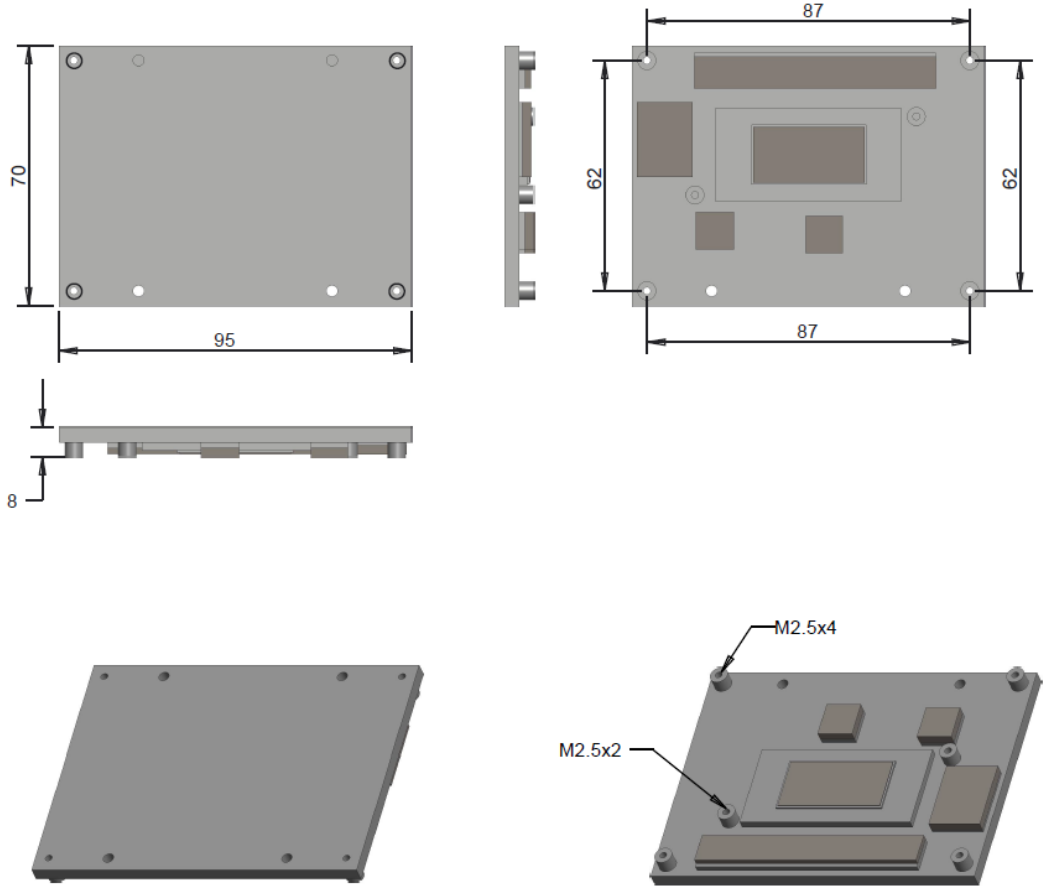


Figure 7 – Heatspreader: HTS

10.4.2 Heatsink with FAN: THSF

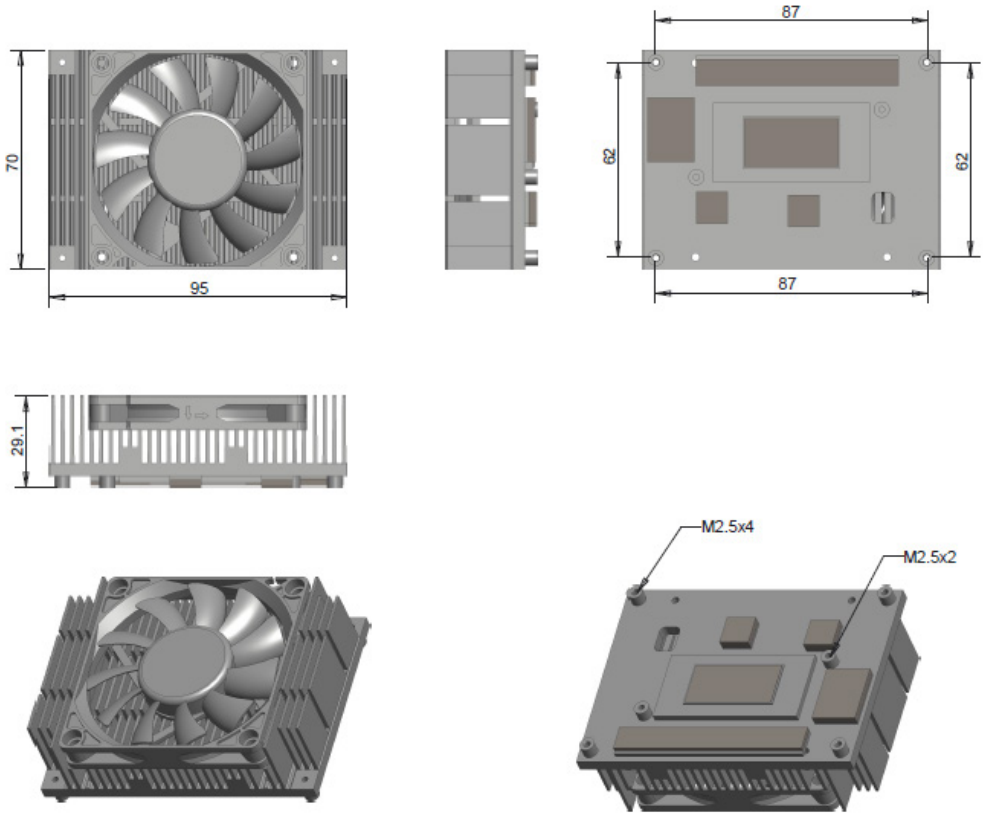


Figure 8 – Heatsink with FAN: THSF

10.5 Board to Board Connectors

To accommodate different stacking heights, the plug connector, or called as male connector, for COM-HPC carrier boards are available in two heights: 5 mm and 10 mm.

Please get recommended plug connector from ADLINK's reference carrier board.

10.6 Mounting Method

There are several standard ways to mount the COM-HPC module with a thermal solution onto a carrier board. In addition to the 5-mm or 10-mm board-to-board connectors, there are also top and bottom mounting. In top mounting, the threaded standoffs are on the carrier board, and the thermal solution is attached with through-hole standoffs. In bottom mounting, the threaded standoffs are on the thermal solution, and the carrier board has through-hole standoffs. **Bottom mounting is the default configuration**.

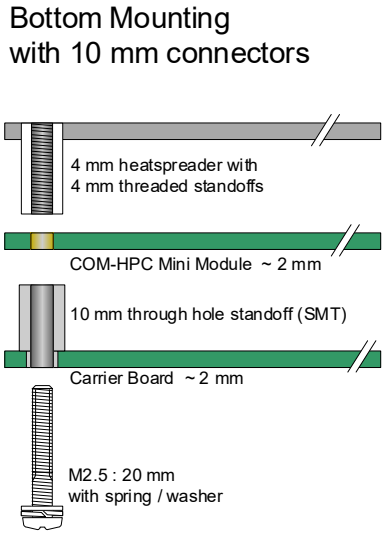


Figure 9 – Mounting method

10.7 Standoff Types

10mm through-hole standoff (SMT type)
P/N: 33-72186-0100-A0

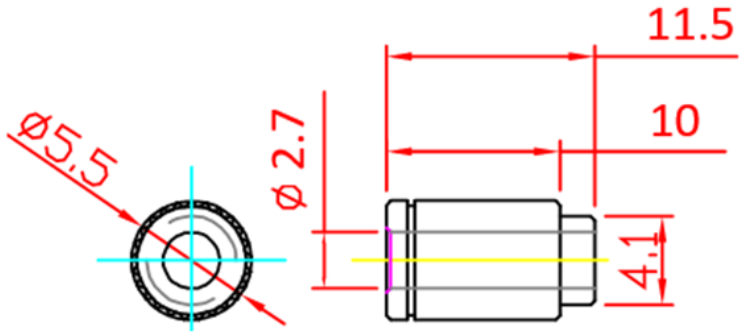
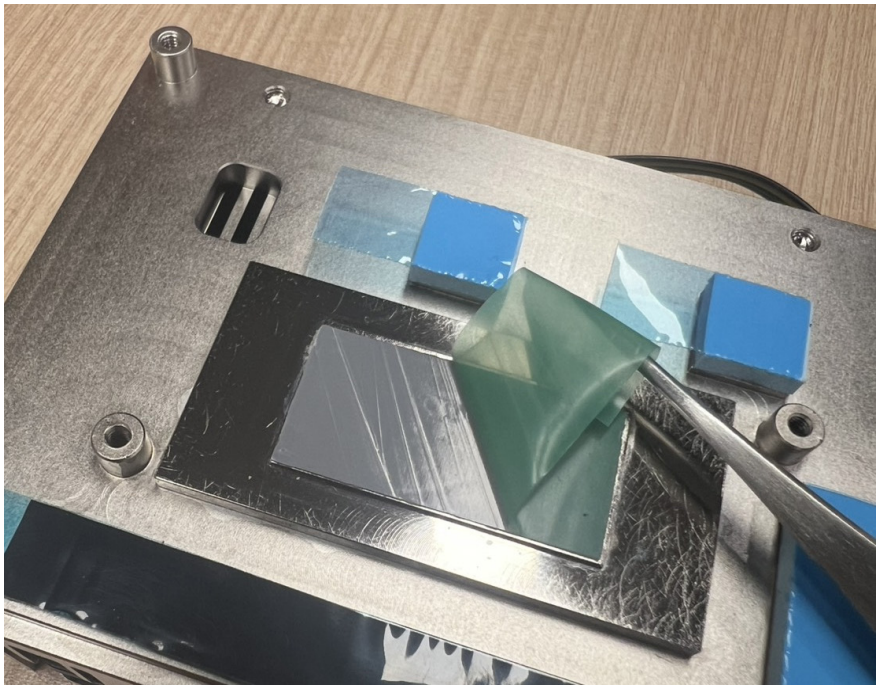


Figure 10 – Standoff types

10.8 Installation

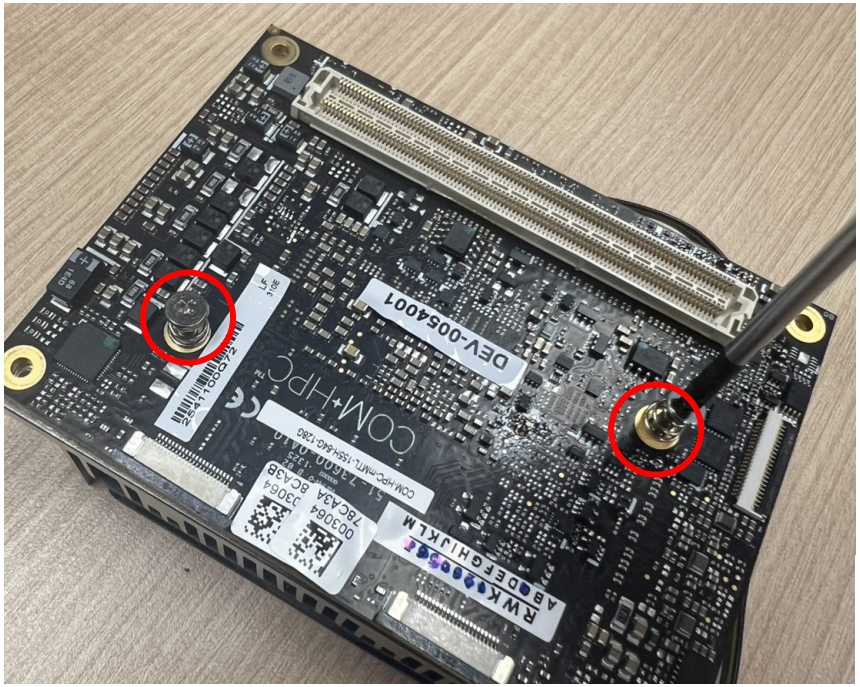
Install a heatspreader or heatsink using the following instructions. The images below are for illustration purposes only.

Step 1: Remove the protective membranes from the thermal pads.

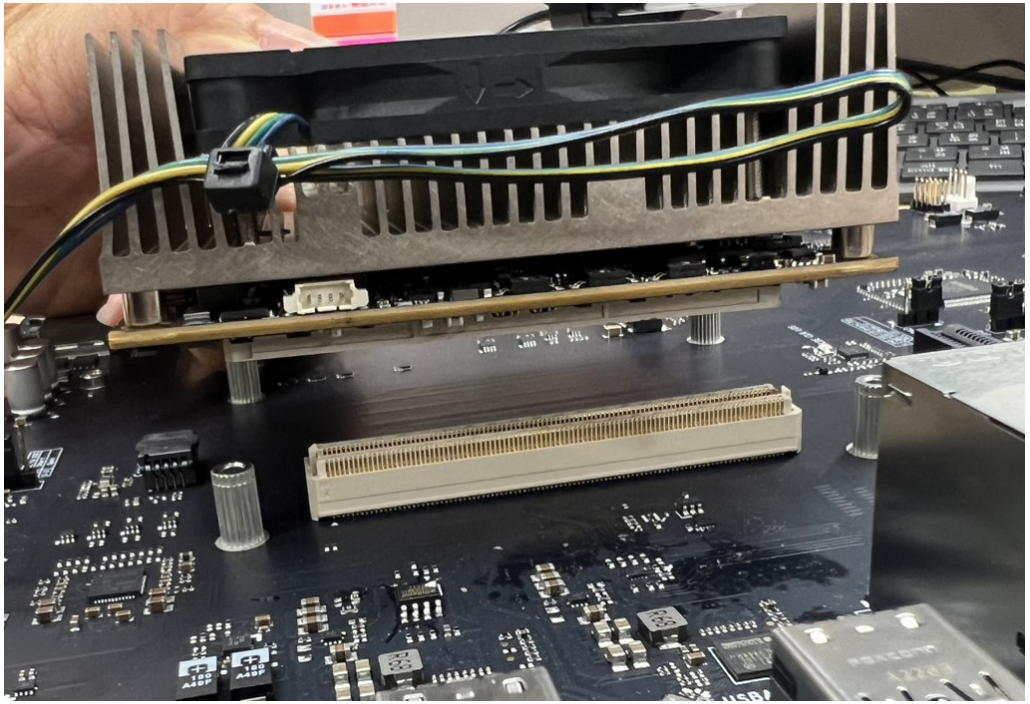


Note: All thermal pads have a protective membrane that may vary by module.

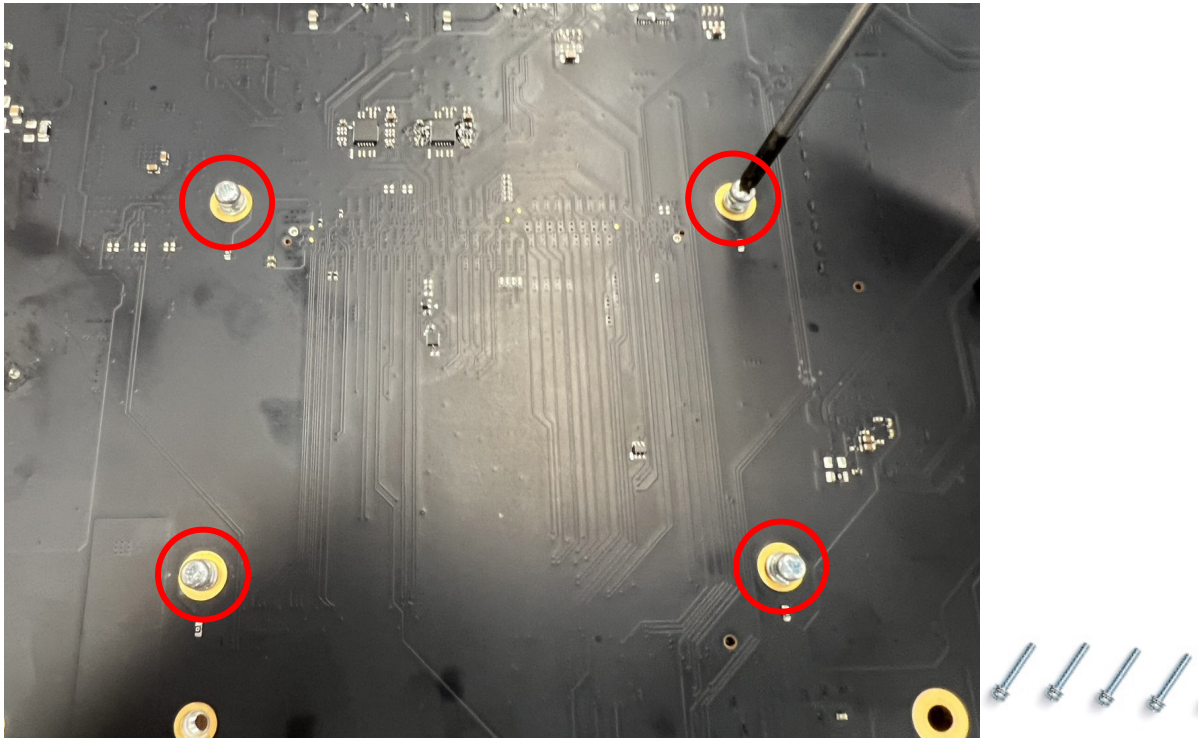
Step 2: Assemble the heatsink onto the COM-HPC Mini module. Use the 2x M2.5, L=6mm screws provided to fasten the heatsink to the module. The number of screw holes and screws may vary by module.



Step 3: Place the COM-HPC Mini module and heatsink assembly onto the connectors on the carrier board, as shown below. Press down on the module until the module is securely seated on the carrier board.



Step 4: Use the four M2.5 (L=18mm) screws provided to secure the COM-HPC Mini module to the carrier board from the solder side.
The number of screw holes and screws depends on the module and carrier board design.



Step 5: If you are installing a heatsink with a fan, plug the fan connector into the COM-HPC mini module.
The location of the FAN connector for the COM-HPC mini module depends on the design.