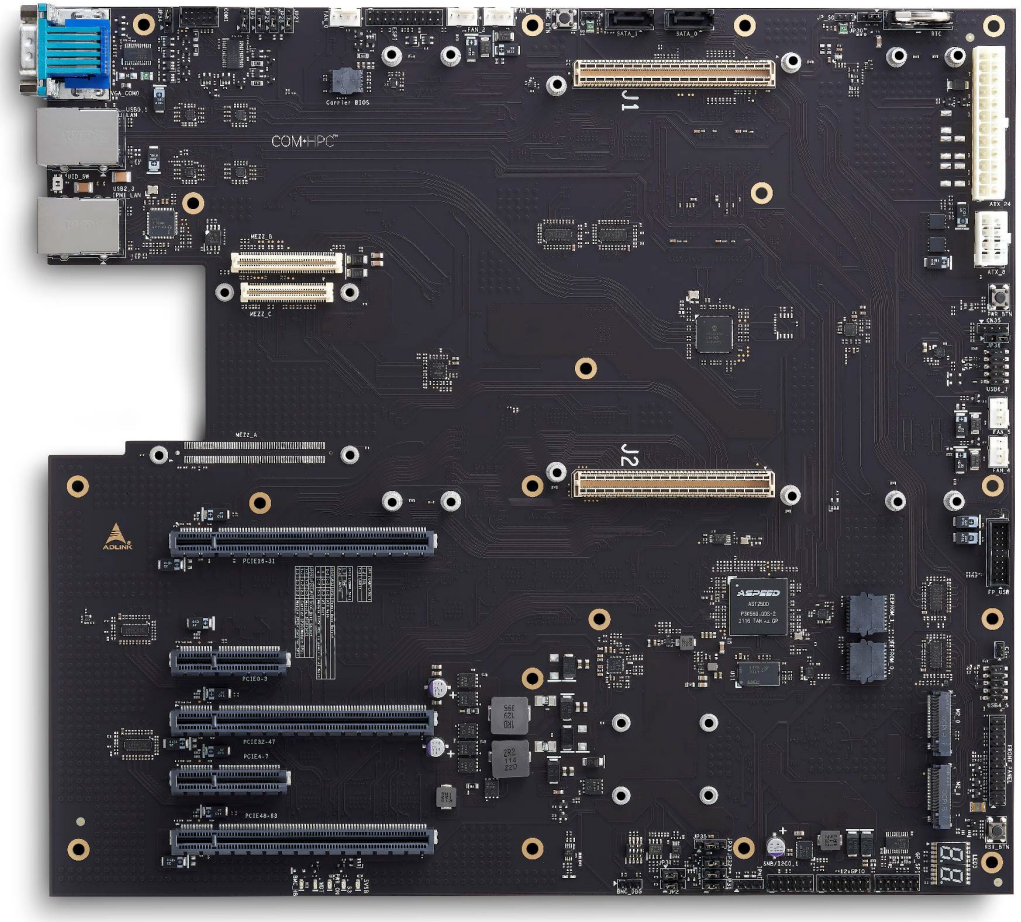
COM-HPC Server Base

User's Guide



COM-HPC™

Revision: Rev. 1.0
Date: 2023-07-12
Part Number: 50M-77106-1000

ADLINK
LEADING EDGE COMPUTING

Revision History

Revision	Description	Date	Author
1.0	Initial release	2023-07-20	CC

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Preface

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For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

Read these safety instructions carefully.

- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

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Conventions

The following conventions may be used throughout this manual, denoting special levels of information

Note: This information adds clarity or specifics to text and illustrations.

Caution: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

Warning: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

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Table of Contents

Revision History 2

Preface 3

1. Introduction 10

2. Special Features 11
   2.1. Three PCI Express x16 11
   2.2. Out-of-Band Management 12
   2.3. High Speed Ethernet Expansion 13

3. Component Location 14

4. Functional Diagram 15

5. Mechanical Dimension 16

6. Connectors and Pinouts 17
   6.1. Carrier Board Signals — Server Type 17
   6.2. Connector Location and Pinout Compatibility 18
   6.3. Carrier Board Design 19
   6.4. COM-HPC Board-to-board Connectors 19
   6.5. PCIe x16 Connectors 25
   6.6. PCIe x4 Connector 26
   6.7. KEY-M Slot Connector 27
   6.8. USB2.0 Ports Header 28
   6.9. USB3.x Ports Header 28
   6.10. SATA Port 29
   6.11. eSPI Debug Connector 30
   6.12. BMC Debug Connector 30
   6.13. COM Port Connector 31
   6.14. I2C0/1 and SMBus Header 32
   6.15. GPIO Header 32
   6.16. External SMBus Header 33
   6.17. Fan Header 33
   6.18. General Purpose SPI Header 35
   6.19. IPMI Header 35

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6.20. Front Panel Control 36
6.21. Power Connectors 37
6.22. Carrier EEPROM Address Switch 38
6.23. Module (I2C0) / BMC (I2C8) Jumpers 39
6.24. Other Jumpers 39
6.25. Power Jumpers 40

7. Secondary BIOS 42

8. Switches, POST and LEDs 43
8.1. Switches (S0-S5) 43
8.2. POST and inductors LEDs 45
8.3. ATX Power Connectors 46
8.4. AT Power Mode 47

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List of Figures

Figure 1 – Carrier top view....11
Figure 2 – Component location....14
Figure 3 – Functional diagram....15
Figure 4 – Mechanical dimensions....16
Figure 5 – Carrier board signals, Server type pinout....17
Figure 6 – Connector location and pinout compatibility....18

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1. Introduction

Warning: This is an EA (early available) engineering manual. The contents may not accurately reflect the actual or final version of this product.

The COM-HPC modular approach of custom carrier combined with off-the-shelf system cores relives developers and manufacturers the need to design their own system core, thereby not only accelerating their proof of concept significantly but also empowers them to upgrade to later generation processors without redesign. The COM-HPC concept reduces engineering complexity, lowers the threshold for total project quantity, and last but not least brings your product to the market in no time. The average time to design a carrier board is less than half the time of a full custom board.

The COM-HPC Server Base, based on PICMG COM-HPC R1.0, is an Extended ATX size carrier board, supplied by ATX and AT power source through 24+8 power connector. Together with the COM-HPC Server Type module of your choice and off-the-shelf add-on cards, you can quickly emulate the functionality of your desired end product for software development and hardware verification.

To build a functional prototype of your target system you will need:

- COM-HPC Server Type module
- COM-HPC Server Base carrier
- PCI Express-based storage or SATA storage (SATA storage solutions are dependent on module specifications)

The COM-HPC Server Base is compatible with Size E and Size D COM-HPC Server Type modules and may accommodate:

- 1x Remote management IPMI BMC and pin header for IPMB
- 3x PCI Express x16 slot, 2x PCI Express x4 slots, and 2x M.2 M-key connector
- OCP connectors for dedicated OCP 10GbE Mezzanines
- 1x VGA, 1x general purpose LAN, 1x remote management LAN, 4x USB 3.0/2.0, 1x DB-9 COM port (at rear I/O)
- 1x USB connector (2-in-1), 2x USB 10 pin header (2-in-1) for front panel

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2. Special Features

2.1. Three PCI Express x16

Maximum 2x FHFL PCI Express cards at PCIE16-31 slot and PCIE32-47 slot, and 1x FHHL PCI Express card at PCIE48-63 slot

PCIE16-31 and PCIE32-47 slots can accommodate up to 2-slot-width PCI Express cards, in the condition of not using PCIE4-7 slot

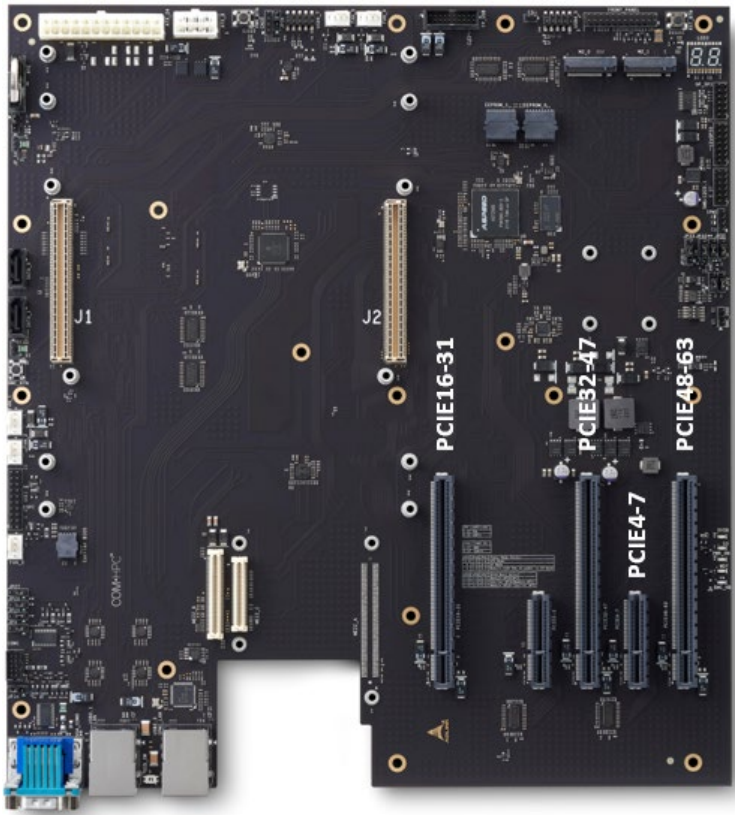

Figure 1 – Carrier top view

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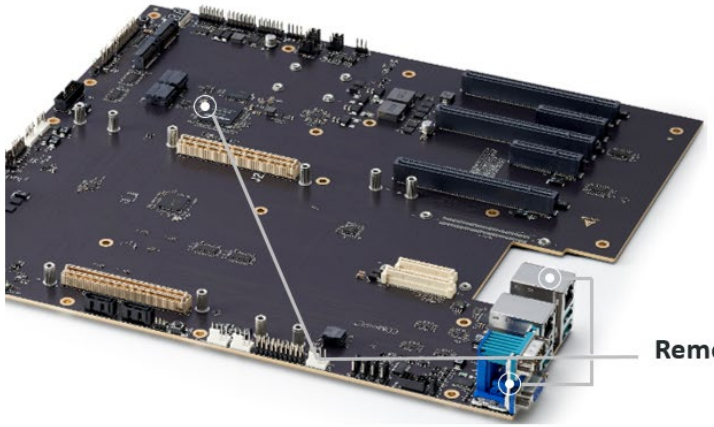
2.2. Out-of-Band Management

Out-of-band (OOB) management features, such as firmware update, power and reset control, performance monitoring and more, are defined by PICMG COM-HPC specifications.

The management architecture is divided into BMC (Board Management Controller, also called IPMI BMC or Carrier BMC) and MMC (Module Management Controller). As defined, BMC is located on the COM-HPC carrier, while MMC is located on the COM-HPC module.

Carrier BMC communicates with MMC through IPMB interface, an I^2C interface with IPMI protocol support.



Remote / Local Management by scenario

- IPMI BMC
- Dedicate Ethernet for remote, VGA and COM port for local

Note: OOB management support and features are dependent on the module used.

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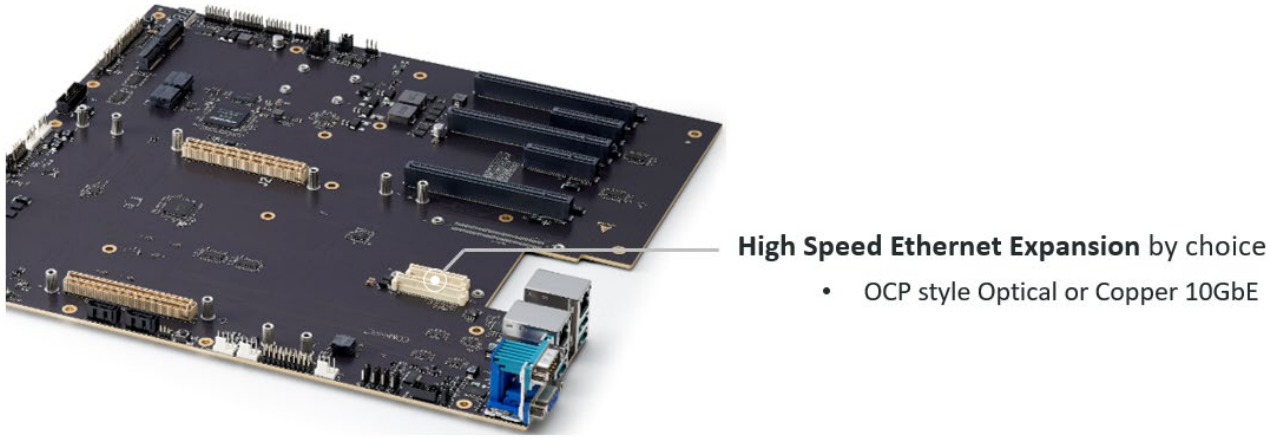
2.3. High Speed Ethernet Expansion

The high-speed Ethernet MACs are located on the COM-HPC module used. The PHY is (if used) located on the COM-HPC carrier as defined by PICMG COM-HPC specifications.

PHY may vary due to the silicon platform or Ethernet controller used, thus a connector-style design instead of a PHY chip on carrier is adopted for further expansion purposes.

OCP connector is adopted and supports dedicated OCP mezzanine card (by choice).



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3. Component Location

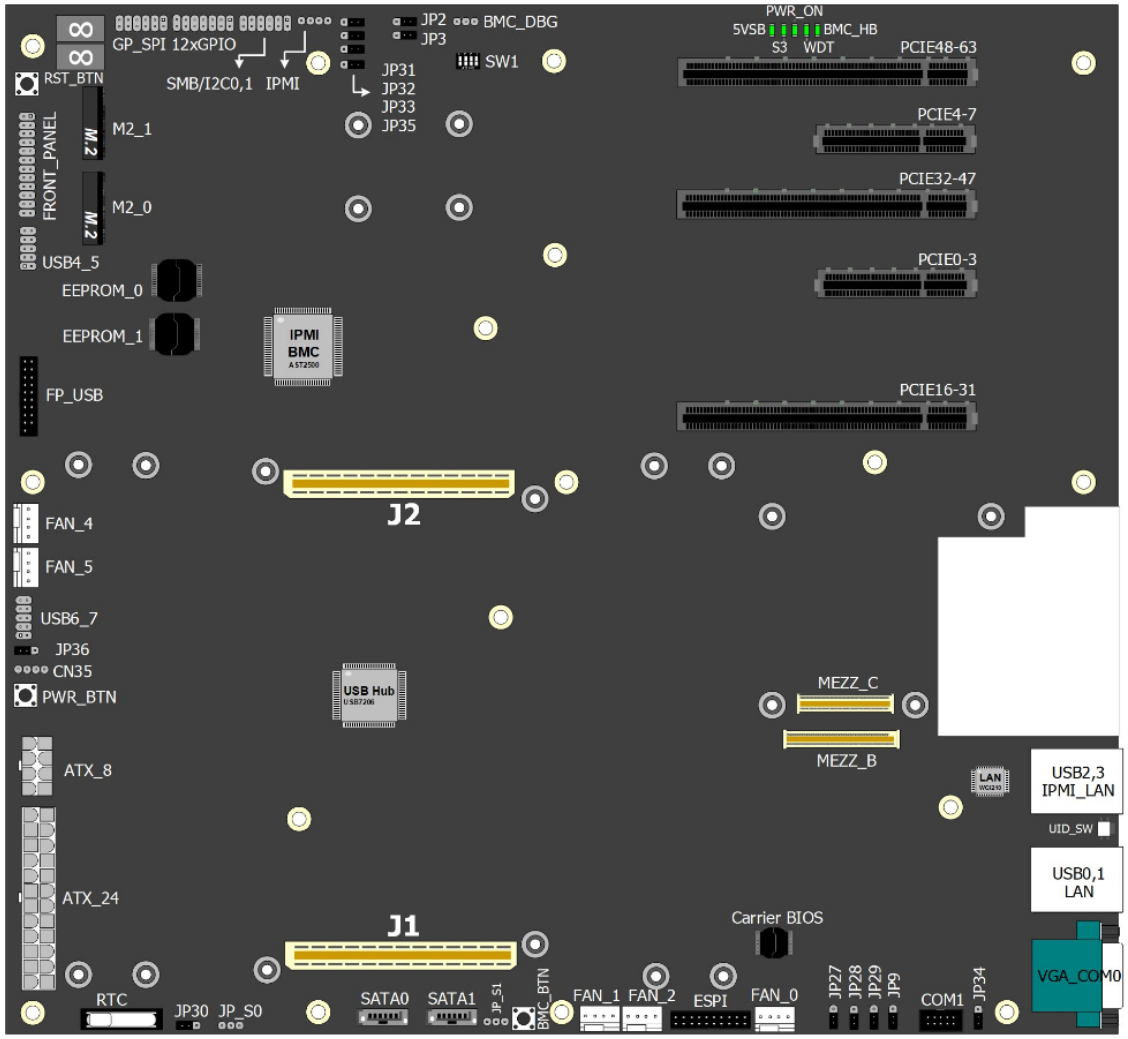

Figure 2 – Component location

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4. Functional Diagram

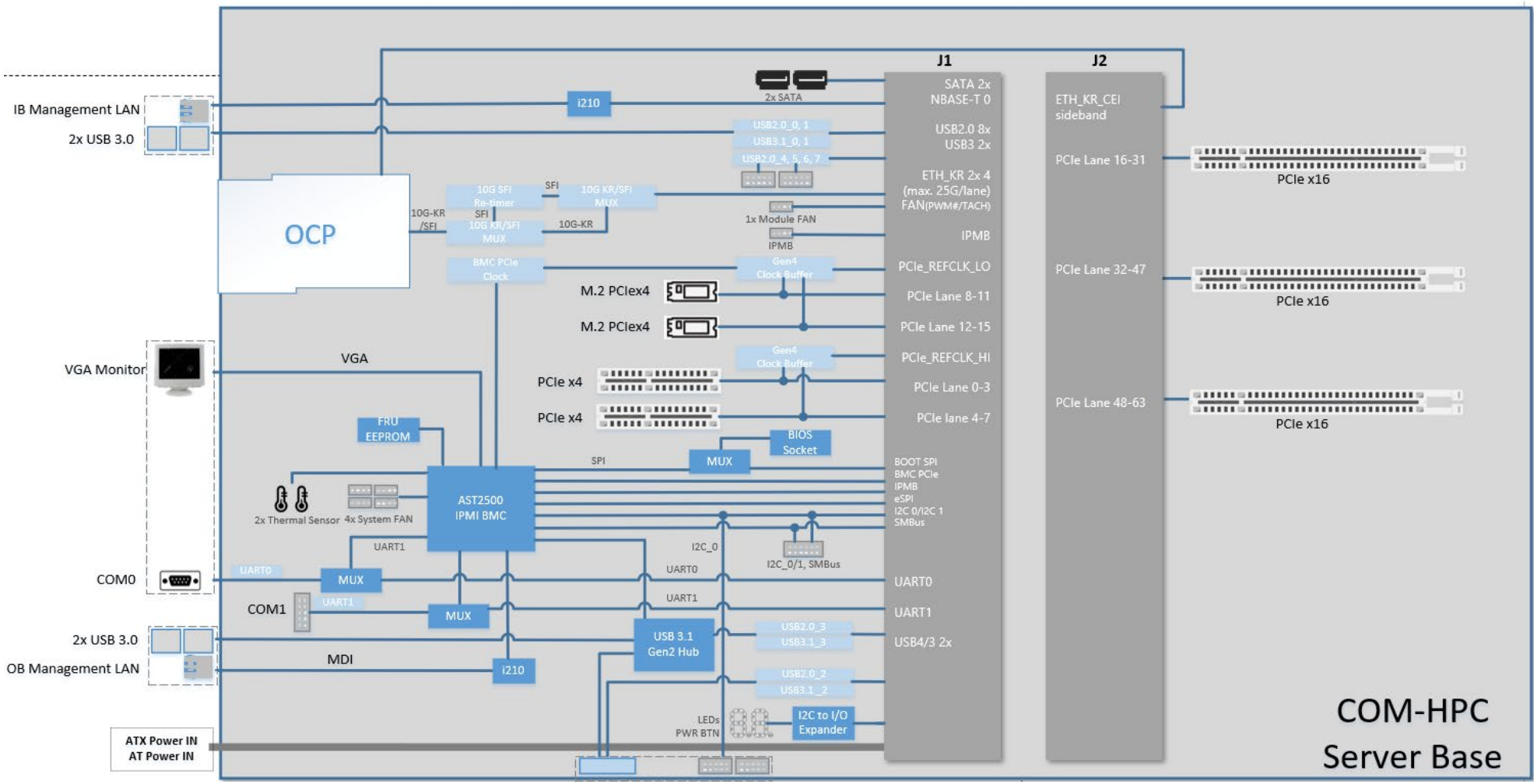

Figure 3 – Functional diagram

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5. Mechanical Dimension

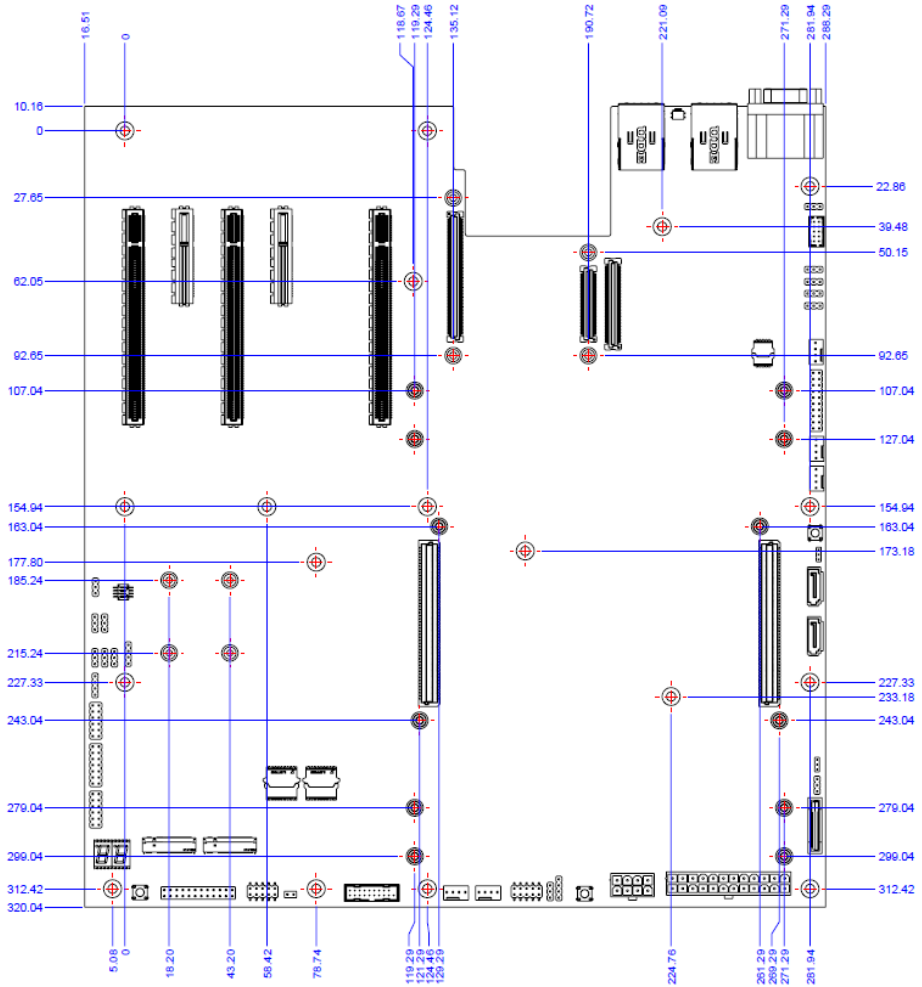

Figure 4 – Mechanical dimensions

Note: All dimensions are shown in millimeters with a tolerance of ± 0.25mm unless otherwise noted.

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6. Connectors and Pinouts

6.1. Carrier Board Signals — Server Type

Figure 5 – Carrier board signals, Server type pinout

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6.2. Connector Location and Pinout Compatibility

Connector positions and pinouts comply with pinout and signal descriptions within *PICMG COM-HPC Carrier Design Guide R2*. This document includes: descriptions of pinouts, signals, and mechanical characteristics of the COM-HPC specification. The COM-HPC Server Base carrier is compatible with COM-HPC modules in Size E and D form factor, Server Type pinout, COM-HPC Module Base Specification R1.0.

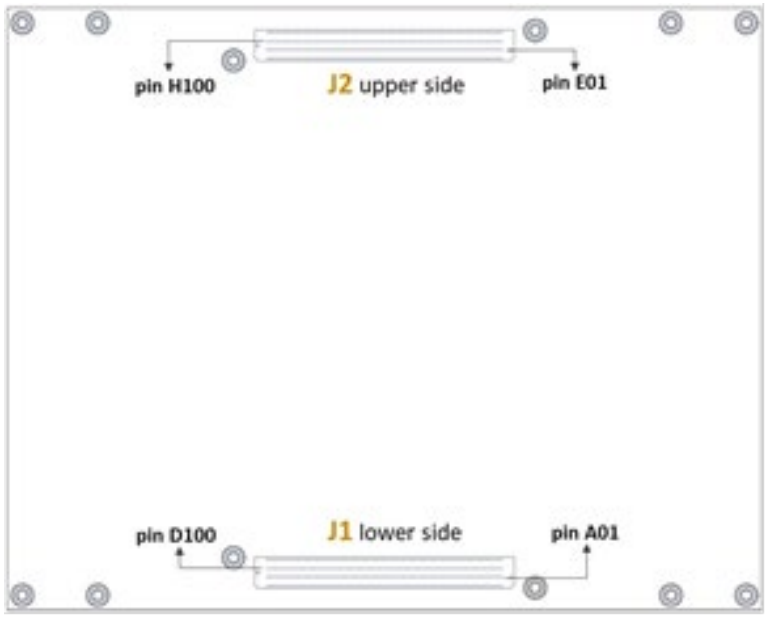

Figure 6 – Connector location and pinout compatibility

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6.3. Carrier Board Design

COM-HPC Server Base follows the PICMG COM-HPC Carrier Design Guide where possible, and its design and schematic have been fully verified. It is recommend to utilize them as references for your carrier board design. COM-HPC Server Base schematics and mechanical files, as well as the CDG, can be downloaded from ADLINK COM's webpage.

6.4. COM-HPC Board-to-board Connectors

Signals and Pinouts for COM-HPC **Server Type** (Size D & E)

Row A			Row B			Row C			Row D	
A1	VCC		B1	VCC		C1	VCC		D1	VCC
A2	VCC		B2	PWRBTN#		C2	RSTBTN#		D2	VCC
A3	VCC		B3	VCC		C3	VCC		D3	VCC
A4	VCC		B4	THERMTRIP#		C4	CARRIER_HOT#		D4	VCC
A5	VCC		B5	VCC		C5	VCC		D5	VCC
A6	VCC		B6	TAMPER#		C6	VIN_PWR_OK		D6	VCC
A7	VCC		B7	VCC		C7	VCC		D7	VCC
A8	VCC		B8	SUS_S3#		C8	SUS_S4_S5#		D8	VCC
A9	VCC		B9	VCC		C9	VCC		D9	VCC
A10	GND		B10	WD_STROBE#		C10	GND		D10	WAKE0#
A11	BATLOW#		B11	WD_OUT		C11	FAN_PWMOUT		D11	WAKE1#
A12	PLTRST#		B12	GND		C12	FAN_TACHIN		D12	GND
A13	GND		B13	USB5-		C13	GND		D13	USB1-
A14	USB7-		B14	USB5+		C14	USB3-		D14	USB1+
A15	USB7+		B15	GND		C15	USB3+		D15	GND
A16	GND		B16	USB4-		C16	GND		D16	USB0-
A17	USB6-		B17	USB4+		C17	USB2-		D17	USB0+
A18	USB6+		B18	GND		C18	USB2+		D18	GND
A19	GND		B19	RSVD		C19	GND		D19	ETH0_RX-
A20	ETH4_RX-		B20	RSVD		C20	ETH0_TX-		D20	ETH0_RX+
A21	ETH4_RX+		B21	RSVD		C21	ETH0_TX+		D21	GND
A22	GND		B22	RSVD		C22	GND		D22	ETH1_RX-

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Row A			Row B			Row C			Row D	
A23	ETH5_RX-		B23	RSVD		C23	ETH1_TX-		D23	ETH1_RX+
A24	ETH5_RX+		B24	VCC_5V_SBY		C24	ETH1_TX+		D24	GND
A25	GND		B25	USB67_OC#		C25	GND		D25	ETH2_RX-
A26	ETH6_RX-		B26	USB45_OC#		C26	ETH2_TX-		D26	ETH2_RX+
A27	ETH6_RX+		B27	USB23_OC#		C27	ETH2_TX+		D27	GND
A28	GND		B28	USB01_OC#		C28	GND		D28	ETH3_RX-
A29	ETH7_RX-		B29	SML1_CLK		C29	ETH3_TX-		D29	ETH3_RX+
A30	ETH7_RX+		B30	SML1_DAT		C30	ETH3_TX+		D30	GND
A31	GND		B31	PMCALERT#		C31	GND		D31	USB3_SSTX-
A32	RSVD		B32	SML0_CLK		C32	USB3_SSRX-		D32	USB3_SSTX+
A33	RSVD		B33	SML0_DAT		C33	USB3_SSRX+		D33	GND
A34	GND		B34	USB_PD_ALERT#		C34	GND		D34	USB2_SSTX-
A35	ETH4_TX-		B35	USB_PD_I2C_CLK		C35	USB2_SSRX-		D35	USB2_SSTX+
A36	ETH4_TX+		B36	USB_PD_I2C_DAT		C36	USB2_SSRX+		D36	GND
A37	GND		B37	USB_RT_ENA		C37	GND		D37	USB1_SSTX0-
A38	ETH5_TX-		B38	USB1_LSRX		C38	USB1_SSRX0-		D38	USB1_SSTX0+
A39	ETH5_TX+		B39	USB1_LSTX		C39	USB1_SSRX0+		D39	GND
A40	GND		B40	USB0_LSRX		C40	GND		D40	USB1_SSTX1-
A41	ETH6_TX-		B41	USB0_LSTX		C41	USB1_SSRX1-		D41	USB1_SSTX1+
A42	ETH6_TX+		B42	GND		C42	USB1_SSRX1+		D42	GND
A43	GND		B43	USB0_AUX-		C43	GND		D43	USB0_SSTX0-
A44	ETH7_TX-		B44	USB0_AUX+		C44	USB0_SSRX0-		D44	USB0_SSTX0+
A45	ETH7_TX+		B45	RSVD		C45	USB0_SSRX0+		D45	GND
A46	GND		B46	RSVD		C46	GND		D46	USB0_SSTX1-
A47	USB1_AUX-		B47	VCC_BOOT_SPI		C47	USB0_SSRX1-		D47	USB0_SSTX1+
A48	USB1_AUX+		B48	BOOT_SPI_CS#		C48	USB0_SSRX1+		D48	GND
A49	GND		B49	BSEL0		C49	GND		D49	SATA0_RX-
A50	eSPI_IO0		B50	BSEL1		C50	BOOT_SPI_IO0		D50	SATA0_RX+
A51	eSPI_IO1		B51	BSEL2		C51	BOOT_SPI_IO1		D51	GND
A52	eSPI_IO2		B52	eSPI_ALERT0#		C52	BOOT_SPI_IO2		D52	SATA0_TX-
A53	eSPI_IO3		B53	eSPI_ALERT1#		C53	BOOT_SPI_IO3		D53	SATA0_TX+
A54	eSPI_CLK		B54	eSPI_CS0#		C54	BOOT_SPI_CLK		D54	GND
A55	GND		B55	eSPI_CS1#		C55	GND		D55	SATA1_RX-
A56	PCIe_CLKREQ0_LO#		B56	eSPI_RST#		C56	PCIe_REFCLK0_HI-		D56	SATA1_RX+
A57	PCIe_CLKREQ0_HI#		B57	GND		C57	PCIe_REFCLK0_HI+		D57	GND
A58	GND		B58	PCIe_BMC_RX-		C58	GND		D58	SATA1_TX-
A59	PCIe_BMC_TX-		B59	PCIe_BMC_RX+		C59	PCIe_REFCLK0_LO-		D59	SATA1_TX+

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Row A			Row B			Row C			Row D	
A60	PCIe_BMC_TX+		B60	GND		C60	PCIe_REFCLK0_LO+		D60	GND
A61	GND		B61	PCIe08_RX-		C61	GND		D61	PCIe00_TX-
A62	PCIe08_TX-		B62	PCIe08_RX+		C62	PCIe00_RX-		D62	PCIe00_TX+
A63	PCIe08_TX+		B63	GND		C63	PCIe00_RX+		D63	GND
A64	GND		B64	PCIe09_RX-		C64	GND		D64	PCIe01_TX-
A65	PCIe09_TX-		B65	PCIe09_RX+		C65	PCIe01_RX-		D65	PCIe01_TX+
A66	PCIe09_TX+		B66	GND		C66	PCIe01_RX+		D66	GND
A67	GND		B67	PCIe10_RX-		C67	GND		D67	PCIe02_TX-
A68	PCIe10_TX-		B68	PCIe10_RX+		C68	PCIe02_RX-		D68	PCIe02_TX+
A69	PCIe10_TX+		B69	GND		C69	PCIe02_RX+		D69	GND
A70	GND		B70	PCIe11_RX-		C70	GND		D70	PCIe03_TX-
A71	PCIe11_TX-		B71	PCIe11_RX+		C71	PCIe03_RX-		D71	PCIe03_TX+
A72	PCIe11_TX+		B72	GND		C72	PCIe03_RX+		D72	GND
A73	GND		B73	PCIe12_RX-		C73	GND		D73	PCIe04_TX-
A74	PCIe12_TX-		B74	PCIe12_RX+		C74	PCIe04_RX-		D74	PCIe04_TX+
A75	PCIe12_TX+		B75	GND		C75	PCIe04_RX+		D75	GND
A76	GND		B76	PCIe13_RX-		C76	GND		D76	PCIe05_TX-
A77	PCIe13_TX-		B77	PCIe13_RX+		C77	PCIe05_RX-		D77	PCIe05_TX+
A78	PCIe13_TX+		B78	GND		C78	PCIe05_RX+		D78	GND
A79	GND		B79	PCIe14_RX-		C79	GND		D79	PCIe06_TX-
A80	PCIe14_TX-		B80	PCIe14_RX+		C80	PCIe06_RX-		D80	PCIe06_TX+
A81	PCIe14_TX+		B81	GND		C81	PCIe06_RX+		D81	GND
A82	GND		B82	PCIe15_RX-		C82	GND		D82	PCIe07_TX-
A83	PCIe15_TX-		B83	PCIe15_RX+		C83	PCIe07_RX-		D83	PCIe07_TX+
A84	PCIe15_TX+		B84	GND		C84	PCIe07_RX+		D84	GND
A85	GND		B85	**RSVD**		C85	GND		D85	NBASET0_MDI0-
A86	VCC_RTC		B86	RSMRST_OUT#		C86	SMB_CLK		D86	NBASET0_MDI0+
A87	SUS_CLK		B87	UART1_TX		C87	SMB_DAT		D87	GND
A88	GPIO_00		B88	UART1_RX		C88	SMB_ALERT#		D88	NBASET0_MDI1-
A89	GPIO_01		B89	UART1_RTS#		C89	UART0_TX		D89	NBASET0_MDI1+
A90	GPIO_02		B90	UART1_CTS#		C90	UART0_RX		D90	GND
A91	GPIO_03		B91	IPMB_CLK		C91	UART0_RTS#		D91	NBASET0_MDI2-
A92	GPIO_04		B92	IPMB_DAT		C92	UART0_CTS#		D92	NBASET0_MDI2+
A93	GPIO_05		B93	GPSPI_MOSI		C93	I2C0_CLK		D93	GND
A94	GPIO_06		B94	GPSPI_MISO		C94	I2C0_DAT		D94	NBASET0_MDI3-
A95	GPIO_07		B95	GPSPI_CS0#		C95	I2C0_ALERT#		D95	NBASET0_MDI3+
A96	GPIO_08		B96	GPSPI_CS1#		C96	I2C1_CLK		D96	GND

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Row A			Row B			Row C			Row D	
A97	GPIO_09		B97	GPSPI_CS2#		C97	I2C1_DAT		D97	NBASET0_LINK_MAX#
A98	GPIO_10		B98	GPSPI_CS3#		C98	NBASET0_SDP		D98	NBASET0_LINK_MID#
A99	GPIO_11		B99	GPSPI_CLK		C99	NBASET0_CTREF		D99	NBASET0_LINK_ACT#
A100	TYPE0		B100	GPSPI_ALERT#		C100	TYPE1		D100	TYPE2

Row E			Row F			Row G			Row H	
E1	RAPID_SHUTDOWN		F1	ETH2_SDP		G1	VCC_5V_SBY		H1	RSVD
E2	GND		F2	ETH3_SDP		G2	RSVD		H2	RSVD
E3	RSVD		F3	ETH4_SDP		G3	RSVD		H3	RSVD
E4	RSVD		F4	ETH5_SDP		G4	RSVD		H4	RSVD
E5	GND		F5	ETH6_SDP		G5	RSVD		H5	RSVD
E6	RSVD		F6	ETH7_SDP		G6	RSVD		H6	RSVD
E7	RSVD		F7	ETH4-7_I2C_CLK		G7	RSVD		H7	RSVD
E8	GND		F8	ETH4-7_I2C_DAT		G8	RSVD		H8	RSVD
E9	RSVD		F9	ETH4-7_INT#		G9	RSVD		H9	RSVD
E10	RSVD		F10	ETH4-7_MDIO_CLK		G10	RSVD		H10	RSVD
E11	GND		F11	ETH4-7_MDIO_DAT		G11	RSVD		H11	RSVD
E12	RSVD		F12	ETH4-7_PHY_INT#		G12	RSVD		H12	RSVD
E13	RSVD		F13	ETH4-7_PHY_RST#		G13	RSVD		H13	RSVD
E14	GND		F14	ETH4-7_PRSNT#		G14	GND		H14	RSVD
E15	RSVD		F15	RSVD		G15	RSVD		H15	RSVD
E16	RSVD		F16	RSVD		G16	RSVD		H16	RSVD
E17	GND		F17	RSVD		G17	RSVD		H17	RSVD
E18	RSVD		F18	RSVD		G18	RSVD		H18	RSVD
E19	RSVD		F19	GND		G19	RSVD		H19	GND
E20	GND		F20	PCIe32_RX-		G20	GND		H20	PCIe40_TX-
E21	PCIe32_TX-		F21	PCIe32_RX+		G21	PCIe40_RX-		H21	PCIe40_TX+
E22	PCIe32_TX+		F22	GND		G22	PCIe40_RX+		H22	GND
E23	GND		F23	PCIe33_RX-		G23	GND		H23	PCIe41_TX-
E24	PCIe33_TX-		F24	PCIe33_RX+		G24	PCIe41_RX-		H24	PCIe41_TX+
E25	PCIe33_TX+		F25	GND		G25	PCIe41_RX+		H25	GND
E26	GND		F26	PCIe34_RX-		G26	GND		H26	PCIe42_TX-
E27	PCIe34_TX-		F27	PCIe34_RX+		G27	PCIe42_RX-		H27	PCIe42_TX+
E28	PCIe34_TX+		F28	GND		G28	PCIe42_RX+		H28	GND
E29	GND		F29	PCIe35_RX-		G29	GND		H29	PCIe43_TX-
E30	PCIe35_TX-		F30	PCIe35_RX+		G30	PCIe43_RX-		H30	PCIe43_TX+

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Row E			Row F			Row G			Row H	
E31	PCIe35_TX+		F31	GND		G31	PCIe43_RX+		H31	GND
E32	GND		F32	PCIe36_RX-		G32	GND		H32	PCIe44_TX-
E33	PCIe36_TX-		F33	PCIe36_RX+		G33	PCIe44_RX-		H33	PCIe44_TX+
E34	PCIe36_TX+		F34	GND		G34	PCIe44_RX+		H34	GND
E35	GND		F35	PCIe37_RX-		G35	GND		H35	PCIe45_TX-
E36	PCIe37_TX-		F36	PCIe37_RX+		G36	PCIe45_RX-		H36	PCIe45_TX+
E37	PCIe37_TX+		F37	GND		G37	PCIe45_RX+		H37	GND
E38	GND		F38	PCIe38_RX-		G38	GND		H38	PCIe46_TX-
E39	PCIe38_TX-		F39	PCIe38_RX+		G39	PCIe46_RX-		H39	PCIe46_TX+
E40	PCIe38_TX+		F40	GND		G40	PCIe46_RX+		H40	GND
E41	GND		F41	PCIe39_RX-		G41	GND		H41	PCIe47_TX-
E42	PCIe39_TX-		F42	PCIe39_RX+		G42	PCIe47_RX-		H42	PCIe47_TX+
E43	PCIe39_TX+		F43	GND		G43	PCIe47_RX+		H43	GND
E44	GND		F44	PCIe16_RX-		G44	GND		H44	PCIe24_TX-
E45	PCIe16_TX-		F45	PCIe16_RX+		G45	PCIe24_RX-		H45	PCIe24_TX+
E46	PCIe16_TX+		F46	GND		G46	PCIe24_RX+		H46	GND
E47	GND		F47	PCIe17_RX-		G47	GND		H47	PCIe25_TX-
E48	PCIe17_TX-		F48	PCIe17_RX+		G48	PCIe25_RX-		H48	PCIe25_TX+
E49	PCIe17_TX+		F49	GND		G49	PCIe25_RX+		H49	GND
E50	GND		F50	PCIe18_RX-		G50	GND		H50	PCIe26_TX-
E51	PCIe18_TX-		F51	PCIe18_RX+		G51	PCIe26_RX-		H51	PCIe26_TX+
E52	PCIe18_TX+		F52	GND		G52	PCIe26_RX+		H52	GND
E53	GND		F53	PCIe19_RX-		G53	GND		H53	PCIe27_TX-
E54	PCIe19_TX-		F54	PCIe19_RX+		G54	PCIe27_RX-		H54	PCIe27_TX+
E55	PCIe19_TX+		F55	GND		G55	PCIe27_RX+		H55	GND
E56	GND		F56	PCIe20_RX-		G56	GND		H56	PCIe28_TX-
E57	PCIe20_TX-		F57	PCIe20_RX+		G57	PCIe28_RX-		H57	PCIe28_TX+
E58	PCIe20_TX+		F58	GND		G58	PCIe28_RX+		H58	GND
E59	GND		F59	PCIe21_RX-		G59	GND		H59	PCIe29_TX-
E60	PCIe21_TX-		F60	PCIe21_RX+		G60	PCIe29_RX-		H60	PCIe29_TX+
E61	PCIe21_TX+		F61	GND		G61	PCIe29_RX+		H61	GND
E62	GND		F62	PCIe22_RX-		G62	GND		H62	PCIe30_TX-
E63	PCIe22_TX-		F63	PCIe22_RX+		G63	PCIe30_RX-		H63	PCIe30_TX+
E64	PCIe22_TX+		F64	GND		G64	PCIe30_RX+		H64	GND
E65	GND		F65	PCIe23_RX-		G65	GND		H65	PCIe31_TX-
E66	PCIe23_TX-		F66	PCIe23_RX+		G66	PCIe31_RX-		H66	PCIe31_TX+
E67	PCIe23_TX+		F67	GND		G67	PCIe31_RX+		H67	GND

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Row E			Row F			Row G			Row H	
E68	GND		F68	PCIe48_RX-		G68	GND		H68	PCIe56_TX-
E69	PCIe48_TX-		F69	PCIe48_RX+		G69	PCIe56_RX-		H69	PCIe56_TX+
E70	PCIe48_TX+		F70	GND		G70	PCIe56_RX+		H70	GND
E71	GND		F71	PCIe49_RX-		G71	GND		H71	PCIe57_TX-
E72	PCIe49_TX-		F72	PCIe49_RX+		G72	PCIe57_RX-		H72	PCIe57_TX+
E73	PCIe49_TX+		F73	GND		G73	PCIe57_RX+		H73	GND
E74	GND		F74	PCIe50_RX-		G74	GND		H74	PCIe58_TX-
E75	PCIe50_TX-		F75	PCIe50_RX+		G75	PCIe58_RX-		H75	PCIe58_TX+
E76	PCIe50_TX+		F76	GND		G76	PCIe58_RX+		H76	GND
E77	GND		F77	PCIe51_RX-		G77	GND		H77	PCIe59_TX-
E78	PCIe51_TX-		F78	PCIe51_RX+		G78	PCIe59_RX-		H78	PCIe59_TX+
E79	PCIe51_TX+		F79	GND		G79	PCIe59_RX+		H79	GND
E80	GND		F80	PCIe52_RX-		G80	GND		H80	PCIe60_TX-
E81	PCIe52_TX-		F81	PCIe52_RX+		G81	PCIe60_RX-		H81	PCIe60_TX+
E82	PCIe52_TX+		F82	GND		G82	PCIe60_RX+		H82	GND
E83	GND		F83	PCIe53_RX-		G83	GND		H83	PCIe61_TX-
E84	PCIe53_TX-		F84	PCIe53_RX+		G84	PCIe61_RX-		H84	PCIe61_TX+
E85	PCIe53_TX+		F85	GND		G85	PCIe61_RX+		H85	GND
E86	GND		F86	PCIe54_RX-		G86	GND		H86	PCIe62_TX-
E87	PCIe54_TX-		F87	PCIe54_RX+		G87	PCIe62_RX-		H87	PCIe62_TX+
E88	PCIe54_TX+		F88	GND		G88	PCIe62_RX+		H88	GND
E89	GND		F89	PCIe55_RX-		G89	GND		H89	PCIe63_TX-
E90	PCIe55_TX-		F90	PCIe55_RX+		G90	PCIe63_RX-		H90	PCIe63_TX+
E91	PCIe55_TX+		F91	GND		G91	PCIe63_RX+		H91	GND
E92	GND		F92	PCIe_REFCLK2-		G92	GND		H92	PCIe_REFCLKIN0-
E93	PCIe_REFCLK1-		F93	PCIe_REFCLK2+		G93	PCIe_REFCLK3-		H93	PCIe_REFCLKIN0+
E94	PCIe_REFCLK1+		F94	GND		G94	PCIe_REFCLK3+		H94	GND
E95	GND		F95	PCIe_CLKREQ3#		G95	GND		H95	PCIe_REFCLKIN1-
E96	PCIe_CLKREQ1#		F96	ETH0-3_PRSNT#		G96	ETH0-3_I2C_CLK		H96	PCIe_REFCLKIN1+
E97	PCIe_CLKREQ2#		F97	ETH0-3_PHY_RST#		G97	ETH0-3_I2C_DAT		H97	GND
E98	PCIe_CLKREQ_OUT0#		F98	ETH0_SDP		G98	ETH0-3_PHY_INT#		H98	ETH0-3_MDIO_CLK
E99	PCIe_CLKREQ_OUT1#		F99	ETH1_SDP		G99	ETH0-3_INT#		H99	ETH0-3_MDIO_DAT
E100	PCIe_PERST_IN0#		F100	PCIe_PERST_IN1#		G100	PCIe_WAKE_OUT0#		H100	PCIe_WAKE_OUT1#

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6.5. PCIe x16 Connectors

CN5: PCIe x16 Slot1: Group 1 Lanes 16:31 assigned PCIe Slot

CN6: PCIe x16 Slot2: Group 2 Lanes 32:47 assigned PCIe Slot

CN7: PCIe x16 Slot3: Group 3 Lanes 48:63 assigned PCIe Slot

Pin	Signal	Pin	Signal
B1	+ 12V	A1	PRSNT
B2	+ 12V	A2	+ 12V
B3	+ 12V	A3	+ 12V
B4	GND	A4	GND
B5	SMB_CLK	A5	JTAG
B6	SMB_DAT	A6	JTAG
B7	GND	A7	JTAG
B8	**+3.3V**	A8	JTAG
B9	JTAG	A9	+ 3.3V
B10	+ 3.3VAUX	A10	+ 3.3V
B11	WAKE#	A11	PERST#
B12	RSVD	A12	GND
B13	GND	A13	REFCLK+
B14	PETp0	A14	REFCLK-
B15	PETn0	A15	GND
B16	GND	A16	PERp0
B17	**PRSNT**	A17	PERn0
B18	GND	A18	GND
B19	PETp1	A19	RSVD
B20	PETn1	A20	GND
B21	GND	A21	PERp1

Pin	Signal	Pin	Signal
B22	GND	A22	PERn1
B23	PETp2	A23	GND
B24	PETn2	A24	GND
B25	GND	A25	PERp2
B26	GND	A26	PERn2
B27	PETp3	A27	GND
B28	PETn3	A28	GND
B29	GND	A29	PERp3
B30	RSVD	A30	PERn3
B31	PRSNT	A31	GND
B32	GND	A32	RSVD
B33	PETp4	A33	RSVD
B34	PETn4	A34	GND
B35	GND	A35	PERp4
B36	GND	A36	PERn4
B37	PETp5	A37	GND
B38	PETn5	A38	GND
B39	GND	A39	PERp5
B40	GND	A40	PERn5
B41	PETp6	A41	GND
B42	PETn6	A42	GND

Pin	Signal	Pin	Signal
B43	GND	A43	PERp6
B44	GND	A44	PERn6
B45	PETp7	A45	GND
B46	PETn7	A46	GND
B47	GND	A47	PERp7
B48	PRSNT	A48	PERn7
B49	GND	A49	GND
B50	PETp8	A50	RSVD
B51	PETn8	A51	GND
B52	GND	A52	PERp8
B53	GND	A53	PERn8
B54	PETp9	A54	GND
B55	PETn9	A55	GND
B56	GND	A56	PERp9
B57	GND	A57	PERn9
B58	PETp10	A58	GND
B59	PETn10	A59	GND
B60	GND	A60	PERp10
B61	GND	A61	PERn10
B62	PETp11	A62	GND
B63	PETn11	A63	GND

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Pin	Signal	Pin	Signal
B64	GND	A64	PERp11
B65	GND	A65	PERn11
B66	PETp12	A66	GND
B67	PETn12	A67	GND
B68	GND	A68	PERp12
B69	GND	A69	PERn12
B70	PETp13	A70	GND

Pin	Signal	Pin	Signal
B71	PETn13	A71	GND
B72	GND	A72	PERp13
B73	GND	A73	PERn13
B74	PETp14	A74	GND
B75	PETn14	A75	GND
B76	GND	A76	PERp14
B77	GND	A77	PERn14

Pin	Signal	Pin	Signal
B78	PETp15	A78	GND
B79	PETn15	A79	GND
B80	GND	A80	PERp15
B81	PRSNT	A81	PERn15
B82	RSVD	A82	GND

6.6. PCIe x4 Connector

PCIEA1: PCIe x4 Slot: Group 0 Lanes 0:3 assigned PCIe Slot

PCIEA2: PCIe x4 Slot: Group 0 Lanes 4:7 assigned PCIe Slot

Pin	Signal	Pin	Signal
B1	+12V	A1	PRSNT
B2	+12V	A2	+12V
B3	+12V	A3	+12V
B4	GND	A4	GND
B5	SMB_CLK	A5	JTAG
B6	SMB_DAT	A6	JTAG
B7	GND	A7	JTAG
B8	+3.3V	A8	JTAG
B9	JTAG	A9	+3.3V
B10	+3.3VAUX	A10	+3.3V
B11	WAKE	A11	PERST#

Pin	Signal	Pin	Signal
B12	RSVD	A12	GND
B13	GND	A13	REFCLK+
B14	PETp0	A14	REFCLK-
B15	PETn0	A15	GND
B16	GND	A16	PERp0
B17	PRSNT	A17	PERn0
B18	GND	A18	GND
B19	PETp1	A19	RSVD
B20	PETn1	A20	GND
B21	GND	A21	PERp1
B22	GND	A22	PERn1

Pin	Signal	Pin	Signal
B23	PETp2	A23	GND
B24	PETn2	A24	GND
B25	GND	A25	PERp2
B26	GND	A26	PERn2
B27	PETp3	A27	GND
B28	PETn3	A28	GND
B29	GND	A29	PERp3
B30	RSVD	A30	PERn3
B31	PRSNT	A31	GND
B32	GND	A32	RSVD

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6.7. KEY-M Slot Connector

M2_0: Group 0 Lanes 8-11 assigned M.2 Slot 1

M2_1: Group 0 Lanes 12-15 assigned M.2 Slot 2

Pin	Signal	Pin	Signal
1	CONFIG	2	+3.3V
3	GND	4	+3.3V
5	PERn3	6	N.C
7	PERp3	8	N.C
9	GND	10	DAS/DSS#
11	PETn3	12	+3.3V
13	PETp3	14	+3.3V
15	GND	16	+3.3V
17	PERn2	18	+3.3V
19	PERp2	20	N.C
21	CONFIG	22	N.C
23	PETn2	24	N.C

Pin	Signal	Pin	Signal
25	PETp2	26	N.C
27	GND	28	N.C
29	PERn1	30	N.C
31	PERp1	32	N.C
33	GND	34	N.C
35	PETn1	36	N.C
37	PETp1	38	DEVSLP
39	GND	40	N.C
41	PERn0	42	N.C
43	PERp0	44	N.C
45	GND	46	N.C
47	PETn0	48	N.C

Pin	Signal	Pin	Signal
49	PETp0	50	PETST#
51	GND	52	CLKREQ#
53	REFCLKN	54	PEWAKE#
55	REFCLKP	56	N.C
57	GND	58	N.C
67	N.C	68	SUSCLK
69	CONFIG	70	+3.3V
71	GND	72	+3.3V
73	GND	74	+3.3V
75	CONFIG		

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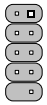
6.8. USB2.0 Ports Header

USB4_5: USB2.0 Port 4 and Port 5 header

USB6_7: USB2.0 Port 6 and Port 7 header

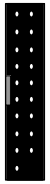
Pin	Signal		
1	+5V	2	+5V
3	U2_USB_R_N	4	U2_USB_R_N
5	U2_USB_R_P	6	U2_USB_R_P
7	GND	8	GND
9	GND	10	NC



6.9. USB3.x Ports Header

FP_USB: USB Front Panel Header

Pin	Signal		
1	TP336	2	USB_DS3_DP_CN
3	USB2_P_CN	4	USB_DS3_DN_CN
5	USB2_N_CN	6	GND
7	GND	8	USB_SSTX5_P_CN
9	USB_SSTX4_P_CN	10	USB_SSTX5_N_CN
11	USB_SSTX4_N_CN	12	GND
13	GND	14	USB_SSRX5_P_CN
15	USB_SSRX4_P_CN	16	USB_SSRX5_N_CN
17	USB_SSRX4_N_CN	18	USB_VBUS
19	+5V		



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6.10. SATA Port

SATA0/SATA1: Serial ATA Port

Pin	Signal
1	GND
2	TX_P
3	TX_N
4	GND
5	RX_P
6	RX_N
7	SATA0_P7

JP_S0/JP_S1: Voltage supply switching for +3.3V or 5V for SATA DOM.

Pin	Status
1-2	+3.3V for SATA
2-3	+5V for SATA
NC	Default

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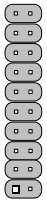
6.11. eSPI Debug Connector

ESPI: for eSPI debugging connection purpose

Pin	Signal	Pin	Signal
1	eSPI_CLK	2	GND
3	eSPI_CS0	4	eSPI_RST
5	RST_DBG_L	6	+5V
7	eSPI_IO_3	8	eSPI_IO_1
9	+ 3.3VSB	10	eSPI_IO_1
11	eSPI_IO_0	12	GND
13	SMB_CK	14	CN_SNB_DAT
15	BIOSRST	16	NC
17	GND	18	eSPI_CS1#
19	eSPI_ALEART0#	20	eSPI_ALEART1#



6.12. BMC Debug Connector

BMC_DBG: UART5 for BMC firmware debugging

Pin	Signal
1	UART_DBG_TXD5
2	GND
3	UART_DBG_RXD5

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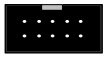
6.13. COM Port Connector

COM1: the Module UART port1

Pin	Signal		
1	CM1_DCD	2	CN1_DSR
3	SER1_RX	4	SER1_RTS_L
5	SER1_TX	6	SER1_CTS_L
7	CM1_DTR	8	CM1_RI
9	GND	10	NC



JP9: MUX of Module UART1 or BMC UART SOL

Jumper	Status
1-2	BMC UART2 SOL <<<<
2-3	Module's UART1

JP34: MUX of Module UART0 or BMC UART1 (Console)

Jumper	Status
1-2	BMC UART1 Console
2-3	Module UART0 <<<<

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6.14. I2C0/1 and SMBus Header

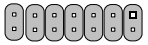
CN23: Module outputs I2C0/1 and SMBus external header

Pin	Signal	Pin	Signal
1	+3.3V	2	+3.3V
3	SMB_CLK	4	I2C0_CLK
5	SMB_DAT	6	I2C0_DAT
7	+3.3V	8	I2C0_ALERT-L
9	I2C1_CLK	10	GND
11	I2C1_DAT	12	GND

6.15. GPIO Header

CN24: Module outputs GPIO Header

Pin	Signal	Pin	Signal
1	+3.3V	2	GPIO_06
3	GPIO_00	4	GPIO_07
5	GPIO_01	6	GPIO_08
7	GPIO_02	8	GPIO_09
9	GPIO_03	10	GPIO_10
11	GPIO_04	12	GPIO_11
13	GPIO_05	14	GND



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6.16. External SMBus Header

CN35: External SMBus for connecting to the MUX of KR/SFI

Pin	Signal
1	GND
2	N.C
3	RT_SDC
4	RT_SDA

6.17. Fan Header

FAN_0: Module controlled FAN

Pin	Signal
1	GND
2	+12V_5V_FAN
3	SENSE_FAN
4	PWMOUT_FAN

FAN_1: BMC controlled FAN 1

Pin	Signal
1	GND
2	+12V_5V_FAN0
3	SENSE_FAN0
4	PWMOUT_FAN0

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FAN_2: BMC controlled FAN 2

Pin	Signal
1	GND
2	+12V_5V_FAN1
3	SENSE_FAN1
4	PWMOUT_FAN1

FAN_4: BMC controlled FAN 4

Pin	Signal
1	GND
2	+12V_5V_FAN3
3	SENSE_FAN3
4	PWMOUT_FAN3

FAN_5: BMC controlled FAN 5

Pin	Signal
1	GND
2	+12V_5V_FAN4
3	SENSE_FAN4
4	PWMOUT_FAN4

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6.18. General Purpose SPI Header

GP_SPI: General Purpose SPI connector for widely used interfaces

Pin	Signal	Pin	Signal
1	+3.3V	2	NC
3	GP_SPI_CLK	4	GP_SPI_MOSI
5	GP_SPI_CS2	6	GP_SPI_MISO
7	GP_SPI_CS3	8	GP_SPI_CS0
9	GP_SPI_ALT	10	GP_SPI_CS1
11	NC	12	GND

6.19. IPMI Header

IPMI: Intelligent Platform Management Bus for platform management functions

Pin	Signal
1	+3.3V
2	IPMB_DAT
3	IPMB_CLK
4	GND

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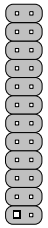
6.20. Front Panel Control

FRONT_PANEL: Power Button, Reset Button, HDD LED, Power LED for front panel header

Pin	Signal	Pin	Signal
23	LAN2_LED_N	24	NMI_SW
21	LAN2_LED_P	22	GND
19	CASE_OPEN_N	20	R_UID_BUT_P
17	SENSOR_SCL	18	GND
15	SENSOR_SDA	16	RST_BUT_P
13	LAN1_LED_N	14	GND
11	LAN1_LED_P	12	PWR_BUT_P
9	SLED_R	10	HDD_LED_N
7	SLED_G	8	HDD_LED_P
5	UID_LED_P	6	PWR_LED_N
3	UID_LED_N	4	FAN_FAIL_LED_N
1	5VSB	2	PWR_LED_P



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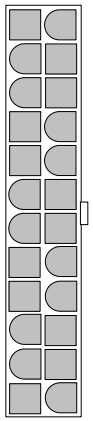
6.21. Power Connectors

ATX_24: ATX 24-pin Power Connector

Connect the ATX 24-pin (or 20-pin) connector to supply power to COM-HPC Server Base carrier.

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	GND	15	COM
4	+5V	16	PWR_ON
5	GND	17	COM
6	+5V	18	COM
7	GND	19	COM
8	PWR_GOOD	20	-5V
9	+5VSB	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	COM



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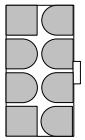
ATX_8: ATX 12V 8-pin Connector.

Connect the ATX 12V 8-pin connector

to supply power to the COM-HPC Server module.

Pin	Signal
1	GND
2	GND
3	GND
4	GND
5	+12V
6	+12V
7	+12V
8	+12V



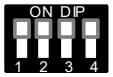
6.22. Carrier EEPROM Address Switch

SW1: COM-HPC Carrier Board EEPROM address setting

Default Address: **AEh**

1	0	1	0	**A2**	**A1**	**A0**	R/W
MSB							**LSB**

SW1	I2C EEPROM_U53
1-8	**A2**_OFF
2-7	**A1**_OFF
3-6	**A0**_OFF



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6.23. Module (I2C0) / BMC (I2C8) Jumpers

JP2: I2C CLK switch for I2C8 (BMC) or I2C0 (module)

Jumper	Status
1-2	I2C8, BMC
2-3	I2C0, Module

JP3: I2C DAT switch for I2C8 (BMC) or I2C0 (module)

Jumper	Status
1-2	I2C8, BMC
2-3	I2C0, Module

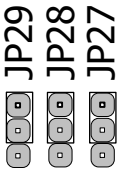
6.24. Other Jumpers

JP27/28/29: BIOS Selection.

Boot from SPI Secondary BIOS, see below for details.

Setting Boot from Module BIOS

JP29	JP28	JP27	BOOT
1-2	1-2	1-2	Module BIOS <<<<



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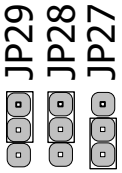
Setting Boot from Carrier BIOS

JP29	JP28	JP27	BOOT
1-2	1-2	2-3	Carrier BIOS <<<<



JP30: Clear CMOS

To clear CMOS, shut down the power and short pins 2 and 3 (short VBT to ground)

Jumper	Status
1-2	Normal <<<<
2-3	Clear CMOS

6.25. Power Jumpers

JP31: AT/ATX Mode

In AT mode, put PS_ON# to ground as short pin 2-3 to force power on.

Jumper	Status
1-2	ATX Mode
2-3	AT Mode <<<<

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JP32: ATX S3 signal switching

In AT mode, put pin 2-3 for S5 output instead Power Button (S3)

Jumper	Status
1-2	ATX (SUS_S3#) <<<<
2-3	AT (SUS_S5#)

JP33: VCC_12V On/Off during S3/S5

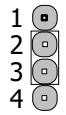
In AT mode, put pin 2-3 to output 12V during S3/S5.

Jumper	Status
1-2	ATX Mode
2-3	AT Mode <<<<

JP35: +5V_SBY supply

In AT mode, put pin 3-4 to output +5V_SBY directly.

Jumper	Status
2-3	ATX PSU <<<<
3-4	AT (DC to DC)



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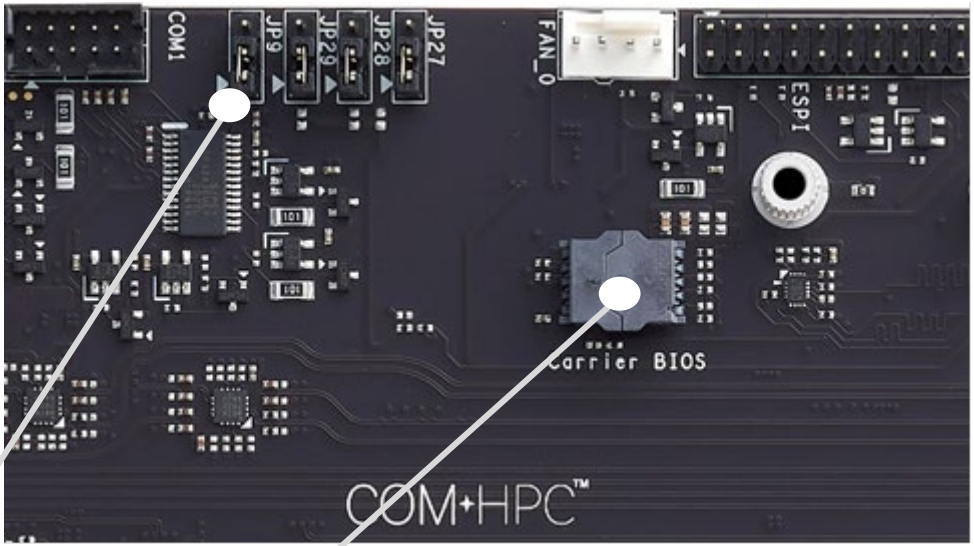
7. Secondary BIOS

The COM-HPC Server-Base supports Secondary BIOS, using Boot Serial Peripheral Interface (SPI) for COM-HPC modules.

Secondary BIOS solutions can be used as an alternative to the on-module BIOS and provide support for the following:

- Testing new BIOS versions
- Development of firmware modifications
- Recovery if soldered BIOS on module is corrupted



To use the BIOS on the module;
short pins 1-2 on **JP27, JP28, JP29**, reference *section 6.23*

To use the BIOS on the carrier board;
Short pins 2-3 on **JP27**, and keep pin 1-2 on JP28, JP29, reference *section 6.23*

Make sure that the **secondary BIOS flash chip** has been properly installed into the Carrier BIOS socket before BOOT BIOS adjusting.

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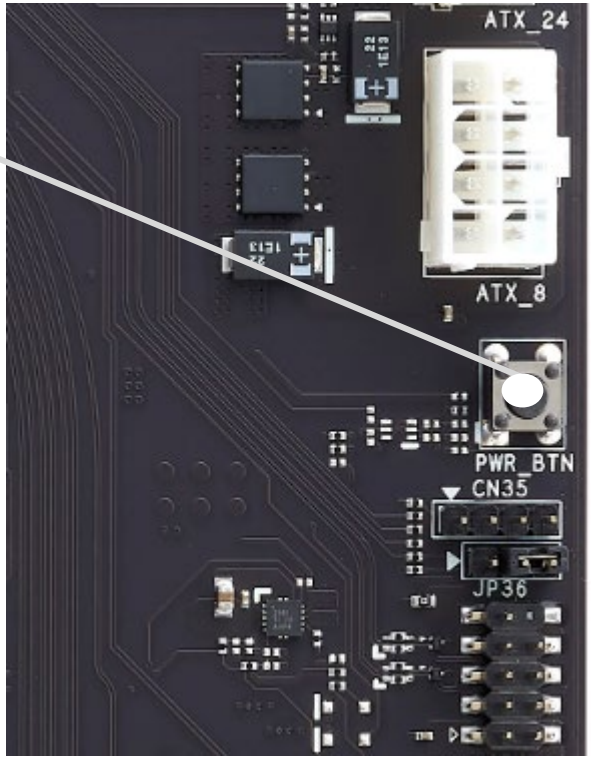
8. Switches, POST and LEDs

8.1. Switches (S0-S5)

There are two switches, at the center and lower-right of the carrier.

PWR_BTN
Indicates getting into S0 from S5 of the system.



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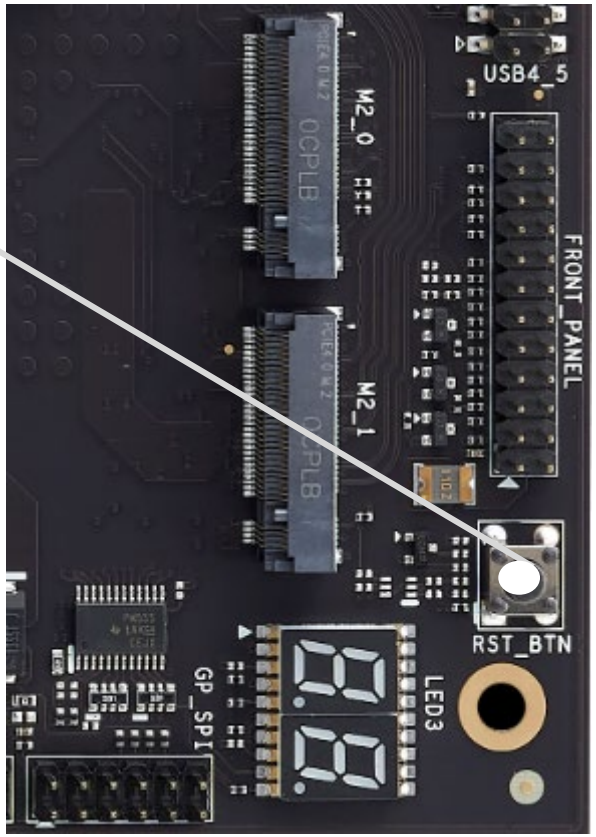
RST_BTN

Indicates resetting of the system.



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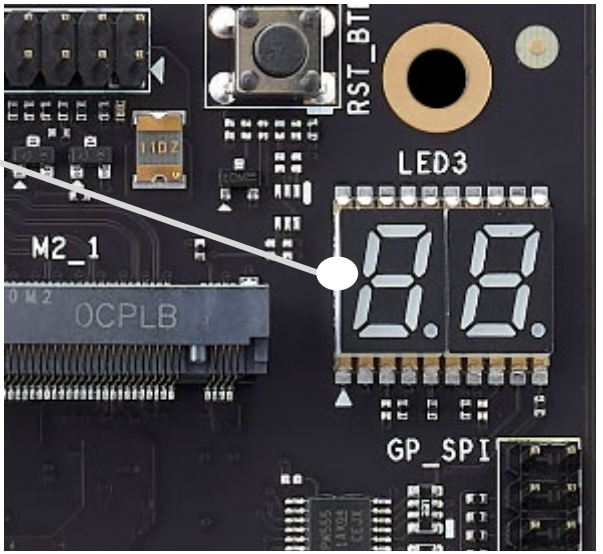
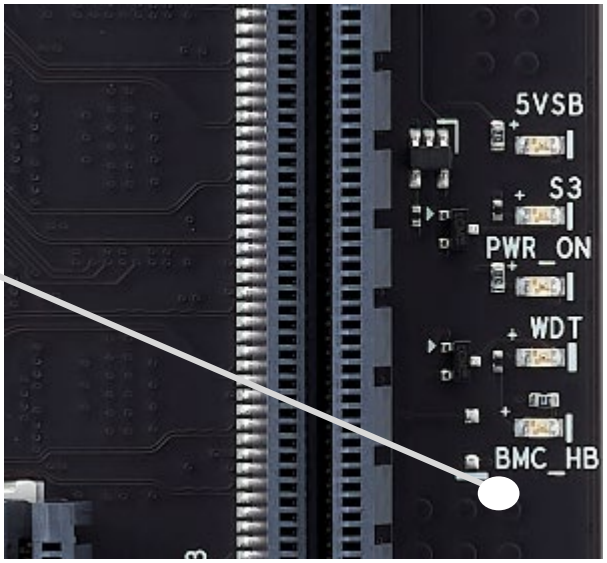
8.2. POST and inductors LEDs

An eSPI-based POST display is added for debugging.
The two 7-SEG LEDs shows the actual **POST data.**



A row of mini-LEDs below the POST display indicates the following:

5VSB: ATX power attached on standby or active
S3: Indicates S3 status
PWR_ON: Indicates power on
WDT: Indicates WDT (watchdog timer) activity
BMC_HB: Heart beat LED indicator output



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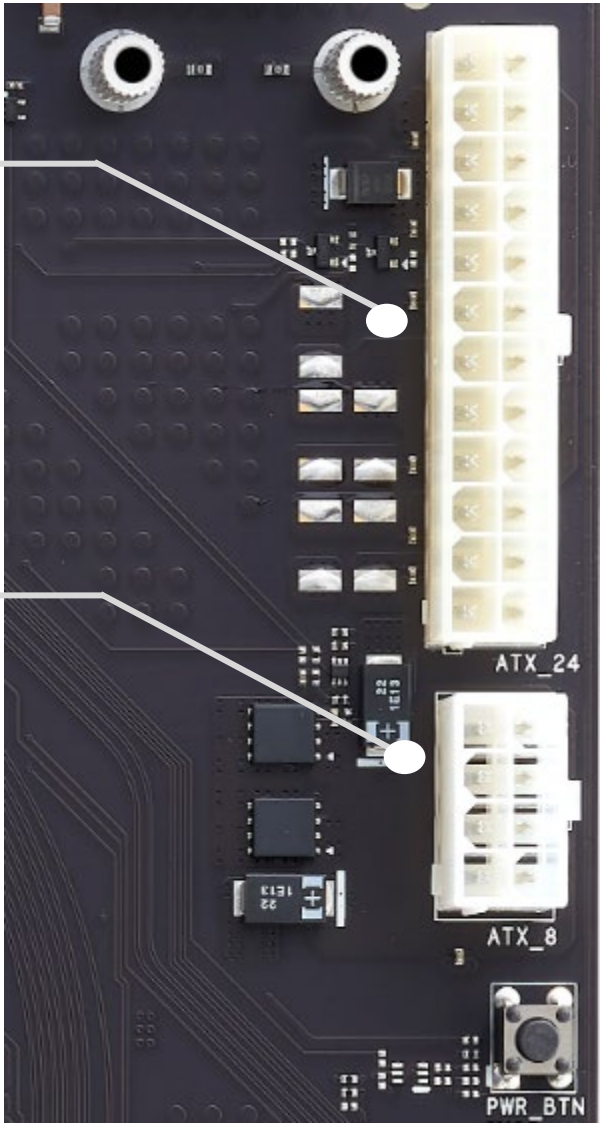
8.3. ATX Power Connectors

The COM-HPC Server Base has one **ATX 24-pin connector** to supply power to the carrier board and one **ATX 12V 8-pin connector** to supply power to the COM-HPC module.



The system will not power on unless an ATX 12V 8-pin connector is connected.

If your power supply has a 24-pin ATX connector, then attach the connectors as shown.

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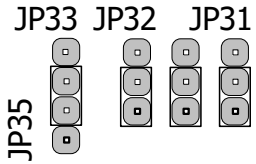
8.4. AT Power Mode

To operate the system in AT Mode with an ATX power supply,
Refer to *section 6.24* jumper settings for details, or follow the instruction below.

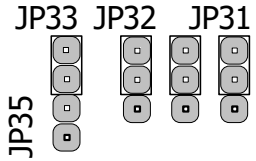
Jumper Settings for **ATX mode**

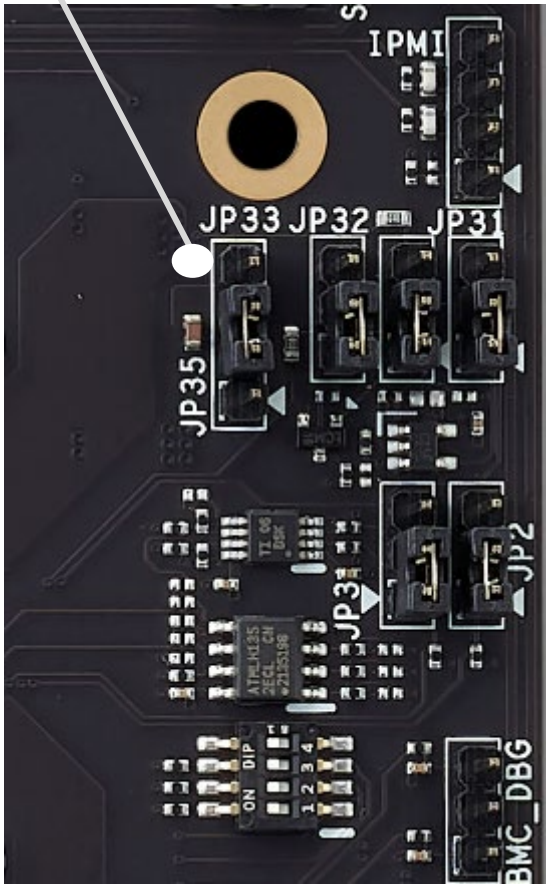
JP31	JP32	JP33	JP35	POWER MODE
1-2	1-2	1-2	2-3	ATX Mode



Jumper Settings for **AT mode**

JP31	JP32	JP33	JP35	POWER MODE
2-3	2-3	2-3	3-4	AT Mode





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