cPCI-6920 Series

Dual Quad-Core Intel® Xeon® Processors
6U Compact PCI Processor Blade with XMC Site

User's Manual

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Revision History

Revision	Release Date	Description of Change(s)
2.00	2008/10/27	Initial Release
2.01	2009/07/16	Correct specifications (RAID support, RTM COM pinouts, SATA connector pinouts, J5 pinouts), BIOS corrections, COM port routing.
2.02	2010/06/18	Update SATA RAID support, RTM support (cPCI-R6000), default CMOS battery; correct GbE, J1, J3 pin assignments; update IPMI User Guide.

Preface

Disclaimer

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Using this Manual

Audience and Scope

The cPCI-6920 User's Manual is intended for hardware technicians and systems operators with knowledge of installing, configuring and operating industrial grade computer systems.

Manual Organization

This manual is organized as follows:

Chapter 1, Introduction: Introduces the cPCI-6920, its features, block diagrams, and package contents.

Chapter 2, Specifications: Presents detailed specification information.

Chapter 3, Functional Description: Describes the cPCI-6920 main functions.

Chapter 4, Board Interfaces: Describes the cPCI-6920 board interfaces.

Chapter 5, Getting Started: Describes the installation of components to the cPCI-6920 and rear transition modules.

Chapter 6, Driver Installation: Provides information on how to install the cPCI-6920 device drivers.

Chapter 7, Utilities: Describes the utilities of the cPCI-6920 Series.

Chapter 8, BIOS Setup: Describes basic navigation for the AMIBIOS®8 BIOS setup utility.

Chapter 9, IPMI User Guide: Provides relevant information for the baseboard management controller (BMC) of the Intelligent Platform Management Interface (IPMI).

Important Safety Instructions: Presents safety instructions all users must follow for the proper setup, installation and usage of equipment and/or software.

Getting Service: Contact information for ADLINK's worldwide offices.

Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.


NOTE:

Additional information, aids, and tips that help users perform tasks.


CAUTION:

Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.


WARNING:

Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

1.1 Overview

The cPCI-6920 Series is a 6U CompactPCI single board computer in single slot (4HP) or dual slot (8HP) width form factor featuring server class chipset and low voltage Quad-Core/Dual-Core Intel® Xeon® processor(s) with high-performance 1066MHz front-side bus (FSB). The single slot version provides one CPU socket which can be equipped with one Quad-Core Intel Xeon (L5408) or one Dual-Core Intel Xeon (LV 5138) processor, and provides two SO-RDIMM sockets for up to 8GB memory capacity. The dual slot version provides two CPU sockets which can be equipped with two Quad-Core Intel Xeon (L5408) or two Dual-Core Intel Xeon (LV 5138) processors, and provides four SO-RDIMM sockets for up to 16GB memory capacity. The cPCI-6920 Series implements the server class Intel® 5100 Memory Controller Hub and ICH9R I/O Hub for optimal performance.

The cPCI-6920 Series supports a 64bit/66MHz CompactPCI bus, one PMC site with 64-bit/66MHz PCI bus or PCI-Express x8 XMC, four PCI-Express® Gigabit Ethernet ports (two on front panel, two for PICMG 2.16), a CompactFlash socket and onboard 4GB USB NAND flash for solid-state storage, optional onboard 2.5” SATA HDD, and SCSI RAID 1 support via the Rear Transition Module (RTM). For flexibility of use, the cPCI-6920 Series can be installed in a standard CompactPCI system slot as system master, or peripheral slot as stand-alone server blade without CompactPCI bus communication. The cPCI-6920 Series is ideally suited for datacom, telecom and military applications.

1.2 Features

- 6U CompactPCI SBC in 4HP or 8HP width form factor
- Single/Dual Quad-Core Intel® Xeon processor(s) 2.13GHz, 12MB L2 cache
- Front Side Bus 1066MHz
- Server class Intel® 5100 Memory Controller Hub and ICH9R I/O Hub
- Dual Channel DDR2 registered and ECC SDRAM at 667MHz
- Two/four SO-RDIMM sockets for maximum up to 16GB memory
- 64bit/66MHz CompactPCI Interface based on PCI specifications
- Supports operation in system slot as system master or in peripheral slot as stand-alone server blade without connectivity to CompactPCI bus
- One PMC site with 64-bit/66MHz PCI bus or PCI-Express x8 XMC
- Four PCI-Express® Gigabit Ethernet ports, two at front, two for PICMG2.16
- One CompactFlash socket and onboard 4GB USB NAND flash for storage option
- Optional 2.5” SATA HDD onboard by DB-SATA adapter kit
- SCSI hardware RAID 1 support at RTM
- SATA software RAID 0/1/5/10 support

1.3 Block Diagram

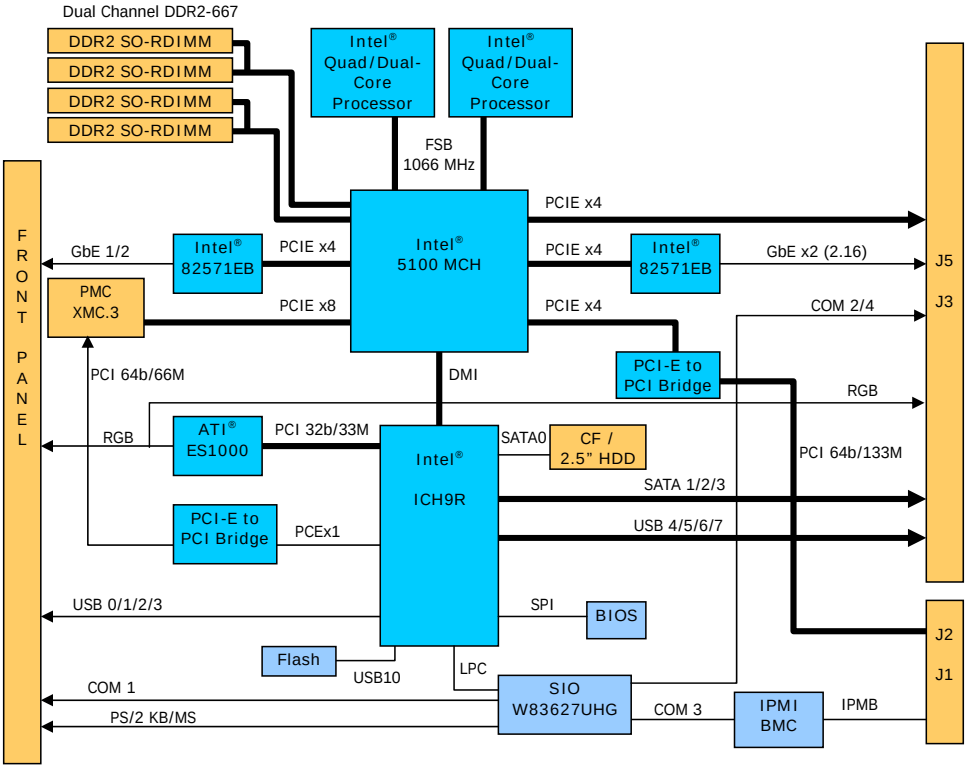

Figure 1-1: cPCI-6920 Series Functional Block Diagram

1.4 Product List

Products included in the cPCI-6920 Series include:

SBC

- cPCI-6920: 4HP (single-slot) width 6U CompactPCI featuring single Dual or Quad-Core Intel® Xeon processor; 1GB, 2GB or 4GB memory by SO-RDIMM; 4GB USB NAND flash on board; removable CompactFlash socket (DB-6920CF), 2xUSB, 2xGbE, VGA
- cPCI-6920D: 8HP (dual-slot) width 6U CompactPCI featuring single/dual Dual or Quad-Core Intel® Xeon processor(s); 1GB, 2GB, 4GB, 8GB memory on SO-RDIMM; 4GB USB NAND flash onboard, removable CompactFlash socket (DB-6920CF), 2x USB, 2x GbE, VGA. The DB-6920L2 adapter provides a PMC/XMC site, 2x USB, COM, KB/MS

Rear Transition Module

- cPCI-R6000: 4HP width Rear Transition Module for CPCI-6920 SBCs with VGA, 2x COM, 3x USB, 2x GbE, SCSI, 2x SATA, Floppy
- cPCI-R6000D: 8HP width Rear Transition Module for CPCI-6920 SBCs with VGA, 2x COM, 3x USB, 2x GbE, SCSI, 2x SATA, Floppy. The DB-R6000L2 adapter is assembled to provide 2x USB, KB/MS, Mic-in, Line-out and removable SATA direct connector (DB-6920SAT) for 2.5” SATA HDD direct connection.

Adapter Kits

- DB-SATA: includes DB-6920SAT adapter board and screws for 2.5” SATA hard drive installation
- DB-CF-SA: includes DB-6920CF adapter board and screws for CompactFlash card

1.5 Package Contents

The cPCI-6920 is packaged with the following components. If any of the items on the contents list are missing or damaged, retain the shipping carton and packing material and contact the dealer for inspection. Please obtain authorization before returning any product to ADLINK. The packing contents of the cPCI-6920 Series are non-standard configurations and may vary depending on customer requests.

CPU module

- cPCI-6920 Series CPU Module
  - CPU, RAM specifications will differ depending on options selected
  - Thermal module is assembled on the board
  - DB-6920CF adapter board is assembled on the board
- Y-cable for PS/2 combo port (8HP version only)
- DB-SATA kit (DB-6920SAT adapter board, screws, standoffs)
- ADLINK All-in-One CD
- User's manual

Rear Transition Module

- The cPCI-R6000 series
- The DB-SATA kit (8HP version only)
- 2.5" HDD bracket (8HP version only)
- Y-cable for PS/2 combo port (8HP version only)
- DVI to VGA (DB-15) adapter
- Ultra-320 SCSI cable

Adapter Kits

- DB-CF-SA kit
  - DB-6920CF adapter board
  - Screw and standoff accessory pack
  - CF card guide

NOTE:

The contents of non-standard cPCI-6920 configurations may vary depending on the customer’s requirements.

CAUTION:

This product must be protected from static discharge and physical shock. Never remove any of the components except at a static-free workstation. Use the anti-static bag shipped with the product when putting the board on a surface. Wear an anti-static wrist strap properly grounded on one of the system's ESD ground jacks when installing or servicing system components.

2 Specifications

2.1 cPCI-6920 SBC Specifications

CompactPCI® Standards	• PICMG® 2.0 CompactPCI® Rev. 3.0 • PICMG® 2.1 Hot Swap Specification Rev.2.0 • PICMG® 2.9 System Management Bus Rev. 1.0 • PCIMG® 2.16 Packet Switching Backplane Rev.1.0
Mechanical	• Standard 6U CompactPCI® • Board size: 233.35mm x 160mm • Single slot (4HP, 20.32mm); Dual slot (8HP, 40.64mm) width • CompactPCI® connectors with J1, J2, J3 and J5
Processor	• FC-LGA771 Quad-Core Intel® Xeon Processor L5408 2.13GHz in 45nm process technology, 12MB on die L2 cache • FC-LGA771 Dual-Core Intel® Xeon Processor LV 5138 2.13GHz in 65nm process technology, 4MB on die L2 cache • Passive heatsink • 4HP cPCI-6920 series support single processor • 8HP cPCI-6920D series support up to dual processors
Chipset	• Intel 5100 Memory Controller Hub (MCH) • Intel ICH9R I/O Controller Hub (ICH)
FSB	• 1066 MHz
Host Memory	• Dual channel DDR2-667 Registered ECC memory • Two SO-RDIMM sockets for 4HP version; four SO-RDIMM sockets for 8HP version • Maximum up to 16GB capacity
CompactPCI Bus	• PCI 64bit/ 66MHz; V(I/O) 3.3V only • Supports operation in system slot as system master or in peripheral slot as stand-alone server blade without connectivity to CompactPCI bus
PMC/XMC	• One PCI 64bit/ 66MHz PMC or PCI-Express x8 XMC site
Gigabit Ethernet	• Two PCI-Express® x4 Intel® 82571EB dual port Gigabit Ethernet controllers • Two 10/100/1000BASE-T egress ports • Two 10/100/1000BASE-T PICMG 2.16 ports (can be routed to optional cPCI-R6000(D) RTM)
Graphics	• ATI ES1000 graphics controller with 2D accelerator • DDR2-533 64MB graphics memory • DB-15 front panel VGA port • Analog RGB up to 32bit 1600x1200@60Hz refresh rate

Serial Port	• One 16C550 compatible DB-9 RS-232 port from Super IO W83627UHG
Storage Interface[1]	• USB NAND Flash 4GB onboard • CompactFlash Type II socket onboard[1] • Optional 2.5” SATA HDD direct connector onboard
BIOS	• AMI Workstation BIOS, SPI flash memory
IPMI Interface	• Supports PICMG® 2.9 secondary system management bus • Implements IPMI functions defined by IPMI Specification v1.5 • ATmega128L-8AU Baseboard Management Controller(BMC) with 128KB programmable in-System Flash, 4KB EEPROM, and 4KB internal SDRAM
Faceplate I/O	**4HP (cPCI-6920):** • 2x USB2.0 ports • 2x 10/100/1000BAST-T Ethernet ports • Analog DB-15 VGA port **8HP (cPCI-6920D):** • 4x USB2.0 ports • 2x 10/100/1000BASE-T Ethernet ports • Analog DB-15 VGA port • DB-9 RS-232 port • PS/2 Keyboard/ Mouse Combo port • PMC/XMC slot
Onboard Peripherals	• CompactFlash socket (optional Serial ATA connector)[1] • USB NAND Flash 4GB
OS Compatibility	• Microsoft Windows XP Professional SP2 • Microsoft Windows Server 2003 • Fedora Core 8 • Other OS support upon request
Environmental	• Operating Temperature[2, 3]: 0 to 55°C with forced air flow • Storage Temperature: -40°C to 85°C • Humidity: 20% to 90%@60°C non-condensing • Shock: 15G peak-to-peak, 11ms duration, non-operating • Vibration[4]: Operating 1.88Grms, 5-500Hz, each axis w/o hard drive.
EMI	• CE EN55022 • FCC Class A

Notes:

1. The CompactFlash socket comes with a removable adapter design (DB-6920CF) and can be replaced with a SATA HDD connector adapter (DB-6920SAT) to directly connect a 2.5” SATA HDD. The 2.5” hard drive space is reserved. The CompactFlash and SATA HDD cannot be installed simultaneously.
2. ADLINK-certified thermal design. The thermal performance is dependent on the chassis cooling design. Forced airflow with 30CFM is required. Temperature limit of optional mass storage devices may affect the thermal specification.
3. The system can be operated in an environment with ambient temperature between 50°C and 55°C, but not exceeding 96 hours per instance, 360 hours per year, and a maximum o.f 15 instances per year
4. The hard drive limits the operational vibration. When application requires higher specification for anti-vibration, it is recommended to use a flash disk or onboard USB NAND flash.

2.2 cPCI-R6000 RTM Specifications

Mechanical	• Standard 6U CompactPCI® rear I/O • Board size: 233.35mm x 80mm • Single slot (4HP, 20.32mm); Dual slot (8HP, 40.64mm) width • CompactPCI® connectors with rJ3 and rJ5
Faceplate I/O	4HP (cPCI-R6000): • 2x USB2.0 ports • 2x 10/100/1000BASE-T Ethernet ports • DVI-I port (Analog signal only) • DB-15 serial port • External 68-pin SCSI socket 8HP (cPCI-R6000D): • 4x USB2.0 ports • 2x 10/100/1000BAST-T Ethernet ports • DVI-I port (Analog signal only) • DB-15 serial port • External 68-pin SCSI socket • PS/2 Keyboard Mouse port • Mic-in, Line-out ports
Onboard Peripherals	4HP (cPCI-R6000): • USB 2.0 5-pin header • RS-232 10-pin header (Tx, Rx signals only) • Internal 68-pin SCSI socket • Floppy connector • 2x 7-pin Serial ATA connectors 8HP (cPCI-R6000D): • USB 2.0 5-pin header • RS-232 10-pin header (Tx, Rx signals only) • Internal 68-pin SCSI socket • Floppy connector • 2x 7-pin Serial ATA connectors • Serial ATA direct connector[1] (opt. CompactFlash socket)[1]
SCSI	• LSI® Logic LSI53C1020 PCI-X Ultra320 SCSI Controller on PCI-X 64-bit/133MHz bus • 320MB per second data transfer rate • Supports RAID 1 (mirroring)

Notes:

1. The Serial ATA connector comes in a removable adapter design (DB-6920SAT) and can be replaced with the CompactFlash socket adapter (DB-6920CF). The CompactFlash and SATA HDD share the same space and cannot be installed simultaneously.

2.3 I/O Connectivity Table

	cPCI-6920 (4HP)		cPCI-6920D (8HP)	
	Faceplate	**Onboard**	**Faceplate**	**Onboard**
Gigabit Ethernet	Y x2		Y x2	
COM 1			Y (DB-9)	
COM 2				
COM 4				
USB 2.0	Y x2		Y x4	
PMC/XMC			Y	
VGA	Y		Y	
Serial ATA		Optional(1)		Optional(1)
Compact Flash		Y		Y
PS/2 KB/MS			Y	
USB Flash		Y		Y
SCSI				
GP LED	Y x4		Y x4	
Reset Button	Y		Y	

Notes:

1. Optional SATA HDD adapter kit (DB-SATA) for 2.5” SATA HDD onboard mounting (2.5”HDD and CF share the same space and cannot be installed simultaneously).

	cPCI-R6000 (4HP)		cPCI-R6000D (8HP)	
	Faceplate	**Onboard**	**Faceplate**	**Onboard**
Gigabit Ethernet	Y x2 (2.16)		Y x2 (2.16)	
COM 1				
COM 2	Y (DB-9)		Y (DB-9)	
COM 4		Y (10-pin)		Y (10-pin)
USB 2.0	Y x2	Y (5-pin)	Y x4	Y (5-pin)
PMC/XMC				
VGA	Y		Y	
Serial ATA		Y x2 (7-pin)		Y x3[2]
Compact Flash				Optional[3]
PS/2 KB/MS			Y	
USB Flash				
SCSI	Y	Y	Y	Y
Floppy		Y		Y
Audio			Y	
GP LED				
Reset Button				

Notes:

2. Two 7-pin SATA connectors for external HDDs and one connector for onboard 2.5” SATA HDD.
3. Optional CF socket adapter kit (DB-CF-SA) for additional CF socket (CF and 2.5” HDD share the same space and cannot be installed simultaneously).

2.4 Power Requirements

In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. **An industrial power supply unit should be able to provide at least twice as much power as the entire system requires of each voltage**. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires of each voltage.

The tolerance of the voltage lines described in the CompactPCI specification (PICMG 2.0 R3.0) is +5%/-3% for 5, 3.3 V and ±5% for ±12V. This specification is for power delivered to each slot and it includes both the power supply and the backplane tolerance.

Voltage	Nominal Value	Tolerance	Max. Ripple (P - P)
5V	+5.0 VDC	+5% / -3%	50 mV
3.3V	+3.3 VDC	+5% / -3%	50 mV
+12V	+12 VDC	+5% / -5%	240 mV
-12V	-12 VDC	+5% / -5%	240 mV
V I/O (PCI I/O Buffer Voltage)	+3.3 VDC or +5 VDC	+5% / -3%	50 mV
GND			

Power Consumption

This section provides information on the power consumption of cPCI-6920 Series when using 1x/2x Dual-Core Intel® Xeon® LV 5138 or 1x/2x Quad-Core Intel® Xeon® L5408 processor(s) with 4x 2GB SO-RDIMM and onboard 60GB SATA hard drive. The systems were tested in Idle Mode and Full Loading Mode under Windows XP.

1x Dual-Core LV 5138			
Windows® XP, Idle			
Power requirement	+3.3V	+5V	Total
Current (A)	9.13	4.46	
Watts (W)	30.13	22.30	52.43
Windows® XP, CPU 100% Usage			
Power requirement	+3.3V	+5V	Total
Current (A)	14.63	9.74	
Watts (W)	40.30	48.70	92.00

2x Dual-Core LV 5138			
Windows® XP, Idle			
Power requirement	+3.3V	+5V	Total
Current (A)	10.84	4.67	
Watts (W)	35.77	23.35	59.12
Windows® XP, CPU 100% Usage			
Power requirement	+3.3V	+5V	Total
Current (A)	14.14	16.93	
Watts (W)	46.66	84.65	131.31

1x Quad-Core L5408			
Windows® XP, Idle			
Power requirement	+3.3V	+5V	Total
Current (A)	10.69	2.54	
Watts (W)	35.28	12.70	47.98
Windows® XP, CPU 100% Usage			
Power requirement	+3.3V	+5V	Total
Current (A)	11.94	13.93	
Watts (W)	39.40	69.65	109.05

2x Quad-Core L5408			
Windows® XP, Idle			
Power requirement	+3.3V	+5V	Total
Current (A)	11.06	3.00	
Watts (W)	36.50	15.00	51.50
Windows® XP, CPU 100% Usage			
Power requirement	+3.3V	+5V	Total
Current (A)	13.23	17.63	
Watts (W)	43.66	88.15	131.81

3 Functional Description

The following sections describe the cPCI-6920 Series features and functions.

3.1 Processors

The 4HP cPCI-6920 supports a single processor and the 8HP cPCI-6920D supports dual processors in the FC-LGA771 package. The following table lists the processors supported by the cPCI-6920 Series and their power ratings.

Features	Quad-Core Intel® Xeon® Processor L5408	Dual-Core Intel® Xeon® Processor LV 5138
Clock	2.13GHz	2.13GHz
L2 cache	12MB	4MB
FSB	1066MHz	1066MHz
Maximum Power (TDP[1])	40W	35W
Nominal T_{CASE_MAX}	72°C	70.8°C
Short-Term T_{CASE_MAX} [2]	87°C	85.8°C

Notes:

1. The highest expected sustainable power while running known power intensive applications. TDP is not the maximum power that the processor can dissipate.
2. The Short-Term Thermal Profile may only be used for short-term excursions to higher ambient operating temperatures, not to exceed 96 hours per instance, 360 hours per year, and a maximum of 15 instances per year, as compliant with NEBS Level 3.

Quad-Core Intel® L5408 Processor

The Quad-Core Intel® Xeon® Processor L5408 is a low power, low voltage, server-class processor utilizing four 45-nm Hi-k next generation Intel® Core™ microarchitecture cores. The processor is manufactured on Intel's 45 nanometer process technology combining high performance with the power efficiencies of a low-power microarchitecture. Some key features include on-die, primary 32-kB instruction cache and 32-kB write-back data cache in each core and 12 MB (2 x 6MB) Level 2 cache with Intel® Advanced Smart Cache Architecture. The processors' Data Prefetch Logic speculatively fetches data to the L2 cache before an L1 cache requests occurs, resulting in reduced effective bus latency and improved performance. The 1066 MHz Front Side Bus (FSB) is a quad-pumped bus running off a 266 MHz system clock making 8.5 GBytes per second data transfer rates possible.

Enhanced thermal and power management capabilities are implemented including Intel® Thermal Monitor (TM1), Thermal Monitor 2 (TM2) and Enhanced Intel SpeedStep® Technology. These technologies are targeted for dual processor configurations in enterprise environments. TM1 and TM2 provide efficient and effective cooling in high temperature situations. Enhanced Intel SpeedStep Technology provides power management capabilities to servers and workstations.

Additional features of the Quad-Core Intel® Xeon® Processor L5408 include Intel® Wide Dynamic Execution, enhanced floating point and multi-media units, Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3), and Streaming SIMD Extensions 4.1 (SSE4.1). Advanced Dynamic Execution improves speculative execution and branch prediction internal to the processor. The floating point and multi-media units include 128-bit wide registers and a separate register for data movement. SSE3 instructions provide highly efficient double-precision floating point, SIMD integer, and memory management operations.

The Quad-Core Intel® Xeon® Processor L5408 supports Intel® 64 Architecture as an enhancement to Intel's IA-32 architecture. This enhancement allows the processor to execute operating systems and applications written to take advantage of the 64-bit extension technology.

Dual-Core Intel® LV 5138 Processor

The Dual-Core Intel® Xeon® Processor LV 5138 is a 64-bit server-class processor utilizing two Intel microarchitecture cores. These processors are based on Intel's 65 nanometer process technology combining high performance with the power efficiencies of a low-power microarchitecture. Some key features include on-die, 32 KB Level 1 instruction and data caches and 4 MB Level 2 cache with Advanced Transfer Cache Architecture. The processors' Data Prefetch Logic speculatively fetches data to the L2 cache before an L1 cache requests occurs, resulting in reduced bus cycle penalties and improved performance. The 1066 MHz Front Side Bus (FSB) is a quad-pumped bus running off a 266 MHz system clock making 8.5 GBytes per second data transfer rates possible.

Enhanced thermal and power management capabilities are implemented including Thermal Monitor (TM1), Thermal Monitor 2 (TM2) and Enhanced Intel SpeedStep® Technology. These technologies are targeted for dual processor in enterprise environments. TM1 and TM2 provide efficient and effective cooling in high temperature situations. Enhanced Intel SpeedStep® Technology provides power management capabilities to servers and workstations.

Additional features of the Dual-Core Intel® Xeon® Processor LV 5138 include Advanced Dynamic Execution, enhanced floating point and multi-media units, Streaming SIMD Extensions 2 (SSE2) and Streaming SIMD Extensions 3 (SSE3). Advanced Dynamic Execution improves speculative execution and branch prediction internal to the processor. The floating point and multi-media units include 128-bit wide registers and a separate register for data movement. SSE3 instructions provide highly efficient double-precision floating point, SIMD integer, and memory management operations. The Dual-Core Intel® Xeon® Processor LV 5138 also supports Intel® Extended Memory 64 Technology (Intel® EM64T) as an enhancement to Intel's IA-32 architecture. This enhancement allows the processor to execute operating systems and applications written to take advantage of the 64-bit extension technology.

3.2 Chipset

The cPCI-6920 Series incorporates the Intel® 5100 Memory Controller Hub (MCH) and I/O Controller Hub (ICH9R).

Intel® 5100 Memory Controller Hub

The Intel® 5100 Memory Controller Hub Chipset is designed for systems based on the Dual-Core Intel® Xeon® processor 5100 series and Quad-Core Intel® Xeon® processor 5400 series and supports FSB operation of 1066 MT/s. The Intel® 5100 MCH provides two FSB processor interfaces, two DDR2 memory channels, six x4 PCI Express bus interfaces configurable to form x4, x8 or x16 ports, an Enterprise South Bridge Interface (ESI), and three SMBus interfaces for system management, PCI Hot Plug* control and DIMM Serial Presence Detect (SPD). The Intel® 5100 Memory Controller Hub Chipset device has DMA Engine (Crystal Beach [CB]) capabilities and supports Intel® I/O Acceleration Technology (Intel® I/OAT).

Intel® I/O Controller Hub 9R

The ICH9R is an I/O controller hub supporting various I/O interfaces including six PCI Express x1 ports, Serial ATA host controllers supporting up to six SATA ports at a speed of 3 Gb/s, twelve external USB 2.0 ports with port disable capability, a System Management Bus interface (SMBus), a Serial Peripheral Interface (SPI) and a Low Pin Count bus (LPC) for BIOS and firmware storage. Additionally, the ICH9R contains a PCI Controller supporting up to four Bus Masters (PCI Local Bus Specification, Rev. 2.3 compliant), an integrated 10/100/1000 LAN controller and a dedicated ESI port for communication with the MCH.

The ICH9R component provides the data buffering and arbitration required to ensure that system interfaces operate efficiently and provide the bandwidth necessary to enable the system to obtain peak performance. The ICH9R component is ACPI compliant Suspend to RAM, Suspend to Disk, and Soft-Off power management states. Through the use of the integrated LAN functions, the ICH9R also supports Alert Standard Format for remote management. **Figure 1-1: cPCI-6920 Series Functional Block Diagram** shows a block diagram of the Intel® 5100 MCH Chipset based platform.

3.3 Memory

The cPCI-6920 Series supports dual channel, registered, ECC DDR2 SDRAM operating at 667MHz. In the 4HP version, Channel 0 is connected to two 200-pin horizontal SO-RDIMM sockets; in the 8HP version, each channel (Channels 0/1) connects to two vertical SO-RDIMM sockets (four sockets). Available COTS DDR2-667 SO-RDIMM densities are 1GB, 2GB, and 4GB.

The cPCI-6920 Series supports up to 16GB of physical memory using the largest system memory configuration supported by 2Gb DRAM devices. All DIMMs must consist of x4 or x8 DDR2 DRAMs. Up to eight different types of DIMMs can be installed. The same type of DIMM does not need to be installed in each rank. A rank on one DIMM can be different than a rank on another DIMM.

Memory configuration changes can only be performed at the factory. Failure to comply with the above may result in damage to your board or improper operation.

3.4 ATI ES1000 Graphics Controller

The ATI ES1000 Graphics Controller provides proven and reliable 2D graphics performance for today's applications in 16-bit or 32-bit color. Detailed features are as follows:

- 32-bit PCI bus (Rev 2.2), 3.3 V with bus mastering support
- Highly-optimized 128-bit engine, capable of processing multiple pixels/clock
- Optimized handling of fonts and text using ATI proprietary techniques
- Acceleration in 8/16/32 bpp modes (8bpp indexed color mode); also enhanced with 4444 aRGB 16 bit mode and 88 alpha/index 16 bit mode
- Single resolution, up to 1600x1200, at 75Hz refresh rate, and 16 bit color (panel display maximum refresh rate for 1600x1200 is 60Hz)

- Support for up to 256MB local frame buffer, or display from system memory via SMA, in either linear or tiled addressing modes
- Virtual desktop support
- Supports JEDEC compatible DDR1 or DDR2 SDRAM or SGRAM
- Total memory sizes from 8MB to 256MB

3.5 PCI-E to PCI Bridge

The cPCI-6920 Series is designed using the Tundra Tsi384 PCI-Express-to-PCI bridge to downgrade PCI-Express links from the Intel chipset to PCI bus. One Tsi384 (U46*) is used to convert the PCI-Express x4 link from the Intel 5100 MCH to a PCI-X 64-bit/133MHz bus on J1 for CompactPCI support. The second Tsi384 (U2-L*) is to convert a PCI-Express x1 link from the Intel ICH9R to a PCI 64-bit/66MHz bus for the PMC site (cPCI-6920D only). The Tsi384 supports 3.3V signaling only.

Note*: See Figure 4-1: cPCI-6920 Board Layout and Figure 4-4: cPCI-6920D Board Layout.

3.6 PMC/XMC Site

The cPCI-6920 series supports a PMC/XMC site for front panel I/O expansion. The PMC site provides a 64bit/66MHz PCI bus link using a Tundra Tsi384 PCI-Express-to-PCI bridge and PCI-Express x1 link from the Intel® ICH9R I/O Hub. The PMC supports +3.3V signaling with no +5V tolerance.

The JN3 connector provides a x8 PCI-Express Link from the Intel® 5100 MCH for the XMC interface. XMC provides a higher transfer speed for I/O expansion than PMC.

3.7 Onboard USB Flash

The cPCI-6920 provides a 4GB USB interface solid state NAND flash device onboard as a mass storage or boot device option. The cPCI-6920 uses two Hynix 16Gbit NAND Flash devices with MLC (Multi-Level Cell) NAND cell and a USB 2.0 controller to enhance NAND management. The 4GB USB flash supports installation of

Windows XP embedded or Linux operating systems or can simply be used as a storage device like a USB flash drive.

3.8 Super I/O

The Winbond W83627UHG Super I/O is supports PS/2 keyboard/ mouse, 16550-compatible serial ports, floppy drive interface, and hardware monitor function to monitor CPU voltage, power supply voltages and system temperature.

3.9 Battery

The cPCI-6920 is provided with a 3.0V “coin cell” lithium battery for the Real Time Clock (RTC). The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. Rayovac BR2032 is equipped on board by default.

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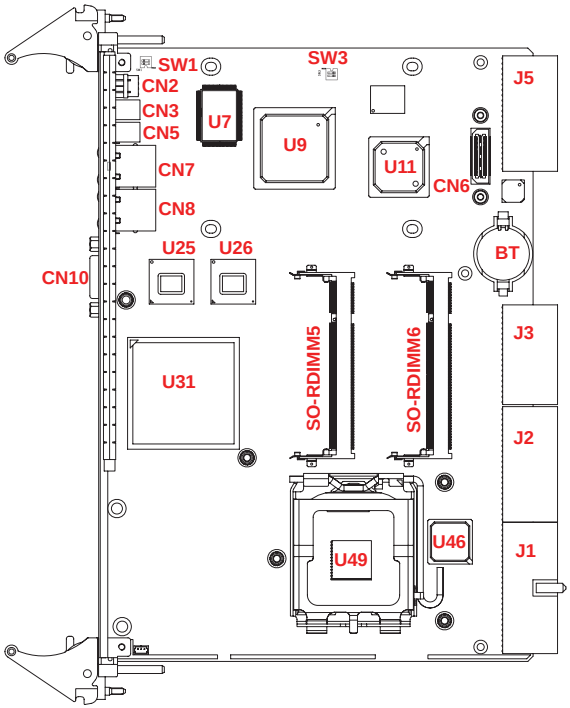
4 Board Interfaces

This chapter illustrates the board layout, connector pin assignments, and jumper settings to familiarize users with the cPCI-6920 Series.

4.1 cPCI-6920 SBC Board Layout



U49	CPU socket	**CN3/5**	USB ports
U46	PCIe to PCI bridge	**CN6**	DB-6920SAT/ DB-6920CF connector
U31	North Bridge	**CN7/8**	GbE ports
U25/26	GbE Controller 82571EB	**CN10**	VGA port
U7	Super I/O W83627UHG	**SO-RDIMMx**	SO-RDIMMs
U9	South Bridge	**BT**	Battery socket
U11	VGA controller	**J1/2/4/5**	CompactPCI Connectors
CN2	LED	**SW1/3**	Switches

Figure 4-1: cPCI-6920 Board Layout

4.2 cPCI-6920 SBC Front Panel

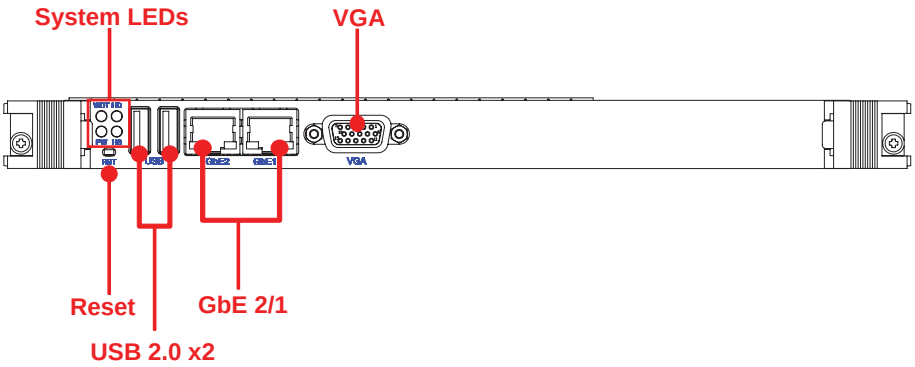
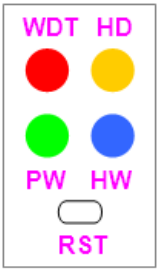


Figure 4-2: cPCI-6920 Front Panel Layout

System LEDs



LED	Color	Condition	Indication
Power (PW)	Green	OFF	System is off
		ON	System is on
		Blink	Fail to power on
HotSwap (HW)	Blue	OFF	Handles closed, System is on
		Fast Blink	Preparing to shut down system (LED: 0.1s on, 0.9s off.)
		ON	Handles open and SBC ready to be removed
		Slow Blink	Voltages out of tolerance: 3.3V, 5V, 12V, 1.5V over ±5% (LED 2s on, 1s off)
WDT (WDT)	Red	OFF	No Watchdog event
		ON	Watchdog event alert
HDD (HD)	Amber	OFF	No read/write access to HDD
		Blink	Data read/write in process

Table 4-1: cPCI-6920 Front Panel System LED Descriptions

4.3 cPCI-6920 SBC Assembly Layout

This section describes the final assembly layout of cPCI-6920 Series. The single-slot width cPCI-6920 provides two 200-pin SO-RDIMM sockets for DDR2-667 SO-RDIMM memory and is equipped with a removable DB-6920CF adapter card to provide CompactFlash slot as standard. The DB-6920CF can be replaced with a DB-6920SAT adapter board to directly mount a 2.5” SATA hard drive. Please contact your sales representative to purchase the DB-6920SAT.

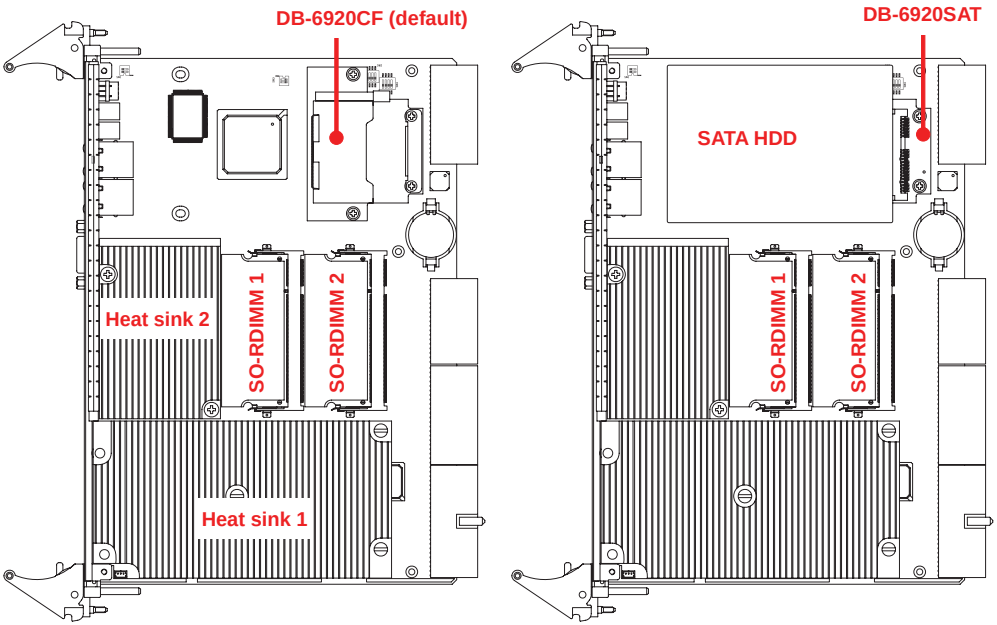
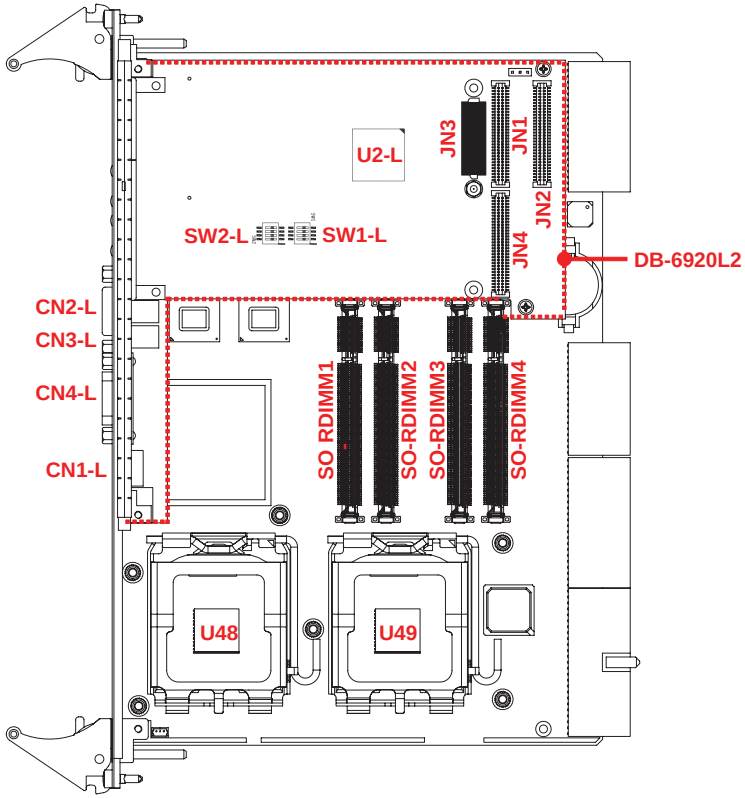


Figure 4-3: cPCI-6920 SBC Assembly Layout

4.4 cPCI-6920D SBC Board Layout

The dual-slot width cPCI-6920D is comprised of the cPCI-6920 single-slot main board and the DB-6920L2 riser card to expand I/O connectivity with PS/2, COM, 2x USB ports and a PMC/XMC site.



U49	CPU 0	**JN4**	PMC connectors
U48	CPU 1	**JN3**	XMC connector
SO-RDIMMx	SO-RDIMM sockets	**U2-L**	PCIe to PCI bridge
JN1	PMC connectors	**SW1-L**	Switch 1
JN2	PMC connectors	**SW2-L**	Switch 2
CN1-L	PS/2 Keyboard Mouse port	**CN3-L**	USB port
CN2-L	USB port	**CN4-L**	COM port

Figure 4-4: cPCI-6920D Board Layout

4.5 cPCI-6920D SBC Front Panel

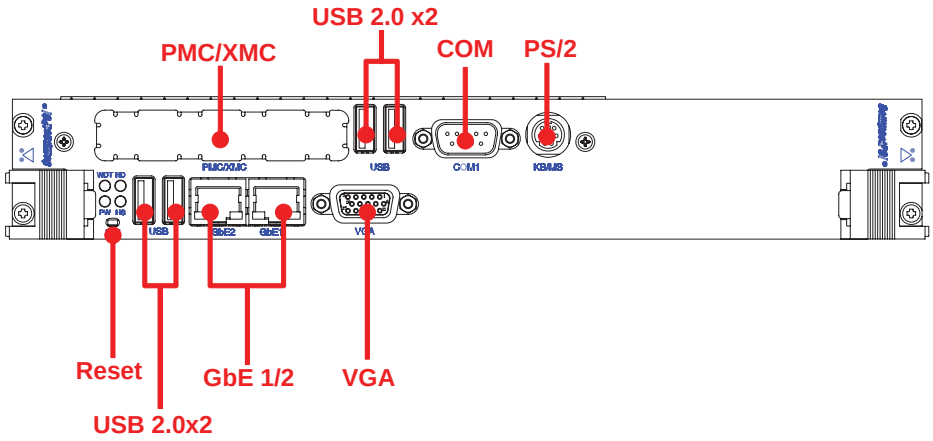
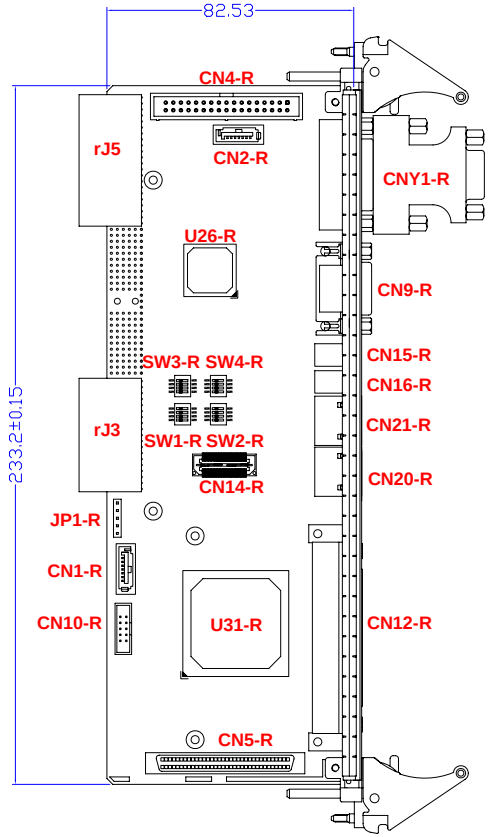


Figure 4-5: cPCI-6920D Front Panel Layout

4.6 cPCI-R6000 RTM Board Layout



U26-R	PCIe-to-PCI bridge	**CN14-R**	DB-R6000L2 connector[1]
U31-R	LSI53C1020 SCSI controller	**CN12-R**	External SCSI connector
JP1-R	USB pin header (5-pin)	**CN15/16-R**	USB ports
CN1/2-R	SATA port (7-pin)	**CN20/21-R**	GbE ports
CN5-R	Internal SCSI connector	**CNY1-R**	DVI to VGA adapter
CN9-R	Serial port	**rJ3/5**	CompactPCI Connectors
CN10-R	Serial pin header (10-pin)	**SW1~4-R**	Switches
CN4-R	Floppy connector		

Figure 4-6: cPCI-R6000 RTM Board Layout

Note(1): Used for cPCI-R6000D RTM – shown here for clarity.

4.7 cPCI-R6000 RTM Front Panel

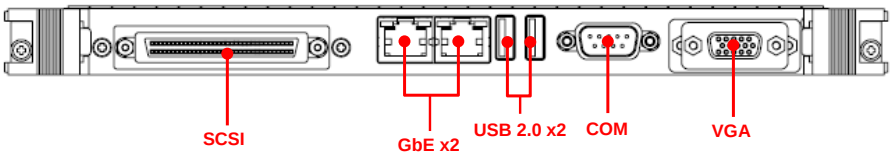
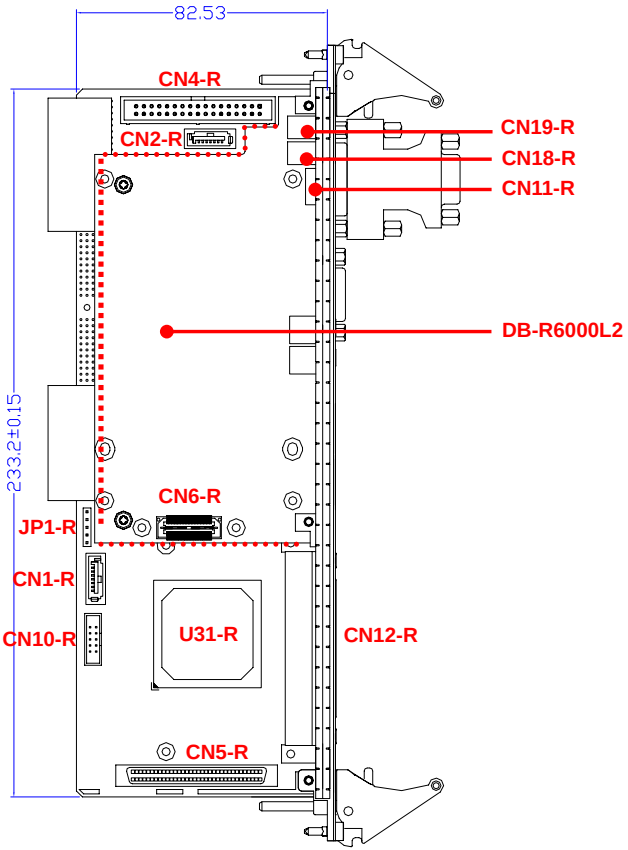


Figure 4-7: cPCI-R6000 RTM Front Panel

4.8 cPCI-R6000D RTM Board Layout



CN1/2-R	SATA port (7-pin)	**CN11-R**	PS/2 KB/MS port
CN4-R	Floppy connector	**CN12-R**	External SCSI connector
CN5-R	Internal SCSI connector	**CN18/19-R**	USB ports
CN6-R	DB-6920SAT/ DB-6920CF connector	**JP1-R**	USB pin header (5-pin)
CN10-R	Serial pin header (10-pin)		

Figure 4-8: cPCI-R6000D RTM Board Layout

4.9 cPCI-R6000D RTM Front Panel

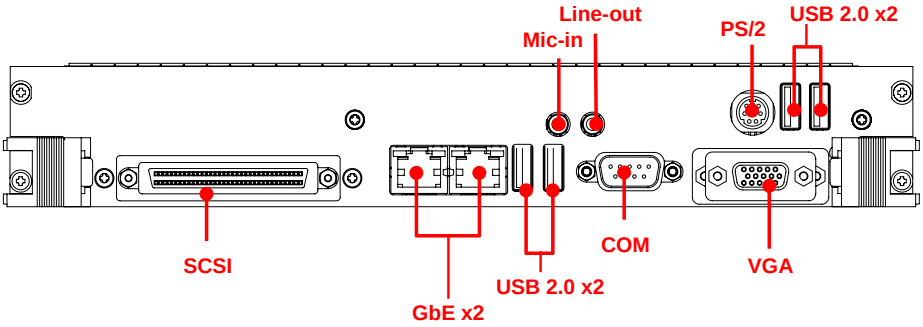


Figure 4-9: cPCI-R6000D RTM Front Panel

4.10 cPCI-R6000D RTM Assembly Layoutl

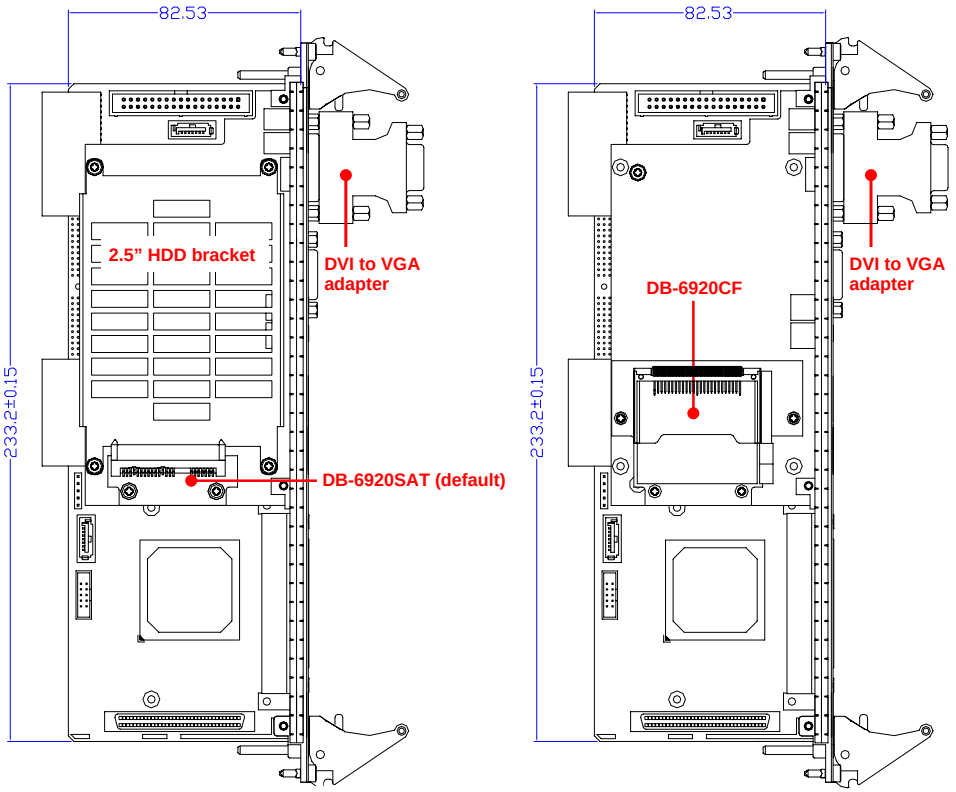


Figure 4-10: cPCI-R6000D RTM Assembly Layout

4.11 Connector Pin Assignments

USB Connectors (CN3,CN5, CN2-L, CN3-L, CN15-R, CN16-R, JP1-R)

Pin #	Signal Name
1	Vcc
2	UV0-
3	UV0+
4	GND

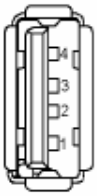


Table 4-2: USB Connector Pin Definition

DB-15 VGA Connector (CN10)

Signal Name	Pin #	Pin #	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
+5V.	9	10	GND
N.C.	11	12	CRTDATA
HSYNC	13	14	VSYNC
CRTCLK	15		

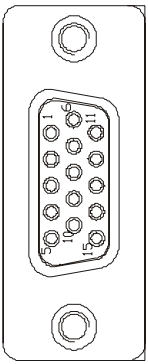


Table 4-3: VGA Connector Pin Definition

RJ-45 Gigabit Ethernet Connectors (CN7, CN8, CN20-R, CN21-R)

Pin #	10BASE-T/ 100BASE-TX	1000BASE-T
1	TX+	BI_DA+
2	TX-	BI_DA-
3	RX+	BI_DB+
4	--	BI_DC+
5	--	BI_DC-
6	RX-	BI_DB-
7	--	BI_DD+
8	--	BI_DD-

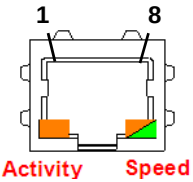


Table 4-4: GbE Connector Pin Definitions

Status (CN4, CN5)		Speed LED (Green/Amber)	Activity LED (Amber)
Network link is not established or system powered off		OFF	OFF
10 Mbps	Link	OFF	ON
	Active	OFF	Blinking
100 Mbps	Link	Green	ON
	Active	Green	Blinking
1000 Mbps	Link	Amber	ON
	Active	Amber	Blinking

Table 4-5: CN7, CN8 Ethernet LED Status Definitions

Status (CN20-R, CN21-R)		Speed LED (Green/Amber)	Activity LED (Amber)
Network link is not established or system powered off		OFF	OFF
10 Mbps	Link	OFF	ON
	Active	OFF	Blinking
100 Mbps	Link	Amber	ON
	Active	Amber	Blinking
1000 Mbps	Link	Green	ON
	Active	Green	Blinking

Table 4-6: GbE LED CN20-R, CN21-R Status Definitions

PS/2 Keyboard/Mouse Connector (CN1-L, CN11-R)

Pin #	Signal	Function
1	KBDATA	Keyboard Data
2	MSDATA	Mouse Data
3	GND	Ground
4	+5V	Power
5	KBCLK	Keyboard Clock
6	MSCLK	Mouse Clock

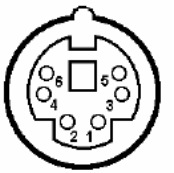


Table 4-7: PS/2 Keyboard/Mouse Connector Pin Definition

DB-9 Serial Port (CN4-L, CN9-R)

Pin #	RS-232
1	DCD, Data carrier detect
2	RXD, Receive data
3	TXD, Transmit data
4	DTR, Data terminal ready
5	GND, Ground
6	DSR, Data set ready
7	RTS, Request to send
8	CTS, Clear to send
9	RI, Ring indicator

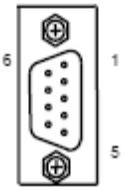


Table 4-8: DB-15 Serial Port Connector Pin Definition

Onboard Serial Port Connector (CN10-R)

Pin #	RS-232
1	Not used
2	Not used
3	RXD, Receive data
4	Not used
5	TXD, Transmit data
6	Not used
7	Not used
8	Not used
9	IsoGND, Isolated ground
10	Not used

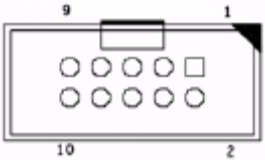
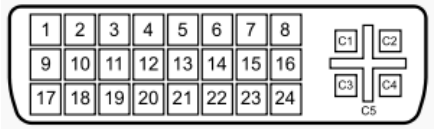


Table 4-9: Onboard Serial Port Connector Pin Definition

DVI-I Connector (CNY1-R)



Pin #	Signal	Pin #	Signal
1	NC	16	NC
2	NC	17	NC
3	GND	18	NC
4	NC	19	GND
5	NC	20	NC
6	DDCCLK_5V	21	NC
7	DDCDAT_5V	22	GND
8	VSYNC	23	NC
9	NC	24	NC
10	NC	C1	RED
11	GND	C2	GREEN
12	NC	C3	BLUE
13	NC	C4	HSYNC
14	P5V	C5	GND
15	GND		

Table 4-10: DVI-I Connector Pin Definition

Serial ATA Connectors (CN5/7)

Pin #	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

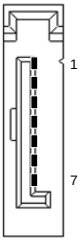


Table 4-11: Serial ATA Connector Pin Definition

Serial ATA Connector on DB-6920SAT

Pin #	Signal
S1	GND
S2	TX+
S3	TX-
S4	GND
S5	RX-
S6	RX+
S7	GND
P1	NC
P2	NC
P3	NC
P4	GND
P5	GND
P6	GND
P7	5V
P8	5V
P9	5V
P10	GND
P11	Reserved
P12	GND
P13~P15	12V

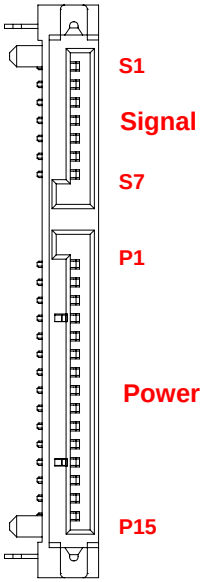


Table 4-12: Serial ATA Connector on DB-6920SAT Pin Definition

68-pin SCSI Connector (CN5-R, CN12-R)

Signal	Pin #	Pin #	Signal
SCSI-SDP12	1	35	SCSI-SDN12
SCSI-SDP13	2	36	SCSI-SDN13
SCSI-SDP14	3	37	SCSI-SDN14
SCSI-SDP15	4	38	SCSI-SDN15
SCSI-SDP1-P1	5	39	SCSI-SDP1-N1
SCSI-SDP0	6	40	SCSI-SDN0
SCSI-SDP1	7	41	SCSI-SDN1
SCSI-SDP2	8	42	SCSI-SDN2
SCSI-SDP3	9	43	SCSI-SDN3
SCSI-SDP4	10	44	SCSI-SDN4
SCSI-SDP5	11	45	SCSI-SDN5
SCSI-SDP6	12	46	SCSI-SDN6
SCSI-SDP7	13	47	SCSI-SDN7
SCSI-SDP0-P0	14	48	SCSI-SDP0-N0
GND	15	49	GND
DIFFSEN	16	50	NC
P3V3_SCSI	17	51	P3V3_SCSI
P3V3_SCSI	18	52	P3V3_SCSI
NC	19	53	NC
GND	20	54	GND
SCSI-SATN-P	21	55	SCSI-SATN-N
GND	22	56	GND
SCSI-SBSY-P	23	57	SCSI-SBSY-N
SCSI-SACK-P	24	58	SCSI-SACK-N
SCSI-SRST-P	25	59	SCSI-SRST-N
SCSI-SMSG-P	26	60	SCSI-SMSG-N
SCSI-SSEL-P	27	61	SCSI-SSEL-N
SCSI-SCD-P	28	62	SCSI-SCD-N
SCSI-SREQ-P	29	63	SCSI-SREQ-N
SCSI-SIO-P	30	64	SCSI-SIO-N
SCSI-SDP8	31	65	SCSI-SDN8
SCSI-SDP9	32	66	SCSI-SDN9
SCSI-SDP10	33	67	SCSI-SDN10
SCSI-SDP11	34	68	SCSI-SDN11

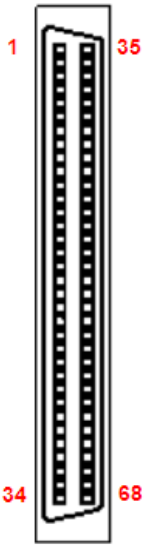


Table 4-13: 68-pin SCSI Pin Definition

Floppy Connector 34-pin (CN4-R)

Pin #	Signal	Pin #	Signal
1	GND	2	Extended Density
3	GND	4	No Connect
5	NC	6	Data Rate
7	GND	8	Index
9	GND	10	Motor A Select
11	GND	12	Drive B Select
13	GND	14	Drive A Select
15	GND	16	Motor B Select
17	GND	18	Step Direction
19	GND	20	Step Pulse
21	GND	22	Write Data
23	GND	24	Write Gate
25	GND	26	Track 0
27	GND	28	Write Protect
29	GND	30	Read Data
31	GND	32	Side 1
33	GND	34	Disk Change

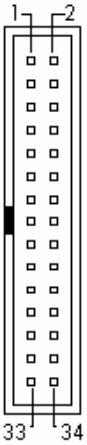


Table 4-14: Floppy Connector Pin Definition

CompactFlash Connector on DB-6920CF

Signal Name	Pin#	Pin#	Signal Name
GND	1	26	GND
DD3	2	27	DD11
DD4	3	28	DD12
DD5	4	29	DD13
DD6	5	30	DD14
DD7	6	31	DD15
CS1J	7	32	CS3J
GND	8	33	GND
GND	9	34	SDIORJ
GND	10	35	SDIOWJ
GND	11	36	5V
GND	12	37	IRQ15
5V	13	38	5V
GND	14	39	PCSEL
GND	15	40	NC
GND	16	41	BRSTDRVJ
GND	17	42	SDIORDY
DA2	18	43	NC
DA1	19	44	SDACKJ
DA0	20	45	IDEACTJ
DD0	21	46	DIAG
DD1	22	47	DD8
DD2	23	48	DD9
IOIS16J	24	49	DD10
GND	25	50	GND

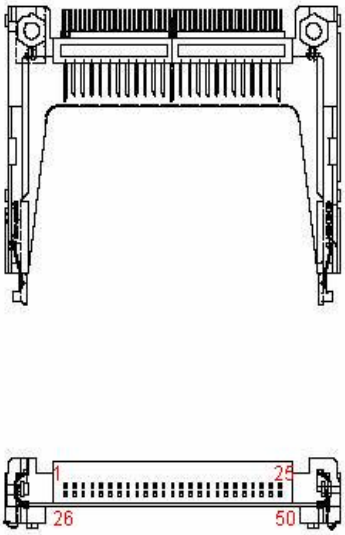
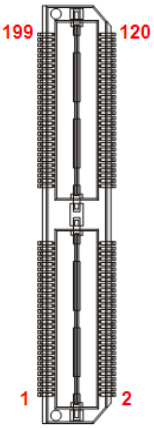


Table 4-15: CompactFlash Connector Pin Definition

DB-6920L2 Connector (CN4)

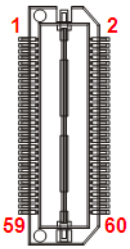
Signal Name	Pin #	Pin #	Signal Name
GND	1	2	GND
PMC_TXP7	3	4	PMC_RXP7
PMC_TXN7	5	6	PMC_RXN7
GND	7	8	GND
PMC_TXP6	9	10	PMC_RXP6
PMC_TXN6	11	12	PMC_RXN6
GND	13	14	GND
PMC_TXP5	15	16	PMC_RXP5
PMC_TXN5	17	18	PMC_RXN5
GND	19	20	GND
PMC_TXP4	21	22	PMC_RXP4
PMC_TXN4	23	24	PMC_RXN4
GND	25	26	GND
PMC_TXP3	27	28	PMC_RXP3
PMC_TXN3	29	30	PMC_RXN3
GND	31	32	GND
PMC_TXP2	33	34	PMC_RXP2
PMC_TXN2	35	36	PMC_RXN2
GND	37	38	GND
PMC_TXP1	39	40	PMC_RXP1
PMC_TXN1	41	42	PMC_RXN1
GND	43	44	GND
PMC_TXP0	45	46	PMC_RXP0
PMC_TXN0	47	48	PMC_RXN0
GND	49	50	GND
PCIE_TXP1	51	52	PCIE_RXP1
PCIE_TXN1	53	54	PCIE_RXN1
GND	55	56	GND
CLK100_B2B_P	57	58	PLTRST_LPC-L
CLK100_B2B_N	59	60	GND
GND	61	62	COM1_DTR-L
GND	63	64	COM1_RST-L



Signal Name	Pin #	Pin #	Signal Name
CLK100_XMC_P	65	66	COM1_RI-L
CLK100_XMC_N	67	68	COM1_DCD-L
GND	69	70	COM1_DSR-L
USB2_FRONT_C-P	71	72	COM1_CTS-L
USB2_FRONT_C-N	73	74	COM1_SOUT
GND	75	76	COM1_SIN
USB3_FRONT_C-P	77	78	GND
USB3_FRONT_C-N	79	80	IPMI_DEB_RX
GND	81	82	IPMI_DEB_TX
USB2_OC-L	83	84	GND
USB3_OC-L	85	86	IPM_CLK
GND	87	88	IPM_DAT
B2B_SATA_RXP0	89	90	XMC_RST-L
B2B_SATA_RXN0	91	92	KBCLK
GND	93	94	KBDATA
B2B_SATA_TXP0	95	96	MSDATA
B2B_SATA_TXN0	97	98	MSCLK
GND	99	100	GND
P5V_STB	101	102	P12V
P5V_STB	103	104	P12V
N12V	105	106	P5V
P3V3	107	108	P5V
P3V3	109	110	P5V
P3V3	111	112	P5V
P3V3	113	114	P5V
P3V3	115	116	P5V
P3V3	117	118	P5V
GND	119	120	GND

Table 4-16: DB-6920L2 Connector Pin Definition

DB-6920CF/DB-6920SAT Connector (CN6, CN6-R)

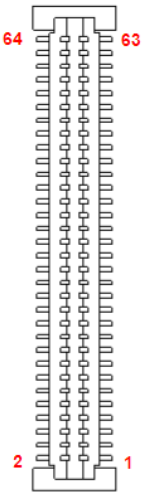


Signal Name	Pin #	Pin #	Signal Name
GND	1	2	GND
GND	3	4	GND
GND	5	6	GND
GND	7	8	GND
GND	9	10	GND
GND	11	12	GND
GND	13	14	GND
GND	15	16	GND
GND	17	18	GND
GND	19	20	GND
GND	21	22	GND
GND	23	24	GND
GND	25	26	GND
GND	27	28	GND
GND	29	30	GND
P3V3	31	32	P5V
P3V3	33	34	P5V
P3V3	35	36	P5V
P3V3	37	38	P5V
P1V8	39	40	NC
P1V8	41	42	NC
P1V8	43	44	NC
GND	45	46	GND
GND	47	48	SATA-TXN0
GND	49	50	SATA-TXP0
SATA-RXN0	51	52	GND
SATA-RXP0	53	54	GND
GND	55	56	RESET#
GND	57	58	GND
GND	59	60	GND

Table 4-17: DB-6920CF/DB-6920SAT Connector Pin Definition

PMC Connector (JN1, JN2, JN3, JNX1)

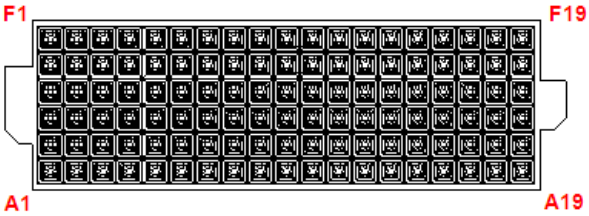
Pin#	JN1 Signal	JN2 Signal	JN3 Signal	JNX1 Signal
1	PMC_TCK	P12V	PIO1	NC
2	N12V	PMC_TRST-L	PIO2	GND
3	GND	PMC_TMS	PIO3	GND
4	PCIX_INTA-L	NC (PMC_TDO)	PIO4	PCIX_CBE-L7
5	PCIX_INTB-L	PMC_TDI	PIO5	PCIX_CBE-L6
6	PCIX_INTC-L	GND	PIO6	PCIX_CBE-L5
7	PMC_MOD-L1	GND	PIO7	PCIX_CBE-L4
8	P5V	NC	PIO8	GND
9	PCIX_INTD-L	NC	PIO9	PMC_VIO
10	NC	NC	PIO10	PCIX_PAR64
11	GND	PMC_MOD-L2	PIO11	PCIX_AD63
12	P3V3_PMCAUX	P3V3	PIO12	PCIX_AD62
13	CLK66_PCIX_PMC	PMC_RST-L	PIO13	PCIX_AD61
14	GND	PMC_MOD-L3	PIO14	GND
15	GND	P3V3	PIO15	GND
16	PCIX_GNT-L0	PMC_MOD-L4	PIO16	PCIX_AD60
17	PCIX_REQ-L0	PMC_PME-L	PIO17	PCIX_AD59
18	P5V	GND	PIO18	PCIX_AD58
19	PMC_VIO	PCIX_AD30	PIO19	PCIX_AD57
20	PCIX_AD31	PCIX_AD29	PIO20	GND
21	PCIX_AD28	GND	PIO21	GND
22	PCIX_AD27	PCIX_AD26	PIO22	PCIX_AD56
23	PCIX_AD25	PCIX_AD24	PIO23	PCIX_AD55
24	GND	PCIX_AD23	PIO24	PCIX_AD54
25	GND	PMC_IDSEL	PIO25	PCIX_AD53
26	PCIX_CBE-L3	PCIX_AD23	PIO26	GND
27	PCIX_AD22	P3V3	PIO27	GND
28	PCIX_AD21	PCIX_AD20	PIO28	PCIX_AD52
29	PCIX_AD19	PCIX_AD18	PIO29	PCIX_AD51
30	P5V	GND	PIO30	PCIX_AD50
31	PCIX_FRAME-L	PCIX_AD16	PIO31	PCIX_AD49
32	PCIX_AD17	PCIX_CBE-L2	PIO32	GND
33	PCIX_FRAME-L	GND	PIO33	GND



Pin#	JN1 Signal	JN2 Signal	JN3 Signal	JNX1 Signal
34	GND	NC	PIO34	PCIX_AD48
35	GND	PCIX_TRDY-L	PIO35	PCIX_AD47
36	PCIX_IRDY-L	P3V3	PIO36	PCIX_AD46
37	PCIX_DEVSEL-L	GND	PIO37	PCIX_AD45
38	P5V	PCIX_STOP-L	PIO38	GND
39	PCIX_PCIXCAP	PCIX_PERR-L	PIO39	GND
40	PCIX_LOCK-L	GND	PIO40	PCIX_AD44
41	NC	P3V3	PIO41	PCIX_AD43
42	NC	PCIX_SERR-L	PIO42	PCIX_AD42
43	PCIX_PAR	PCIX_CBE-L1	PIO43	PCIX_AD41
44	GND	GND	PIO44	GND
45	PMC_VIO	PCIX_AD14	PIO45	GND
46	PCIX_AD15	PCIX_AD13	PIO46	PCIX_AD40
47	PCIX_AD12	PCIX_M66EN	PIO47	PCIX_AD39
48	PCIX_AD11	PCIX_AD10	PIO48	PCIX_AD38
49	PCIX_AD9	PCIX_AD8	PIO49	PCIX_AD37
50	P5V	P3V3	PIO50	GND
51	GND	PCIX_AD7	PIO51	GND
52	PCIX_CBE-L0	NC	PIO52	PCIX_AD36
53	PCIX_AD6	P3V3	PIO53	PCIX_AD35
54	PCIX_AD5	NC	PIO54	PCIX_AD34
55	PCIX_AD4	NC	PIO55	PCIX_AD33
56	GND	GND	PIO56	GND
57	PMC_VIO	NC	PIO57	GND
58	PCIX_AD3	NC	PIO58	PCIX_AD32
59	PCIX_AD2	GND	PIO59	NC
60	PCIX_AD1	NC	PIO60	NC
61	PCIX_AD0	PCIX_ACK64-L	PIO61	NC
62	P5V	P3V3	PIO62	GND
63	GND	GND	PIO63	GND
64	PCIX_REQ64-L	NC	PIO64	NC

Table 4-18: PMC Connector Pin Definition

XMC Connector (JN3)



Pin#	A	B	C	D	E	F
1	PETp0	PETn0	3.3V	PETp1	PETn1	VPWR
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PETp2	PETn2	3.3V	PETp3	PETn3	VPWR
4	GND	GND	TCK	GND	GND	MRSTO#
5	PETp4	PETn4	3.3V	PETp5	PETn5	VPWR
6	GND	GND	TMS	GND	GND	+12V
7	PETp6	PETn6	3.3V	PETp7	PETn7	VPWR
8	GND	GND	TDI	GND	GND	-12V
9	NC	NC	NC	NC	NC	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	PERp0	PERn0	MBIST#	PERp1	PERn1	VPWR
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PERp2	PERn2	3.3V AUX	PERp3	PERn3	VPWR
14	GND	GND	GA2	GND	GND	MSDA
15	PERp4	PERn4	NC	PERp5	PERn5	VPWR
16	GND	GND	MVMRO	GND	GND	MSCL
17	PERp6	PERn6	NC	PERp7	PERn7	NC
18	GND	GND	NC	GND	GND	NC
19	REFCLK+0	REFCLK-0	NC	WAKE#	ROOT0#	NC

Table 4-19: XMC Connector Pin Definition

DB-R6000L2 Connector (CN14)

Signal Name	Pin #	Pin #	Signal Name
SATA-T1P	1	2	USB-P3
SATA-T1N	3	4	USB-N3
GND	5	6	GND
SATA-R1P	7	8	USB-OC3#
SATA-R1N	9	10	GND
GND	11	12	GND
GND	13	14	USB-P2
HAD_RST-L	15	16	USB-N2
HAD_SYNC	17	18	GND
HAD_SDOUT	19	20	USB-OC2#
HAD_BIT_CLK	21	22	GND
HAD_SDIN0	23	24	PS2-KBC
GND	25	26	PS2-KBD
HAD_SDIN1	27	28	PS2-MSD
HAD_SDIN2	29	30	PS2-MSC
HAD_SDIN3	31	32	GND
GND	33	34	RESET#
GND	35	36	GND
GND	37	38	GND
GND	39	40	GND
GND	41	42	GND
GND	43	44	GND
GND	45	46	GND
GND	47	48	GND
GND	49	50	GND
P5V	51	52	P1V8
P5V	53	54	P1V8
P5V	55	56	P1V8
P5V	57	58	NC
P5V	59	60	NC
GND	61	62	GND

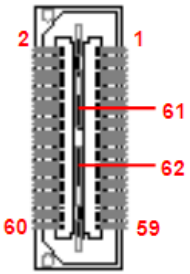


Table 4-20: DB-R6000L2 Connector Pin Definition

CompactPCI J1 Connector Pin Assignment

Pin	Z	A	B	C	D	E	F
1	GND	P5V_STB	N12V_STB	CPCI_TRST-L	P12V_CPCIJ1	P5V_STB	GND
2	GND	CPCI_TCK	P5V_STB	CPCI_TMS	NC	CPCI_TDI	GND
3	GND	JCPCI_INTA-L	JCPCI_INTB-L	JCPCI_INTC-L	P5V_STB	JCPCI_INTD-L	GND
4	GND	P5V_IPMB	JCPCI_HEALTHY-L	CPCI_VIO	NC	NC	GND
5	GND	NC	NC	JCPCI_RESET-L	GND	CPCI_GNT-L0	GND
6	GND	JCPCI_REQ-L0	CPCI_PRESENT-L	P3V3_STB	CPCI_CLK0	JCPCI_AD31	GND
7	GND	AD30	JCPCI_AD29	JCPCI_AD28	GND	JCPCI_AD27	GND
8	GND	JCPCI_AD26	GND	CPCI_VIO	JCPCI_AD25	JCPCI_AD24	GND
9	GND	JCPCI_CBE-L3	JCPCI_IDSEL	JCPCI_AD23	GND	JCPCI_AD22	GND
10	GND	JCPCI_AD21	GND	P3V3_STB	JCPCI_AD20	JCPCI_AD19	GND
11	GND	JCPCI_AD18	JCPCI_AD17	JCPCI_AD16	GND	JCPCI_BE-L2	GND
12-14	Key						
15	GND	P3V3_STB	JCPCI_FRAME-L	JCPCI_IRDY-L	CPCI_BDSEL-L	JCPCI_TRDY-L	GND
16	GND	JCPCI_DEVSEL-L	CPCI_PCIXCAP	CPCI_VIO	JCPCI_STOP-L	JCPCI_LOCK-L	GND
17	GND	P3V3_STB	IPMB_SCL	IPMB_SDA	GND	JCPCI_PERR-L	GND
18	GND	JCPCI_SERR-L	GND	P3V3_STB	JCPCI_PAR	JCPCI_CBE-L1	GND
19	GND	P3V3_STB	JCPCI_AD15	JCPCI_AD14	GND	JCPCI_AD13	GND
20	GND	JCPCI_AD12	GND	CPCI_VIO	JCPCI_AD11	JCPCI_AD10	GND
21	GND	P3V3_STB	JCPCI_AD9	JCPCI_AD8	CPCI_M66EN	JCPCI_CBE-L0	GND
22	GND	JCPCI_AD7	GND	P3V3_STB	JCPCI_AD6	JCPCI_AD5	GND
23	GND	P3V3_STB	JCPCI_AD4	JCPCI_AD3	P5V_STB	JCPCI_AD2	GND
24	GND	JCPCI_AD1	P5V_STB	CPCI_VIO	AD0	ACK	GND
25	GND	P5V_STB	JCPCI_REQ64-L	JCPCI_ENUM-L	P3V3_STB	P5V_STB	GND

Table 4-21: CompactPCI J1 Connector Pin Definition

Note: There is a yellow coding key in the J1 Connector to prevent plugging the blade into a 5V backplane.

CompactPCI J2 Connector Pin Assignment

Pin	Z	A	B	C	D	E	F
1	GND	CPCI_CLK1	GND	JCPCI_REQ-L1	CPCI_GNT-L1	JCPCI_REQ-L2	GND
2	GND	CPCI_CLK2	CPCI_CLK3	SYSEN-L	CPCI_GNT-L2	JCPCI_REQ-L3	GND
3	GND	CPCI_CLK4	GND	CPCI_GNT-L3	JCPCI_REQ-L4	JCPCI_GNT-L4	GND
4	GND	CPCI_VIO	NC	JCPCI_CBE-L7	GND	JCPCI_CBE-L6	GND
5	GND	JCPCI_CBE-L5	GND	CPCI_VIO	JCPCI_CBE-L4	JCPCI_PAR64	GND
6	GND	JCPCI_AD63	JCPCI_AD62	JCPCI_AD61	GND	JCPCI_AD60	GND
7	GND	JCPCI_AD59	GND	CPCI_VIO	JCPCI_AD58	JCPCI_AD57	GND
8	GND	JCPCI_AD56	JCPCI_AD55	JCPCI_AD54	GND	JCPCI_AD53	GND
9	GND	JCPCI_AD52	GND	CPCI_VIO	JCPCI_AD51	JCPCI_AD50	GND
10	GND	JCPCI_AD49	JCPCI_AD48	JCPCI_AD47	GND	JCPCI_AD46	GND
11	GND	JCPCI_AD45	GND	CPCI_VIO	JCPCI_AD44	JCPCI_AD43	GND
12	GND	JCPCI_AD42	JCPCI_AD41	JCPCI_AD40	GND	JCPCI_AD39	GND
13	GND	JCPCI_AD38	GND	CPCI_VIO	JCPCI_AD37	JCPCI_AD36	GND
14	GND	JCPCI_AD35	JCPCI_AD34	JCPCI_AD33	GND	JCPCI_AD32	GND
15	GND	NC	GND	CPCI_FAL-L	JCPCI_REQ-L5	CPCI_GNT-L5	GND
16	GND	NC	NC	CPCI_DEG-L	GND	NC	GND
17	GND	NC	GND	J2_RSTBTN-L	JCPCI_REQ-L6	CPCI_GNT-L6	GND
18	GND	NC	NC	NC	GND	NC	GND
19	GND	GND	GND	NC	NC	NC	GND
20	GND	CPCI_CLK5	GND	NC	GND	NC	GND
21	GND	CPCI_CLK6	GND	NC	NC	NC	GND
22	GND	GA4	GA3	GA2	GA1	GA0	GND

Table 4-22: CompactPCI J2 Connector Pin Definition

CompactPCI J3 Pin Assignment

Pin	Z	A	B	C	D	E	F
1	GND	HDA_RST-L	HDA_SYNC	HDA_BIT_CLK	HDA_SDOUT	HAD_SDIN0	GND
2	GND	HAD_SDIN1	HAD_SDIN2	HAD_SDIN3	NC	NC	GND
3	GND	PS2-KBD	PS2-KBC	NC	PS2-MSD	PS2-MSC	GND
4	GND	SATA-T1P	SATA-T1N	GND	SATA-T2P	SATA-T2N	GND
5	GND	GND	GND	NC	GND	GND	GND
6	GND	SATA-R1P	SATA-R1N	GND	SATA-R2P	SATA-R2N	GND
7	GND	COM4-TX	COM4-RX	COM2-DCD	I2C_CLK	I2C_DAT	GND
8	GND	COM2-RX	COM2-TX	COM2-DTR	COM2-DSR	COM2-RTS	GND
9	GND	COM2-CTS	COM2-RI	RGB-BLUE	RGB-RED	RGB-GREEN	GND
10	GND	USB-OC9-L	RGB-DDCCLK	RGB-DDCDAT	RGB-HSYNC	RGB-VSYNC	GND
11	GND	USB-P8	USB-N8	GND	USB-P9	USB-N9	GND
12	GND	USB-P6	USB-N6	GND	USB-P7	USB-N7	GND
13	GND	USB-P4	USB-N4	GND	USB-P5	USB-N5	GND
14	GND	USB-OC4-L	USB-OC5-L	USB-OC6-L	USB-OC7-L	USB-OC8-L	GND
15	GND	LANBA_TXDP1	LANBA_TXDN1	GND	LANBA_TXDP3	LANBA_TXDN3	GND
16	GND	LANBA_TXDP0	LANBA_TXDN0	GND	LANBA_TXDP2	LANBA_TXDN2	GND
17	GND	LANBB_TXDP1	LANBB_TXDN1	GND	LANBB_TXDP3	LANBB_TXDN3	GND
18	GND	LANBB_TXDP0	LANBB_TXDN0	GND	LANBB_TXDP2	LANBB_TXDN2	GND
19	GND	P5V	P5V	P12V	P5V	P5V	GND

Table 4-23: CompactPCI J3 Connector Pin Definition

High definition audio
PS/2 keyboard/Mouse
Serial ATA
Serial port
USB port
Ethernet port
RGB
I2C

CompactPCI J5 Pin Assignment

Pin	Z	A	B	C	D	E	F
1	GND	PCIE-TP0	PCIE-TN0	GND	PCIE-RP0	PCIE-RN0	GND
2	GND	PCIE-TP1	PCIE-TN1	GND	PCIE-RP1	PCIE-RN1	GND
3	GND	PCIE-TP2	PCIE-TN2	GND	PCIE-RP2	PCIE-RN2	GND
4	GND	PCIE-TP3	PCIE-TN3	GND	PCIE-RP3	PCIERN3	GND
5	GND	GND	GND	GND	GND	GND	GND
6	GND	CLKP0	CLKN0	GND	RESET-L	NC	GND
7	GND	NC	NC	NC	NC	NC	GND
8	GND	NC	NC	NC	NC	NC	GND
9	GND	GPIO13	GPIO16	GPIO33	GPIO34	GPIO56	GND
10	GND	NC	NC	GND	NC	NC	GND
11	GND	NC	NC	GND	NC	NC	GND
12	GND	NC	NC	NC	NC	NC	GND
13	GND	LANBA_100-L	LANBB_100-L	NC	LANBB_1G-L	LANBA_1G-L	GND
14	GND	NC	NC	GND	SATA-T3P	SATA-T3N	GND
15	GND	NC	NC	NC	SATA-R3P	SATA-R3N	GND
16	GND	MTR0-L	INDEX-L	RTM_ID1	NC	DENSEL-L	GND
17	GND	DIR-L	NC	RTM_ID2	DSEL0-L	NC	GND
18	GND	TRK0-L	WGATE-L	DETECT-L	WDATA-L	STEP-L	GND
19	GND	DSKCHG-L	HDSEL-L	NC	RDATA-L	WRPORT-L	GND
20	GND	NC	NC	GND	NC	NC	GND
21	GND	NC	NC	GND	NC	NC	GND
22	GND	P1V8_LAN	LANBA_LINK	LANBA_ACT#	LANBB_LINK	LANBB_ACT#	GND

Table 4-24: CompactPCI J5 Connector Pin Definition

PCI-Express x4
GPIO
Serial ATA
Floppy
Ethernet port

4.12 Switch and Jumper Settings

Reset Switch (SW1)

When the Switch SW1 is set to Chassis Reset Enable, a cPCI-6920 SBC installed in a system slot will be reset when the reset button on the front panel is pressed, and all peripheral cards on the CompactPCI bus will be reset. A cPCI-6920 installed in a peripheral slot will not be reset due to isolation from the CompactPCI bus.

Mode	1	2
Chassis Reset Enable (default)	ON	OFF
Chassis Reset Disable	OFF	OFF

Table 4-25: Reset Switch (SW1) Settings

Boot Device Switch (SW3)

The Switch SW3 sets the system to boot from the onboard SPI BIOS. The default is setting is ON.

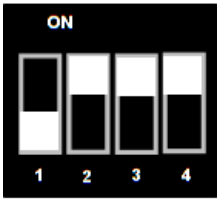
Mode	1	2
Boot by SPI BIOS (Default)	ON	ON

Table 4-26: Boot Device Switch (SW3) Settings

Changing this setting may cause the system to fail to boot.

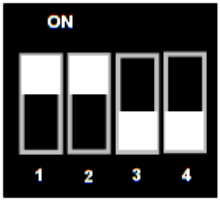
Debugging Switch (SW1-L)

The Switch SW1-L is located on the DB-6920L2 adapter board and is reserved for debugging purposes. The default setting is "pin 1 OFF", "pins 2-4 ON". Do not change these settings.



COM1 & IPMI Switch (SW2-L)

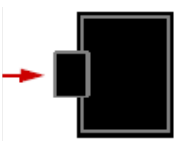
The Switch SW2-L is located on the DB-6920L2 adapter board to set DB-9 port (CN4-L) as a standard RS-232 serial port or IPMI debugging port.



Mode	1	2	3	4
RS-232 COM port (default)	ON	ON	OFF	OFF
IPMI debugging port	OFF	OFF	ON	ON

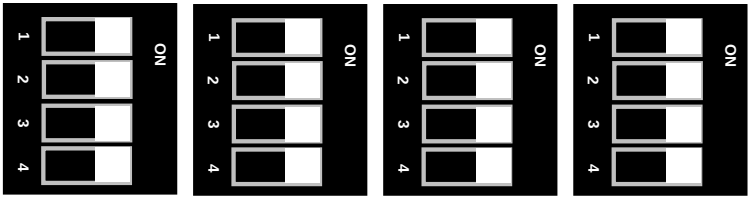
Clear CMOS (SW5)

The cPCI-6920 comes with Clear CMOS switch to reset the CMOS values to default. Press the Switch SW5 located on the solder side near the J1 connector to clear the CMOS.



PICMG 2.16 Switches (SW1-R ,SW2-R, SW3-R, SW4-R)

The cPCI-R6000(D) supports GbE3 and GbE4 on either the 2.16 backplane or rear I/O. The PICMG® 2.16 backplane and rear I/O cannot be accessed simultaneously. Switches SW1-R to SW4-R must be set to connect GbE3 and GbE4 to either the 2.16 backplane or to the RTM. The following table shows how to set the switches to enable either the 2.16 backplane or RTM for GbE3 and GbE4. All switches are set to ON by default.



SW1-R SW2-R SW3-R SW4-R

Connect GbE3/4 to	GbE3 (SW1-R, SW2-R)	GbE4 (SW3-R, SW4-R)
PICMG® 2.16 Backplane	All OFF	All OFF
Rear faceplate RJ-45 connectors (default)	All ON	All ON

5 Getting Started

This chapter describes the installation of the following components to the cPCI-6920 and rear transition modules:

- Memory module
- CompactFlash card
- 2.5” SATA Hard Drive Disk
- CPU module installation to chassis
- RTM installation to chassis

5.1 CPU and Heatsink

The 4HP cPCI-6920 supports one Dual/Quad-Core Intel® LV Xeon® processor and the 8HP cPCI-6920D supports up to two Dual/Quad-Core Intel® LV Xeon® processors. The cPCI-6920 Series comes with CPU(s) and heatsink pre-installed. Removal of heatsink/CPU by users is not recommended. Please contact your ADLINK service representative for assistance.

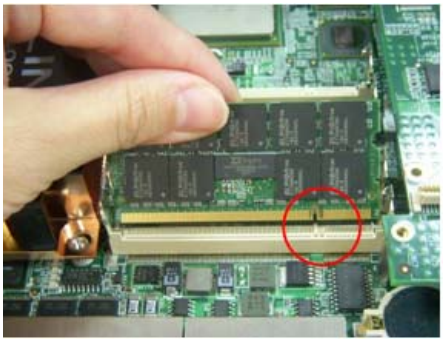
5.2 Memory Module Installation

The cPCI-6920 series supports DDR2-667 registered memory modules with ECC via two SO-RDIMM sockets in the 4HP version and four SO-RDIMM sockets in the 8HP version. The SO-RDIMM modules have a 200-pin footprint and are notched to facilitate correct installation in the SO-RDIMM sockets.

Installing the Memory Modules

1. Install sequence: SO-RDIMM4, SO-RDIMM3, SO-RDIMM2, SO-RDIMM1 in 8HP version (below left) and SO-RDIMM6, SO-RDIMM5 in 4HP version (below right).

2. Align the notch in the memory module with the key on the SO-RDIMM slot.



3. Press down on the module until is it is properly seated in the socket.

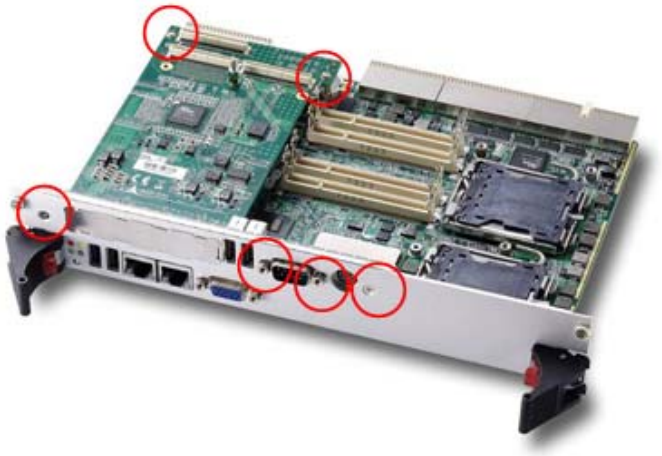
5.3 CompactFlash Card Installation

Both 4HP and 8HP versions of the cPCI-6920 are equipped with a removable CompactFlash adapter (DB-6920CF) that provides an internal CF card slot. In the cPCI-R6000D RTM, a DB-CF-SA kit (DB-6920CF adapter card) can be installed for an additional CompactFlash slot. CompactFlash storage is required by some industrial applications for its resistance to vibration and convenient installation/replacement.

NOTE:

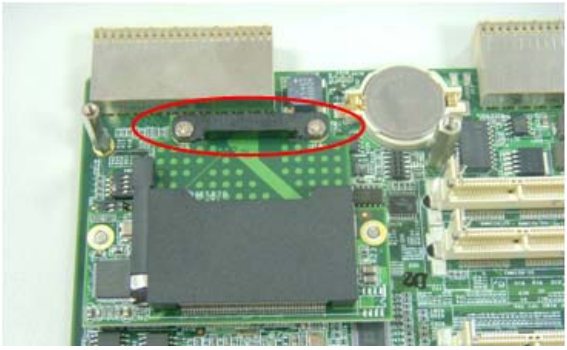
For the 8HP cPCI-6920D, the Layer 2 Adapter (DB-6920L2) must be removed before installing the CompactFlash card. To remove DB-6920L2 adapter, remove the 4x screws and 2x standoffs from the front panel and adapter board as shown below.

.



Installing a CF card - cPCI-6920 Series

1. Remove the card retaining bracket from CF adapter by removing the two screws.

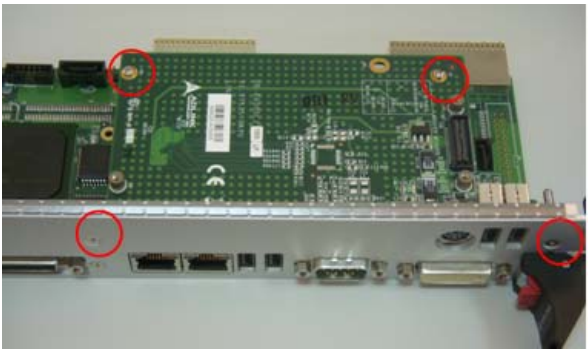


2. Insert the CF card into the CF slot on the adapter then replace the card retaining bracket to prevent the CF card from sliding out of the slot.

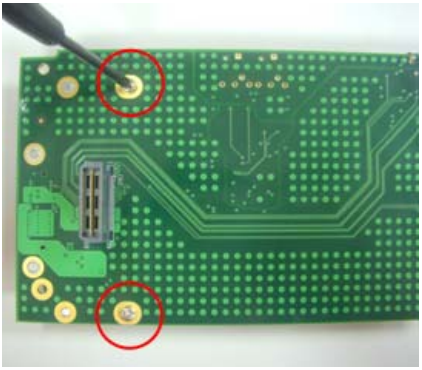
3. Reinstall the DB-6920L2 adapter as required for the 8HP cPCI-6920D.

Installing a CF card - cPCI-R6000D RTM

1. Remove the Layer 2 Adapter DB-R6000L2 by loosening the 4 screws as shown below.

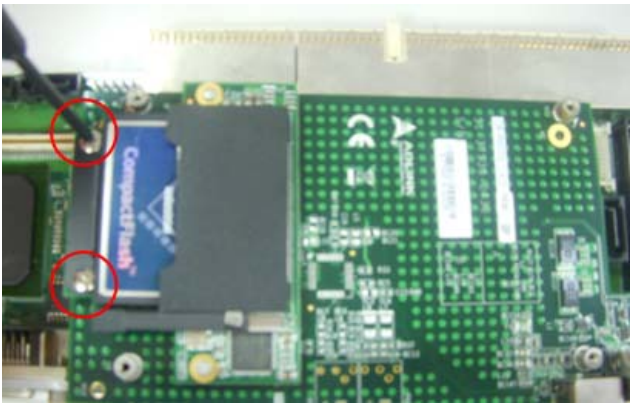


2. Install the DB-6920CF adapter to the RTM using the board-to-board connector.
3. Secure the DB-6920CF to the RTM using two screws from the solder side of Layer 2 Adapter of RTM.



4. Reinstall the Layer 2 Adapter to the RTM.

5. Insert the CF card into the CF slot on the adapter, then replace the card retaining bracket to prevent the CF card from sliding out of the slot.



5.4 Hard Drive Installation

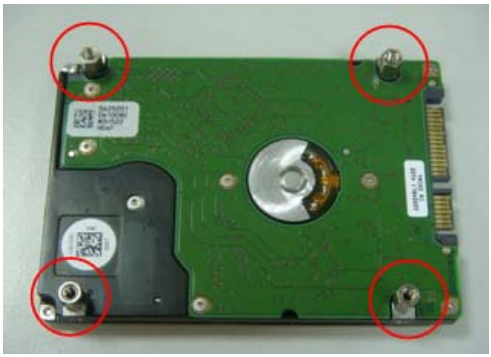
The cPCI-6920 Series provides space to install a slim type 2.5” Serial-ATA hard drive. The DB-SATA adapter kit (DB-6920SAT adapter and standoffs) is included in the package for hard drive installation. Before installing a hard drive, please remove the DB-6920CF adapter from board. The cPCI-R6000D RTM comes with a SATA HDD adapter as standard.

NOTE:

For the 8HP cPCI-6920D, the Layer 2 Adapter (DB-6920L2) must be removed before installing hard drive as described in **Section 5.3 CompactFlash Card Installation** above.

Installing a Hard Drive - cPCI-6920 Series

1. Attach the four standoffs provided with the DB-SATA adapter kit onto the SATA hard drive as shown below.

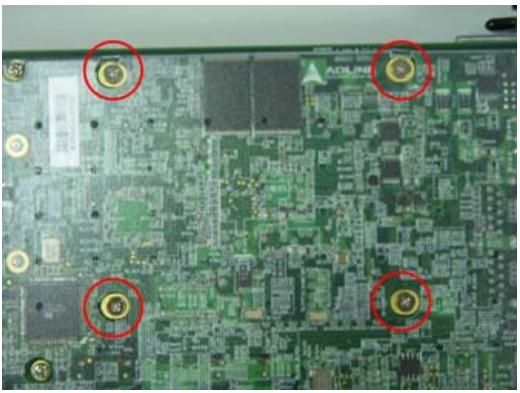


2. Attach the DB-6920SAT adapter board to the hard drive connectors.

3. Position the hard drive assembly on the cPCI-6920 so that the standoffs on the hard drive align with the screw holes on the board, and the connector on the DB-6920SAT adapter board is aligned with the board-to-board connector (CN6).

4. Press the DB-6920SAT adapter to the board-to-board connector until it is properly seated. Secure the adapter to the board with the two screws provided.

5. Secure the hard drive with four screws from the board's solder side.



6. Reinstall the DB-6920L2 adapter as required for the 8HP cPCI-6920D.

CAUTION:

When removing the hard drive, be careful to grasp the adapter board and lift upwards in a vertical motion to disconnect it from the board-to-board connector. This will avoid damaging the adapter board and connectors.

Installing a Hard Drive - cPCI-R6000D RTM

1. Attach the DB-6920SAT adapter board to the hard drive connectors.

2. Screw the hard drive to the bracket provided as shown.

3. Align the hard drive and bracket assembly with the board-to-board connector and standoffs and press down until it is properly seated. Secure the adapter and hard drive with 6x screws as shown.

5.5 Installing the cPCI-6920 to the Chassis

The cPCI-6920 may be installed in a system or peripheral slot of a 6U CompactPCI chassis. These instructions are for reference only. Refer to the user guide that comes with the chassis for more information.

1. Be sure to select the correct slot depending on the operational purpose of the module. The system power may now be powered on or off.
2. Remove the blank face cover from the selected slot, if necessary.
3. Press down on the release catches of the cPCI-6920 ejector handles.
4. Remove the black plastic caps securing the mounting screws to the front panel.
5. Align the module's top and bottom edges to the chassis card guides, and then carefully slide the module into the chassis. A slight resistance may be felt when inserting the module. If the resistance it too strong, check if there are bent pins on the backplane or if the board's connector pins are not properly aligned with connectors on the backplane. Then push the board until it is completely flush with the chassis.
6. Push the ejector handles outwards to secure the module in place, and then fasten the screws on the module front panel.
7. Connect the cables and peripherals to the board, and then turn the chassis on if necessary.

5.6 RTM (cPCI-R6000) Installation

The installation and removal procedures for a RTM are the same as those for CompactPCI boards. Because they are shorter than front boards, pay careful attention when inserting or removing RTMs.

Refer to previous sections for peripheral connectivity of all I/O ports on the RTM. When installing the cPCI-6920 Series and related RTMs, make sure the RTM is the correct matching model.

NOTE:

You must install the correct RTM to enable functions (I/O interfaces) on the rear panel. Installation of non-compatible RTMs may damage the system board and/or other RTMs.

6 Driver Installation

The cPCI-6920 drivers are available from the ADLINK All-In-One CD at **X:\cPCI\cPCI-6920**, or from the ADLINK website (**http://www.adlinktech.com**). The following describes the driver installation procedures for Windows® XP and Windows® Server 2003:

1. Install the Windows operating system before installing any driver. Most standard I/O device drivers are installed during Windows installation.
2. Install the chipset driver by running the program **...\Chipset\InfInst_AUTOL_8.6.0.1006.exe**.
3. Install the VGA driver and utilities. Refer to **Section 6.1** for details on how to install the VGA driver in Windows® operating systems.
4. Install the LAN drivers by running the program **...\LAN\PRO2KXP_13.exe**.
5. Install the SCSI driver for RTM cPCI-R6000(D) if required. Refer to **Section 6.2**.

We recommend using the drivers provided on the ADLINK All-in-One CD or downloaded from the ADLINK website to ensure compatibility. Contact ADLINK to get support for VxWorks BSP drivers.

6.1 Installing the VGA Driver

1. Click **Start**, right-click on **My Computer**, then select **Properties** from the drop-down menu.
2. Click on the **Hardware** tab, then click **Device Manager**.
3. Right-click on the **Video Controller** (VGA Compatible) item, then click **Properties** from the drop-down menu.
4. From the **General** tab, click **Reinstall Driver**.
5. Click **Next** when the **Upgrade Device Driver Wizard** window appears.
6. Select **Search** for a suitable driver for my device (recommended), then click **Next**.
7. Check the **Specify a location** option, and then click **Next**.
8. When prompted to locate the file, click **Browse**, then select the **C2_29263.inf** from this directory on the ADLINK All-In-One CD: **…\VGA\2KXP_INF**.
9. When the file is found, click **OK**, then click **Next**.
10. Follow screen procedures to install the drivers, and then restart the system to complete installation.

6.2 Installing the SCSI Driver

The SCSI driver installation procedure for Windows XP is described as below. It is not necessary to install the SCSI driver on Windows 2003 Server as it has a built-in driver.

1. Click **Start**, right-click on **My Computer**, then select **Properties** from the drop-down menu.
2. Click on the **Hardware** tab, then click **Device Manager**.
3. Right-click on the **Video Controller** (VGA Compatible) item, then click **Properties** from the drop-down menu.
4. From the **General** tab, click **Reinstall Driver**.
5. Select **Yes**, this time only and click **Next** when the **Upgrade Device Driver Wizard** window appears.
6. Select **Install from a list on specific location** [Advanced], then click **Next**.
7. Uncheck **Search removable media** [floppy, CD-ROM...], and check **Include this location in the search:**, then click **Browse**.
8. Select the **xp_x86** folder from this directory on the ADLINK All-In-One CD: **…X:\cPCI\cPCI-6920\SCSI**.
9. Click **OK**, then click **Next**.
10. Click **Continue Anyway** to go on, and click **Finish** to complete the installation.

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7 Utilities

7.1 Watchdog Timer

This section describes the operation of the cPCI-6920's watchdog timer (WDT). The primary function of the WDT is to monitor the cPCI-6920's operation and to reset the system if a software application fails to function as programmed. The following WDT functions may be controlled using a software application:

- enabling and disabling
- reloading timeout value

The cPCI-6920 custom WDT circuit is implemented using the internal IO of the Winbond SuperIO W83627UHG which is at 2Eh of LPC. The basic functions of the WDT include:

- Starting the timer countdown
- Enabling or disabling WDT
- Enabling or disabling WDT countdown LED ON
- Reloading the timeout value to keep the watchdog from timing out
- Setting the range of the timeout period from 1 to 15300 seconds
- Sending a RESET signal to the system when the watchdog times out

Using the Watchdog in an Application

The following section describes using the WDT functions in an application. The WDT reset function is explained in the previous section. This can be controlled through the registers in the cPCI-6920's SuperIO.

An application using the reset feature enables the watchdog function, sets the count-down period, and reloads the timeout value periodically to keep it from resetting the system. If the timer countdown value is not reloaded, the watchdog resets the system hardware after its counter reaches zero.

ADLINK provides a demo DOS utility in the ADLINK All-In-One CD. You can find it in the following directory: X:\cPCI\cPCI-6920\WDT.

Sample Code

The sample program written in C shown below offers an interactive way to test the Watchdog Timer under DOS.

```
#include<stdio.h>
#include<dos.h>

static unsigned int W83627UHG_ioPort = 0x2e;

void Enter_W83627UHG_Config(unsigned int flag)
{
     if(flag) W83627UHG_ioPort = 0x4e;
     outportb(W83627UHG_ioPort, 0x87);
     outportb(W83627UHG_ioPort, 0x87);
}

void Get_W83627UHG_ID(unsigned int &ID1, unsigned int
     &ID2)
{
     outportb(W83627UHG_ioPort, 0x20);
     ID1 = inportb(W83627UHG_ioPort+1);
     outportb(W83627UHG_ioPort, 0x21);
     ID2 = inportb(W83627UHG_ioPort+1);
}

void W83627UHG_WDT_Run(unsigned int count_value, unsigned
     int PLEDflag)
{
     unsigned int tempCount, registerValue;

     outportb(W83627UHG_ioPort, 0x07);
     outportb(W83627UHG_ioPort+1, 8); // CR07 set Logical
     Device 8

     if(count_value >= 60)
     {
          outportb(W83627UHG_ioPort, 0xf5);
          registerValue = inportb(W83627UHG_ioPort+1);
          registerValue |= 0x04;
          outportb(W83627UHG_ioPort+1, registerValue); /
     / set Minute mode
```

```
        tempCount = count_value / 60;
        if((count_value%60) > 30)
            tempCount++;
        if(tempCount > 255)
            tempCount = 255;
        printf("WDT timeout in %d minutes.\n",
tempCount);
}
else
{
        outportb(W83627UHG_ioPort, 0xf5);
        registerValue = inportb(W83627UHG_ioPort+1);
        registerValue &= 0xfb;
        outportb(W83627UHG_ioPort+1, registerValue); /
/ set second mode

        tempCount = count_value;
}

if(tempCount)
{
        outportb(W83627UHG_ioPort, 0x30);
        registerValue = inportb(W83627UHG_ioPort+1);
        registerValue |= 0x01;
        outportb(W83627UHG_ioPort+1, registerValue); /
/ set WDTO# and PLED are active.

        outportb(W83627UHG_ioPort, 0xf5);
        registerValue = inportb(W83627UHG_ioPort+1);
        registerValue |= 0x02;
        outportb(W83627UHG_ioPort+1, registerValue); /
/ Enable KCB reset.

        if(PLEDflag)
        {
            outportb(W83627UHG_ioPort, 0x07);
            outportb(W83627UHG_ioPort+1, 9); // CR07
set Logical Device 9

            outportb(W83627UHG_ioPort, 0x30);
            registerValue =
inportb(W83627UHG_ioPort+1);
```

```
            registerValue |= 0x02; // set GPIO2 is
active
            outportb(W83627UHG_ioPort+1,
registerValue);

            outportb(W83627UHG_ioPort, 0xe4);
            registerValue =
inportb(W83627UHG_ioPort+1);
            registerValue &= 0xf7; // set GPIO23 is
output function
            outportb(W83627UHG_ioPort+1,
registerValue);

            outportb(W83627UHG_ioPort, 0xe5);
            registerValue =
inportb(W83627UHG_ioPort+1);
            registerValue &= 0xf7; // set GPIO23 is
Low
            outportb(W83627UHG_ioPort+1,
registerValue);
      }

      printf("WDT timeout in %d seconds.\n",
tempCount);
}
else
{
      outportb(W83627UHG_ioPort, 0x07);
      outportb(W83627UHG_ioPort+1, 9); // CR07 set
Logical Device 9

      outportb(W83627UHG_ioPort, 0x30);
      registerValue = inportb(W83627UHG_ioPort+1);
      registerValue |= 0x02; // set GPIO2 is active
      outportb(W83627UHG_ioPort+1, registerValue);

      outportb(W83627UHG_ioPort, 0xe4);
      registerValue = inportb(W83627UHG_ioPort+1);
      registerValue &= 0xf7; // set GPIO23 is output
function
      outportb(W83627UHG_ioPort+1, registerValue);

      outportb(W83627UHG_ioPort, 0xe5);
```

```
            registerValue = inportb(W83627UHG_ioPort+1);
            registerValue |= 0x08; // set GPIO23 is High
            outportb(W83627UHG_ioPort+1, registerValue);

            printf("WDT is Disabled.\n");
      }

      outportb(W83627UHG_ioPort, 0x07);
      outportb(W83627UHG_ioPort+1, 8); // CR07 set Logical
      Device 8
      outportb(W83627UHG_ioPort, 0xf6);
      outportb(W83627UHG_ioPort+1, tempCount); // set WDT
      count value..
}

void Exit_W83627UHG_Config(unsigned int flag)
{
      if(flag) W83627UHG_ioPort = 0x4e;
      outportb(W83627UHG_ioPort, 0xaa);
```

7.2 Preboot Execution Environment (PXE)

The cPCI-6920 series supports the Intel® Preboot Execution Environment (PXE) that is capable of booting up or executing an OS installation through an Ethernet ports. To use PXE, there must be a DHCP server on the network with one or more servers running PXE and MTFTP services. It could be a Windows® 2003 server running DHCP, PXE, and MTFTP services or a dedicated DHCP server with one or more additional servers running PXE and MTFTP services.

To build a network environment with PXE support:

1. Setup a DHCP server with PXE tag configuration
2. Install the PXE and MTFTP services
3. Make a boot image file on the PXE server (i.e. the boot server)
4. Enable the PXE boot function on the client computer

8 BIOS Setup

The following chapter describes basic navigation for the AMIBIOS®8 BIOS setup utility.

8.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keyboard when you see the following text prompt:
   < Press DEL to run Setup >
3. After you press the < Delete > key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu, such as Chipset and Power menus.

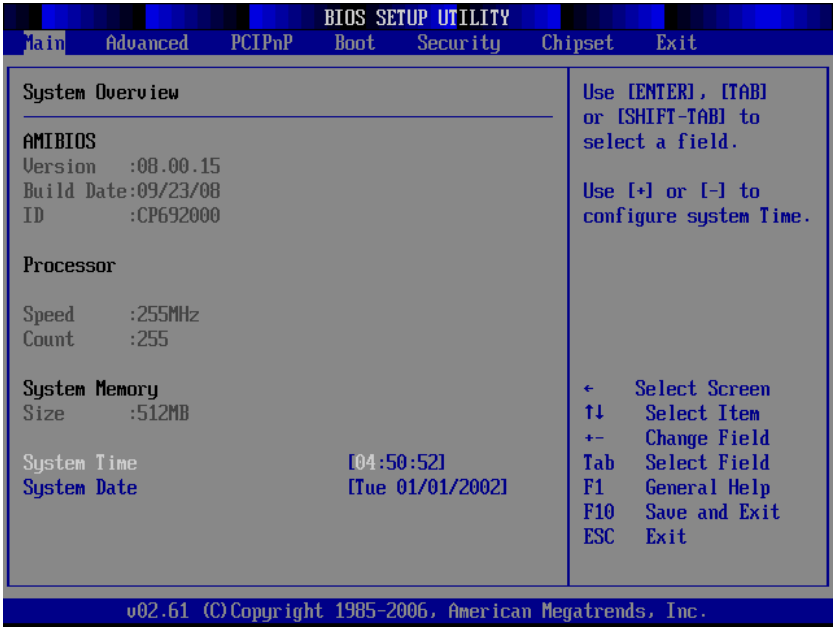
Note: In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

Setup Menu

The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed" options cannot be configured, "Blue" options can be.

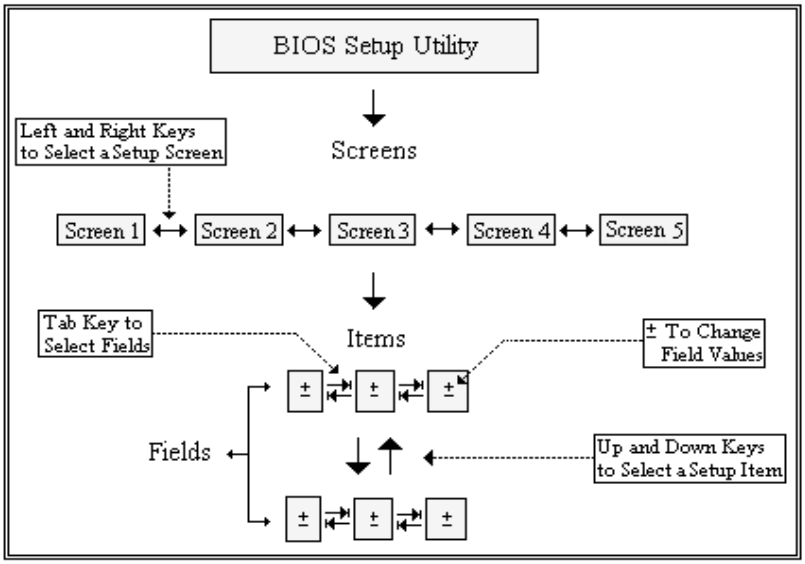
The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.



Navigation

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process.

These keys include < F1 >, < F10 >, < Enter >, < ESC >, < Arrow > keys, and so on. .



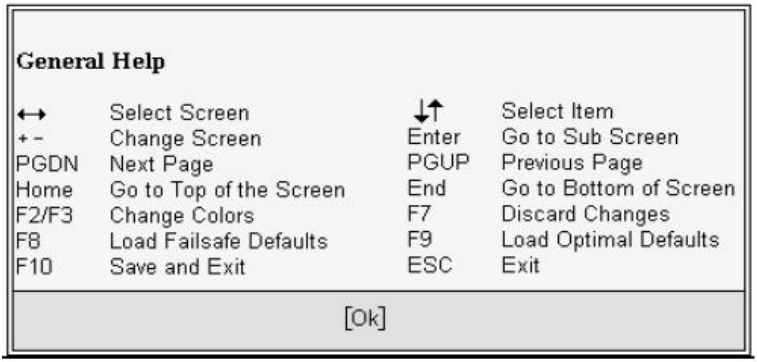
Note: There is a hot key legend located in the right frame on most setup screens.

The < F8 > key on your keyboard is the Fail-Safe key. It is not displayed on the key legend by default. To set the Fail-Safe settings of the BIOS, press the < F8 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The Fail-Safe settings allow the motherboard to boot up with the least amount of options set. This can lessen the probability of conflicting settings.

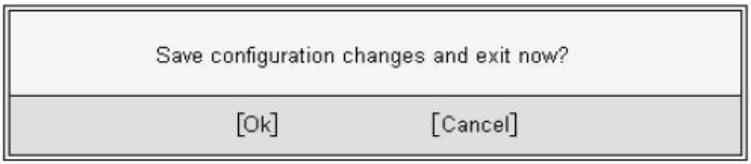
Hotkey Descriptions

F1 The < F1 > key allows you to display the General Help screen.

Press the < F1 > key to open the General Help screen.

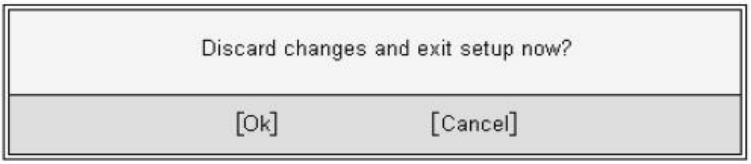


F10 The < F10 > key allows you to save any changes you have made and exit Setup. Press the < F10 > key to save your changes. The following screen will appear:



Press the < Enter > key to save the configuration and exit. You can also use the < Arrow > key to select Cancel and then press the < Enter > key to abort this function and return to the previous screen.

ESC The < Esc > key allows you to discard any changes you have made and exit the Setup. Press the < Esc > key to exit the setup without saving your changes. The following screen will appear:

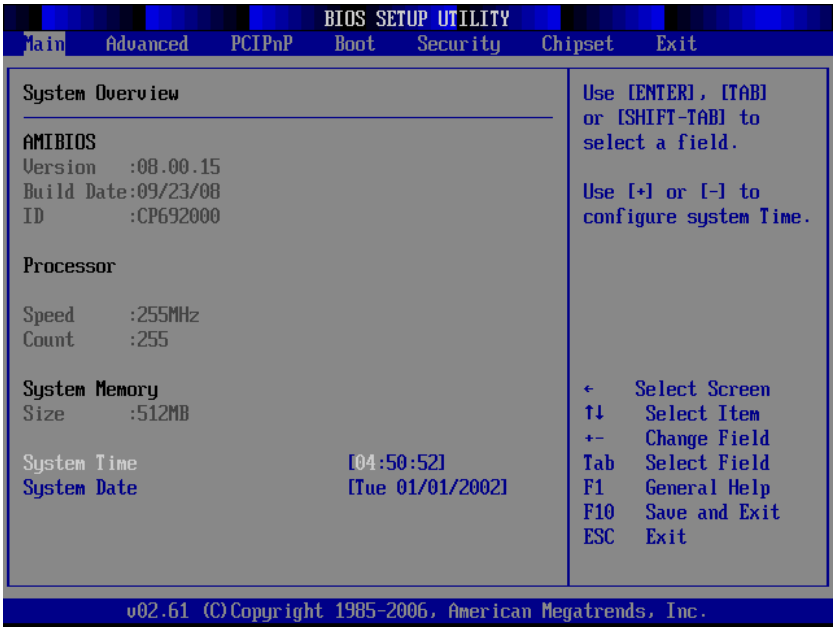


Press the < Enter > key to discard changes and exit. You can also use the < Arrow > key to select Cancel and then press the < Enter > key to abort this function and return to the previous screen.

Enter The < Enter > key allows you to display or change the setup option listed for a particular setup item. The < Enter > key can also allow you to display the setup sub-screens.

8.2 Main Setup

When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



System Time/System Date

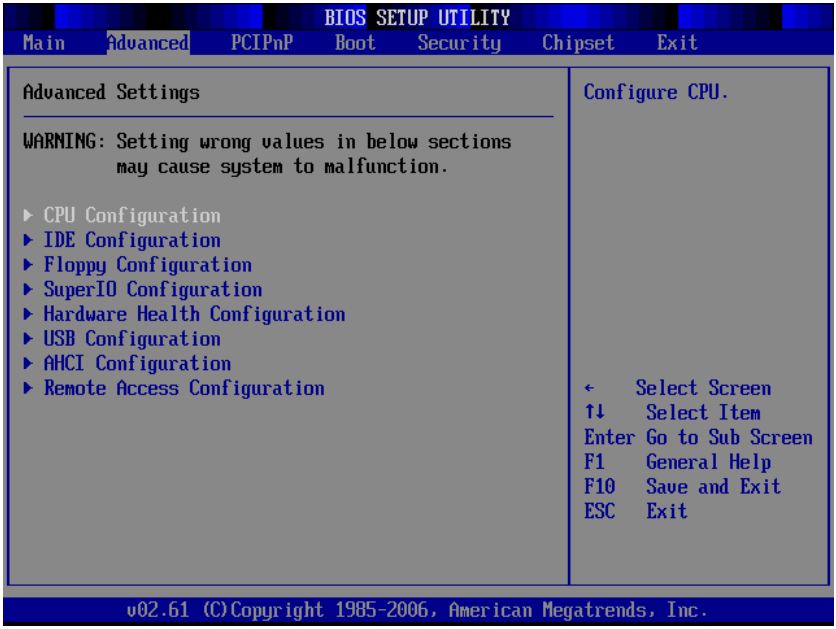
Use this option to change the system time and date. Highlight System Time or System Date using the < Arrow > keys. Enter new values using the keyboard. Press the < Tab > key or the < Arrow > keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

8.3 Advanced BIOS Setup

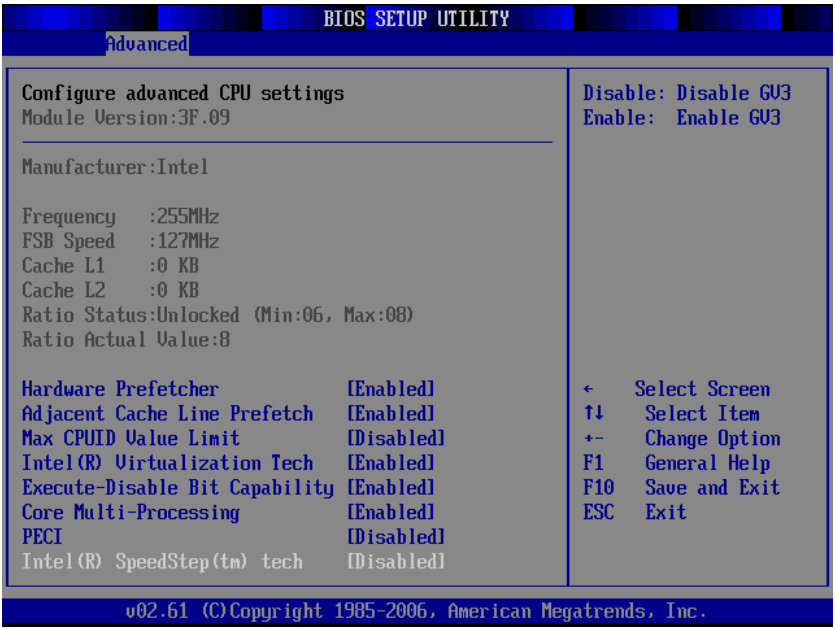
Select the Advanced tab from the setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as SuperIO Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the < Arrow > keys. The Advanced BIOS Setup screen is shown below.

The sub menus are described on the following pages.



8.3.1 CPU Configuration

You can use this screen to select options for the CPU Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the CPU Configuration screen is shown below.



Hardware Prefetcher

When enabled, the processor's hardware prefetcher will be enabled and allowed to automatically prefetch data and code for the processor. When disabled, the processor's hardware prefetcher will be disabled.

Adjacent Cache Line Prefetch

When enabled, the processor will retrieve the currently requested cache line, as well as the subsequent cache line.

When disabled, the processor will only retrieve the currently requested cache line.

Max CPUID Value Limit

When the computer is booted up, the operating system executes the CPUID instruction to identify the processor and its capabilities. Before it can do so, it must first query the processor to find out the highest input value CPUID recognized. This determines the kind of basic information CPUID can provide the operating system. This option allows you to circumvent problems with older operating systems.

When Enabled, the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When Disabled, the processor will return the actual maximum CPUID input value of the processor when queried.

Intel(R) Virtualization Tech

Intel Virtualization Technology is a set of platform features that support virtualization of platform hardware and multiple software environmentss. When enabled, it offers data center managers the ability to consolidate multiple workloads on one physical server system.

Execute-Disable Bit Capability

Intel's Execute Disable Bit functionality can help prevent certain classes of malicious buffer overflow attacks when combined with a supporting operating system. Execute Disable Bit allows the processor to classify areas in memory by where application code can execute and where it cannot. When a malicious worm attempt to insert code in the buffer, the processor disables code execution, preventing damage and worm propagation.

Core Multi-Processing

This item enables/disables multi-core processing functionality for multi-core processors.

PECI

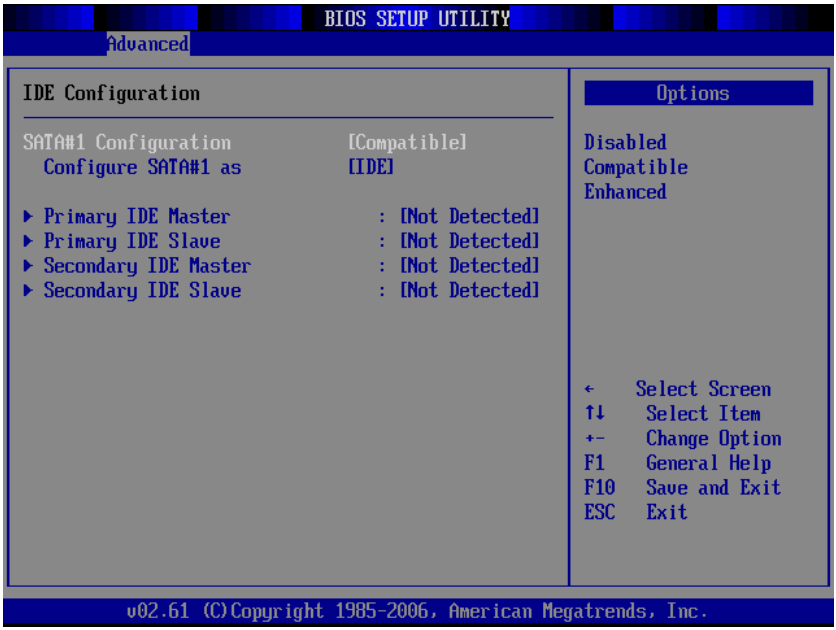
Enables/disables the Platform Environment Control Interface (PECI).

Intel(R) Speedstep(tm) Tech

Intel SpeedStep technology allows the system to dynamically adjust processor voltage and core frequency, which can result in decreased average power consumption and decreased average heat production.

8.3.2 IDE Configuration

You can use this screen to select options for the IDE Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the IDE Configuration screen is shown below.



SATA#1 Configuration

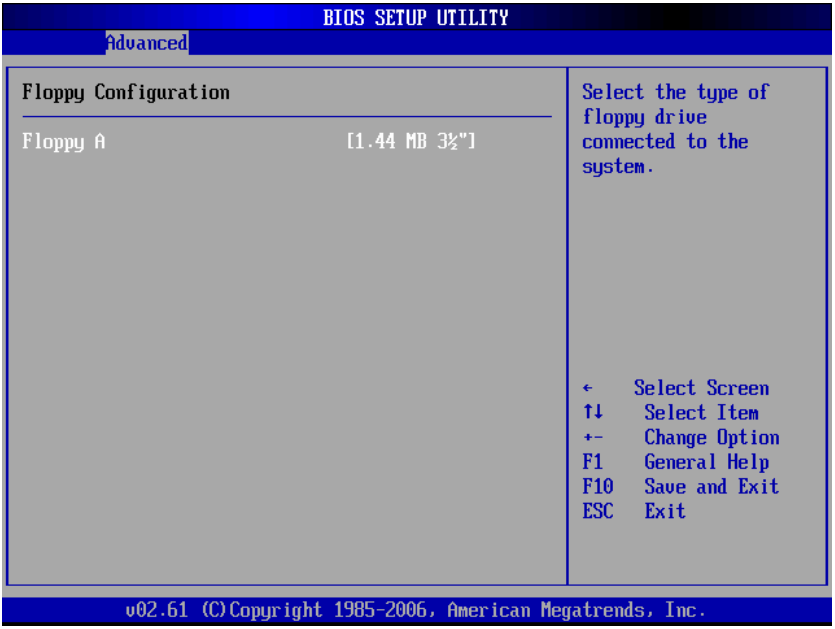
This item specifies which mode the SATA channels should be initialized in. The settings are **Disabled**, **Compatible** and **Enhanced**. When running in Compatible mode, SATA channel can be configured as a legacy IDE channel.

IDE Master/Slave

Select one of the hard disk drives to configure it. Press < Enter > to access its sub menu.

8.3.3 Floppy Configuration

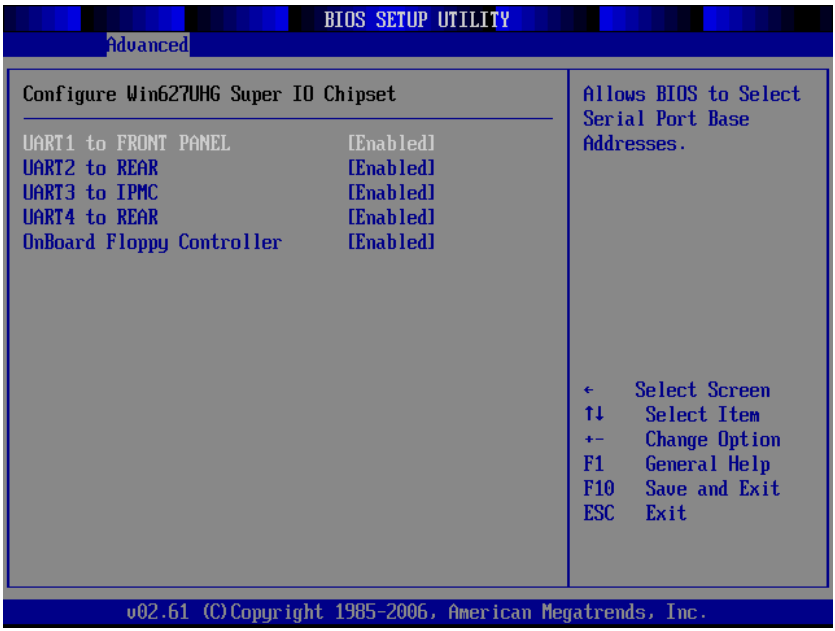
You can use this screen to select options for the Floppy Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the Floppy Configuration screen is shown below.



Options: 360 KB 5 ¼", 1.2 MB 5 ¼", 720 KB 3 ½", 1.44 MB 3 ½", 2.88 MB 3 ½".

8.3.4 Super IO Configuration

You can use this screen to select options for the Super IO settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



UART1 to FRONT PANEL

This option sets the UART1 to the Front Panel.

- **Disabled:** Set this value to prevent the serial port from accessing any system resources. When this option is set to Disabled, the serial port physically becomes unavailable.
- **Enabled:** Set this value to allow the serial port to use 3F8 as its I/O port address and IRQ 4 for the interrupt address.

UART2 to REAR

This option sets the UART2 to Rear I/O.

- **Disabled:** Set this value to prevent the serial port from accessing any system resources. When this option is set to Disabled, the serial port physically becomes unavailable.
- **Enabled:** Set this value to allow the serial port to use 2F8 as its I/O port address and IRQ 10 for the interrupt address.

UART3 to IPMC

This option sets the UART3 to IPMC.

- **Disabled:** Set this value to prevent the serial port from accessing any system resources. When this option is set to Disabled, the serial port physically becomes unavailable.
- **Enabled:** Set this value to allow the serial port to use 3E8 as its I/O port address and IRQ 3 for the interrupt address.

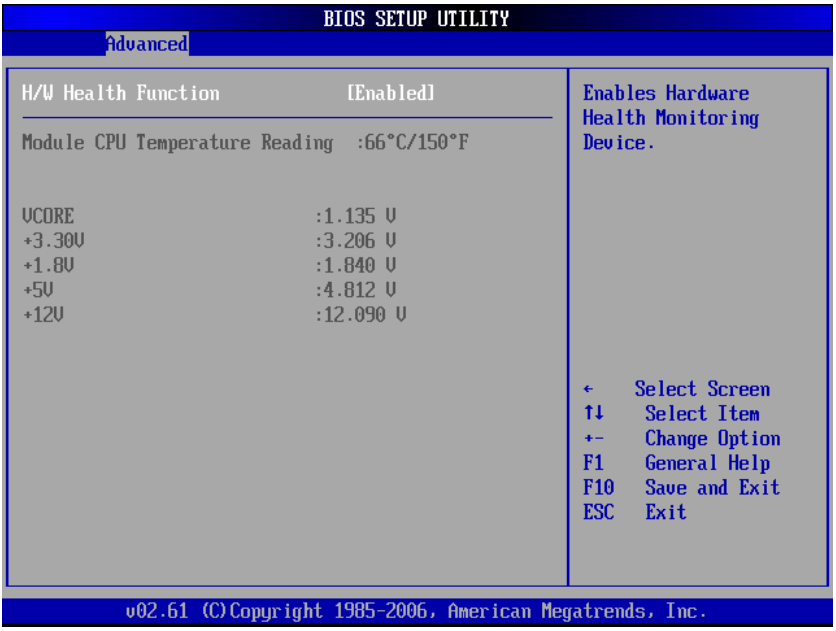
UART4 to REAR

This option sets the UART4 to Rear I/O.

- **Disabled:** Set this value to prevent the serial port from accessing any system resources. When this option is set to Disabled, the serial port physically becomes unavailable.
- **Enabled:** Set this value to allow the serial port to use 2E8 as its I/O port address and IRQ 11 for the interrupt address.

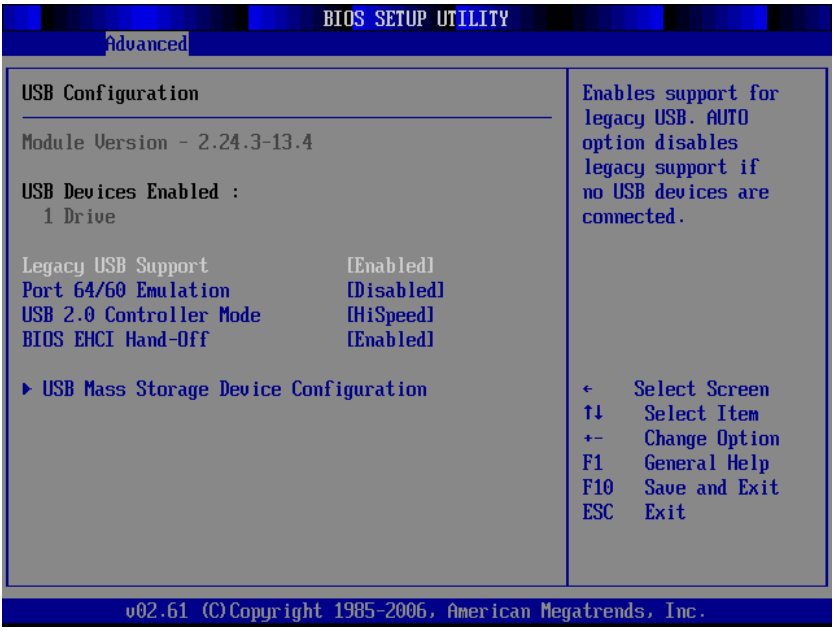
8.3.5 Hardware Health Configuration

This option displays the current status of all of the monitored hardware devices/components such as voltages and temperatures. The options are Enabled and Disabled.



8.3.6 USB Configuration

You can use this screen to select options for the USB Configuration. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



Legacy USB Support

Legacy USB Support refers to USB mouse and keyboard support. Normally if this option is not enabled, any attached USB mouse or USB keyboard will not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there are no USB drivers loaded on the system. Set this value to enable or disable the Legacy USB Support.

- **Disabled:** Set this value to prevent the use of any USB device in DOS or during system boot.
- **Enabled:** Set this value to allow the use of USB devices during boot and while using DOS.
- **Auto:** This option auto detects USB Keyboards or Mice and if found, allows them to be utilized during boot and while using DOS.

Port 64/60 Emulation

This option uses USB to receive the IO port 64/60 trap to emulate the legacy keyboard controller.

USB 2.0 Controller Mode

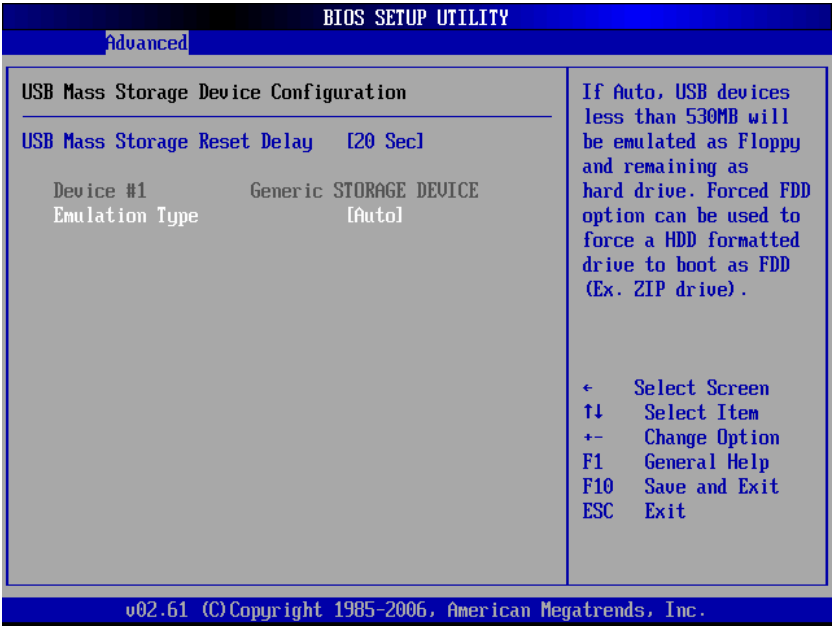
The USB 2.0 Controller Mode configures the data rate of the USB port. The options are FullSpeed (12 Mbps) and HiSpeed (480 Mbps).

BIOS EHCI hand-off

This option provides a workaround for operating systems without ECHI hand-off support. The EHCI ownership change should claim by EHCI driver.

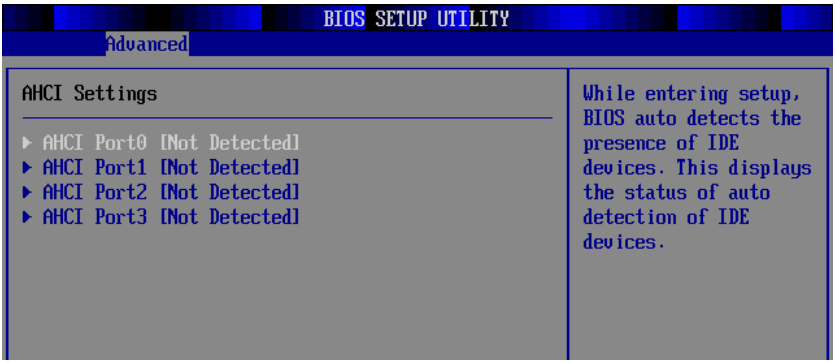
USB Mass Storage Device Configuration

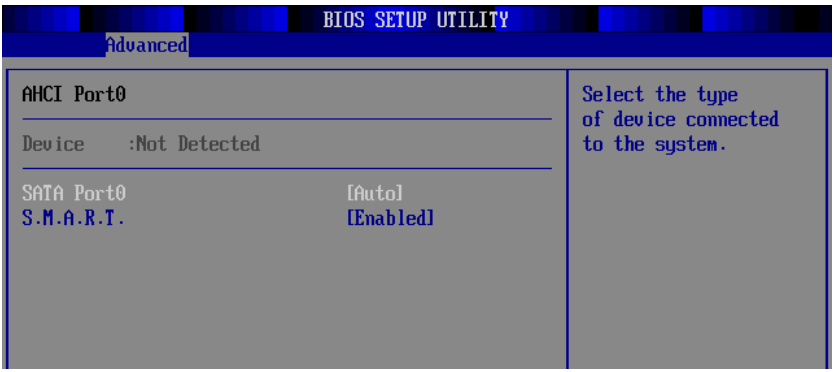
This is a submenu for configuring the USB Mass Storage Class Devices when BIOS finds they are in use on USB ports. Emulation Type can be set according to the type of attached USB mass storage device(s). If set to Auto, USB devices less than 530MB will be emulated as Floppy and those greater than 530MB will remain as hard drive. The Forced FDD option can be used to force a hard disk type drive (such as a Zip drive) to boot as FDD.



8.3.7 AHCI Configuration

Select the Advanced tab from the setup screen to enter the AHCI Configuration Setup screen. You can display the AHCI Setup options by highlighting it using the < Arrow > keys.





SATA Port0/1/2/3

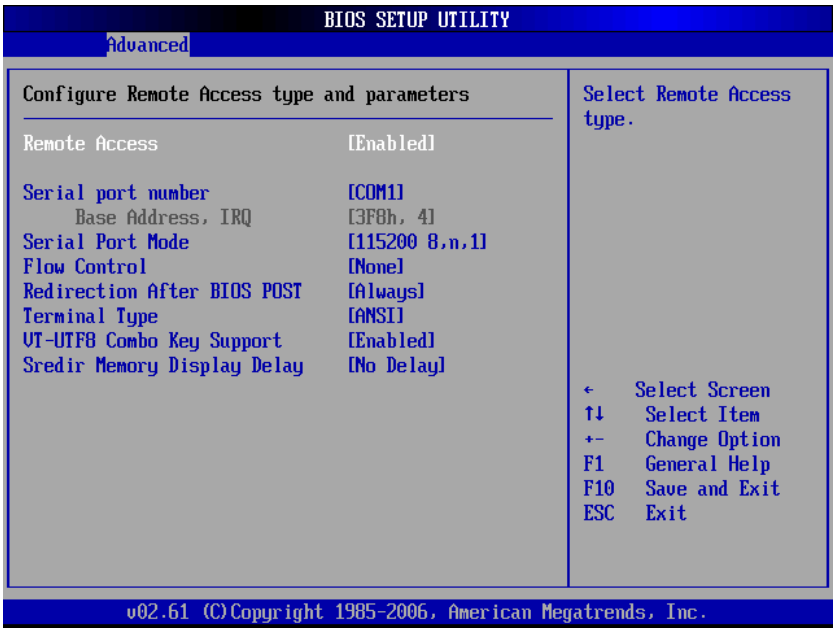
Select the type of device connected to the system.

S.M.A.R.T

S.M.A.R.T. (Self-Monitoring Analysis and Reporting Technology) is a utility that monitors your disk status to predict hard disk failure.

8.3.8 Remote Access Configuration

Remote access configuration provides the settings to allow remote access by another computer to get POST messages and send commands through serial port access.



Remote Access

Select this option to Enable or Disable the BIOS remote access feature.

Note: Enabling Remote Access requires a dedicated serial port connection. Once both serial ports are configured to disabled, you should set this value to Disabled or it may cause abnormal boot.

Serial Port Number

Select the serial port you want to use for the remote access interface. You can set the value for this option to COM1, COM2 or COM4.

Note: If you have changed the resource assignment of the serial ports in Advanced> SuperIO Configuration, you must Save Changes and Exit, reboot the system, and enter the setup menu again in order to see those changes reflected in the available Remote Access options.

Serial Port Mode

Select the baud rate you want the serial port to use for console redirection. The options are 115200 8,n,1; 57600 8,n,1; 19200 8,n,1; and 09600 8,n,1.

Flow Control

Set this option to select Flow Control for console redirection. The settings for this value are None, Hardware, or Software.

Redirection After BIOS POST

This option allows you to set Redirection configuration after BIOS POST. The settings for this value are Disabled, Boot Loader, or Always.

- **Disabled:** Set this value to turn off the redirection after POST
- **Boot Loader:** Set this value to allow the redirection to be active during POST and Boot Loader.
- **Always:** Set this value to allow the redirection to be always active.

Terminal Type

This option is used to select either VT100/VT-UTF8 or ANSI terminal type. The settings for this value are ANSI, VT100, or VT-UTF8.

VT-UTF8 Combo Key Support

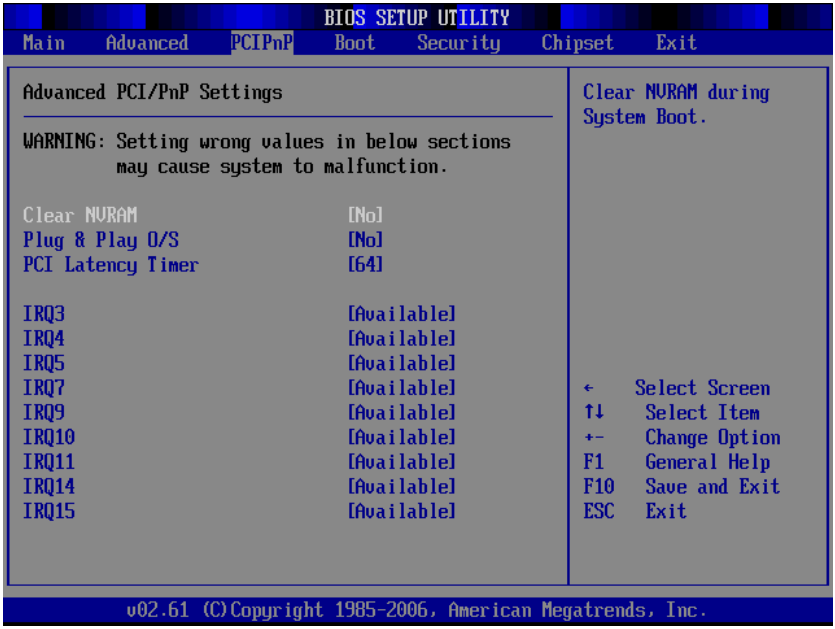
This option enables VT-UTF8 Combination Key Support for ANSI/VT100 terminals. The settings for this value are Enabled or Disabled.

Sredir Memory Display Delay

This option gives the delay in seconds to display memory information. The options for this value are No Delay, Delay 1 Sec, Delay 2 Sec, or Delay 4 Sec.

8.4 Advanced PCI/PnP Settings

Select the PCI/PnP tab from the setup screen to enter the Plug and Play BIOS Setup screen. You can display a Plug and Play BIOS Setup option by highlighting it using the < Arrow > keys. The Plug and Play BIOS Setup screen is shown below.



Clear NVRAM

Set this to enable/disable Clear NVRAM during system boot

Plug & Play O/S

- **No:** Let the BIOS configure all the devices in the system.
- **Yes:** Let the operating system configure Plug and Play (PnP) devices not required for boot if your system has a Plug and Play operating system.

PCI Latency Timer

Value in units of PCI clocks for the PCI device latency timer register.

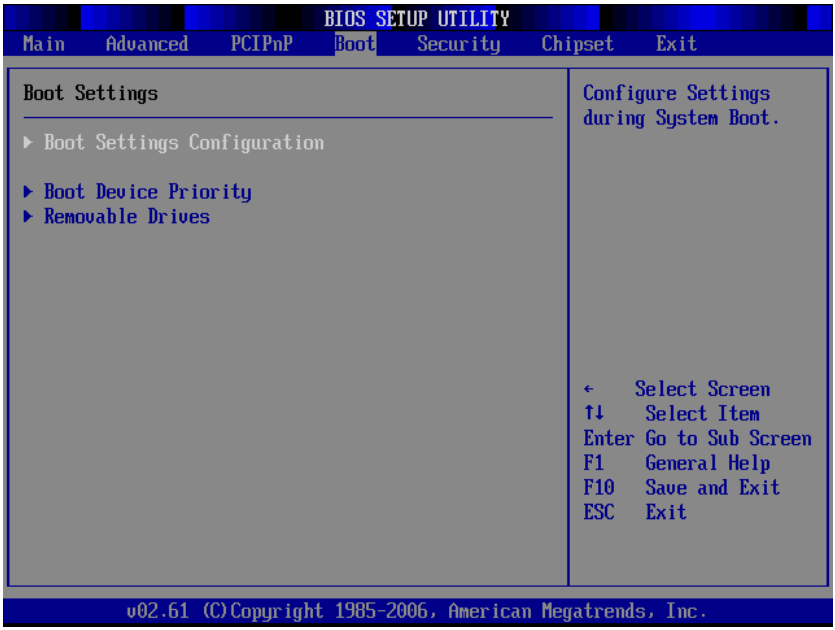
IRQ Channel

Set this value to allow the IRQ/DMA channel settings to be modified.

- **Available:** This setting allows the specified IRQ/DMA channel to be used by a PCI/PnP device.
- **Reserved:** This setting allows the specified IRQ/DMA channel to be used by a legacy ISA device.

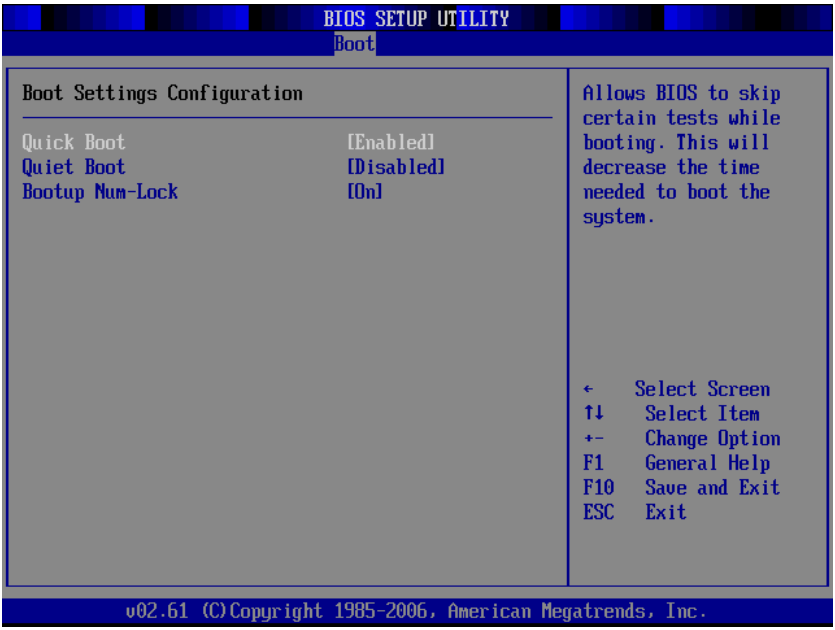
8.5 Boot Settings

Select the Boot tab from the setup screen to enter the Boot BIOS Setup screen. You can select any of the items in the left frame of the screen, such as Boot Device Priority, to go to the sub menu for that item. You can display a Boot BIOS Setup option by highlighting it using the < Arrow > keys. The Boot Settings screen is shown below:



8.5.1 Boot Settings Configuration

Use this screen to select options for the Boot Settings Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



Quick Boot

Enabling this setting will cause the BIOS power-on self test routine to skip some of its tests during bootup for faster system boot.

Quiet Boot

When this feature is **enabled**, the BIOS will display the OEM logo during the boot-up sequence, hiding normal POST messages.

When it is **disabled**, the BIOS will display the normal POST messages, instead of the OEM logo.

Bootup Num-Lock

This option sets the Num Lock status when the system is powered on. Setting to [On] will turn on the Num Lock key when the system is powered on. Setting to [Off] will allow users to use the arrow keys on the numeric keypad.

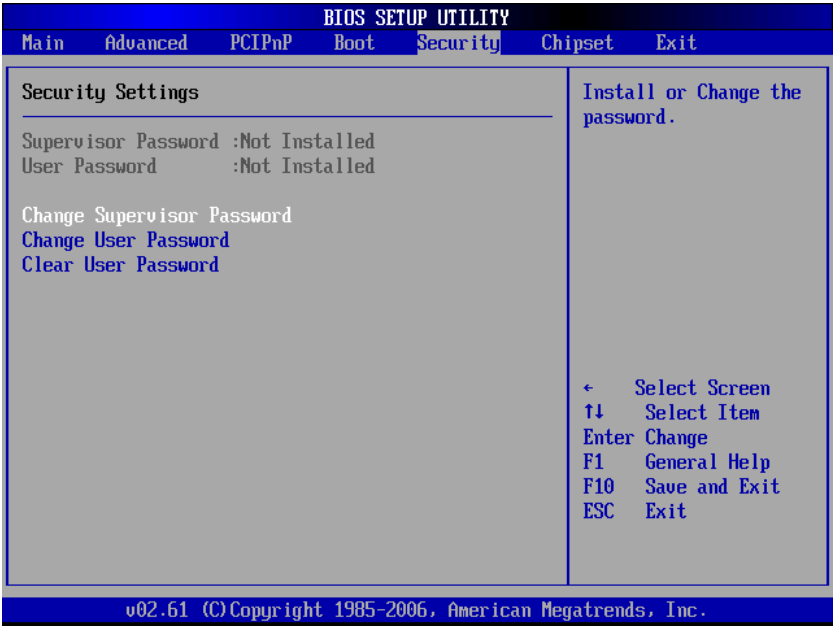
8.5.2 Boot Device Priority

The items allow you to set the sequence of boot devices where BIOS attempts to load the disk operating system. First press <Enter> to enter the sub-menu. Then you may use the arrow keys to select the desired device, then press <+>, <-> or <PageUp>, <PageDown> key to move it up/down in the priority list.

8.5.3 Boot Device Groups

The Boot devices are listed in groups by device type. First press <Enter> to enter the sub-menu. Then you may use the arrow keys to select the desired device, then press <+>, <-> or <PageUp>, <PageDown> key to move it up/down in the priority list. Only the first device in each device group will be available for selection in the Boot Device Priority option.

8.6 Security Setup



Password Support

Two Levels of Password Protection

Provides both a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first.

The system can be configured so that all users must enter a password every time the system boots or when Setup is executed, using either or either the Supervisor password or User password.

The Supervisor and User passwords activate two different levels of password security. If you select password support, you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed. Make sure you write it down. If you forget it, you must drain NVRAM and re-configure.

Remember the Password

Keep a record of the new password when the password is changed. If you forget the password, you must erase the system configuration information in NVRAM.

To access the sub menu for the following items, select the item and press < Enter >:

- Change Supervisor Password
- Change User Password
- Clear User Password

Supervisor Password

Indicates whether a supervisor password has been set.

User Password

Indicates whether a user password has been set.

Change Supervisor Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to change the supervisor password.

Change User Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to change the user password.

Clear User Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to clear the user password.

Change Supervisor Password

Select Change Supervisor Password from the Security Setup menu and press < Enter >.

Enter New Password:

Type the password and press < Enter >. The screen does not display the characters entered. Retype the password as prompted

and press < Enter >. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after completes.

Change User Password

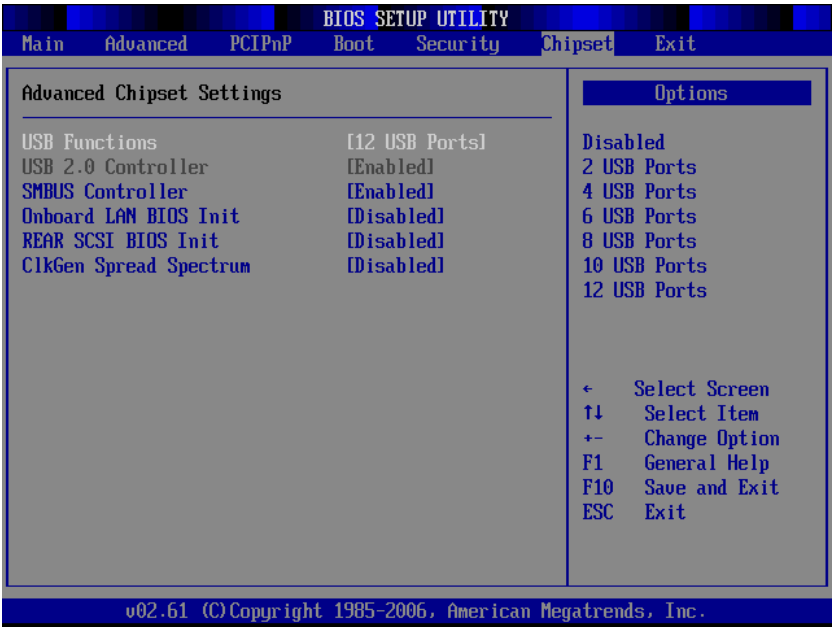
Select Change User Password from the Security Setup menu and press < Enter >.

Enter New Password:

Type the password and press < Enter >. The screen does not display the characters entered. Retype the password as prompted and press < Enter >. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after completes.

8.7 Chipset Setup

Select the Chipset tab from the setup screen to enter the Chipset BIOS Setup screen. You can select any of the items in the left frame of the screen to go to the sub menu for that item. The Chipset BIOS Setup screen is shown below.



USB Functions

Set this value to allow the system to disable, enable, and select a set number of onboard USB ports.

USB 2.0 Controller

This option takes effect only when USB Functions are enabled. Enabling will allow USB 2.0 functionality to all USB ports.

SMBus Controller

Set this value to enable/disable the SMBus Controller

Onboard LAN BIOS Init

Set this value to enable/disable the invoking of onboard LAN's PXE ROM. Disabling can shorten the POST time by not initializing LAN PXE ROM. Enable it if boot from LAN is needed.

Rear SCSI BIOS Init

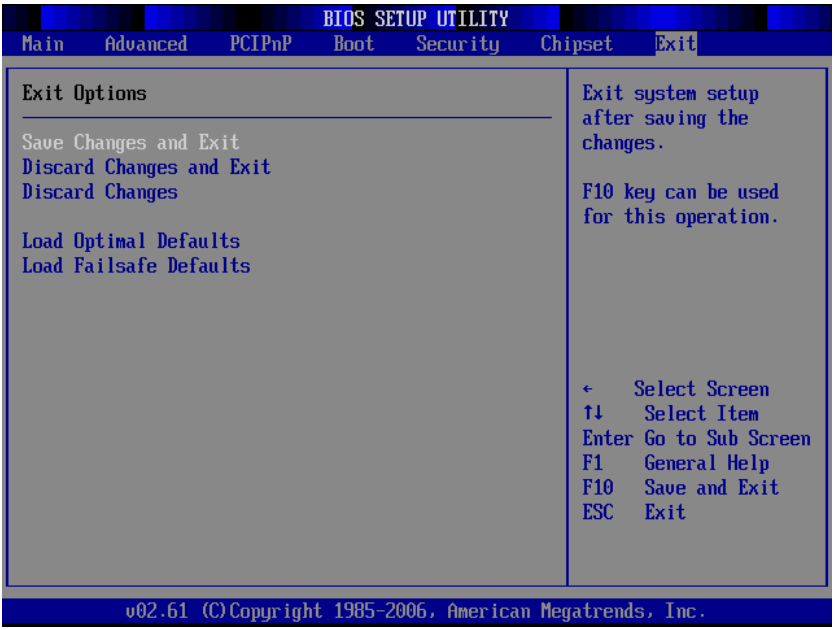
Set this value to enable/disable the invoking of REAR SCSI ROM. Disabling can shorten the POST time without initializing SCSI ROM. Enable it if boot from SCSI is needed.

ClkGen Spread Spectrum

This field enables/disables support of the ClkGen Spread Spectrum function.

8.8 Exit Menu

Select the Exit tab from the setup screen to enter the Exit BIOS Setup screen. You can display an Exit BIOS Setup option by highlighting it using the < Arrow > keys. The Exit BIOS Setup screen is shown below.



Save Changes and Exit

When you have completed the system configuration changes, select this option to leave Setup and reboot the computer so the new system configuration parameters can take effect.

Save Configuration Changes and Exit Now?

[Ok] [Cancel]

appears in the window. Select Ok to save changes and exit.

Discard Changes and Exit

Select this option to quit Setup without making any permanent changes to the system configuration.

Discard Changes and Exit Setup Now?

[Ok] [Cancel]

appears in the window. Select Ok to discard changes and exit.

Discard Changes

Select Discard Changes from the Exit menu and press < Enter >.

Select Ok to discard changes.

Load Optimal Defaults

Automatically sets all Setup options to a complete set of default settings when you select this option. The Optimal settings are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Optimal Setup options if your computer is experiencing system configuration problems.

Select Load Optimal Defaults from the Exit menu and press < Enter >.

This page intentionally left blank.

Select Ok to load optimal defaults.

Load Failsafe Defaults

Automatically sets all Setup options to a complete set of default settings when you select this option. The Failsafe settings are designed for maximum system stability, but not maximum performance. Select the FailSafe Setup options if your computer is experiencing system configuration problems.

Select Load Fail-Safe Defaults from the Exit menu and press < Enter >.

Load FailSafe Defaults?

[Ok] [Cancel]

appears in the window. Select Ok to load FailSafe defaults.

9 IPMI User Guide

9.1 Introduction

This chapter is written for those who already have a basic understanding of the newest implementation of the baseboard management controller (BMC) of the Intelligent Platform Management Interface (IPMI) specification rev. 1.5. It also describes the OEM extension IPMI command usages which are not listed in the IPMI specification.

9.2 Summary of Commands Supported by IPMC

The table below lists all the commands supported by the IPMC. The rightmost column indicates if the command is required by PICMG 3.0/PICMG 2.9, or is optional.

Command	IPMI Spec	NetFn	CMD	IPM Controller Req (PICMG 3.0/2.9)
IPM Device "Global" Commands				
Get Device ID	17.1	App	01h	Mandatory/Mandatory
Cold Reset	17.2	App	02h	Optional/Optional
Warm Reset	17.3	App	03h	Optional/Optional
Get Self Test Results	17.4	App	04h	Mandatory/Mandatory
Get Device GUID	17.8	App	08h	Optional/Optional
Broadcast "Get Device ID"	17.9	App	01h	Mandatory/Mandatory
IPMI Messaging Support Commands				
Send Message	18.7	App	34h	Optional/Optional
BMC Watchdog Timer				
Reset Watchdog Timer	21.5	App	22h	Mandatory/Optional
Set Watchdog Timer	21.6	App	24h	Mandatory/Optional
Get Watchdog Timer	21.7	App	25h	Mandatory/Optional
Event Commands				
Set Event Receiver	23.1	S/E	00h	Mandatory/Optional
Get Event Receiver	23.2	S/E	01h	Mandatory/Optional
Platform Event (a.k.a. "Event Message")	23.3	S/E	02h	Mandatory/Optional

Command	IPMI Spec	NetFn	CMD	IPM Controller Req (PICMG 3.0/2.9)
Sensor Device Commands				
Get Device SDR Info	29.2	S/E	20h	Mandatory/Optional
Get Device SDR	29.3	S/E	21h	Mandatory/Optional
Reserve Device SDR Repository	29.4	S/E	22h	Mandatory/Optional
Set Sensor Hysteresis	29.6	S/E	24h	Optional/Optional
Get Sensor Hysteresis	29.7	S/E	25h	Optional/Optional
Set Sensor Threshold	29.8	S/E	26h	Optional/Optional
Get Sensor Threshold	29.9	S/E	27h	Optional/Optional
Set Sensor Event Enable	29.10	S/E	28h	Optional/Optional
Get Sensor Event Enable	29.11	S/E	29h	Optional/Optional
Get Sensor Event Status	29.13	S/E	2Bh	Optional/Optional
Get Sensor Reading	29.14	S/E	2Dh	Mandatory/Optional
Get Sensor Type	29.16	S/E	2Fh	Optional/Optional
FRU Device Commands				
Get FRU Inventory Area Info	28.1	Storage	10h	Mandatory/Optional
Read FRU Data	28.2	Storage	11h	Mandatory/Optional
Write FRU Data	28.3	Storage	12h	Mandatory/Optional

9.3 OEM Commands Summary Table

Command	NetFn Code	Cmd Code
OemShowRevision	OEM (C0h)	12h
OemRescanGaInput	OEM (C0h)	22h
OemTestFunction	OEM (C0h)	30h
OemSetBlueLEDLongBlinking	OEM (C0h)	31h
OemReportGeoAddress	OEM (C0h)	F0h
OemEnableSmbus	OEM (C0h)	F2h
OemDisableSmbus	OEM (C0h)	F3h
OemDispDebugVariable	OEM (C0h)	F4h
OemResetHost	OEM (C0h)	F5h
OemPowerOff	OEM (C0h)	F6h
OemPowerOn	OEM (C0h)	F7h

OemShowRevision

This command is used to show the current information of the firmware including the firmware revision, the product ID, and additional features.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	12h	OEM defined command
Response	0	Complete Code	00h means OK
	1	A5h	Internal check byte. Always A5h
	2	*Firmware Rev	‘V’ in ASCII code for verification
	3	*Firmware Rev	Revision info high byte
	4	*Firmware Rev	Revision info low byte
	5	*Product ID	‘P’ in ASCII code for verification
	6	*Product ID	Product info high byte
	7	*Product ID	Product info low byte
	8	*Special info	‘S’ in ASCII code for verification
	9	*Special info	Addition info byte
	10	5Ah	Internal check byte. Always 5Ah

OemRescanGaInput

This command is used to rescan the geo-address input pins and reset the IPMB address according to the input value.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	22h	OEM defined command
Response	0	Complete Code	00h means OK
	1	New IPMB address	New IPMB address value

OemTestFunction

Internal test purposes only.

OemSetBlueLEDLongBlinking

This command is used to enable/disable the slow blinking of the blue HotSwap LED when a voltage is detected to be over ±5% out of range for five seconds (see Table 4-1 on page 24). Disabled by default.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	31h	OEM defined command
	2	00h or 01h	00h: disable slow blink capability 01h: enable slow blink capability
Response	0	Complete Code	00h means OK

OemReportGeoAddress

This command can report the IPMB address, the GA pin input status, and the event forwarding control value.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F0h	OEM defined command
Response	0	Complete Code	00h means OK
	1	IPMB address	IPMB address value
	2	GA value	GA pin input status
	3	Control value	Current control value of event forwarding

OemEnableSmbus

This command is used to turn on the I2C bus when it is off during boot up process. Usually BIOS will perform this command after booting in boards with ServerWorks chipset.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F2h	OEM defined command
Response	0	Complete Code	00h means OK

OemDisableSmbus

This command is used to shut down I2C bus access.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F3h	OEM defined command
Response	0	Complete Code	00h means OK

OemDispDebugVariable

This command can report up to 5 interval values for debug purposes. For developers only.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F4h	OEM defined command
Response	0	Complete Code	00h means OK
	1	*Debug variable 1	
	2	*Debug variable 2	
	3	*Debug variable 3	
	4	*Debug variable 4	
	5	*Debug variable 5	

OemResetHost

This command is implemented to control the system's status if rebooting is required. Operators can control the system remotely.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F5h	OEM defined command
Response	0	Complete Code	00h means OK

OemPowerOff

This command is implemented to control the system's status if power-off is required. Operators can control the system remotely.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F6h	OEM defined command
Response	0	Complete Code	00h means OK

OemPowerOn

This command is implemented to control the system's status if power-on is required. Operators can control the system remotely.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F7h	OEM defined command
Response	0	Complete Code	00h means OK

9.4 CompactPCI Address Map

Since more than one system may be installed in a single chassis, we allocate each IPMB address based on GA input as peripheral cards. The CompactPCI Peripheral Address Mapping Table is given below.

CompactPCI Peripheral Address Mapping			
Geo. Addr.	**IPMB Addr.**	**Geo. Addr.**	**IPMB Addr.**
0	**Disabled**	16	D0h
1	B0h	17	D2h
2	B2h	18	D4h
3	B4h	19	D6h
4	B6h	20	D8h
5	B8h	21	DAh
6	Bah	22	DCh
7	BCh	23	DEh
8	BEh	24	E0h
9	Coh	25	E2h
10	C4h	26	E4h
11	C6h	27	E6h
12	C8h	28	E8h
13	CAh	29	EAh
14	CCh	30	ECh
15	CEh	**31**	**Disabled**

9.5 Communications with IPMC

Operating systems need to use a serial port to communicate with the IPMC. The resource setting of the serial port must be IO: 0x3E8 and IRQ: 3. The communication setting of the serial port must be BaudRate: 9600, DataBit: 8, ParityCheck: None, StopBit: 1, and FlowControl: None. In Windows XP, use “COM3” to communicate with the IPMC.

9.6 IPMI Sensors List

Sensor Number	Sensor name	Normal Reading	Sensor Reading Value of IPMI Get Sensor Reading Command
01h	BMC Watchdog		Timeout action: 000b = no action 001b = Hard Reset 000b = Power Down 011b = Power Cycle 100b - 111b = reserved
02h	3.3V	3.3 V	Raw data of 3.3V sensor
03h	5V	5 V	Raw data of 5.0V sensor
04h	12V	12 V	Raw data of 12.0V sensor
05h	1.5V	1.5 V	Raw data of 1.5V sensor
06h	CPU0 Temp	40°C	Raw data of CPU0 Temp sensor
07h	CPU1 Temp	40°C	Raw data of CPU1 Temp sensor
08h	SYSTEM Temp	25°C	Raw data of SYSTEM Temp sensor
09h	Power Good		3.3V, 5V, and 12V status: 0x01= Power Good 0x02 = Power Fail
0ah	SYS_PWROK		All system power status: 0x01 = SYS_PWR OK 0x02 = SYS_PWR Fail
0bh	BIOS CHANGE		Current Bios Number: 0x01 = Bios1 0x02 = Bios2
0ch	BIOS POST ERROR		Post error status and Bios Recovery status: 0x00 = BIOS_NONE 0x01 = BIOS_RESET 0x02 = BIOS_ROM_CHECK 0x04= BIOS_HARDWARE_INIT 0x20= BIOS_BURN_FINISH

9.7 Relevant Documents

Document Title	Revision	Source
Intelligent Platform Management Interface Specification v1.5	Document Revision 1.1 February 20, 2002	Intel Corp. http://www.intel.com/design/servers/ipmi/license_ipmi.htm
PICMG 2.9 D1.0 CompactPCI System Management Specification	January 21, 2000	
Intelligent Platform Management Bus Communications Protocol Specification v0.9	Document Revision 0.15 June 24, 1997	Intel Corp. http://www.intel.com/design/servers/ipmi/license_ipmi.htm

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Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

A Lithium-type battery may be provided for uninterrupted, backup or emergency power.

Risk of explosion if battery is replaced with one of an incorrect type. Dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

Getting Service

Contact us should you require any service or assistance.

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