ETX

ETX-AT

User's Manual

Manual Revision: 2.02

Revision Date: October 27, 2009

Part Number: 50-1J020-1020

ADLINK TECHNOLOGY INC.

Revision History

Revision	Date	Change(s)
2.00	2009/05/18	Initial Release
2.01	2009/08/05	Correct LAN specification, remove SSD support, add SSDDR support
2.02	2009/10/27	Change SSDDR support to BOM option, update Ordering Information, Block Diagram

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Preface

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AMIBIOS®8 is a registered trademark of American Megatrends, Inc. ETX® is a registered trademark of Kontron Embedded Modules GmbH.

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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

Additional information, aids, and tips that help users perform tasks.

Information to prevent *mino*r physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

Information to prevent *serious* physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

1 Introduction

1.1 Description

The ETX-AT is an ETX v3.02 compliant module specially designed to facilitate speedy development of semi custom designs. ETX is an open standard that targets the market for embedded OEM projects. An ETX core combined with a custom made carrier board represents a value solution that allows OEM customers to get to the market fast. The new ETX v3.02 specification adds SATA support to ETX in the form of two connectors on the module itself, leaving the ETX board-to-board interface 100% compatible with baseboards designed under the earlier ETX v2.xx specification.

The ETX-AT is positioned as an entry level ETX module for generic systems, but is also suitable for systems requiring a full set of graphics features. The module comes with integrated support for high resolution CRT, single/dual channel 18/24-bits LVDS, and TV out (SDTV and HDTV)

Built on Intel's 45nm process, the Intel® Atom™ processor N270 with 512 kByte L2 cache on the ETX-AT features a thermal design power of just 2.5 watts at peak levels while supporting Intel® SpeedStep® Technology. The Intel® Atom™ processor N270 also supports Hyper Threading Technology, essentially giving it the performance of a dual core processor. Its thermal design and powerful CPU core allows the ETX-AT to provide the same or even better performance than earlier generation modules at more modest power consumption.

In addition to two SATA ports, the module offers dual channel EIDE supporting both PIO and UDMA modes, four USB ports, two serial ports, one parallel port (SPP/ECP/EPP) shared with FDD, one PS2 keyboard/mouse interface and power management functionality. Additionally onboard is an 10/100Base-T Ethernet port, and an HD Audio Codec.

The ETX-AT fully supports PCI and legacy ISA based on high speed PCI/ISA bridge. The module comes equipped with AMIBIOS®8 supporting embedded features such as: Remote Console, CMOS backup for battery-less operation, CPU and System Monitoring, and a Watchdog Timer.

The ETX-AT has been designed and verified for use with Virtium's SSDDR SODIMM dual function memory modules, while maintaining full backwards compatibility with standard SODIMM memory. Virtium's SSDDR combines a NAND Flash Serial ATA Solid State Drive (SATA SSD) and DDR2 memory on a single SODIMM module by utilizing reserved pins on the SODIMM for SATA interface signal transfer, thereby remaining fully JEDEC compatible.

The ETX-AT is available with native Intel single channel 18-bit LVDS support or with single/dual channel 18/24-bit LVDS based on the Chrontel CH7308B connected via SDVO.

The ETX-AT is a RoHS compliant and leadfree product.

2 Specifications

2.1 General

- CPU: Intel® Atom™ N270, FSB 533, 1.6 GHz with 512 KB L2 cache,
  2.5 W, on-die primary 32-kB instructions cache and
  - 24-kB write-back data cache
  - 2-thread support
  - Advanced gunning transceiver logic (AGTL+) bus driver technology
  - Enhanced Intel® SpeedStep® Technology
  - Source synchronous double-pumped (2x) Address
  - Source synchronous quad-pumped (4x) Data
  - C0~C4 low power states supported
- Memory: Single SODIMM socket supporting:
  - up to 2 GB of non-ECC, un-buffered, 533 MHz standard DDR2 SODIMM memory
  - Virtium SSDDR type module combining NAND flash SATA Solid State Drive and DDR2 memory on a single SODIMM module (ETX-AT-N270-SD/18SD only)
- Chipset: Intel® 945GSE Express Graphic Memory Controller Hub and Intel® I/O Controller Hub 7 Mobile (ICH7M)
- BIOS: AMIBIOS®8 with CMOS backup in 8 Mbit SPI BIOS
- Hardware Monitor: Supply voltages and CPU temperature
- Watchdog Timer: Programmable timer ranges to generate RESET
- Expansion Busses: 32-bit PCI 2.3 Masters at 33 MHz
  ISA 16-bit
  SMBus/I2C

2.2 Integrated Video

- Chipset: Intel® Graphics Media Accelerator 950 integrated into 945GSE GMCH supporting dual independent display
- CRT Interface: Analog CRT support up to 2048 x1536 resolution @ 70Hz (QXGA)
- LVDS Interface:
  - single channel 18-bit TFT with resolution up to 1280x1024 (ETX-AT-N270-18)
  - single/dual channel 18/24-bit TFT with resolution up to 1600x1200 (ETX-AT-N270)
- TV-out: NTSC/PAL, SDTV, HDTV 480p/720p/1080i/1080p modes supported (without Macrovision)

2.3 Audio

- Chipset: Integrated in Intel® I/O Controller Hub 7 Mobile (ICH7M)
- Audio Codec: AC'97 or HDA type on carrier

2.4 LAN

- Chipset: ICH7M integrated MAC with Intel® 82562 PHY
- Interface: 10/100 Mbps with Wake-on-LAN and Alert on LAN support

2.5 Multi I/O

- IDE (PATA): Two channels IDE with UDMA 100 support
- SATA: Two channels SATA-150 (ETX-AT-N270-SD/18SD support 1 channel only)
- USB: Supports up to eight ports USB v.2.0

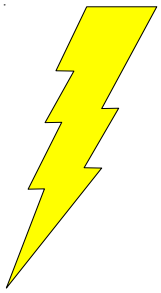
2.6 Super I/O

- Chipset: W83627HG
- Serial: Two high speed RS-232C ports (COM1/COM2)
- IrDA: SIR IrDA 1.1 compliant
- Parallel: SPP, EPP, and ECP mode (pin out shared with FDD)
- FDD: One drive (pin out shared with LPT)
- Keyboard & Mouse: One PS/2 keyboard and one PS/2 mouse

2.7 TPM (Trusted Platform Module)

- Chipset: Infineon SLB9635TT1.2
- Type: TPM 1.2

2.8 Power Specifications



- Input Power: AT mode and ATX mode
- Power Management: ACPI 3.0 compliant with battery support
- Power States: supports S0, S1, S3, S4, S5

Test Configuration

Function	Configuration
CPU	Intel® Atom™ Processor N270, 512MB L2, 533MHz, 45nm, 1.6GHz
Memory	Apacer PC2-4300 CL4 512MB
Graphics	945GSE
SATA Channel	Seagate Barracuda 7200.10 160BG
Backplane	ETX-Proto
Power Supply	LEMACS HG2-6350P 350W

Intel® Atom™ N270, 1.6 GHz

Power State	Power Requirement	Current	Power
DOS (idle)	+5V	2.26A	11.3W
Linux (idle)	+5V	2.15A	10.75W
Windows XP logon screen (idle)	+5V	2.25A	11.25W
Windows XP CPU Stress (Kpower)	+5V	2.54A	12.7W
Windows XP Total System Stress (Burnin)	+5V	2.48A	12.4W
S5 Mode (soft off)	5V Standby	131.6mA	0.658W
S4 Mode (hibernate)	5V Standby	65.6mA	0.328W
S3 Mode (suspend to RAM)	5V Standby	79.1mA	0.396W

CMOS Battery Power Consumption

Current (+3V)	Power
2.6 µA	0.0000078 W

2.9 Operating Systems Support

- Standard Support
  - Windows XP 32-bit
  - Windows Vista 32-bit
  - Linux 2.6.x
- Extended Support (BSP)
  - Embedded XP BSP
  - WinCE 6.0 BSP
  - Linux 2.6.x BSP
- Libraries, API support
  - AIDI I2C Library for Win32, WinCE and Linux

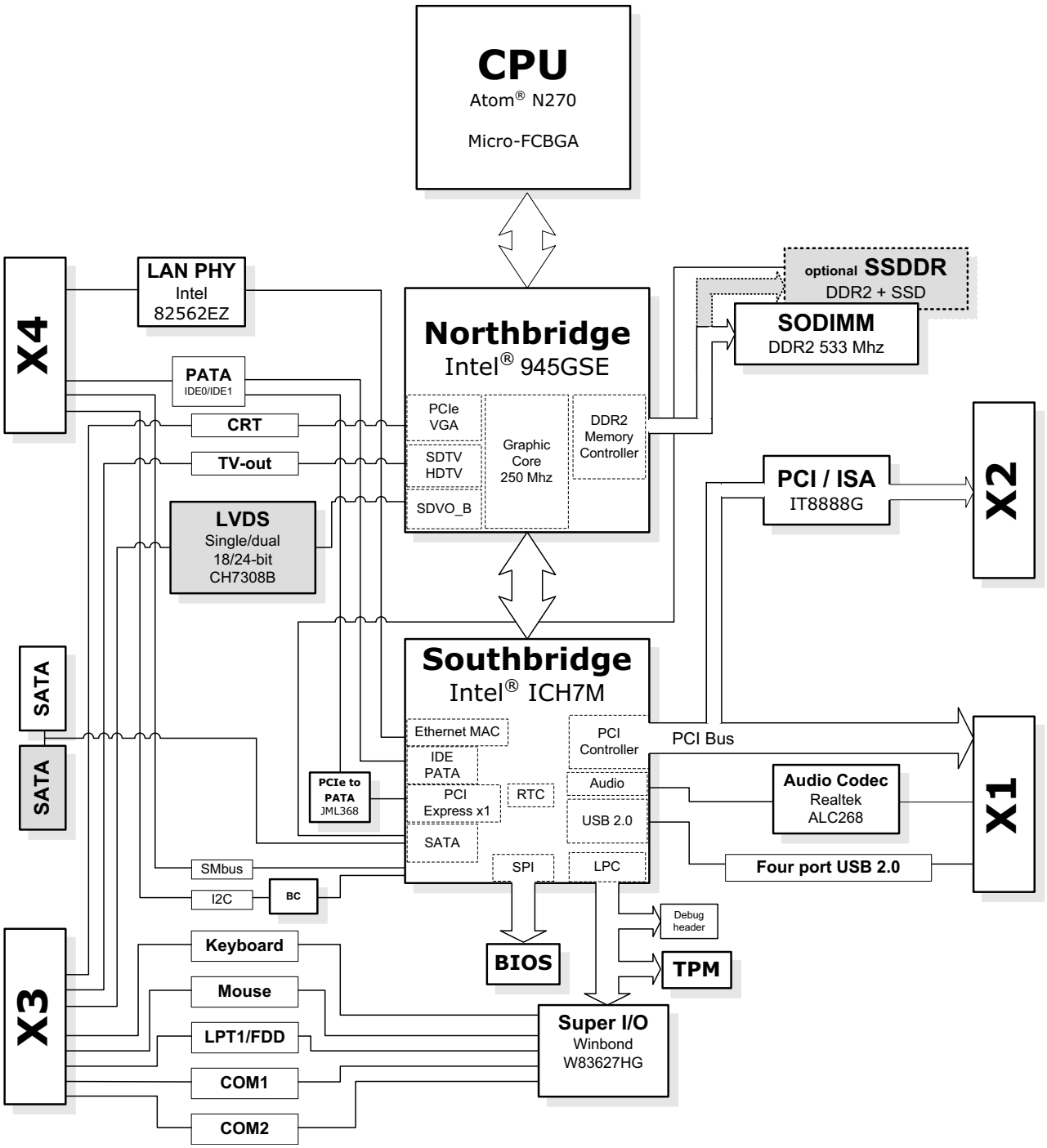
2.10 Mechanical and Environmental

- Form factor and Type: ETX rev 3.02
- Dimensions: 95 x 114 mm
- Standard Operating Temperature: 0°C to 60°C
- Relative Humidity: 5% to 95%
- Shock : 15G peak-to-peak, 11ms duration, non-operation
- Vibration:
  Non-operating : 1.88 Grms, 5-500 Hz, each axis
  Operating : 0.5 Grms, 5-500 Hz, each axis
- Certification : CE, FCC

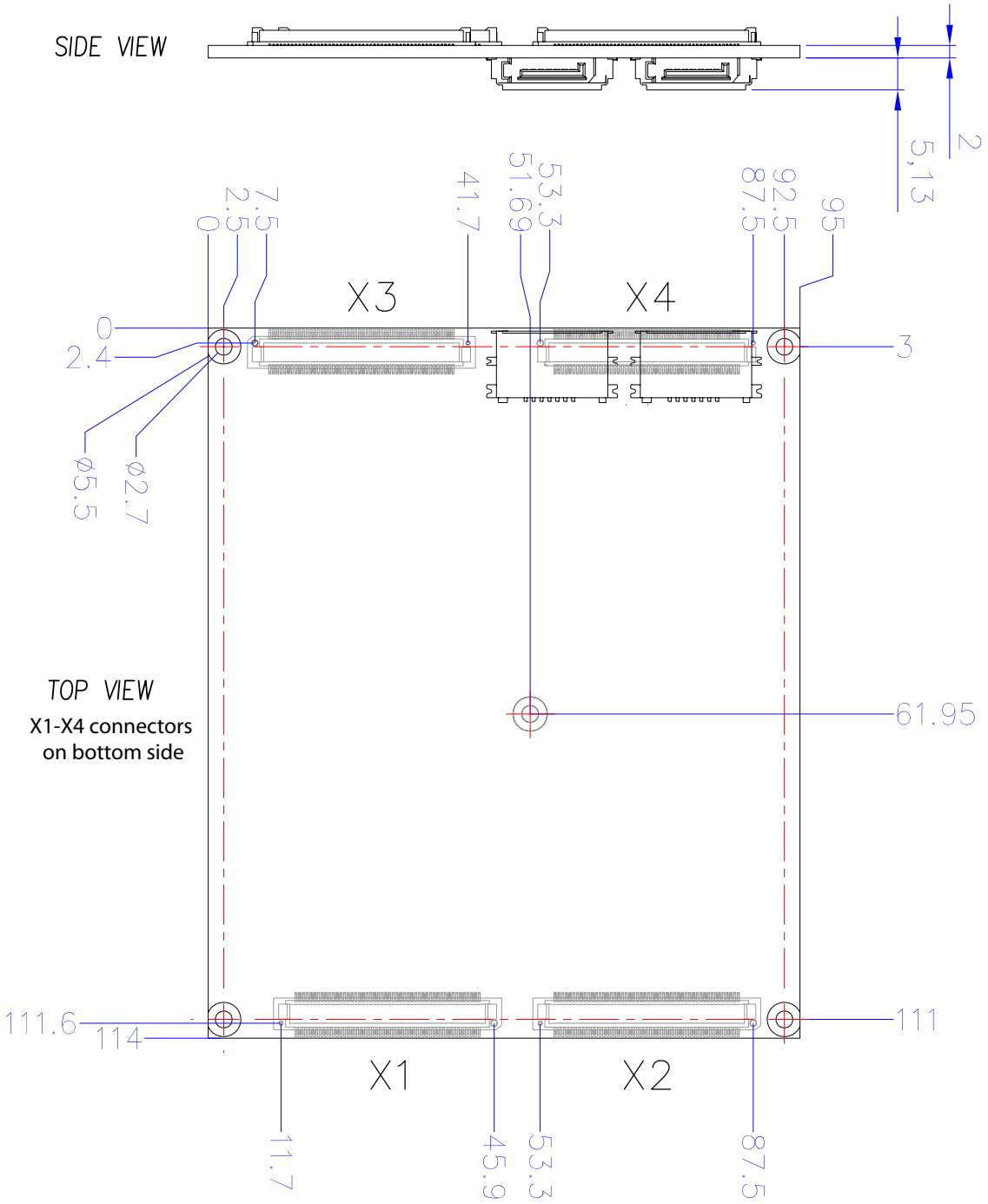
2.11 Ordering Information

- ETX-AT-N270
  ETX Module with Intel® Atom™ processor N270 and 945GSE / ICH7M chipset and support for single/dual channel 24-bit LVDS
- ETX-AT-N270-18
  ETX Module with Intel® Atom™ processor N270 and 945GSE / ICH7M chipset and support for single channel 18-bit LVDS
- ETX-AT-N270-SD / ETX-AT-N270-18SD
  ETX Module with Intel® Atom™ processor N270 and 945GSE / ICH7M chipset with 24-bit integrated LVDS and SSDDR support (“18SD” supports 18-bit LVDS)

3 Function Diagram



4 Mechanical Dimensions



All ∅ tolerances ± 0.05 mm
Other tolerances ± 0.2 mm

5 Embedded Functions

All embedded board functions on ADLINK's Computer on Modules are supported at the operating system level using the ADLINK Intelligent Device Interface (AIDI) library. The AIDI API programming interface is compatible and identical across all supported ADLINK Computer on Modules and all supported operating systems. The AIDI library includes a demo program to demonstrate the library's functionallity.

5.1 Watchdog Timer

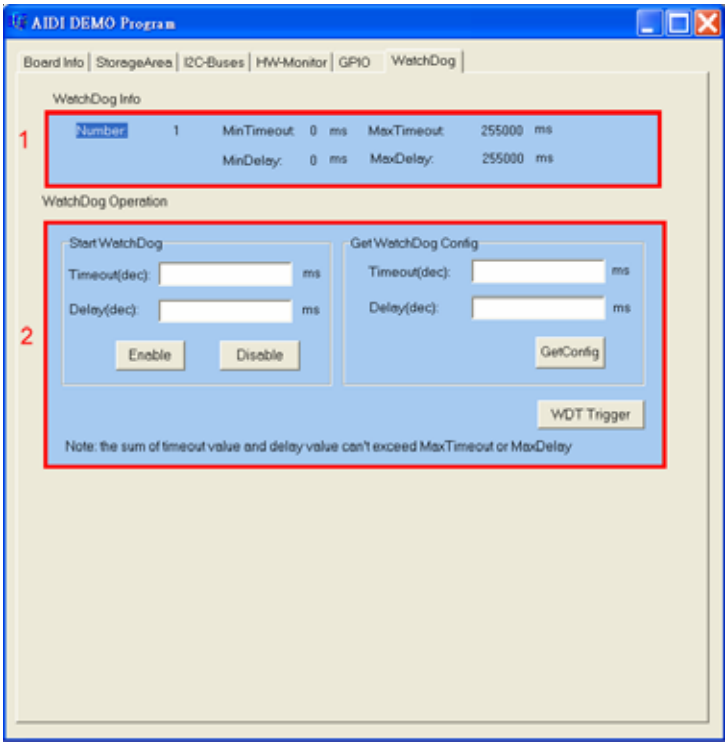
The ETX-AT implements a Watchdog timer that can be used to automatically detect software execution problems or system hangs and reset the board if necessary. The Watchdog timer consists of a counter that counts down from an initial value to zero. When the system is operating normally, the software that sets the intial value periodically resets the counter so that the it never reaches zero. If the counter reaches zero before the software resets it, the system is presumed to be malfunctioning and a reset signal is asserted.

The AIDI Library Watchdog functions support Watchdog control of the board. If the Watchdog begins countdown and reaches zero, it will access the CPU's RESET signal to reset the system. This application must call another function named AidiWDogTrigger that triggers the Watchdog to restart to prevent system reset.

AIDI Demo Program
- Watchdog Tab

The AIDI Demo Program allows retrieval of the current Watchdog status and updating of the Watchdog settings

If the Watchdog is enabled, the user can click the *WDT Trigger* button to manually reset the counter and prevent the system from resetting



5.2 Hardware Monitoring

To ensure system health of your embedded system ADLINK's Computer on Modules come with built in support for monitoring of CPU temperatures and critical module voltage levels.

The AIDI Library provides simple APIs at the application level to support these functions and adds alarm functions when voltage or temperature levels exceeds the upper or lower limit set by the user.

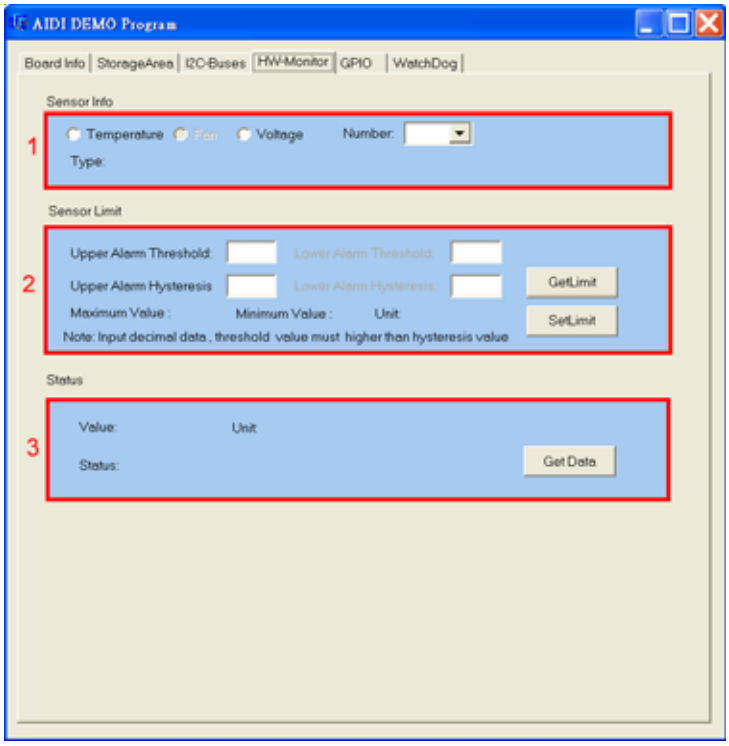
On the ETX-AT the following monitored values can be read from the module:
CPU temperature, Vcore, 1.05V, 3.3V, 5V and VBAT.

AIDI Demo Program
- HW Monitor Tab

Field 1 displays detected sensors (number).

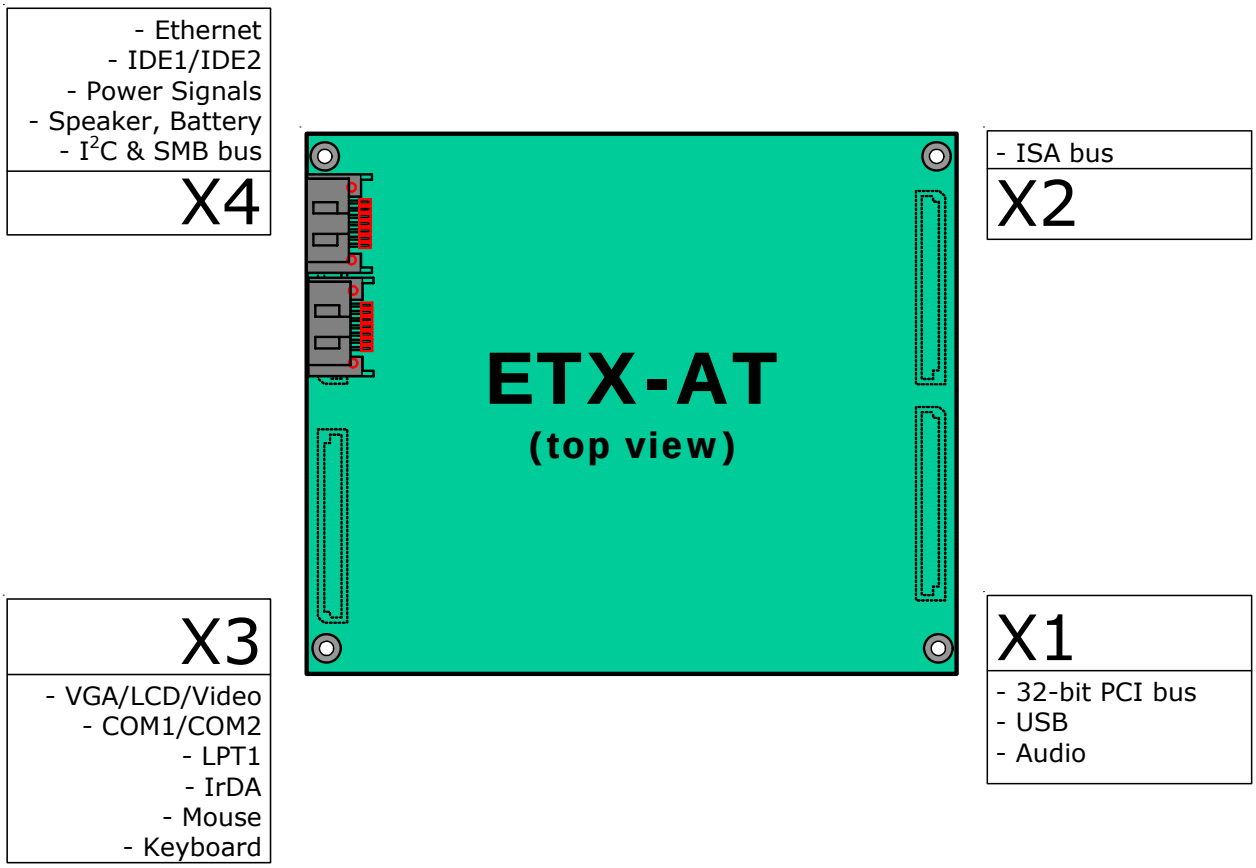
Field 2 allows setting of upper and lower alarm limits.

Field 3 displays read out information of sensors.



6 Pin-out and Signal Descriptions

6.1 Connector Locations



6.2 Pin Compatibility

All pins on X1, X2, X3, and X4 of the ETX-AT comply with pin and signal descriptions used in the ETX Specification version 3.02. This document contains a description of pins, signal descriptions, and mechanical characteristics of the ETX form factor.

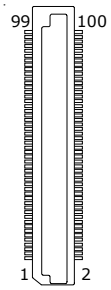
NOTE:

Compared to earlier ETX revisons (ETX rev 2.x)
ETX 3.02 revision adds “SATA connectors on the module” to the ETX specification and is further pin to pin compatible with earlier 2.x ETX revisions.
(X1, X2, X3, X4 pinout on rev 2.x equal those on revison 3.02)

6.3 Pin Definitions

X1: PCI-bus, USB, & Audio

X1



Pin	Signal	Pin	Signal
1	GND	2	GND
3	PCICLK3	4	PCICLK4
5	GND	6	GND
7	PCICLK1	8	PCICLK2
9	REQ3#	10	GNT3#
11	GNT2#	12	3V[1]
13	REQ2#	14	GNT1#
15	REQ1#	16	3V[1]
17	GNT0#	18	RSV
19	5VCC	20	5VCC
21	SERIRQ	22	REQ0#
23	AD0	24	3V[1]
25	AD1	26	AD2
27	AD4	28	AD3
29	AD6	30	AD5
31	CBE0#	32	AD7
33	AD8	34	AD9
35	GND	36	GND
37	AD10	38	AUXAL
39	AD11	40	MIC
41	AD12	42	AUXAR
43	AD13	44	ASVCC
45	AD14	46	SDNL
47	AD15	48	ASSGND
49	CBE1#	50	SNDR

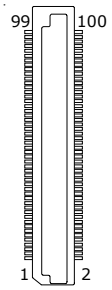
Pin	Signal	Pin	Signal
51	5VCC	52	5VCC
53	PAR	54	SERR#
55	GPERR	56	RSV
57	PME#	58	USB2-
59	LOCK#	60	DEVSEL#
61	TRDY#	62	USB3-
63	IRDY#	64	STOP#
65	FRAME#	66	USB2+
67	GND	68	GND
69	AD16	70	CBE2#
71	AD17	72	USB3+
73	AD19	74	AD18
75	AD20	76	USB0N
77	AD22	78	AD21
79	AD23	80	USB1-
81	AD24	82	CBE3#
83	5VCC	84	5VCC
85	AD25	86	AD26
87	AD28	88	USB0+
89	AD27	90	AD29
91	AD30	92	USB1+
93	PCIRST#	94	AD31
95	INTC#	96	INTD#
97	INTA#	98	INTB#
99	GND	100	GND

NOTE: The 3V (3.3 V ±5%) is generated onboard. Pins may be used to power devices on the carrier board up to a maximum load of 500 mA.

CAUTION: Do not connect the 3V pin to external 3.3V supply power.

X2: ISA Bus

X2



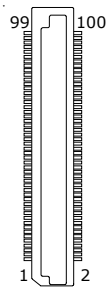
Pin	Signal	Pin	Signal
1	GND	2	GND
3	SD14	4	SD15
5	SD13	6	MASTER#
7	SD12	8	DREQ7
9	SD11	10	DACK7#
11	SD10	12	DREQ6
13	SD9	14	DACK6#
15	SD8	16	DREQ5
17	MEMW#	18	DACK5#
19	MEMR#	20	DREQ0
21	LA17	22	DACK0#
23	LA18	24	IRQ14
25	LA19	26	IRQ15
27	LA20	28	IRQ12[1]
29	LA21	30	IRQ11
31	LA22	32	IRQ10
33	LA23	34	IO16#
35	GND	36	GND
37	SBHE#	38	M16#
39	SA0	40	OSC
41	SA1	42	BALE
43	SA2	44	TC
45	SA3	46	DACK2#
47	SA4	48	IRQ3
49	SA5	50	IRQ4

Pin	Signal	Pin	Signal
51	5VCC	52	5VCC
53	SA6	54	IRQ5
55	SA7	56	IRQ6
57	SA8	58	IRQ7
59	SA9	60	SYSCLK
61	SA10	62	REFSH#
63	SA11	64	DREQ1
65	SA12	66	DACK1#
67	GND	68	GND
69	SA13	70	DREQ3
71	SA14	72	DACK3#
73	SA15	74	IOR#
75	SA16	76	IOW#
77	SA18	78	SA17
79	SA19	80	SMEMR#
81	IOCHRDY	82	AEN
83	5VCC	84	5VCC
85	SD0	86	SMEMW#
87	SD2	88	SD1
89	SD3	90	NOWS#
91	DREQ2	92	SD4
93	SD5	94	IRQ9
95	SD6	96	SD7
97	IOCHK#	98	RSTDRV
99	GND	100	GND

NOTE: [1]IRQ12 is reserved for a PS/2 mouse.

X3: CRT, LCD (LVDS), & Video

X3



Pin	Signal	Pin	Signal
1	GND	2	GND
3	R	4	B
5	HSY	6	G
7	VSY	8	DDCK
9	NC	10	DDDA
11	LCD16	12	LCD18
13	LCD17	14	LCD19
15	GND	16	GND
17	LCD13	18	LCD15
19	LCD12	20	LCD14
21	GND	22	GND
23	LCD8	24	LCD11
25	LCD9	26	LCD10
27	GND	28	GND
29	LCD4	30	LCD7
31	LCD5	32	LCD6
33	GND	34	GND
35	LCD1	36	LCD3
37	LCD0	38	LCD2
39	5VCC	40	5VCC
41	JILI_SDA	42	LTGO0
43	JILI_SCL	44	BLON#
45	NC	46	DIGON
47	COMP	48	Y
49	NC	50	C

First LVDS Channel

Signal	LVDS Signal	
LCD0	Txout 0-	
LCD1	Txout 0+	
LCD2	Txout 1-	
LCD3	Txout 1+	
LCD4	Txout 2-	
LCD5	Txout 2+	
LCD6	Txclk -	
LCD7	Txclk +	
LCD8	Txout 3-	* *
LCD9	Txout 3+	* *

Second LVDS Channel

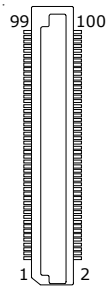
Signal	LVDS Signal	
LCD10	Txout 0-	* *
LCD11	Txout 0+	* *
LCD12	Txout 1-	* *
LCD13	Txout 1+	* *
LCD14	Txout 2-	* *
LCD15	Txout 2+	* *
LCD16	Txclk -	* *
LCD17	Txclk +	* *
LCD18	Txout 3-	* *
LCD19	Txout 3+	* *

NOTE:

* * These signals are not connected on module type ETX-AT-N270-18(SD)

X3: COM1/2, LPT1 or FDD, IrDA, Mouse, & Keyboard

X3



The pinout on the X3 connector for parallel-port interfaces can alternatively be assigned as a floppy disk drive interface in the BIOS (see Sec. 8.3.5, Super IO Configuration). Alternative pinouts for the two interfaces are shown in the tables below. The left table shows the standard functions of the pins in parallel port mode and the he right table shows the alternate function pinout in floppy disk drive mode.

LPT Mode

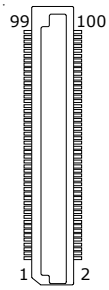
Pin	Signal	Pin	Signal
51	LPT/FLPY#	52	RESERVED
53	5VCC	54	GND
55	STB#	56	AFD#
57	RESERVED	58	PD7
59	IRRX	60	ERR#
61	IRTX	62	PD6
63	RXD2	64	INIT#
65	GND	66	GND
67	RTS2#	68	PD5
69	DTR2#	70	SLIN#
71	DCD2#	72	PD4
73	DSR2#	74	PD3
75	CTS2#	76	PD2
77	TXD2	78	PD1
79	RI2#	80	PD0
81	5VCC	82	5VCC
83	RXD1	84	ACK#
85	RTS1#	86	BUSY
87	DTR1#	88	PE
89	DCD1#	90	SLCT#
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

FDD Mode

Pin	Signal	Pin	Signal
51	LPT/FLPY#	52	RESERVED
53	5VCC	54	GND
55	RESERVED	56	DENSEL
57	RESERVED	58	RESERVED
59	IRRX	60	HDSEL#
61	IRTX	62	RESERVED
63	RXD2	64	DIR#
65	GND	66	GND
67	RTS2#	68	RESERVED
69	DTR2#	70	STEP#
71	DCD2#	72	DSKCHG#
73	DSR2#	74	RDATA#
75	CTS2#	76	WP#
77	TXD2	78	TRK0#
79	RI2#	80	INDEX#
81	5VCC	82	5VCC
83	RXD1	84	DRV
85	RTS1#	86	MOT
87	DTR1#	88	WDATA#
89	DCD1#	90	WGATE#
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

X4: IDE1, IDE2, Ethernet, & Miscellaneous

X4



Pin	Signal	Pin	Signal
1	GND	2	GND
3	5V_SB	4	PWGIN
5	PS_ON	6	SPEAKER
7	PWRBTN#	8	BATT
9	KBINH	10	LILED#
11	RSMRST#[1]	12	ACTLED#
13	ROMKBCS#[2]	14	SPDLED#
15	EXT_PRG[2]	16	I2CLK[3]
17	5VCC	18	5VCC
19	OVCR#	20	NC
21	EXTSMI#	22	I2DAT[3]
23	SMBCLK[3]	24	SMBDATA[3]
25	S_CS3#	26	SMBALRT#
27	S_CS1#	28	NC
29	S_A2	30	P_CS3#
31	S_A0	32	P_CS1#
33	GND	34	GND
35	PDIAG_S	36	P_A2
37	S_A1	38	P_A0
39	S_INTRQ	40	P_A1
41	BATLOW#[2]	42	GPE1#[2]
43	S_AK#	44	P_INTRQ
45	S_RDY	46	P_AK#
47	S_IOR#	48	P_RDY
49	5VCC	50	5VCC

Pin	Signal	Pin	Signal
51	S_IOW#	52	P_IOR#
53	S_DRQ	54	P_IOW#
55	S_D15	56	P_DRQ
57	S_D0	58	P_D15
59	S_D14	60	P_D0
61	S_D1	62	P_D14
63	S_D13	64	P_D1
65	GND	66	GND
67	S_D2	68	P_D13
69	S_D12	70	P_D2
71	S_D3	72	P_D12
73	S_D11	74	P_D3
75	S_D4	76	P_D11
77	S_D10	78	P_D4
79	S_D5	80	P_D10
81	5VCC	82	5VCC
83	S_D9	84	P_D5
85	S_D6	86	P_D9
87	S_D8	88	P_D6
89	GPE2#[2]	90	CBLID_P#
91	RXD#	92	P_D8
93	RXD	94	S_D7
95	TXD#	96	P_D7
97	TXD	98	HDRST#
99	GND	100	GND

NOTE:

[1]May be affected by external circuitry to reset the power management logic of the ETX module. Most designs do not use and pin is not connected.

[2]Reserved, do not connect

[3]See also: section 7.7 System Management Bus (I2C-compatible)

[4]Available, but not supported on the ETX-AT

6.4 Signal Descriptions

X1

Pin	Signal	Description	Type	PU/PD	Comment
1	GND	Ground	PWR	-	-
2	GND	Ground	PWR	-	-
3	PCICLK3	PCI Clock Slot 3	O-3,3	-	-
4	PCICLK4	PCI Clock Slot 4	O-3,3	-	-
5	GND	Ground	PWR	-	-
6	GND	Ground	PWR	-	-
7	PCICLK1	PCI Clock Slot 1	O-3,3	-	-
8	PCICLK2	PCI Clock Slot 2	O-3,3	-	-
9	REQ3#	PCI Bus Request 3	I-3,3	PU 8k2 3,3V	-
10	GNT3#	PCI Bus Grant 3	O-3,3	-	int. PU 20k 3,3V
11	GNT2#	PCI Bus Grant 2	O-3,3	-	int. PU 20k 3,3V
12	3V	Power +3,3V	PWR	-	-
13	REQ2#	PCI Bus Request 2	I-3,3	PU 8k2 3,3V	-
14	GNT1#	PCI Bus Grant 1	O-3,3	-	int. PU 20k 3,3V
15	REQ1#	PCI Bus Request 1	I-3,3	PU 8k2 3,3V	-
16	3V	Power +3,3V	PWR	-	-
17	GNT0#	PCI Bus Grant 0	O-3,3	-	int. PU 20k 3,3V
18	RSVD	-	NC	-	Reserved
19	5VCC	Power +5V	PWR	-	-
20	5VCC	Power +5V	PWR	-	-
21	SERIRQ	Serial Interrupt Reqest	IO-3,3	PU 8k2 3,3V	-
22	REQ0#	PCI Bus Request 0	I-3,3	PU 8k2 3,3V	-
23	AD0	PCI Adress & Data Bus line	IO-3,3	-	
24	3V	Power +3,3V	PWR	-	-
25	AD1	PCI Adress & Data Bus line	IO-3,3	-	-
26	AD2	PCI Adress & Data Bus line	IO-3,3	-	-
27	AD4	PCI Adress & Data Bus line	IO-3,3	-	-
28	AD3	PCI Adress & Data Bus line	IO-3,3	-	-
29	AD6	PCI Adress & Data Bus line	IO-3,3	-	-
30	AD5	PCI Adress & Data Bus line	IO-3,3	-	-
31	CBE0#	PCI Bus Command and Byte enables 0	IO-3,3	-	-
32	AD7	PCI Adress & Data Bus line	IO-3,3	-	-
33	AD8	PCI Adress & Data Bus line	IO-3,3	-	-
34	AD9	PCI Adress & Data Bus line	IO-3,3	-	-
35	GND	Ground	PWR	-	-
36	GND	Ground	PWR	-	-
37	AD10	PCI Adress & Data Bus line	IO-3,3	-	-
38	AUXAL	Auxiliary Line Input Left	I		
39	AD11	PCI Adress & Data Bus line	IO-3,3	-	-
40	MIC	Microphone Input	I	-	-
41	AD12	PCI Adress & Data Bus line	IO-3,3	-	-
42	AUXAR	Auxiliary Line Input Right	I		
43	AD13	PCI Adress & Data Bus line	IO-3,3	-	-
44	ASVCC	Analog Supply of Sound Controller	O-5	-	-
45	AD14	PCI Adress & Data Bus line	IO-3,3	-	-
46	SNDL	Audio Out Left	O	-	-
47	AD15	PCI Adress & Data Bus line	IO-3,3	-	-
48	ASGND	Analog Ground of Sound Controller	P	-	-
49	CBE1#	PCI Bus Command and Byte enables 1	IO-3,3	-	-
50	SNDR	Audio Out Right	O	-	-

Signal Descriptions (cont'd)

X1

Pin	Signal	Description	Type	PU/PD	Comment
51	5VCC	Power +5V	PWR		
52	5VCC	Power +5V	PWR		
53	PAR	PCI Bus Parity	IO-3,3		
54	SERR#	PCI Bus System Error	IO-3,3	PU 8k2 3,3V	
55	GPERR#	PCI Bus Grant Error	IO-3,3	PU 8k2 3,3V	
56	RSV	-	NC		Reserved
57	PME#	PCI Power Management Event	IO-3,3		int. PU 20k 3,3V
58	USB2N	USB Data- Port2	I/O - DP		int. PD 15k
59	LOCK#	PCI Bus Lock	IO-3,3	PU 8k2 3,3V	
60	DEVSEL#	PCI Bus Device Select	IO-3,3	PU 8k2 3,3V	
61	TRDY#	PIC Bus Target Ready	IO-3,3	PU 8k2 3,3V	
62	USB3N	USB Data- Port3	I/O - DP		int. PD 15k
63	IRDY#	PCI Bus Initiator Ready	IO-3,3	PU 8k2 3,3V	
64	STOP#	PCI Bus Stop	IO-3,3	PU 8k2 3,3V	
65	FRAME#	PCI Bus Cycle Frame	IO-3,3	PU 8k2 3,3V	
66	USB2P	USB Data+ Port2	I/O - DP		int. PD 15k
67	GND	Ground	PWR		
68	GND	Ground	PWR		
69	AD16	PCI Adress & Data Bus line	IO-3,3		
70	CBE2#	PCI Bus Command and Byte enables 2	IO-3,3		
71	AD17	PCI Adress & Data Bus line	IO-3,3		
72	USB3P	USB Data+ Port3	I/O - DP		int. PD 15k
73	AD19	PCI Adress & Data Bus line	IO-3,3		
74	AD18	PCI Adress & Data Bus line	IO-3,3		
75	AD20	PCI Adress & Data Bus line	IO-3,3		
76	USB0N	USB Data- Port0	I/O - DP		int. PD 15k
77	AD22	PCI Adress & Data Bus line	IO-3,3		
78	AD21	PCI Adress & Data Bus line	IO-3,3		
79	AD23	PCI Adress & Data Bus line	IO-3,3		
80	USB1N	USB Data- Port1	I/O - DP		int. PD 15k
81	AD24	PCI Adress & Data Bus line	IO-3,3		
82	CBE3#	PCI Bus Command and Byte enables 3	IO-3,3		
83	5VCC	Power +5V	PWR		
84	5VCC	Power +5V	PWR		
85	AD25	PCI Adress & Data Bus line	IO-3,3		
86	AD26	PCI Adress & Data Bus line	IO-3,3		
87	AD28	PCI Adress & Data Bus line	IO-3,3		
88	USB0P	USB Data+ Port0	I/O - DP		int. PD 15k
89	AD27	PCI Adress & Data Bus line	IO-3,3		
90	AD29	PCI Adress & Data Bus line	IO-3,3		
91	AD30	PCI Adress & Data Bus line	IO-3,3		
92	USB1P	USB Data+ Port1	I/O - DP		int. PD 15k
93	PCIRST#	PCI Bus Reset	O-3,3		
94	AD31	PCI Adress & Data Bus line	IO-3,3		
95	INTC#	PCI BUS Interrupt Reauest C	I-3,3	PU 8k2 3,3V	
96	INTD#	PCI BUS Interrupt Reauest D	I-3,3	PU 8k2 3,3V	
97	INTA#	PCI BUS Interrupt Reauest A	I-3,3	PU 8k2 3,3V	
98	INTB#	PCI BUS Interrupt Reauest B	I-3,3	PU 8k2 3,3V	
99	GND	Ground	PWR		
100	GND	Ground	PWR		

Signal Descriptions (cont'd)

X2

Pin	Signal	Description	Type	PU/PD	Comment
1	GND	Ground	PWR	-	-
2	GND	Ground	PWR	-	-
3	SD14	ISA Data Bus	IO-5	PU 4k7 5V	int. PU 50k 5V in
4	SD15	ISA Data Bus	IO-5	PU 4k7 5V	int. PU 50k 5V in
5	SD13	ISA Data Bus	IO-5	PU 4k7 5V	int. PU 50k 5V in
6	MASTER#	ISA 16-Bit Master	I-5	PU 330R 5V	int. PU 50k 5V in
7	SD12	ISA Data Bus	IO-5	PU 4k7 5V	int. PU 50k 5V in
8	DREQ7	ISA DMA Request 7	I-5	PU 4k7 5V	int. PD 50k
9	SD11	ISA Data Bus	IO-5	PU 4k7 5V	int. PU 50k 5V in
10	DACK7#	ISA DMA Acknowledge 7	IO-5	PU 4k7 5V	int. PU 50k 5V in
11	SD10	ISA Data Bus	IO-5	PU 4k7 5V	int. PU 50k 5V in
12	DREQ6	ISA DMA Request 6	I-5	PU 4k7 5V	int. PD 50k
13	SD9	ISA Data Bus	IO-5	PU 4k7 5V	int. PU 50k 5V in
14	DACK6#	ISA DMA Acknowledge 6	IO-5	PU 4k7 5V	int. PU 50k 5V in
15	SD8	ISA Data Bus	IO-5	PU 4k7 5V	int. PU 50k 5V in
16	DREQ5	ISA DMA Request 5	I-5	PU 4k7 5V	int. PD 50k
17	MEMW#	ISA Memory Write	IO-5	PU 4k7 5V	int. PU 50k 5V in
18	DACK5#	ISA DMA Acknowledge 5	IO-5	PU 4k7 5V	int. PU 50k 5V in
19	MEMR#	ISA Memory Read	IO-5	PU 4k7 5V	int. PU 50k 5V in
20	DREQ0	ISA DMA Request 0	I-5	PU 4k7 5V	int. PD 50k
21	LA17	ISA Address Bus (SA17)	O-5	PU 4k7 5V	-
22	DACK0#	ISA DMA Acknowledge 0	IO-5	PU 4k7 5V	int. PU 50k 5V in
23	LA18	ISA Address Bus (SA18)	O-5	PU 4k7 5V	-
24	IRQ14	ISA Interrupt Request 14 / ROMChip Select	IO-5	PU 4k7 5V	int. PU 50k 5V in
25	LA19	ISA Address Bus (SA19)	O-5	PU 4k7 5V	-
26	IRQ15	ISA Interrupt Request 15	IO-5	PU 4k7 5V	int. PU 50k 5V in
27	LA20	ISA Address Bus (SA20)	O-5	PU 4k7 5V	-
28	IRQ12	ISA Interrupt Request 12	IO-5	PU 4k7 5V	int. PU 50k 5V in
29	LA21	ISA Address Bus (SA21)	O-5	PU 4k7 5V	-
30	IRQ11	ISA Interrupt Request 11	IO-5	PU 4k7 5V	int. PU 50k 5V in
31	LA22	ISA Address Bus (SA22)	O-5	PU 4k7 5V	-
32	IRQ10	ISA Interrupt Request 10	IO-5	PU 4k7 5V	int. PU 50k 5V in
33	LA23	ISA Address Bus (SA23)	O-5	PU 4k7 5V	
34	IO16#	ISA 16-Bit I/O Access	I-5	PU 330R 5V	int. PU 50k 5V in
35	GND	Ground	PWR	-	-
36	GND	Ground	PWR	-	-
37	SBHE#	ISA System Byte High Enable	IO-5	PU 4k7 5V	int. PU 50k 5V in
38	M16#	ISA 16-Bit Memory Access	IO-5	PU 330R 5V	int. PU 50k 5V in
39	SA0	ISA Address Bus	O-5	PU 4k7 5V	-
40	OSC	ISA Oscillator (CLK_ISA14#)	O-3,3	-	-
41	SA1	ISA Address Bus	O-5	PU 4k7 5V	-
42	BALE	ISA Buffer Address Latch Enable	IO-5	PD 4k7	int. PU 50k 5V in
43	SA2	ISA Address Bus	O-5	PU 4k7 5V	
44	TC	ISA Terminal Count	IO-5	PD 4k7	int. PU 50k 5V in
45	SA3	ISA Address Bus	O-5	PU 4k7 5V	-
46	DACK2#	ISA DMA Acknowledge 2	IO-5	PU 4k7 5V	int. PU 50k 5V in
47	SA4	ISA Address Bus	O-5	PU 4k7 5V	-
48	IRQ3	ISA Interrupt Request 3	IO-5	PU 4k7 5V	int. PU 50k 5V in
49	SA5	ISA Address Bus	O-5	PU 4k7 5V	-
50	IRQ4	ISA Interrupt Request 4	IO-5	PU 4k7 5V	int. PU 50k 5V in

Signal Descriptions (cont'd)

X2

Pin	Signal	Description	Type	PU/PD	Comment
51	5VCC	Power +5V	PWR	-	-
52	5VCC	Power +5V	PWR	-	-
53	SA6	ISA Address Bus	O-5	PU 4k7 5V	-
54	IRQ5	ISA Interrupt Request 5	IO-5	PU 4k7 5V	int. PU 50k 5V in
55	SA7	ISA Address Bus	O-5	PU 4k7 5V	-
56	IRQ6	ISA Interrupt Request 6	IO-5	PU 4k7 5V	int. PU 50k 5V in
57	SA8	ISA Address Bus	O-5	PU 4k7 5V	-
58	IRQ7	ISA Interrupt Request 7	IO-5	PU 4k7 5V	int. PU 50k 5V in
59	SA9	ISA Address Bus	O-5	PU 4k7 5V	-
60	SYSCLK	ISA Bus Clock (CLK_SYS_ISA)	O-3,3	-	-
61	SA10	ISA Address Bus	O-5	PU 4k7 5V	-
62	REFSH#	ISA System Refresh Control	IO-5	PU 1k 5V	int. PU 50k 5V in
63	SA11	ISA Address Bus	O-5	PU 4k7 5V	-
64	DREQ1	ISA DMA Request 1	I-5	PU 4k7 5V	int. PD 50k
65	SA12	ISA Address Bus	O-5	PU 4k7 5V	-
66	DACK1#	ISA DMA Acknowledge 1	IO-5	PU 4k7 5V	int. PU 50k 5V in
67	GND	Ground	PWR	-	-
68	GND	Ground	PWR	-	-
69	SA13	ISA Address Bus	O-5	PU 4k7 5V	-
70	DREQ3	ISA DMA Request 3	I-5	PU 4k7 5V	int. PD 50k
71	SA14	ISA Address Bus	O-5	PU 4k7 5V	-
72	DACK3#	ISA DMA Acknowledge 3	IO-5	PU 4k7 5V	int. PU 50k 5V in
73	SA15	ISA Address Bus	O-5	PU 4k7 5V	-
74	IOR#	ISA I/O Read	IO-5	PU 4k7 5V	int. PU 50k 5V in
75	SA16	ISA Address Bus	O-5	PU 4k7 5V	-
76	IOW#	ISA I/O Write	IO-5	PU 4k7 5V	int. PU 50k 5V in
77	SA18	ISA Address Bus	O-5	PU 4k7 5V	-
78	SA17	ISA Address Bus	O-5	PU 4k7 5V	-
79	SA19	ISA Address Bus	O-5	PU 4k7 5V	-
80	SMEMR#	ISA System Memory Read	IO-5	PU 4k7 5V	int. PU 50k 5V in
81	IOCHRDY	ISA I/O Channel Ready	IO-5	PU 1k 5V	int. PU 50k 5V in
82	AEN	ISA Address Enable	IO-5	PD 47k	int. PU 50k 5V in
83	5VCC	Power +5V	PWR	-	-
84	5VCC	Power +5V	PWR	-	-
85	SD0	ISA Data Bus	IO-5	PU 4k7 5V	int. PU 50k 5V in
86	SMEMW#	ISA System Memory Write	IO-5	PU 4k7 5V	int. PU 50k 5V in
87	SD2	ISA Data Bus	IO-5	PU 4k7 5V	int. PU 50k 5V in
88	SD1	ISA Data Bus	IO-5	PU 4k7 5V	int. PU 50k 5V in
89	SD3	ISA Data Bus	IO-5	PU 4k7 5V	int. PU 50k 5V in
90	NOWS#	ISA No Wait Staits	I-5	PU 330R 5V	int. PU 50k 5V in
91	DREQ2	ISA DMA Request 2	I-5	PU 4k7 5V	int. PD 50k
92	SD4	ISA Data Bus	IO-5	PU 4k7 5V	int. PU 50k 5V in
93	SD5	ISA Data Bus	IO-5	PU 4k7 5V	int. PU 50k 5V in
94	IRQ9	ISA Interrupt Request 9	IO-5	PU 4k7 5V	int. PU 50k 5V in
95	SD6	ISA Data Bus	IO-5	PU 4k7 5V	int. PU 50k 5V in
96	SD7	ISA Data Bus	IO-5	PU 4k7 5V	int. PU 50k 5V in
97	IOCHK#	ISA I/O Channel Check	I-5	PU 4k7 5V	int. PU 50k 5V in
98	RSTDRV	ISA Reset	O-5	-	-
99	GND	Ground	PWR	-	-
100	GND	Ground	PWR	-	-

Signal Descriptions (cont'd)

X3

Pin	Signal	Description	Type	PU/PD	Comment
1	GND	Ground	PWR	-	-
2	GND	Ground	PWR	-	-
3	R	Analog Video Out RGB - Red Channel	OA	PD 150R	-
4	B	Analog Video Out RGB - Blue Channel	OA	PD 150R	-
5	HSY	Horizontal Synchronization Pulse	O-3,3	-	-
6	G	Analog Video Out RGB - Green Channel	OA	PD 150R	-
7	VSY	Vertical Synchronization Pulse	O-3,3	-	-
8	DDCK	Display Data Channel Clock	IO-5	PU 2k2 3,3V	-
9	DETECT#	Panel Hot-Plug Detection	NC		-
10	DDDA	Display Data Channel Data	IO-5	PU 2k2 3,3V	-
11	LCD16	Second LVDS Channel Data Txclk -	O - DP	-	NC on ETX-AT-N270-18
12	LCD18	Second LVDS Channel Data Txout 3-	O - DP	-	NC on ETX-AT-N270-18
13	LCD17	Second LVDS Channel Data Txclk +	O - DP	-	NC on ETX-AT-N270-18
14	LCD19	Second LVDS Channel Data Txout 3+	O - DP	-	NC on ETX-AT-N270-18
15	GND	Ground	PWR	-	-
16	GND	Ground	PWR	-	-
17	LCD13	Second LVDS Channel Data Txout 1+	O - DP	-	NC on ETX-AT-N270-18
18	LCD15	Second LVDS Channel Data Txout 2+	O - DP	-	NC on ETX-AT-N270-18
19	LCD12	Second LVDS Channel Data Txout 1-	O - DP	-	NC on ETX-AT-N270-18
20	LCD14	Second LVDS Channel Data Txout 2-	O - DP	-	NC on ETX-AT-N270-18
21	GND	Ground	PWR	-	-
22	GND	Ground	PWR	-	-
23	LCD8	First LVDS Channel Data Txout 3-	O - DP	-	NC on ETX-AT-N270-18
24	LCD11	Second LVDS Channel Data Txout 0+	O - DP	-	-
25	LCD9	First LVDS Channel Data Txout 3+	O - DP	-	NC on ETX-AT-N270-18
26	LCD10	Second LVDS Channel Data Txout 0-	O - DP	-	-
27	GND	Ground	PWR	-	-
28	GND	Ground	PWR	-	-
29	LCD4	First LVDS Channel Data Txout 2-	O - DP	-	-
30	LCD7	First LVDS Channel Data Txclk +	O - DP	-	-
31	LCD5	First LVDS Channel Data Txout 2+	O - DP	-	-
32	LCD6	First LVDS Channel Data Txclk -	O - DP	-	-
33	GND	Ground	PWR	-	-
34	GND	Ground	PWR	-	-
35	LCD1	First LVDS Channel Data Txout 0+	O - DP	-	-
36	LCD3	First LVDS Channel Data Txout 1+	O - DP	-	-
37	LCD0	First LVDS Channel Data Txout 0-	O - DP	-	-
38	LCD2	First LVDS Channel Data Txout 1-	O - DP	-	-
39	5VCC	Power +5V	PWR	-	-
40	5VCC	Power +5V	PWR	-	-
41	JILI_DAT	JILI I2C Data Signal	IO-3,3	PU 10k 3,3V	-
42	LTGIO0	Display Backlight Control	O-5	-	-
43	JILI_CLK	JILI I2C Clock Signal	IO-3,3	PU 10k 3,3V	-
44	BLON#	Display Backlight On	O-5	-	-
45	BIASON	Display Contrast	NC	-	-
46	DIGON	Display Power On	O-5	-	-
47	COMP	Composite Video / SCART Blue	OA	-	-
48	Y	S-Video Luminance / SCART Red	OA	-	-
49	SYNC	Composite Sync	NC	-	-
50	C	S-Video Chrominance / SCART Green	OA	-	-

Signal Descriptions (cont'd)

X3

Pin	Signal	Description	Type	PU/PD	Comment
51	LPT | FLPY#	LPT / Floppy Interface Select	IO-3,3	PU 10k 3,3V	-
52	RSV	-	NC	-	-
53	5VCC	Power +5V	PWR	-	-
54	GND	Ground	PWR	-	-
55	STB# | RSV	LPT Strobe Signal	O-5	-	-
56	AFD# | DENSEL	LPT Automatic Feed / Floppy Density Select	O-5	-	-
57	RSV	-	NC	-	-
58	PD7 | RSV	LPT Data Bus D7	IO-5	-	-
59	IRRX	Infrared Receive	I-5	-	-
60	ERR# | HDSEL#	LPT Error / Floppy Head Select	IO-5	-	-
61	IRTX	Infrared Transmit	O-5	-	-
62	PD6 | RSV	LPT Data Bus D6	IO-5	-	-
63	RXD2	Data Receive COM2	I-5	-	-
64	INIT# | DIR#	LPT Initiate / Floppy Direction	O-5	-	-
65	GND	Ground	PWR	-	-
66	GND	Ground	PWR	-	-
67	RTS2#	Request to Send COM2	O-5	-	-
68	PD5 | RSV	LPT Data Bus D5	IO-5	-	-
69	DTR2#	Data Terminal Ready COM2	O-5	-	-
70	SLIN# | STEP#	LPT Select / Floppy Motor Step	O-5	-	-
71	DCD2#	Data Carrier Detect COM2	I-5	-	-
72	PD4 | DSKCHG#	LPT Data Bus D4	IO-5	-	-
73	DSR2#	Data Set Ready COM2	I-5	-	-
74	PD3 | RDATA#	LPT Data Bus D3	IO-5	-	-
75	CTS2#	Clear to Send COM2	I-5	-	-
76	PD2 | WP#	LPT Data Bus D2	IO-5	-	-
77	TXD2	Data Transmit COM2	O-5	PU 4k7 5V	-
78	PD1 | TRK0#	LPT Data Bus D1	IO-5	-	-
79	RI2#	Ring Indicator COM2	I-5	-	-
80	PD0 | INDEX#	LPT Data Bus D0	IO-5	-	-
81	5VCC	Power +5V	PWR	-	-
82	5VCC	Power +5V	PWR	-	-
83	RXD1#	Data Receive COM1	I-5	-	-
84	ACK# | DRV	LPT Acknowledge / Floppy Drive Select	IO-5	-	-
85	RTS1#	Request to Send COM1	O-5	PD 4k7	-
86	BUSY# | MOT	LPT Busy / Floppy Motor Select	IO-5	-	-
87	DTR1#	Data Terminal Ready COM1	O-5	-	-
88	PE | WDATA#	LPT Paper Empty / Floppy Raw Write Data	IO-5	-	-
89	DCD1#	Data Carrier Detect COM1	I-5	-	-
90	SLCT#|WGATE#	LPT Power On / Floppy Write Enable	IO-5	-	-
91	DSR1#	Data Set Ready COM1	I-5	-	-
92	MSCLK	Mouse Clock	O-5	PU 4k7 5V	-
93	CTS1#	Clear to Send COM1	I-5	-	-
94	MSDAT	Mouse Data	O-5	PU 4k7 5V	-
95	TXD1	Data Transmit COM1	O-5	PU 4k7 5V	-
96	KBCLK	Keyboard Clock	O-5	PU 4k7 5V	-
97	RI1#	Ring Indicator COM1	I-5	-	-
98	KBDAT	Keyboard Data	O-5	PU 4k7 5V	-
99	GND	Ground	PWR	-	-
100	GND	Ground	PWR	-	-

Signal Descriptions (cont'd)

X4

Pin	Signal	Description	Type	PU/PD	Comment
1	GND	Ground	PWR	-	-
2	GND	Ground	PWR	-	-
3	5V_SB	Supply of internal suspend Circuit	PWR	-	-
4	PWGIN	Power Good / Reset Input	I-3,3	-	-
5	PS_ON	Power Supply On	O-5	PU 4k7 3,3VSB	-
6	SPEAKER	Speaker Output	O-5	PU 1k 5V	-
7	PWRBTN#	Power Button	I-5	PU 10k 3,3VSB	-
8	BATT	Battery Supply	PWR	-	-
9	KBINH	Keyboard Inhibit Control Input	I-5	PU 8k2 5V	-
10	LILED	Ethernet Link LED	O-3,3	-	-
11	RSMRST#	Resume Reset input	I-3,3	PU 20k 3,3VSB	-
12	ACTLED	Ethernet Activity LED	O-3,3	-	-
13	ROMKBCS#	-	NC	-	-
14	SPDLED	Ethernet Speed LED	O-3,3	-	-
15	EXT_PRG	-	NC	-	-
16	I2CLK	I2C Bus Clock	O-5	PU 10k 3,3V	
17	5VCC	Power +5V	PWR	-	-
18	5VCC	Power +5V	PWR	-	-
19	OVCR#	Over Current Detect for USB	I-3,3	PU 4k7 3,3VSB	-
20	GPCS#	-	NC	-	-
21	EXTSMI#	System Management Interrupt Input	I-3,3	PU 8k2 3,3V	-
22	I2DAT	I2C Bus Data	IO-5	PU 10k 3,3V	-
23	SMBCLK	SM Bus Clock	O-3,3	PU 2k2 3,3V	-
24	SMBDATA	SM Bus Data	IO-3,3	PU 2k2 3,3V	-
25	S_CS3#	Secondary IDE Chip Select Channel 1	O-3,3	-	-
26	SMBALERT	SM Bus Alert	I-3,3	PU 10k 3,3VSB	-
27	S_CS1#	Secondary IDE Chip Select Channel 0	O-3,3	-	-
28	DASP_S	-	I-3,3	PD 10k	-
29	S_A2	Secondary IDE Adress Bus	O-3,3	-	-
30	P_CS3#	Primary IDE Chip Select Channel 1	O-3,3	-	-
31	S_A0	Secondary IDE Adress Bus	O-3,3	-	-
32	P_CS1#	Primary IDE Chip Select Channel 0	O-3,3	-	-
33	GND	Ground	PWR	-	-
34	GND	Ground	PWR	-	-
35	PDIAG_S	80-conductor IDE cable Channel 1	I-3,3	-	-
36	P_A2	Primary IDE Adress Bus	O-3,3	-	-
37	S_A1	Secondary IDE Adress Bus	O-3,3	-	-
38	P_A0	Primary IDE Adress Bus	O-3,3	-	-
39	S_INTRQ	Secondary IDE Interrupt Request	I-3,3	PD 10k	-
40	P_A1	Primary IDE Adress Bus	O-3,3	-	-
41	BATLOW#	Battery Low	I-3,3		-
42	GPE1#	-	NC	-	-
43	S_AK#	Secondary IDE DMA Acknowledge	O-3,3	-	-
44	P_INTRQ	Primary IDE Interrupt Reqeuest	I-3,3	PU 8k2 3,3V	-
45	S_RDY	Secondary IDE Ready	I-3,3	PU 4k7 3,3V	-
46	P_AK#	Primary IDE DMA Acknowledge	O-3,3	-	-
47	S_IOR#	Secondary IDE IO Read	O-3,3	-	-
48	P_RDY	Primary IDE Ready	I-3,3	PU 4k7 3,3V	-
49	5VCC	Power +5V	PWR	-	-
50	5VCC	Power +5V	PWR	-	-

Signal Descriptions (cont'd)

X4

Pin	Signal	Description	Type	PU/PD	Comment
51	S_IOW#	Secondary IDE IO Write	O-3,3	-	-
52	P_IOR#	Primary IDE IO Read	O-3,3	-	-
53	S_DRQ	Secondary IDE DMA Request	I-3,3	-	-
54	P_IOW#	Primary IDE IO Write	O-3,3	-	-
55	S_D15	Secondary IDE Data Bus	IO	-	-
56	P_DRQ	Primary IDE DMA Request	I-3,3	-	-
57	S_D0	Secondary IDE Data Bus	IO	-	-
58	P_D15	Primary IDE Data Bus	IO	-	-
59	S_D14	Secondary IDE Data Bus	IO	-	-
60	P_D0	Primary IDE Data Bus	IO	-	-
61	S_D1	Secondary IDE Data Bus	IO	-	-
62	P_D14	Primary IDE Data Bus	IO	-	-
63	S_D13	Secondary IDE Data Bus	IO	-	-
64	P_D1	Primary IDE Data Bus	IO	-	-
65	GND	Ground	PWR	-	-
66	GND	Ground	PWR	-	-
67	S_D2	Secondary IDE Data Bus	IO	-	-
68	P_D13	Primary IDE Data Bus	IO	-	-
69	S_D12	Secondary IDE Data Bus	IO	-	-
70	P_D2	Primary IDE Data Bus	IO	-	-
71	S_D3	Secondary IDE Data Bus	IO	-	-
72	P_D12	Primary IDE Data Bus	IO	-	-
73	S_D11	Secondary IDE Data Bus	IO	-	-
74	P_D3	Primary IDE Data Bus	IO	-	-
75	S_D4	Secondary IDE Data Bus	IO	-	-
76	P_D11	Primary IDE Data Bus	IO	-	-
77	S_D10	Secondary IDE Data Bus	IO	-	-
78	P_D4	Primary IDE Data Bus	IO	-	-
79	S_D5	Secondary IDE Data Bus	IO	-	-
80	P_D10	Primary IDE Data Bus	IO	-	-
81	5VCC	Power +5V	PWR	-	-
82	5VCC	Power +5V	PWR	-	-
83	S_D9	Secondary IDE Data Bus	IO	-	-
84	P_D5	Primary IDE Data Bus	IO	-	-
85	S_D6	Secondary IDE Data Bus	IO	-	-
86	P_D9	Primary IDE Data Bus	IO	-	-
87	S_D8	Secondary IDE Data Bus	IO	-	-
88	P_D6	Primary IDE Data Bus	IO	-	-
89	GPE2#	-	NC	-	-
90	CBLID_P#	80-conductor IDE cable Channel 0	I-3,3	-	-
91	RXD#	Ethernet Receive Differential Signal (RXD-)	I - DP	-	-
92	P_D8	Primary IDE Data Bus	IO	-	-
93	RXD	Ethernet Receive Differential Signal (RXD+)	I - DP	-	-
94	S_D7	Secondary IDE Data Bus	IO	-	-
95	TXD#	Ethernet Transmit Differential Signal (TXD-)	O -DP	-	-
96	P_D7	Primary IDE Data Bus	IO	-	int. PD 11k5
97	TXD	Ethernet Transmit Differential Signal (TXD+)	O -DP	-	-
98	HDRST#	Hard Drive Reset	O-3,3	-	-
99	GND	Ground	PWR	-	-
100	GND	Ground	PWR	-	-

Signal Descriptions (cont'd)

Signal Type Legend	
IO-2,5	Bi-directional 2,5 V Input/Output
IO-3,3	Bi-directional 3,3 V Input/Output
IO-5	Bi-directional 5 V Input/Output
I-3,3	3,3 V Input
I-5	5 V Input
O-2,5	2,5 V Output
O-3,3	3,3 V Output
O-5	5 V Output
IO	Input/Output
OA	Analog Output
I/O - DP	Differential Pair Input/Output
O - DP	Differential Pair Output
I - DP	Differential Pair Input
PWR	Power or Ground
PU	Pull-Up Resistor
PD	Pull-Down Resistor
NC	Not Connected / Reserved

7 System Resources

7.1 System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
(4GB-2MB)	FFE00000 - FFFFFFFF	2 MB	High BIOS Area
(4GB-18MB)-(4GB-17MB-1)	FEE00000 - FEEFFFFF	1 MB	FSB Interrupt Memory Space
(4GB-19MB)-(4GB-18MB-1)	FED00000 – FEDFFFFF	1 MB	Chipset configuration Space
(4GB-20MB)-(4GB-19MB-1)	FEC00000 – FECFFFFF	1 MB	APIC Configuration Space
15MB - 16MB	F00000 - FFFFFF	1 MB	ISA Hole
960 K - 1024 K	F0000 - FFFFF	64 KB	System BIOS Area
896 K - 960 K	E0000 - EFFFF	64 KB	Extended System BIOS Area
768 K - 896 K	C0000 - DFFFF	128 KB	PCI expansion ROM area C0000 - CEFFF: Onboard VGA BIOS CF000 - D0FFF: PXE option ROM when onboard LAN boot ROM is enabled.
640 K - 768 K	A0000 - BFFFF	128 KB	Video Buffer & SMM space
0 K - 640 K	00000 - 9FFFF	640 KB	DOS Area

7.2 Direct Memory Access Channels

Channel Number	Data Width	System Resource
0	8-bits	Parallel port, Note 1
1	8-bits	Parallel port, Note 1
2	8-bits	Diskette drive, Note 1
3	8-bits	Parallel port, Note 1
4		Reserved, Cascade Channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

DMA channel 0/1/3 is selected when using parallel port. DMA2 is used by Floppy.

7.3 I/O Address Map

Address (hex)	Size	Description
0000 – 001F	32 bytes	DMA controller
0020 – 0021	2 bytes	Interrupt controller
0024 – 0025	2 bytes	Interrupt controller
0028 – 0029	2 bytes	Interrupt controller
002C – 002D	2 bytes	Interrupt controller
002E - 002F	2 bytes	LPC SIO
0030 – 0031	2 bytes	Interrupt controller
0034 – 0035	2 bytes	Interrupt controller
0038 – 0039	2 bytes	Interrupt controller
003C – 003D	2 bytes	Interrupt controller
0040 – 0043	4 bytes	Counter/Timer
0048 – 004B	4 bytes	Counter/Timer
004E – 004F	2 bytes	TPM configuration port
0050 – 0053	4 bytes	Counter/Timer
0060	1 byte	Keyboard controller
0061	1 byte	NMI, speaker control
0063	1 byte	NMI controller
0064	1 byte	Keyboard controller
0065	1 byte	NMI controller
0067	1 byte	NMI controller
0070 – 0071	2 bytes	Real time clock controller
0072 – 0073	2 bytes	Real time clock controller
0074 – 0075	2 bytes	Real time clock controller
0076 – 0077	2 bytes	Real time clock controller
0080 – 0091	18 bytes	DMA controller
0092	1 bytes	Reset Generator
0093 – 009F	13 bytes	DMA controller
00A0 – 00A1	2 bytes	Interrupt controller
00A4 – 00A5	2 bytes	Interrupt controller
00A8 – 00A9	2 bytes	Interrupt controller
00AC – 00AD	2 bytes	Interrupt controller
00B0 – 00B1	2 bytes	Interrupt controller
00B2 – 00B3	2 bytes	Power Management
00B4 – 00B5	2 bytes	Interrupt controller
00B8 – 00B9	2 bytes	Interrupt controller
00BC – 00BD	2 bytes	Interrupt controller
00C0 – 00DF	32 bytes	DMA controller
00F0 – 00FF	16 bytes	Numeric processor
0170 – 0177	8 bytes	Secondary IDE controller
01F0 – 01F7	8 bytes	Primary IDE controller
0274 – 0277	4 bytes	ISA PnP read port
0278 – 027F	8 bytes	LPT2
0290 – 029F	16 bytes	Onboard Sensor index(0x295)/data port (0x296)
02E8 – 02EF	8 bytes	COM4/Video

I/O Address Map (cont'd)

Address (hex)	Size	Description
02F8 – 02FF	8 bytes	COM2
0376 – 0377	2 bytes	Secondary IDE controller
0378 – 037F	8 bytes	LPT1
03B0 – 03BB	12 bytes	Video (monochrome)
03BC – 03BF	4 bytes	LPT3
03C0 – 03DF	32 bytes	Video (VGA†)
03E8 – 03EF	8 bytes	COM3
03F0 – 03F5, 03F7	7 bytes	Diskette controller
03F6 – 03F7	2 bytes	Primary IDE controller
03F8 – 03FF	8 bytes	COM1
0400 – 041F	32 bytes	Onboard SMBus control registers
0480 – 04BF	64 bytes	GPIO control registers
04D0 – 04D1	2 bytes	Edge/level triggered PIC
0800 – 087F	128 bytes	ACPI control registers
0A79 – 0A79	1 bytes	ISA PnP read data Port
0CF8 – 0CFF*	8 bytes	PCI configuration registers
0CF9**	1 byte	Reset control register
04700 – 0470F	16 bytes	TPM control registers
0C4802-0C49F	32Byte	USB Host Controller
0C800-0C81F	32Byte	USB Host Controller
0C880-0C89F	32Byte	USB Host Controller
0CC00-0CC1F	32Byte	USB Host Controller
0CC80-CC87	8Byte	Video
0D480-0D48F	16Byte	PCI IDE Controller
0D800-0D803	4Byte	PCI IDE Controller
0DC00-0DC03	4Byte	PCI IDE Controller
0DC80-ODC87	8Byte	PCI IDE Controller
0FFA0-0FFAF	16Byte	Serial ATA Storage Controller

NOTE:

* DWORD access only
** Byte access only

7.4 Interrupt Request (IRQ) Lines

PIC Mode

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
0	Counter 0	N/A	No
1	Keyboard controller	N/A	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 2 (COM2) / PCI	IRQ3 via SERIRQ	Note (1)
4	Serial Port 1 (COM1) / PCI	IRQ4 via SERIRQ	Note (1)
5	Parallel Port 2 (LPT2) / PCI	IRQ5 via SERIRQ	Note (1)
6	Floppy Drive Controller	IRQ6 via SERIRQ	No
7	Parallel Port 1 (LPT1) / PCI	IRQ7 via SERIRQ,	Note (1)
8	Real-time clock	N/A	No
9	SCI / PCI	IRQ9 via SERIRQ	Note (1)
10	PCI	IRQ10 via SERIRQ	Note (1)
11	PCI	IRQ11 via SERIRQ	Note (1)
12	PS/2 Mouse / PCI	IRQ12 via SERIRQ	Note (1)
13	Math Processor	N/A	No
14	Primary IDE controller / PCI	IRQ14 via SERIRQ	Note (1)
15	Secondary IDE controller / PCI	IRQ15 via SERIRQ	Note (1)

(1) These IRQs can be used for PCI devices when onboard device is disabled.

APIC Mode

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
0	Counter 0	N/A	No
1	Keyboard controller	N/A	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 2 (COM2) / PC	IRQ3 via SERIRQ	Note (1)
4	Serial Port 1 (COM1) / PCI	IRQ4 via SERIRQ	Note (1)
5	Parallel Port 2 (LPT2) / PCI	IRQ5 via SERIRQ	Note (1)
6	Floppy Drive Controller	IRQ6 via SERIRQ	No
7	Parallel Port 1 (LPT1) / PCI / ISA	IRQ7 via SERIRQ	Note (1)
8	Real-time clock	N/A No	
9	SCI / PCI	IRQ9 via SERIRQ	Note (1),
10	PCI	IRQ10 via SERIRQ	Note (1)
11	PCI	IRQ11 via SERIRQ	Note (1)
12	PS/2 Mouse / PCI	IRQ12 via SERIRQ	Note (1)
13	Math Processor	N/A	No
14	Primary IDE controller / PCI	IRQ14 via SERIRQ	Note (1)

APIC Mode (cont'd)

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
15	Secondary IDE controller / PCI	IRQ15 via SERIRQ	Note (1)
16	N/A	PCI Slot INT A, USB, VGA controller, Audio controller, IDE controller	Yes
17	N/A	PCI Slot INT B, USB	Yes
18	N/A	PCI Slot INT C	Yes
19	N/A	PCI Slot INT D, USB controller	Yes
20	N/A		No
21	N/A		No
22	N/A		No
23	N/A	EHCI, USB	No

(1) These IRQs can be used for PCI devices when an onboard device is disabled.

7.5 PCI Configuration Space Map

Bus #	Device #	Function #	Routing	Description
00h	00h	00h	N/A	Intel 945 GSE GMCH Host-Hub Interface Bridge
00h	02h	00h	Internal	Intel Integrated Graphics Device
00h	02h	01h	Internal	Intel Integrated Graphics Device (Function 1)
00h	1Bh	00h	Internal	High Definition Audio controller
00h	1Ch	00h	Internal	Intel ICH Express Root port
00h	1Dh	00h	Internal	Intel USB UHCI Controller 1
00h	1Dh	01h	Internal	Intel USB UHCI Controller 2
00h	1Dh	02h	Internal	Intel USB UHCI Controller 3
00h	1Dh	03h	Internal	Intel USB UHCI Controller 4
00h	1Dh	07h	Internal	Intel USB EHCI Controller
00h	1Eh	00h	N/A	Intel Hub Interface to PCI Bridge
00h	1Fh	00h	N/A	Intel LPC Interface Bridge
00h	1Fh	01h	Internal	Intel IDE Controller
00h	1Fh	02h	Internal	Intel SATA controller
00h	1Fh	03h	Internal	Intel SMBus Controller
01h	00h	00h	onboard	JMB368 PCI IDE controller
02h	07h	00h	onboard	ITE8888 PCI to ISA Bridge
02h	08h	00h	onboard	Onboard LAN controller

7.6 PCI Interrupt Routing Map

PIRQ	A	B	C	D	E	F	G	H
INT Line	INTA	INTB	INTC	INTD				
VGA	X							
UHCI 1	X							
UHCI 2		X						
UHCI 3			X					
UHCI 4				X				
EHCI	X							
SATA			X					
SMbus			X					
Audio	X							
PCI Slot1	INTA	INTB	INTC	INTD				
PCI Slot2	INTB	INTC	INTD	INTA				
PCI Slot3	INTC	INTD	INTA	INTB				
PCI Slot4	INTD	INTA	INTB	INTC				
LAN					INTA			

7.7 System Management Bus (I2C-compatible)

Internally the SMB bus and I2C bus are one and the same. The ICH7-M Southbridge supports SMBDAT and SMBCLK lines that are I2C-compatible.

The X4 connector has pins for both the I2C and SMB bus. Both are connected to the same internal bus: the SMB bus. It is advisable to always connect external I2C devices to the I2C pins and SMB devices to the SMB pins to ensure compatibility with other modules that might support two internal busses (a separate I2C and SMB bus).

Address	Function	Device
2Eh	Super I/O Read/Write	SIO
A0h	Memory SPD	SO-DIMM
D2h	Clock Generator	CLK GEN

8 BIOS Setup Utility

The following chapter describes basic navigation for the AMIBIOS8 BIOS setup utility.

8.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keyboard when you see the following text prompt:

   < Press DEL or Delete to run Setup >

3. After you press the < Delete > key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu, such as Chipset and Power menus.

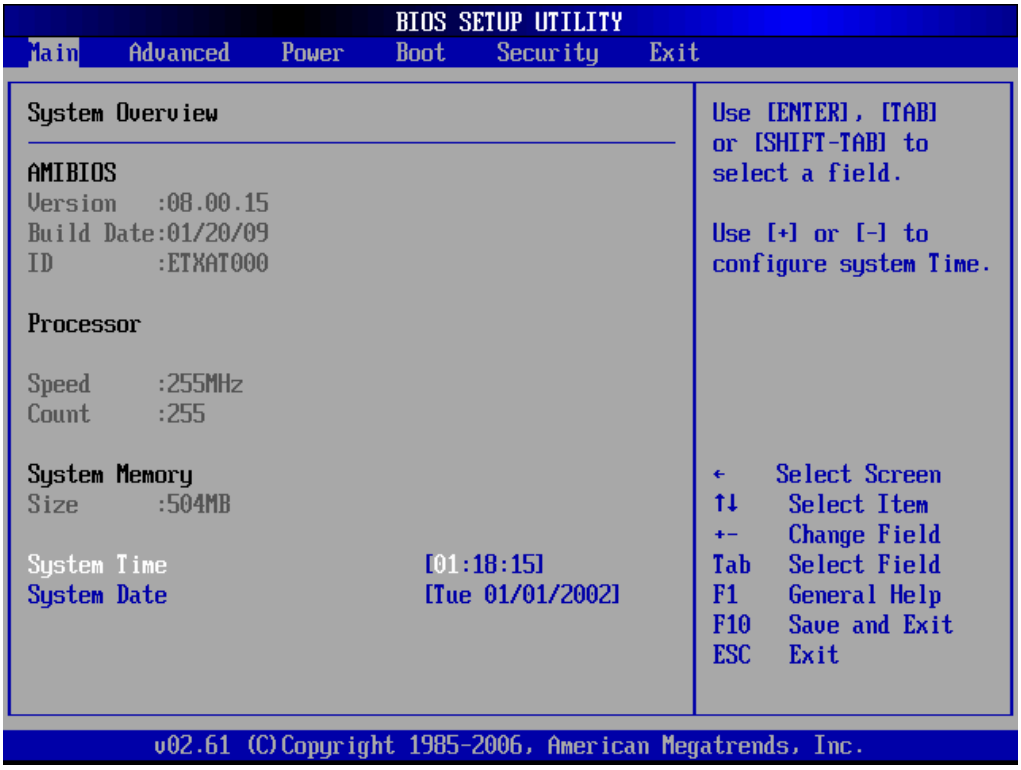
NOTE: In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

8.1.1 Main Setup Menu

The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

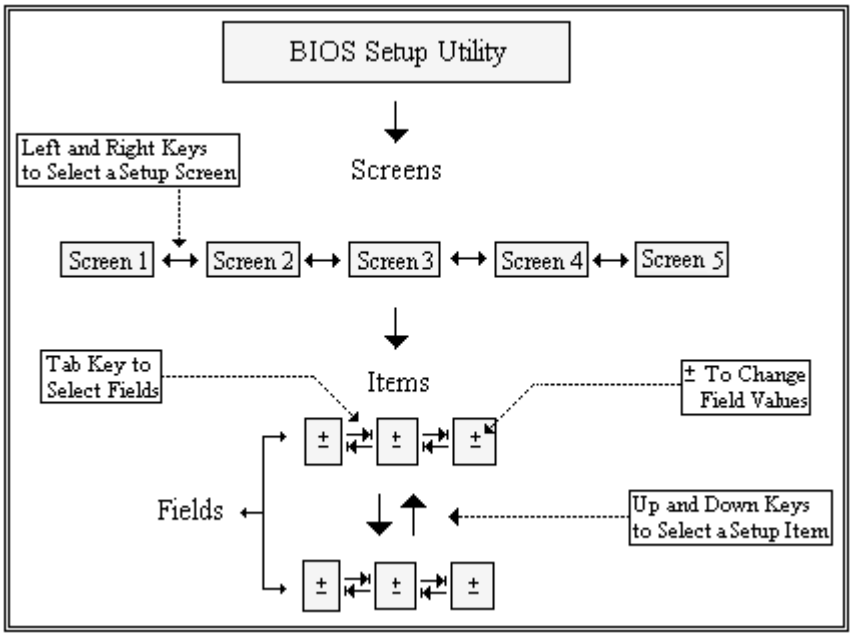
The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed" options cannot be configured, "Blue" options can be.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.



8.1.2 Navigation

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process.
These keys include < F1 >, < F10 >, < Enter >, < ESC >, < Arrow > keys, and so on.

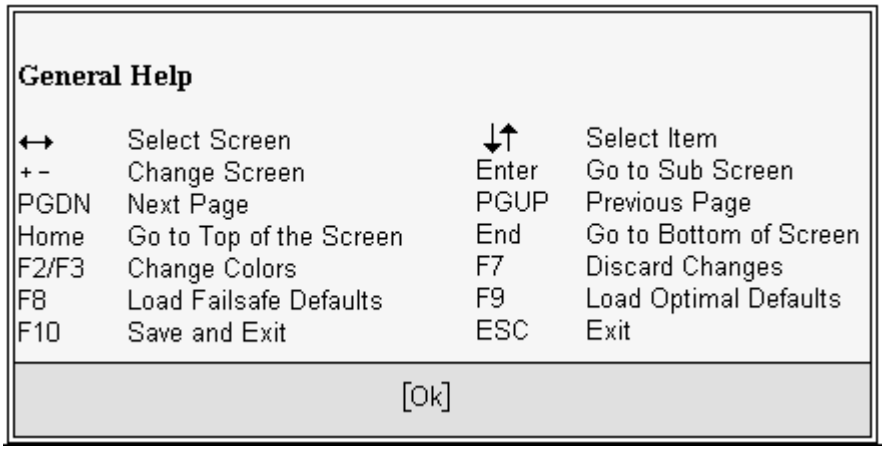


NOTE: There is a hot key legend located in the right frame on most setup screens.

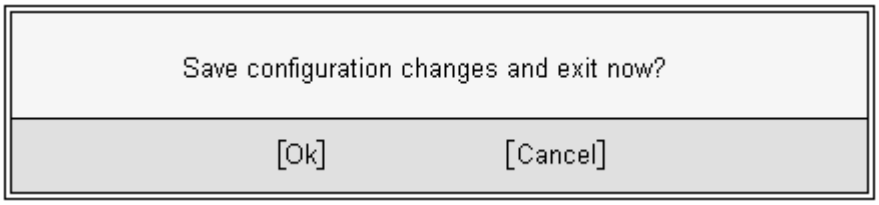
Hot Key	Description
→←	Left/Right The *Left and Right* < Arrow > keys allow you to select a setup screen. For example: Main screen, Advanced screen, Chipset screen, and so on.
↑↓	Up/Down The *Up and Down* < Arrow > keys allow you to select a setup item or sub-screen.
+ −	Plus/Minus The *Plus and Minus* < Arrow > keys allow you to change the field value of a particular setup item. For example: Date and Time.
Tab	The < Tab > key allows you to select setup fields.

NOTE: The < F8 > key on your keyboard is the Fail-Safe key. It is not displayed on the key legend by default. To set the Fail-Safe settings of the BIOS, press the < F8 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The Fail-Safe settings allow the motherboard to boot up with the least amount of options set. This can lessen the probability of conflicting settings.

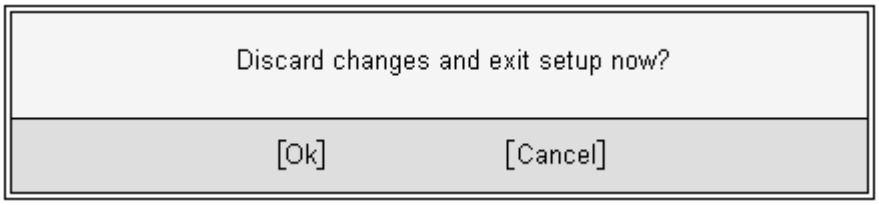
Hot Key	Description
F1	The < F1 > key allows you to display the *General Help screen*. Press the < F1 > key to open the *General Help screen*.



F10	The < F10 > key allows you to save any changes you have made and exit Setup. Press the < F10 > key to save your changes. The following screen will appear:



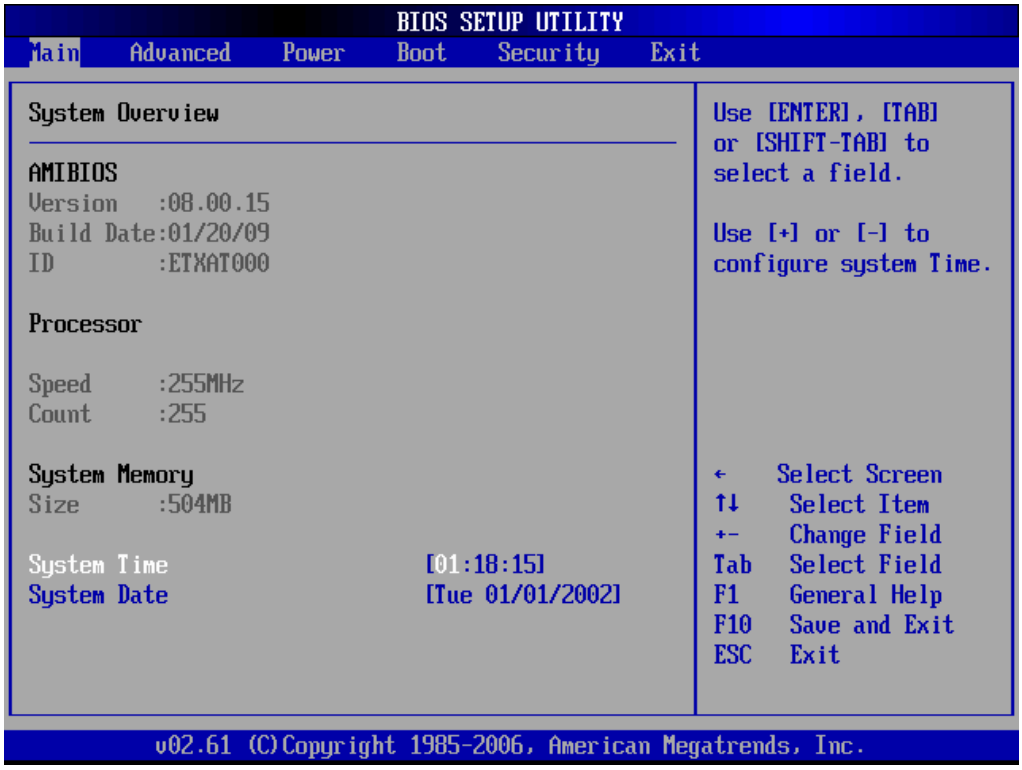
	Press the < Enter > key to save the configuration and exit. You can also use the < Arrow > key to select *Cancel* and then press the < Enter > key to abort this function and return to the previous screen.
ESC	The < Esc > key allows you to discard any changes you have made and exit the Setup. Press the < Esc > key to exit the setup without saving your changes. The following screen will appear:



	Press the < Enter > key to discard changes and exit. You can also use the < Arrow > key to select *Cancel* and then press the < Enter > key to abort this function and return to the previous screen.
Enter	The < Enter > key allows you to display or change the setup option listed for a particular setup item. The < Enter > key can also allow you to display the setup sub-screens.

8.2 Main Setup

When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the *Main* tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



8.2.1 System Time/System Date

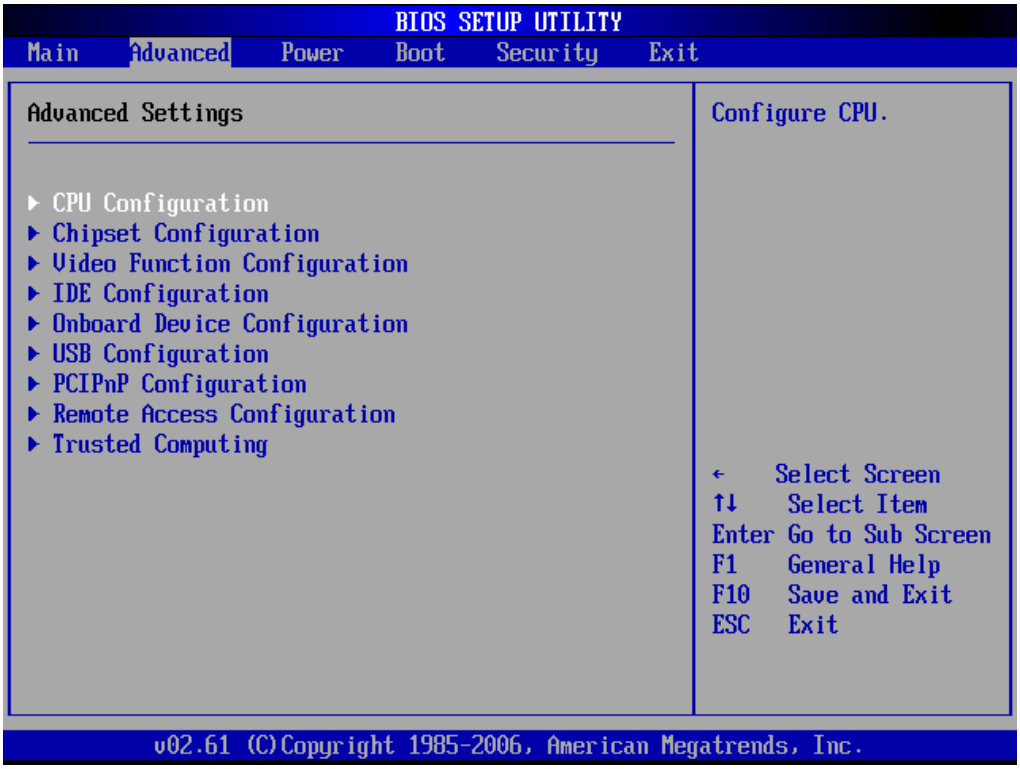
Use this option to change the system time and date. Highlight *System Time* or *System Date* using the < `Arrow` > keys. Enter new values using the keyboard. Press the < `Tab` > key or the < `Arrow` > keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

NOTE: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

8.3 Advanced BIOS Setup

Select the *Advanced* tab from the setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as SuperIO Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the < `Arrow` > keys. The Advanced BIOS Setup screen is shown below.

The sub menus are described on the following pages.

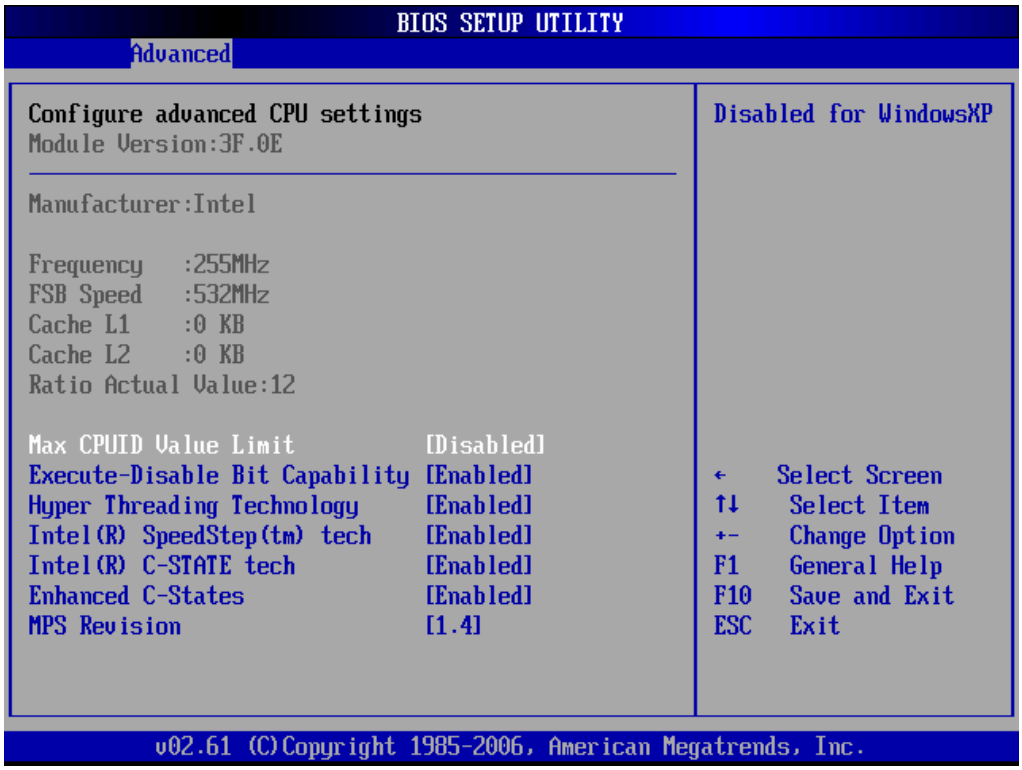


Setting incorrect or conflicting values in Advanced BIOS Setup may cause system malfunctions.

8.3.1 CPU Configuration

CPU Configuration Settings

You can use this screen to select options for the CPU Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the *CPU Configuration* screen is shown below.



Max CPUID Value Limit

When the computer is boots, the operating system executes its CPUID instruction to identify the processor and its capabilities. Before it can do so, it must first query the processor to find out the highest input value the CPUID recognizes. This determines the kind of basic information CPUID can provide the operating system. This option allows you to circumvent problems with older operating systems.

When Enabled, the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When Disabled, the processor will return the actual maximum CPUID input value of the processor when queried.

Execute Disable Bit Capability

This is an Intel hardware-based security feature that can help reduce system exposure to viruses and malicious code. It allows the processor to classify areas in memory where application code can or cannot execute. When a malicious worm attempts to insert code in the buffer, the processor disables its code execution, preventing damage and worm propagation. To use Execute Disable Bit you must have a PC or server with a processor with Execute Disable Bit capability and a supporting operating system.

Hyper Threading Technology

This item allows you to Enable/Disable Hyper-Threading Technology.

Intel® SpeedStep tech

This option enables or disables Intel SpeedStep technology.

Intel® C-STATE tech

This item allows you to Enable/Disable the C-STATE function. C-STATE make the power and thermal control unit part of the core logic and not part of the chipset as before.

Enhanced C-STATE

This item allows you to Enable/Disable the Enhanced C-STATE function.

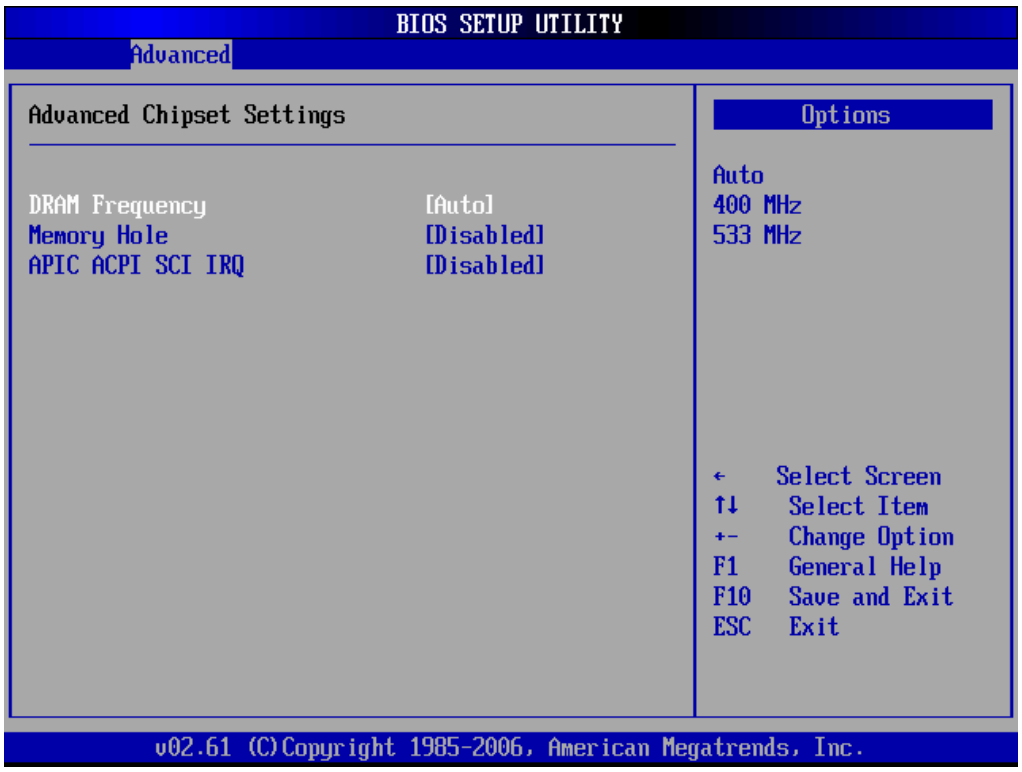
MPS Revision

This item allows you to select which MPS revision to use for the operating system.

8.3.2 Chipset Configuration

Chipset Configuration Settings

Select the Chipset tab from the setup screen to enter the Chipset BIOS Setup screen. You can select any of Chipset BIOS Setup options by highlighting it using the < Arrow > keys. The Chipset BIOS Setup screen is shown below.



DRAM Frequency

Set DRAM frequency. You can let frequency be set by BIOS automatically or configure it manually.

Configure DRAM Timing by SPD

Enable/Disable the timing set of DRAM is configured from SPD or set by manually.

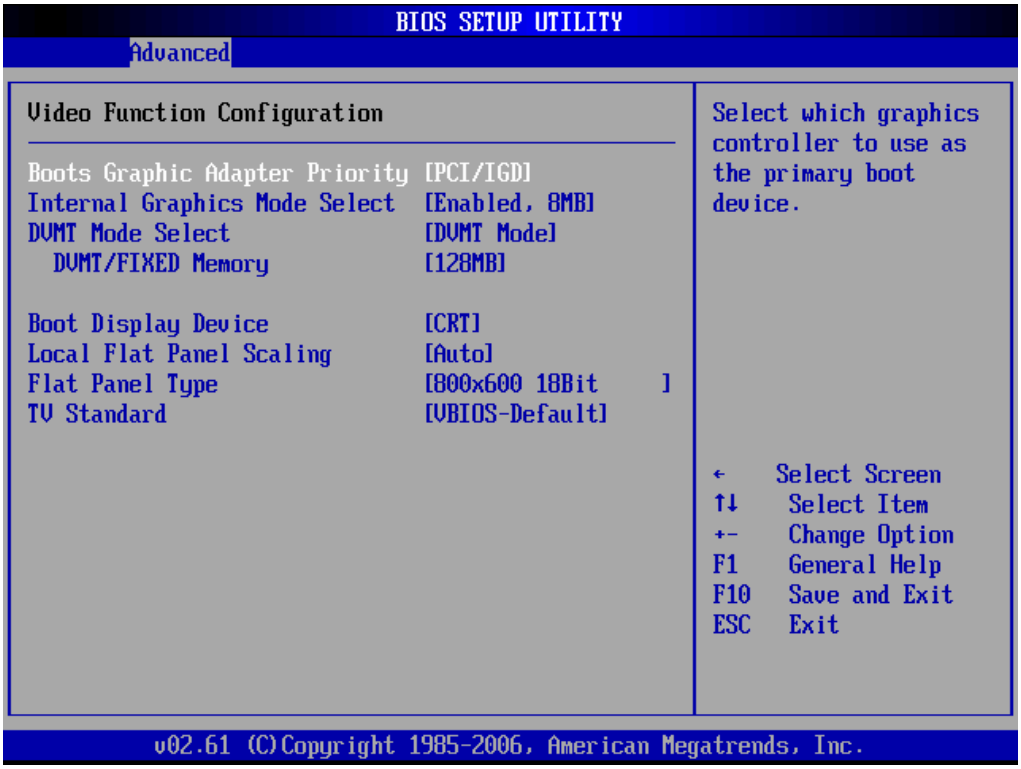
APIC ACPI SCI IRQ

This item allows you to enable or disable the APIC ACPI SCI interrupt.

8.3.3 Video Function Configuration

Video Function Configuration Settings

You can use this screen to select options for Video Function configuration settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The video function BIOS Setup screen is shown below.



Boots Graphic Adapter Priority

Select which graphics controller to use as the primary boot display device. IGD=Integrated Graphic device. PCI means external PCI graphics device.

Internal Graphics Mode Select

Select amount of system memory which is used by internal graphics device.

DVMT Mode Select

Unified Memory Architecture (UMA) is a concept whereby system memory is shared by both CPU and graphics processor. While this reduces cost, it also reduces the system's performance by taking up a large portion of memory for the graphics processor. Intel's Dynamic Video Memory Technology (DVMT) takes that concept further by allowing the system to dynamically allocate

memory resources according to the demands of the system at any point in time. The key idea in DVMT is to improve the efficiency of the memory allocated to either system or graphics processor.

When set to Fixed Mode, the graphics driver will reserve a fixed portion of the system memory as graphics memory. When set to DVMT Mode, the graphics chip will dynamically allocate system memory as graphics memory, according to system and graphics requirements. When set to Combo Mode, the graphics driver will allocate a fixed amount of memory as dedicated graphics memory, as well as allow more system memory to be dynamically allocated between the graphics processor and the operating system.

DVMT/FIXED Memory

Set the amount of memory according to DVMT Mode Select.

Boot Display Device

Select which display interface you want to make it active.

Local Flat Panel Scaling

Allows you to determine how various resolutions appear on your LCD display.

Auto: The scaling unit on your graphics card will rescale the image before it reaches your LCD display. This option results in the best image quality.

Forced Scaling: This option will maintain the original aspect ratio of the chosen resolution and display it with black bars to the sides/above/below the on-screen image as required.

Disabled: The image isn't scaled at all, but instead your LCD display will run at its maximum resolution and the image will display in the centre of your LCD display. This may result in a black border around the sides of the image.

Flat Panel Type

Once LVDS is selected from Boot Display Device, this option opens some resolution settings for correct timing out to LVDS interface you want to use.

TV Standard

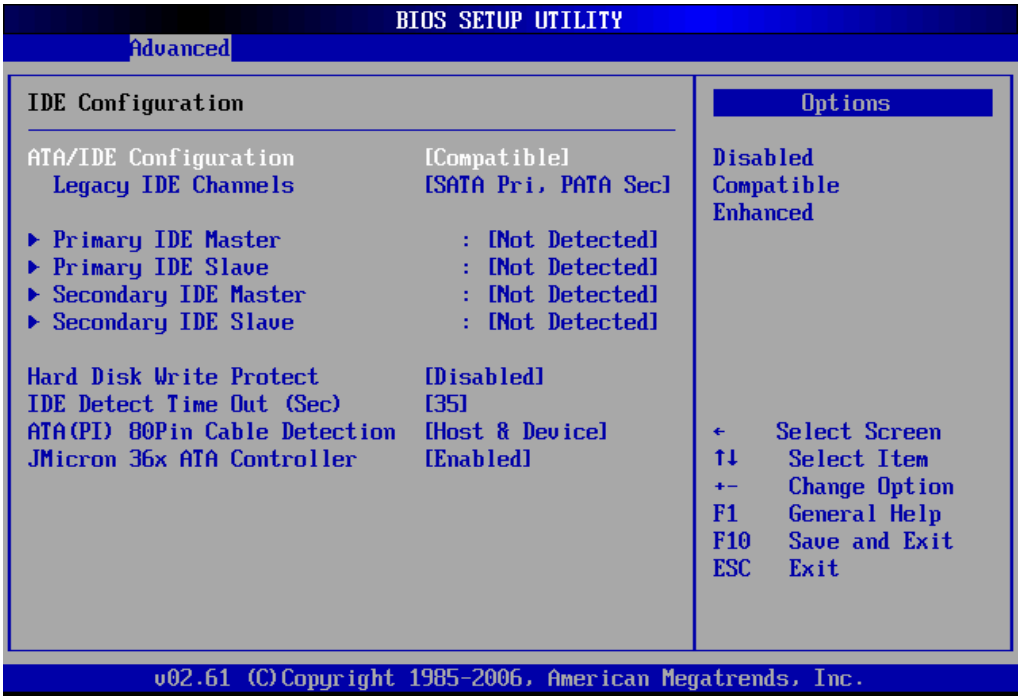
This field allows you to set the appropriate standard for your TV.

VBIOS-Default: Default setting of onboard VGA BIOS.
NTSC: National Television System Committee
PAL: Phase Alternating Line

8.3.4 IDE Configuration

IDE Configuration Settings

You can use this screen to select options for the IDE Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the *IDE Configuration* screen is shown below.



ATA/IDE Configuration

This item specifies whether the IDE channels should be initialized in Compatible or Enhanced mode of operation. The settings are Disabled, Compatible and Enhanced.

Legacy IDE Channels

When running in compatible mode, the SATA channel can be configured as a legacy IDE channel. The location of the IDE channel is selectable.

Primary IDE Master/Slave, Secondary IDE Master/Slave

Select one of the hard disk drives to configure it. Press < Enter > to access its sub menu.

Hard Disk Write Protect

Set this value to Enabled to prevent the hard disk drive from being overwritten.

IDE Detect Time Out

This field allows you to set the time to stop searching for IDE devices within the specified number of seconds.

ATA(PI)80Pin Cable Detection

Selects the method used to detect the type of IDE cable used.

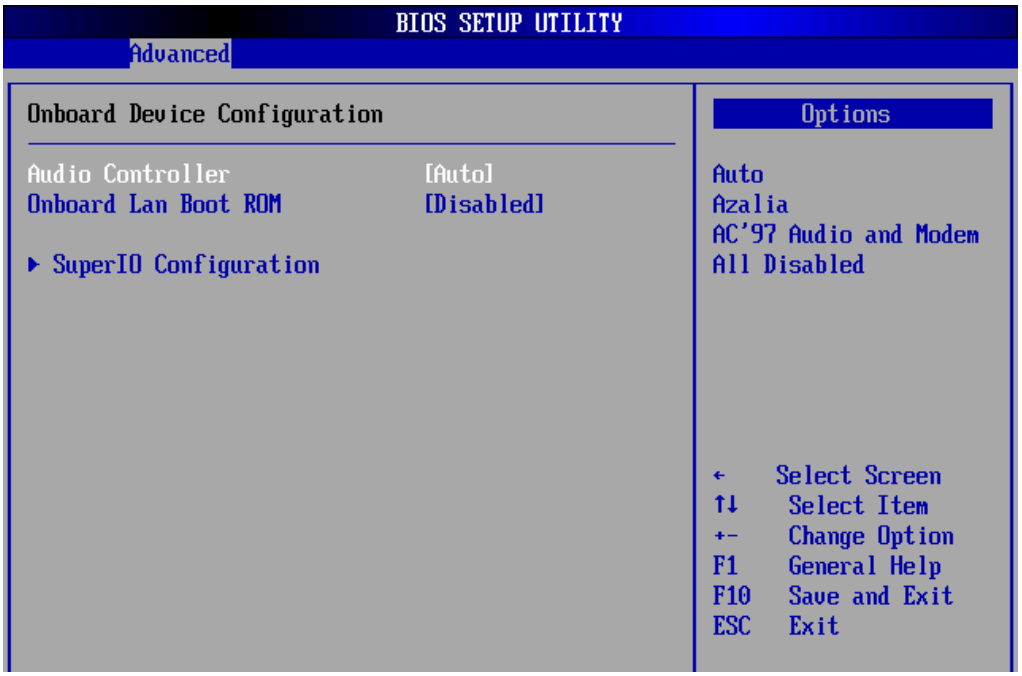
JMicron 36x ATA Controller

This field allows you to Enable/Disable the onboard PCI-E to IDE controller.

8.3.5 Onboard Device Configuration

Onboard Device Configuration Settings

You can use this screen to specify options for the onboard device configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



Audio Controller

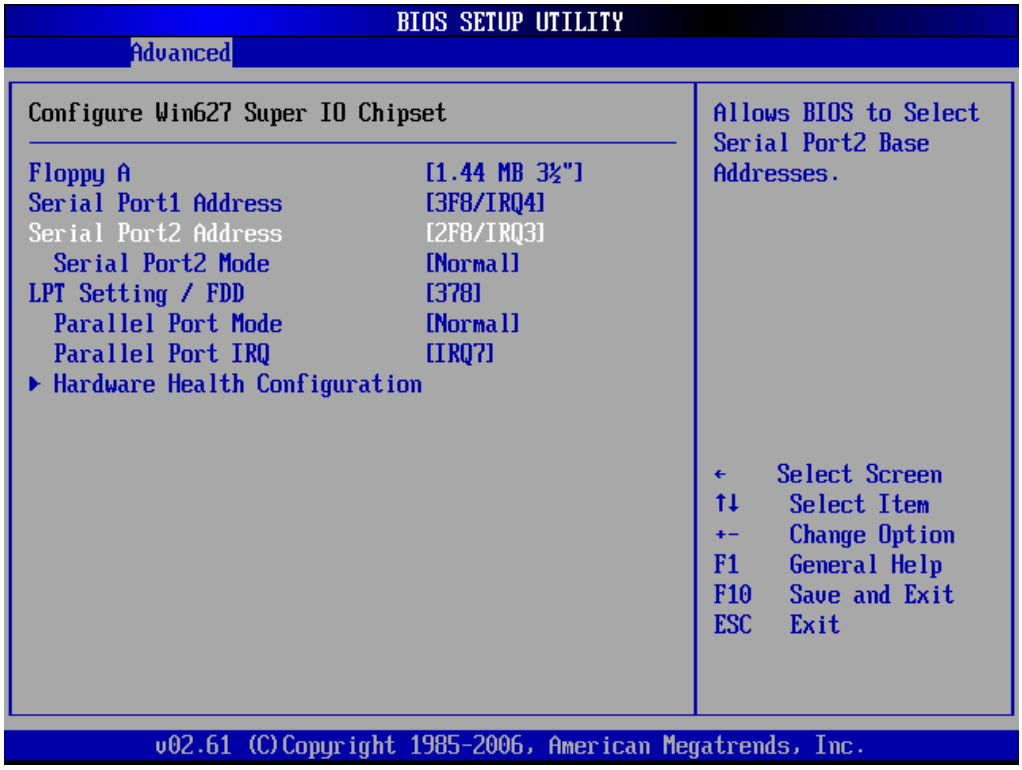
Set this value to Enable/Disable the Audio Controller.

Onboard Lan Boot ROM

Set this value to enable/disable the onboard LAN's PXE ROM to enable boot from LAN. Setting to Disabled can shorten the POST time without initializing LAN PXE ROM if boot from LAN is not needed.

SuperIO Configuration Screen

SuperIO configuration screen is a sub-menu of Onboard Device Configuration. You can use this screen to select options for the Super IO settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



Floppy A

Use this field to specify options for the Floppy Configuration Settings.

Options: Disabled, 360 KB 5 ¼", 1.2 MB 5 ¼", 720 KB 3 ½", 1.44 MB 3 ½", 2.88 MB 3 ½".

OnBoard Floppy Controller

This option enables/disables the Super IO's floppy controller.

Serial Port1 Address

This option specifies the base I/O port address and Interrupt Request address of serial port 1.

Option	Description
Disabled	Set this value to prevent the serial port from accessing any system resources. When this option is set to Disabled, the serial port physically becomes unavailable.
3F8/IRQ4	Set this value to allow the serial port to use 3F8 as its I/O port address and IRQ 4 for the interrupt address.
3E8/IRQ4	Set this value to allow the serial port to use 3E8 as its I/O port address and IRQ 4 for the interrupt address.
2F8/IRQ3	Set this value to allow the serial port to use 2F8 as its I/O port address and IRQ 3 for the interrupt address.
2E8/IRQ3	Set this value to allow the serial port to use 2E8 as its I/O port address and IRQ 3 for the interrupt address.

Serial Port2 Address

This option specifies the base I/O port address and Interrupt Request address of Serial Port2. The settings of Serial Port2 are the same as Serial Port1. However, the setting used by Serial Port1 will not be available for Serial Port2. For example, if Serial Port1 uses 3F8/IRQ4, the option, the 3F8/IRQ4 will not appear in the options of Serial Port2.

Serial Port2 Mode

This option allows the BIOS to select a mode for Serial Port2. The settings are Normal, IrDA, and ASK IR.

LPT Setting / FDD

This option can configure the SuperIO to operate in FDD mode or parallel (LPT) mode.In LPT mode, this option lets you configure the SuperIO's parallel port address. Options: FDD, Disabled, (LPT mode) 378, 278, 3BC.

Parallel Port Mode

This option specifies the parallel port mode.

Option	Description
Normal	Set this value to allow the standard parallel port mode to be used.
EPP	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bidirectional data transfer driven by the host device.
ECP	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Megabits per second. ECP provides symmetric Bidirectional communication.
EPP+ECP	Allows the parallel port to support both the ECP and EPP modes simultaneously.

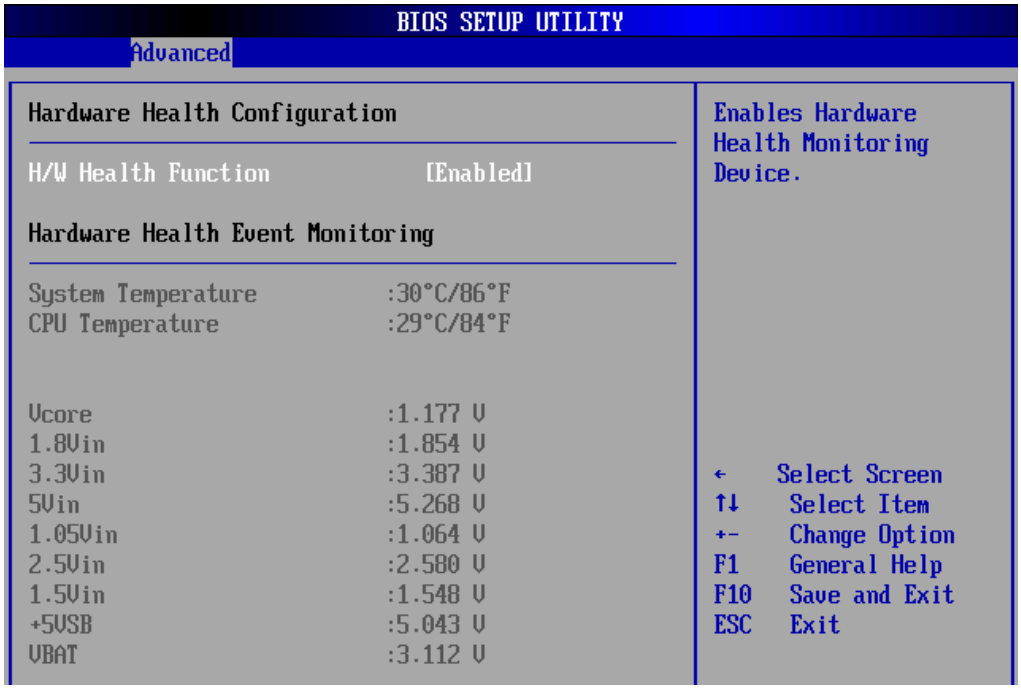
Parallel Port IRQ

This option specifies the IRQ used by the parallel port.

Option	Description
IRQ5	Set this value to allow the serial port to use Interrupt 5.
IRQ7	Set this value to allow the serial port to use Interrupt 7. The majority of parallel ports on computer systems use IRQ7 and I/O Port 378H as the standard setting.

Hardware Health Configuration

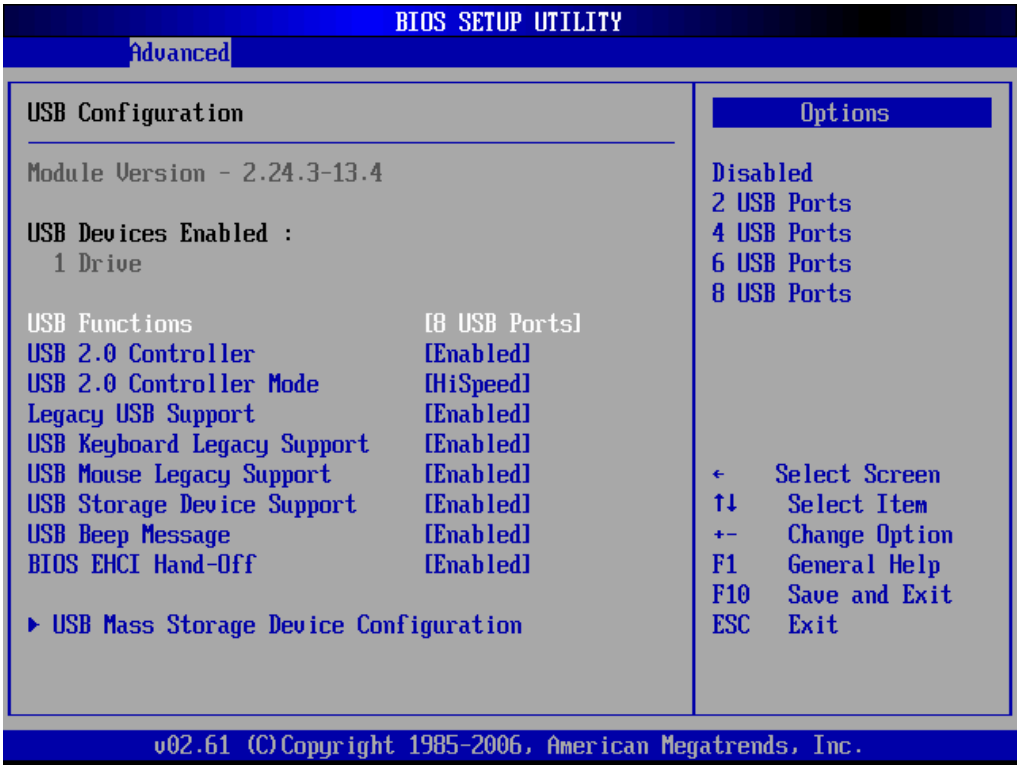
This option displays the current status of all of monitored hardware devices/components such as voltages and temperatures. The options are Enabled and Disabled.



8.3.6 USB Configuration

USB Configuration Settings

You can use this screen to specify options for the USB configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



USB Function

Set this value to allow the system to Disable, Enable, and select a set number of onboard USB ports.

USB 2.0 Controller

Depends on the setting of USB Function. If USB Function is set to Disabled, this option will have no effect. Enabled will open USB 2.0 functionality to all USB ports.

USB 2.0 Controller Mode

The USB 2.0 Controller Mode configures the data rate of the USB port. The options are FullSpeed (12 Mbps) and HiSpeed (480 Mbps).

Legacy USB Support

Legacy USB Support refers to USB mouse and keyboard support. Normally if this option is not enabled, any attached USB mouse or keyboard will not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or keyboard can control the system even when there are no USB drivers loaded on the system. Set this value to enable or disable the Legacy USB Support (see below).

Option	Description
Disabled	Set this value to prevent the use of any USB device in DOS or during system boot.
Enabled	Set this value to allow the use of USB devices during boot and while using DOS.
Auto	This option auto detects USB Keyboards or Mice and if found, allows them to be utilized during boot and while using DOS.

USB Beep Message

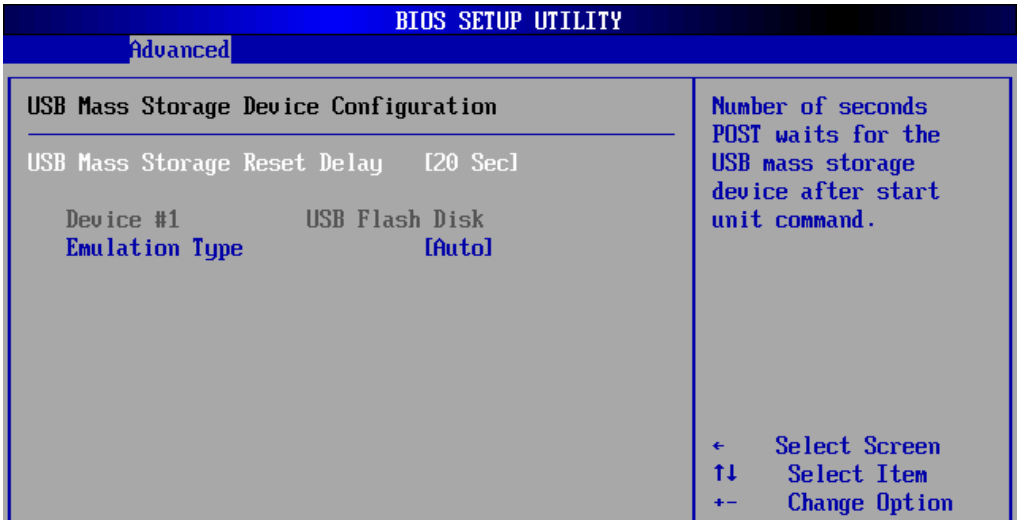
Allows you to Enable/Disable the beep during USB device enumeration.

BIOS EHCI hand-off

This option provides a work around for OSes without ECHI hand-off support. The EHCI ownership change should be claimed by the EHCI driver.

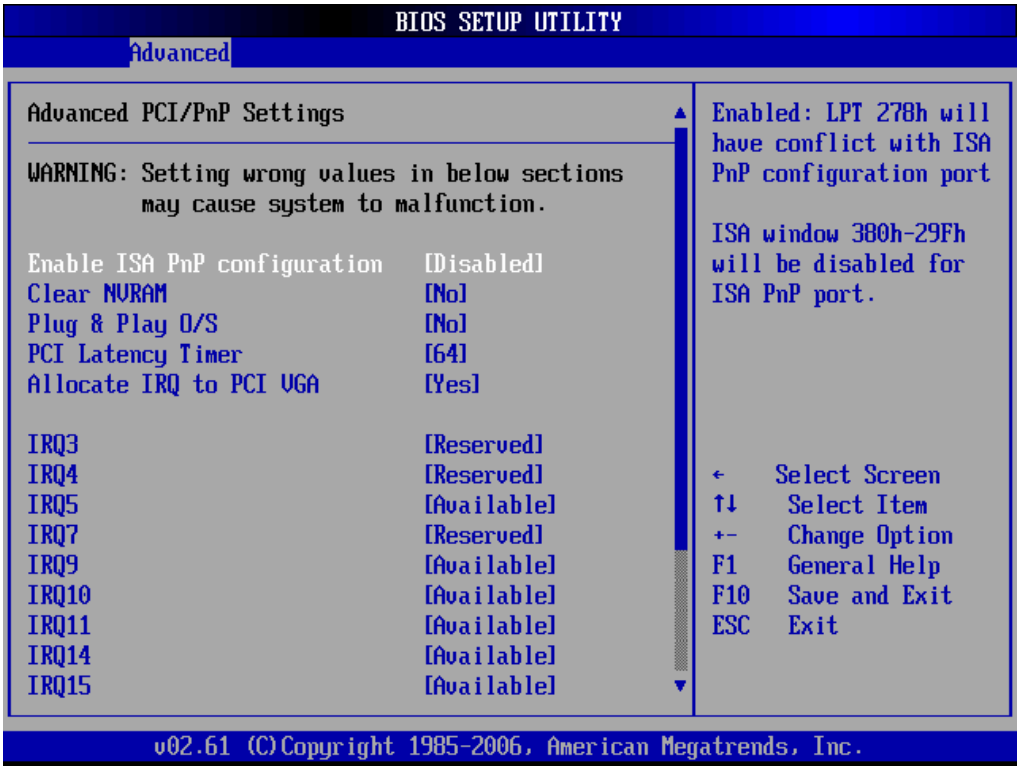
USB Mass Storage Device Configuration

This is a submenu for configuring the USB Mass Storage Class Devices when BIOS finds they are in use on the USB ports. Emulation Type can be set according to the type of attached USB mass storage device(s).). If set to Auto, USB devices less than 530MB will be emulated as Floppy and those greater than 530MB will remain as hard drive. The Forced FDD option can be used to force a hard disk type drive (such as a Zip drive) to boot as FDD.



8.3.7 PCIPnP Configuration

You can display a Plug and Play BIOS Setup option by highlighting it using the < Arrow > keys to select an item. The Plug and Play BIOS Setup screen is shown below.



Enable ISA PnP configuration

Some ISA PnP cards need BIOS to configure resources of the card. Due to the limited IO ranges that the PCI-to-ISA bridge can forward to ISA bus, the ISA PnP configuration I/O port is disabled by default. The board only opens some ISA I/O port windows for use. When there is an ISA PnP card that needs a resource to be configured, enable this item and BIOS will detect and configure the resource of the ISA PnP card automatically.

Clear NVRAM

This option clears ESCD (Extended System Configuration Data) information in NVRAM.

Plug & Play O/S

When set to "Yes" and a Plug and Play operating system is installed, the operating system configures the Plug and Play devices not required for boot.

PCI Latency Timer

Set this value to allow the PCI Latency Timer to be adjusted. This option sets the latency of all PCI devices on the PCI bus.

Allocate IRQ to PCI VGA

When set to "Yes", the BIOS will assign an IRQ for a PCI VGA card.

IRQ

Set this value to allow the IRQ settings to be modified.

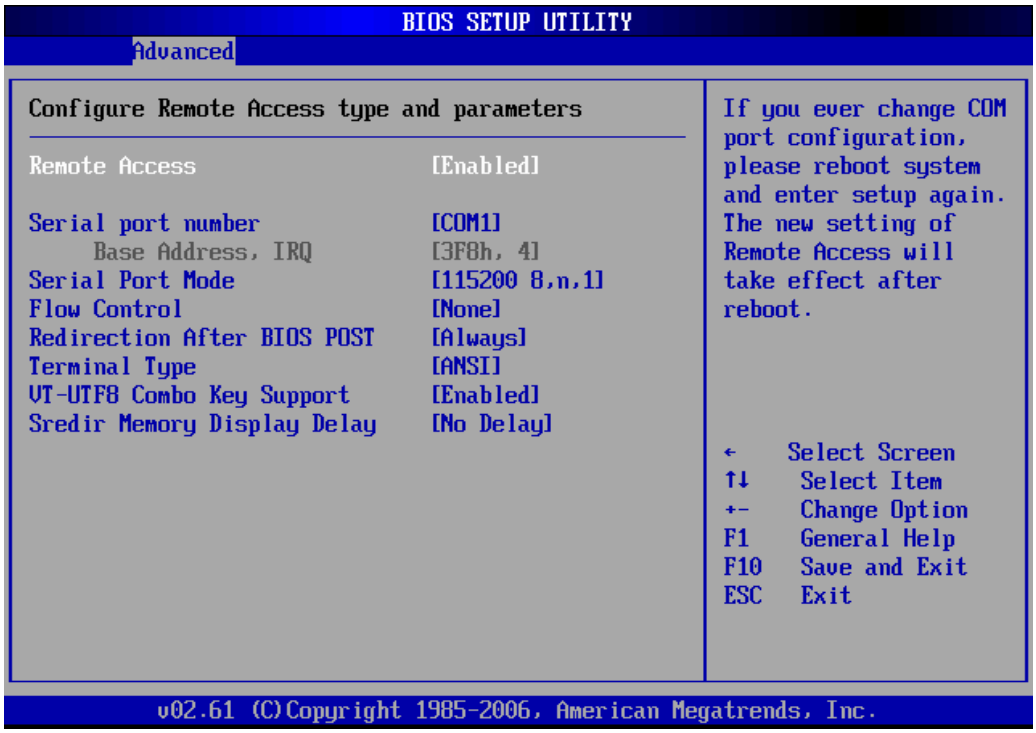
Available - This setting allows the specified IRQ to be used by a PCI/PnP device.

Reserved - This setting allows the specified IRQ to be used by a legacy ISA device.

8.3.8 Remote Access Configuration

Remote Access Configuration

Remote access configuration provides the settings to allow remote access by another computer to get POST messages and send commands through serial port access.



Remote Access

Select this option to Enable or Disable the BIOS remote access feature here.

NOTE: Enabled Remote Access requires a dedicated serial port connection. Once both serial ports are configured to disabled, you should set this value to Disabled or it may cause abnormal boot.

Serial Port Number

Select the serial port you want to use for the remote access interface. You can set the value for this option to either COM1 or COM2.

NOTE: If you have changed the resource assignment of the serial ports in Advanced>Onboard Device Configuration>SuperIO Configuration, you must Save Changes and Exit, reboot the system, and enter the setup menu again in order to see those changes reflected in the available Remote Access options.

Serial Port Mode

Select the baud rate you want the serial port to use for console redirection. The options are 115200 8,n,1; 57600 8,n,1; 19200 8,n,1; and 09600 8,n,1.

Flow Control

Set this option to select Flow Control for console redirection. The settings for this value are None, Hardware, or Software.

Redirection After BIOS POST

This option allows you to set Redirection configuration after BIOS POST. The settings for this value are Disabled, Boot Loader, or Always.

Option	Description
Disabled	Set this value to turn off the redirection after POST
Boot Loader	Set this value to allow the redirection to be active during POST and Boot Loader.
Always	Set this value to allow the redirection to be always active.

Terminal Type

This option is used to select either VT100/VT-UTF8 or ANSI terminal type. The settings for this value are ANSI, VT100, or VT-UTF8.

VT-UTF8 Combo Key Support

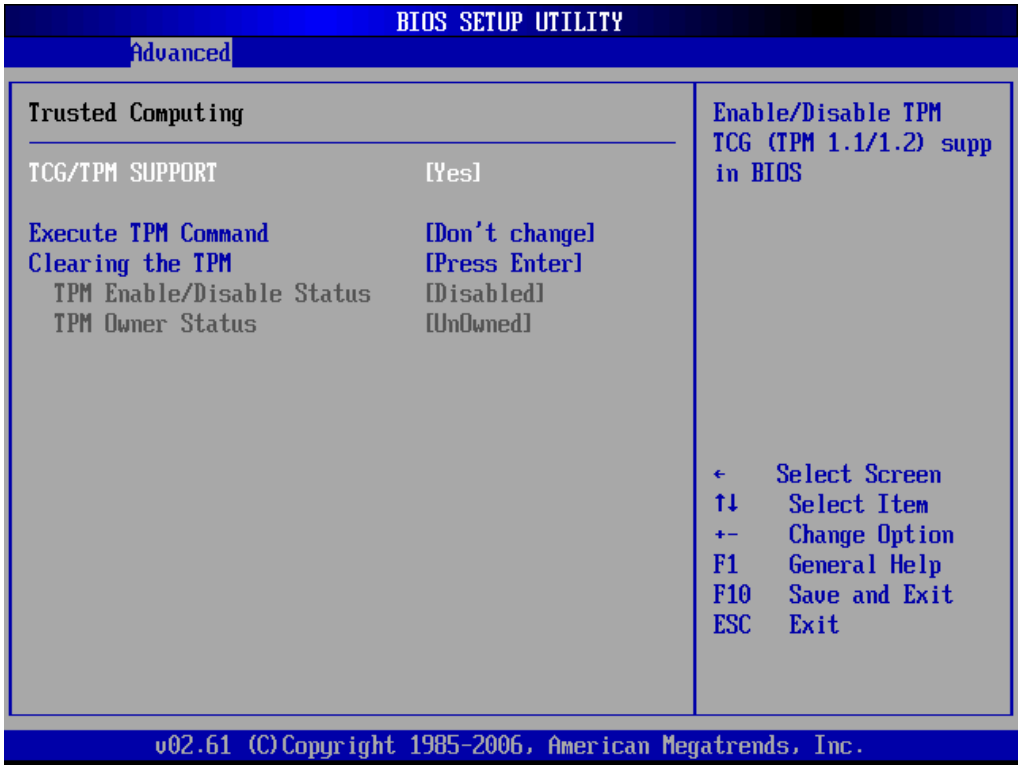
This option enables VT-UTF8 Combination Key Support for ANSI/VT100 terminals. The settings for this value are Enabled or Disabled.

Sredir Memory Display Delay

This option gives the delay in seconds to display memory information. The options for this value are No Delay, Delay 1 Sec, Delay 2 Sec, or Delay 4 Sec.

8.3.9 Trusted Computing

Trusted computing is an industry standard to make personal computers more secure through a dedicated hardware chip, called a Trusted Platform Module (TPM). This option allows you to enable or disable the TPM support.

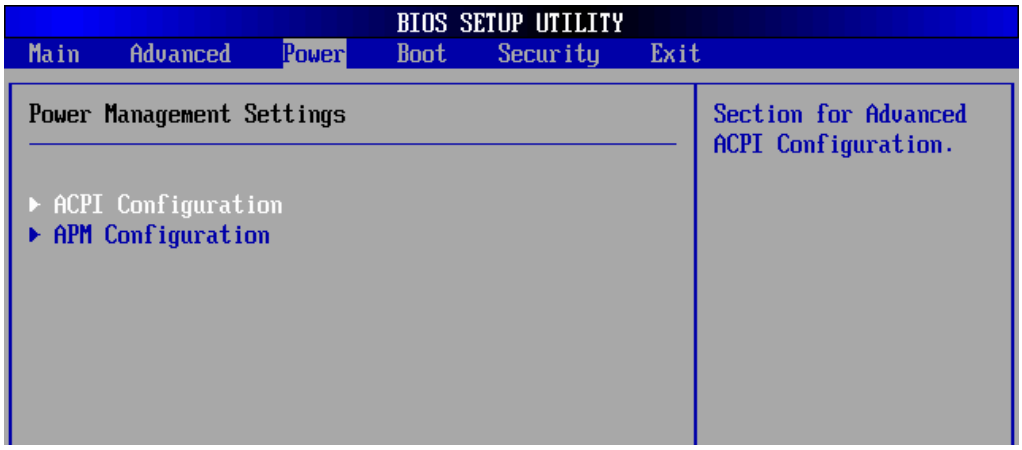


Execute TPM Command

This field is used to Enable(activate)/Disable(deactivate) the Execute TPM Command function.

8.4 Power Management

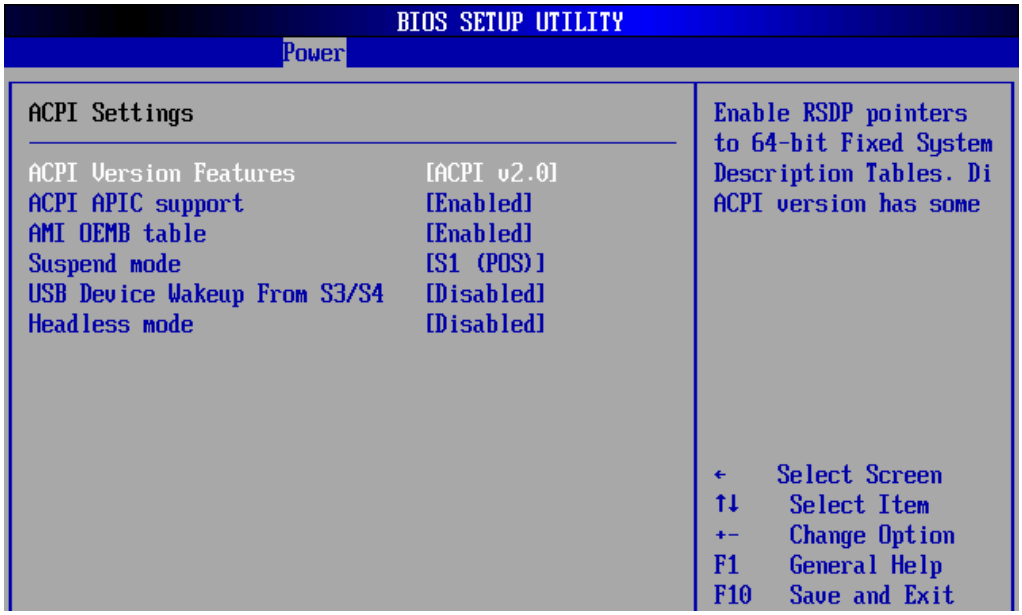
Select the Power tab from the setup screen to enter the power management BIOS Setup screen. You can select any of the items in the left frame of the screen, such as ACPI Configuration, to go to the sub menu for that item. The power management BIOS Setup screen is shown below.



8.4.1 ACPI Configuration

Advanced ACPI Configuration

You can use this screen to select options for the ACPI Advanced Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on this page. The screen is shown below.



ACPI Version Features

The item allows you to select the ACPI version.

ACPI APIC Support

Used to enable or disable the Advanced Programmable Interrupt Controller (APIC) for PC2001 compliance. Enabling APIC mode will expand available IRQs resources for the system

AMI OEMB Table

Include OEMB table pointer to R(X)SDT pointer lists.

Suspend mode

This setting selects either S1 (POS) or S3 (STR) system suspend mode. The Optimal and Fail-Safe Default setting is S3 (STR).

Option	Description
S1 (POS)	Power On Suspend - Under this setting the CPU is not executing instructions, all power resources that supply system level reference of S0 are off, system memory context is maintained, devices that reference power resources that are on are on, and devices that can wake-up the system can cause the cpu to continue to execute from where it left off.
S3 (STR)	Suspend to RAM - Under this setting the system enters a low power state instead of being completely shut off. This allows the computer system to boot up in a few seconds.

USB Device Wakeup from S3/S4

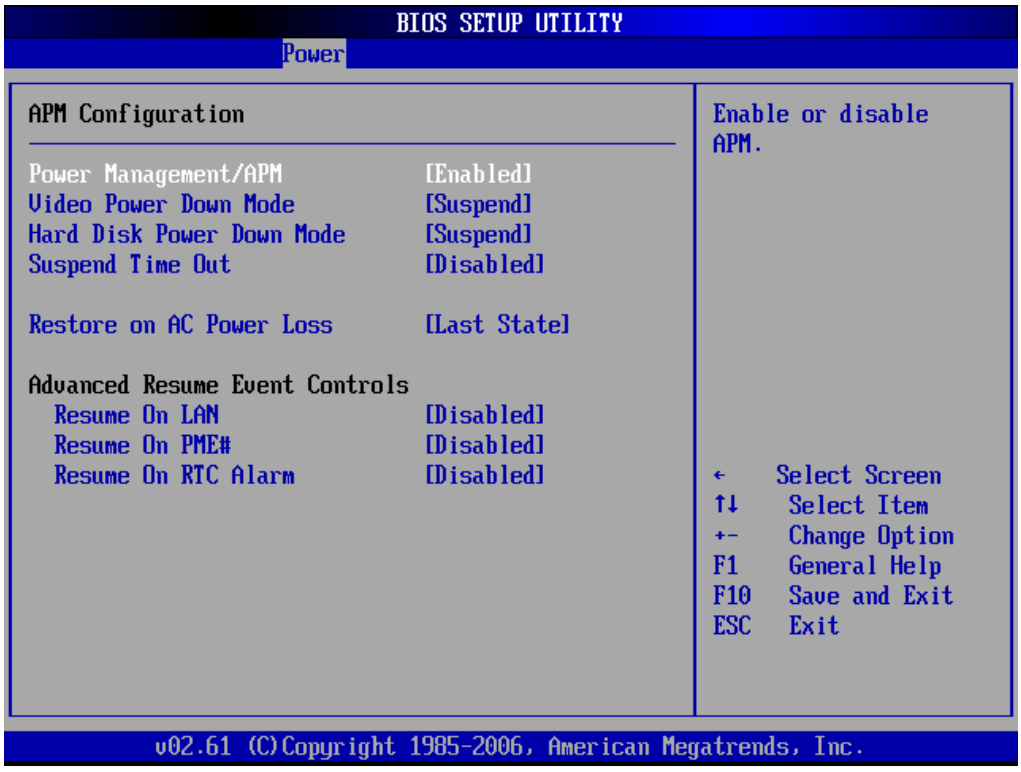
This option allows a USB device to wake up the system from S3/S4.

Headless mode

This is a server-specific feature. A headless server is one that operates without a keyboard, monitor or mouse. To run in headless mode, both BIOS and operating system (e.g. Windows Server 2003) must support headless operation

8.4.2 APM Configuration

Select the Advanced tab from the setup screen to enter the APM Configuration Setup screen. You can display a Power Management/APM Setup option by highlighting it using the < Arrow > keys.



Power Management/APM

Set this value to *Enable* or *Disable* Power Management/APM (Advanced Power Management) features.

Video Power Down Mode

This option specifies the Power State that the video subsystem enters when the BIOS places it in a power saving state after the specified period of display inactivity has expired. The options are *Disabled* and *Suspend*.

Hard Disk Drive Power Down Mode

This option specifies the power conserving state that the hard disk drive enters after the specified period of hard drive inactivity has expired.

Suspend Time Out

This option specifies the length of time the system waits before it enters suspend mode. The options are Disabled, 1 Min, 2 Min, 4 Min, 8 Min, 10 Min, 20 Min, 30 Min, 40 Min, 50 Min, and 60 Min.

Restore on AC Power Loss

Determines what state the computer enters when AC power is restored after a power loss. The options for this value are Last State, Power On and Power Off.

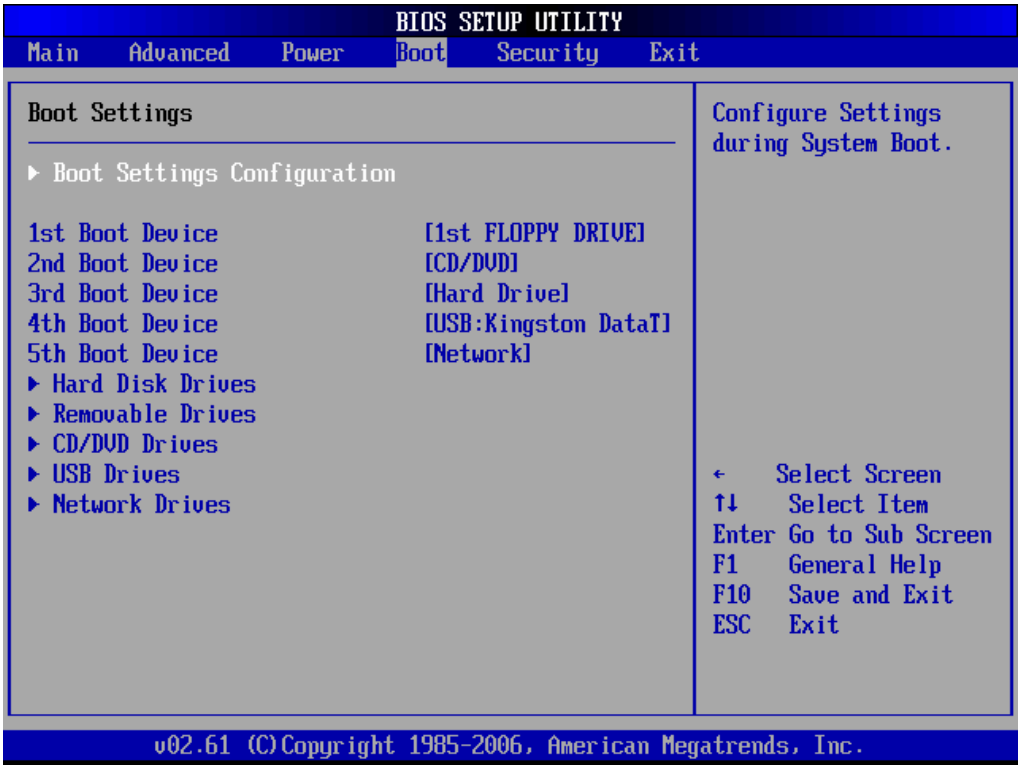
Option	Description
Power Off	Set this value to always power off the system while AC power is restored.
Power On	Set this value to always power on the system while AC power is restored.
Last State	Set this value to power off/on the system depending on the last system power state while AC power is restored.

Advanced Resume Event Controls

These settings specify which events will generate a system wake event. The available events are On LAN, PME# and RTC Alarm. The options are *Enabled* and *Disabled*.

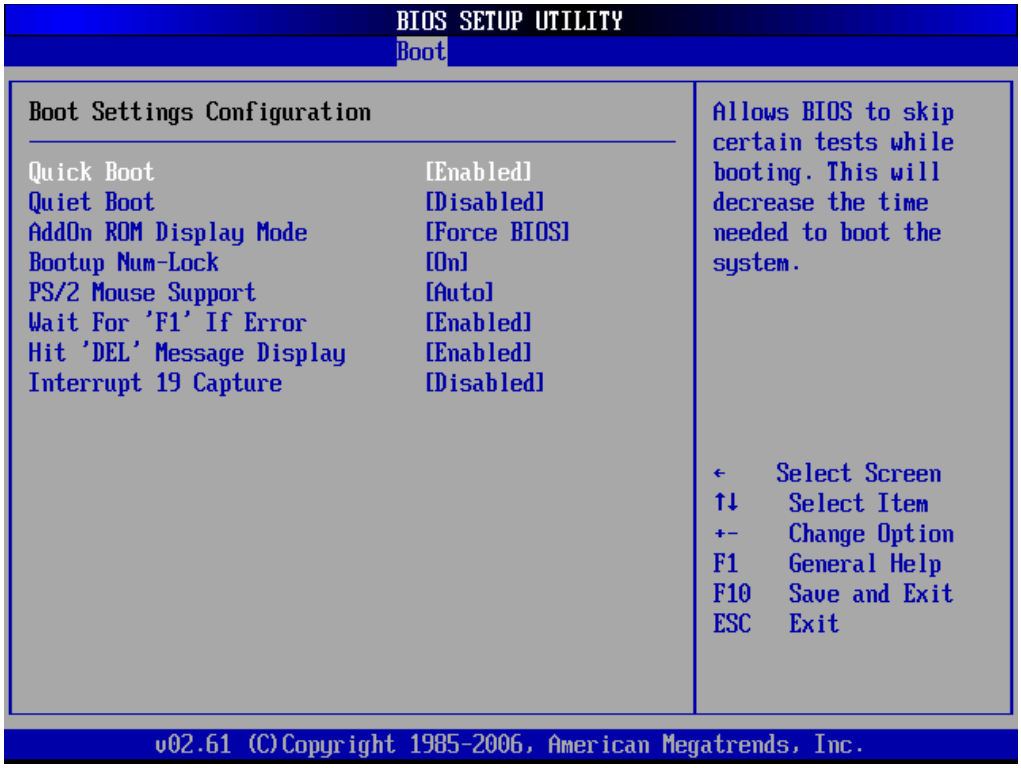
8.5 Boot Setup

Select the Boot tab from the setup screen to enter the Boot BIOS Setup screen. You can select any of the items in the left frame of the screen, such as Boot Device Priority, to go to the sub menu for that item. You can display an Boot BIOS Setup option by highlighting it using the < Arrow > keys. The Boot Settings screen is shown below:



Boot Settings Configuration

Use this screen to select options for the Boot Settings Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



Quick Boot

Disabled - Set this value to allow the BIOS to perform all POST tests.
Enabled - Set this value to allow the BIOS to skip certain POST tests to boot faster.

Quiet Boot

Disabled - Set this value to allow the computer system to display the POST messages.
Enabled - Set this value to allow the computer system to display the OEM logo.

AddOn ROM Display Mode

This BIOS feature controls the display of ROM messages from the BIOS of add-on devices like the graphics card or the SATA controller during the boot sequence. When set to Force BIOS, AddOn ROM messages will be forced to display during the boot sequence. When set to Keep Current, AddOn ROM messages will only be displayed if the third-party manufacturer had set the add-on device to do so.

An AddOn ROM typically consists of firmware that is called by the system BIOS. For example, an adapter card that controls a boot device might contain firmware that is used to connect the device to the system once the AddOn ROM is loaded.

Bootup Num-Lock

Set this value to allow the Number Lock setting to be modified during boot up. Off – This option does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard will light up when the Number Lock is engaged. On – Set this value to allow the Number Lock on the keyboard to be enabled automatically when the computer system is boot up. This allows the immediate use of 10-keys numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard will be lit.

PS/2 Mouse Support

Allows you to enable/disable PS/2 mouse support.

Wait for 'F1' If Error

If this option is set to Disabled, AMIBIOS does not wait for you to press the <F1> key after an error message.

Hit 'DEL' Message Display

When set to Enabled, the system displays the message "Press DEL to run Setup during POST".

Interrupt 19 Capture

Interrupt 19 is the software interrupt that handles the boot disk function. When enabled, this BIOS feature allows the AddOn ROM of these host adapotors to "capture" Interrupt 19 during the boot process so that drives attached to these adaptors can function as bootable disks. In addition, it allows you to gain access to the host adaptor's AddOn ROM setup utility, fi one is available.

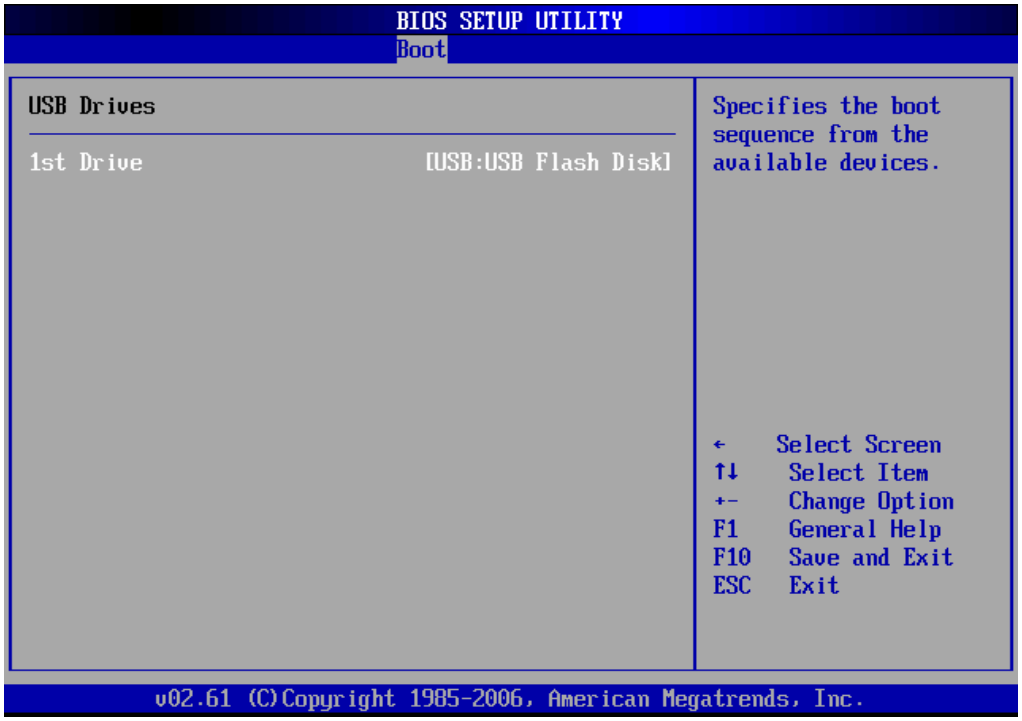
When disabled, the AddOn ROM of these host adaptors will not be able to "capture" interrupt 19. Thereforce, you will not be able to boot operating systems form any bootable disks attached to these host adaptors. Nor will you be able to gain access to their AddOn ROM utilities.

Boot Device Priority

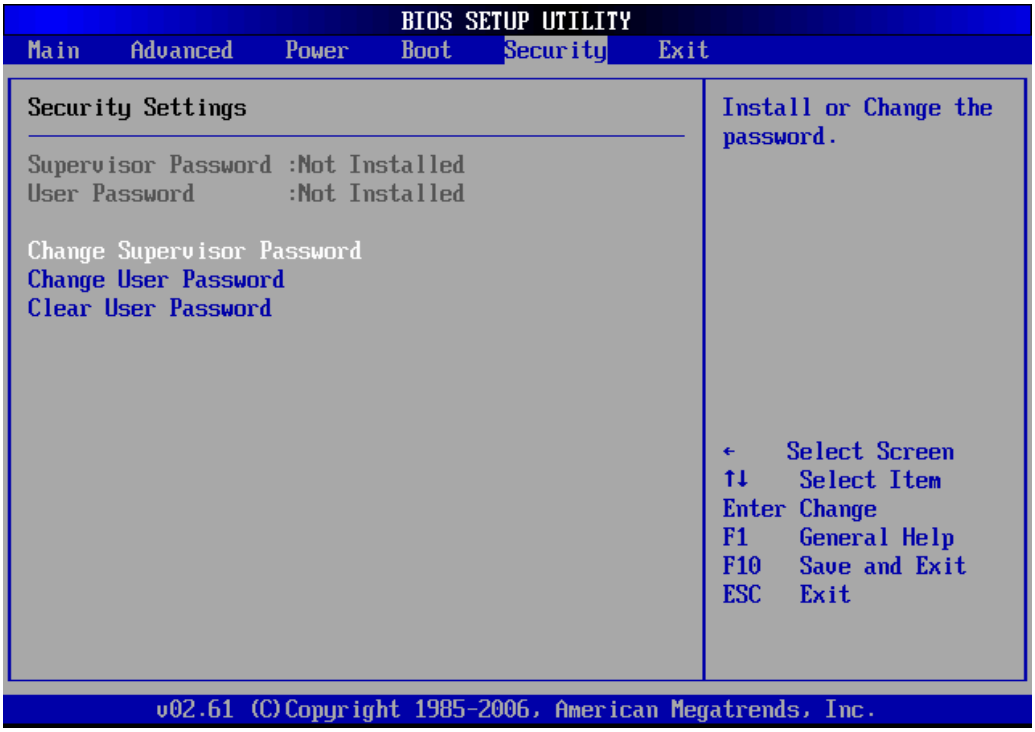
Set the boot device options to determine the sequence in which the computer checks which device to boot from.

Boot Device Groups

The Boot devices are listed in groups by device type. First press <Enter> to enter the sub-menu. Then you may use the arrow keys to select the desired device, then press <+>, <-> or <PageUp>, <PageDown> key to move it up/down in the priority list. For example, USB storage disks will be listed as “USB Drives” in the sub-menu as below. Only the first device in each device group will be available for selection in the Boot Device Priority option.



8.6 Security Setup



8.6.1 Password Support

Two Levels of Password Protection

Provides both a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first.

The system can be configured so that all users must enter a password every time the system boots or when Setup is executed, using either or either the Supervisor password or User password.

The Supervisor and User passwords activate two different levels of password security. If you select password support, you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed. Make sure you write it down. If you forget it, you must drain NVRAM and re-configure.

Remember the Password

Keep a record of the new password when the password is changed. If you forget the password, you must erase the system configuration information in NVRAM.

Select Security Setup from the Setup main BIOS setup menu. Security Setup options, such as password protection and virus protection, are described in this section. To access the sub menu for the following items, select the item and press < `Enter` >:

- Change Supervisor Password
- Change User Password
- Clear User Password

Supervisor Password

Indicates whether a supervisor password has been set.

User Password

Indicates whether a user password has been set.

Change Supervisor Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to change the supervisor password.

Change User Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to change the user password.

Clear User Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to clear the user password.

8.6.2 Change Supervisor Password

Select Change Supervisor Password from the Security Setup menu and press < Enter >.

```
Enter New Password:
```

Type the password and press < Enter >. The screen does not display the characters entered. Retype the password as prompted and press < Enter >. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after setup completes.

8.6.3 Change User Password

Select Change User Password from the Security Setup menu and press < Enter >.

```
Enter New Password:
```

Type the password and press < Enter >. The screen does not display the characters entered. Retype the password as prompted and press < Enter >. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after setup completes.

8.6.4 Clear User Password

Select Clear User Password from the Security Setup menu and press < Enter >.

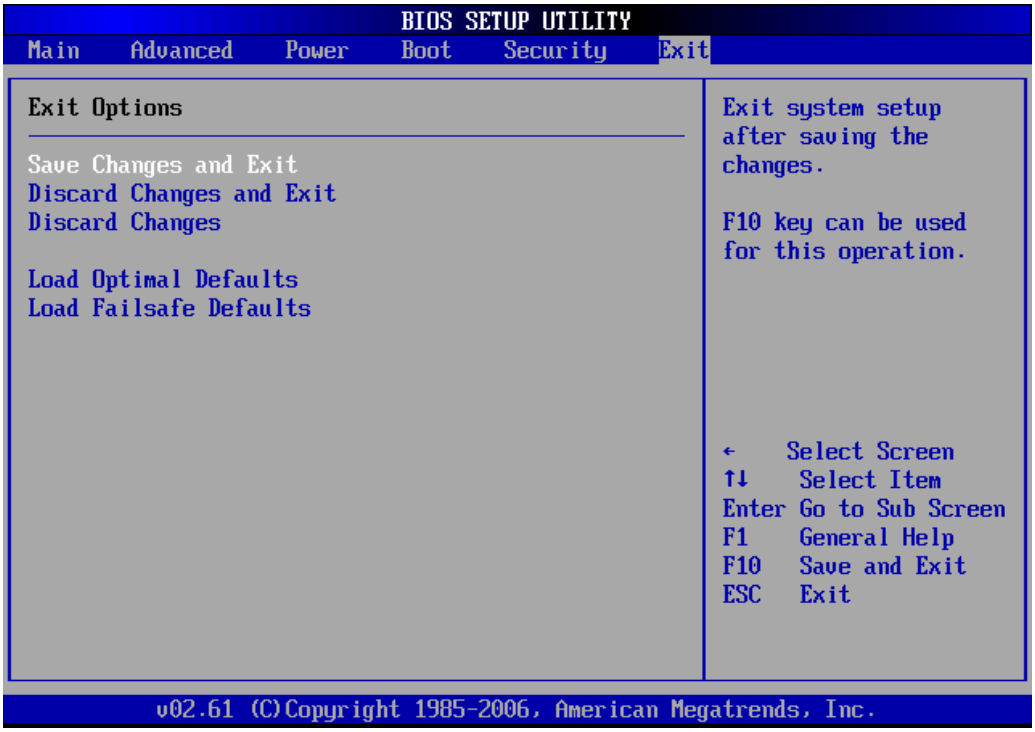
```
Clear New Password

[Ok]  [Cancel]
```

Type the password and press < Enter >. The screen does not display the characters entered. Retype the password as prompted and press < Enter >. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after setup completes.

8.7 Exit Menu

Select the *Exit* tab from the setup screen to enter the Exit BIOS Setup screen. You can display an Exit BIOS Setup option by highlighting it using the < Arrow > keys. The Exit BIOS Setup screen is shown below.



Save Changes and Exit

When you have completed the system configuration changes, select this option to leave Setup and reboot the computer so the new system configuration parameters can take effect. Select Exit Saving Changes from the Exit menu and press < Enter >.

```
Save Configuration Changes and Exit Now?

[Ok]  [Cancel]
```

appears in the window. Select Ok to save changes and exit.

Discard Changes and Exit

Select this option to quit Setup without making any permanent changes to the system configuration. Select Exit Discarding Changes from the Exit menu and press <Enter>.

```
Discard Changes and Exit Setup Now?

[Ok]  [Cancel]
```

appears in the window. Select *Ok* to discard changes and exit.

Discard Changes

Select Discard Changes from the Exit menu and press < Enter >.

Select *Ok* to discard changes.

Load Optimal Defaults

Automatically sets all Setup options to a complete set of default settings when you Select this option. The Optimal settings are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Optimal Setup options if your computer is experiencing system configuration problems.

Select Load Optimal Defaults from the Exit menu and press < Enter >.

Select *Ok* to load optimal defaults.

Load Failsafe Defaults

Automatically sets all Setup options to a complete set of default settings when you Select this option. The Failsafe settings are designed for maximum system stability, but not maximum performance. Select the Fail-Safe Setup options if your computer is experiencing system configuration problems.

Select Load Fail-Safe Defaults from the Exit menu and press < Enter >.

```
Load Fail-Safe Defaults?

[Ok]  [Cancel]
```

appears in the window. Select Ok to load Fail-Safe defaults.

9 BIOS Checkpoints, Beep Codes

This section of this document lists checkpoints and beep codes generated by AMIBIOS. The checkpoints defined in this document are inherent to the AMIBIOS generic core, and do not include any chipset or board specific checkpoint definitions.

Checkpoints and Beep Codes Definition

A checkpoint is either a byte or word value output to I/O port 80h. The BIOS outputs checkpoints throughout bootblock and Power-On Self Test (POST) to indicate the task the system is currently executing. Checkpoints are very useful for debugging problems that occur during the preboot process.

Beep codes are used by the BIOS to indicate a serious or fatal error. They are used when an error occurs before the system video has been initialized, and generated by the system board speaker.

Viewing BIOS Checkpoints

Viewing all checkpoints generated by the BIOS requires a checkpoint card, also referred to as a "POST Card" or "POST Diagnostic Card". These are ISA or PCI add-in cards that show the value of I/O port 80h on a LED display.

Some computers display checkpoints in the bottom right corner of the screen during POST. This display method is limited, since it only displays checkpoints that occur after the video card has been activated.

Keep in mind that not all computers using AMIBIOS enable this feature. In most cases, a checkpoint card is the best tool for viewing AMIBIOS checkpoints.

9.1 Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS:

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs from add-in PCI devices.

Checkpoint	Description
Before D0	If boot block debugger is enabled, CPU cache-as-RAM functionality is enabled at this point. Stack will be enabled from this point.
D0	Early Boot Strap Processor (BSP) initialization like microcode update, frequency and other CPU critical initialization. Early chipset initialization is done.
D1	Early super I/O initialization is done including RTC and keyboard controller. Serial port is enabled at this point if needed for debugging. NMI is disabled. Perform keyboard controller BAT test. Save power-on CPUID value in scratch CMOS. Go to flat mode with 4GB limit and GA20 enabled.
D2	Verify the boot block checksum. System will hang here if checksum is bad.
D3	Disable CACHE before memory detection. Execute full memory sizing module. If memory sizing module not executed, start memory refresh and do memory sizing in Boot block code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM. Copies compressed boot block code to memory in right segments. Copies BIOS from ROM to RAM for faster access. Performs main BIOS checksum and updates recovery status accordingly.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. If BIOS recovery is necessary, control flows to checkpoint E0. See Bootblock Recovery Code Checkpoints section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See POST Code Checkpoints section of document for more information.
DC	System is waking from ACPI S3 state
E1-E8, EC-EE	OEM memory detection/configuration error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.

9.2 Bootblock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS:

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs From add-in PCI devices.

Checkpoint	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.
FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

9.3 POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS preboot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs From add-in PCI devices.

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer.Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
07	Fixes CPU POST interface calling pointer.
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache – Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor
C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
20	Relocate System Management Interrupt vector for all CPU in the system.
24	Uncompress and initialize any platform specific BIOS modules. GPNV is initialized at this checkpoint.
2A	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.

POST Code Checkpoints cont'd:

Checkpoint	Description
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information. USB controllers are initialized at this point.
39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, ... etc.) successfully installed in the system and update the BDA, EBDA...etc.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory. Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed / requested. Check boot password if installed.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disable NMI as selected
90	Initialization of system management interrupt by invoking all handlers. *Please note this checkpoint comes right after checkpoint 20h*
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module. Display boot option popup menu.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector.
AB	Prepare BBS for Int 19 boot. Init MP tables.
AC	End of POST initialization of chipset registers. De-initializes the ADM module.
B1	Save system context for ACPI. Prepare CPU for OS boot including final MTRR values.
00	Passes control to OS Loader (typically INT19h).

9.4 OEM POST Error Checkpoints

Checkpoints from the range 61h to 70h are reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.

9.5 DIM Code Checkpoints

The Device Initialization Manager (DIM) gets control at various times during BIOS POST to initialize different system busses. The following table describes the main checkpoints where the DIM module is accessed:

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs from add-in PCI devices.

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI- PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.

While control is in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two fields. The details of the high byte of these checkpoints are as follows:

HIGH BYTE XY

The upper nibble 'X' indicates the function number that is being executed. 'X' can be from 0 to 7.

0 = func#0, disable all devices on the BUS concerned.
1 = func#1, static devices initialization on the BUS concerned.
2 = func#2, output device initialization on the BUS concerned.
3 = func#3, input device initialization on the BUS concerned.
4 = func#4, IPL device initialization on the BUS concerned.
5 = func#5, general device initialization on the BUS concerned.
6 = func#6, error reporting for the BUS concerned.
7 = func#7, add-on ROM initialization for all BUSes.
8 = func#8, BBS ROM initialization for all BUSes.

The lower nibble 'Y' indicates the BUS on which the different routines are being executed. 'Y' can be from 0 to 5.

0 = Generic DIM (Device Initialization Manager).
1 = Onboard System devices.
2 = ISA devices.
3 = EISA devices.
4 = ISA PnP devices.
5 = PCI devices.

9.6 ACPI Runtime Checkpoints

ACPI checkpoints are displayed when an ACPI capable operating system either enters or leaves a sleep state. The following table describes the type of checkpoints that may occur during ACPI sleep or wake events:

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs from add-in PCI devices.

9.7 Boot Block Beep Codes

No. of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
3	Base Memory error
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

9.8 POST BIOS Beep Codes

No. of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
3	Base memory read/write test error
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

9.9 Troubleshooting POST BIOS Beep Codes

No. of Beeps	Description
1, 2 or 3	Reseat the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. - If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. - If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning card.
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

Appendix A: **Connectors and Mounting**

A.1 **Carrier Board ETX Connecter Heights** (Hirose FX8/FX8C Receptacles)

For different stacking heights, the receptacles for ETX carrier boards are available in two heights, 3 mm and 9.5 mm. When 3 mm receptacles are chosen, the carrier board should be free of components.

FX8-100S-SV

100-pin board-to-board connector for
3 mm board stacking

This connector can be used with :
- 3 mm through-hole standoffs (SMT type)
- 3 mm threaded standoffs (DIP type)

FX8C-100S-SV5

100-pin board-to-board connector for
9.5 mm board stacking

This connector can be used with :
- 9.5 mm through-hole standoffs (SMT type)
- 9.5 mm threaded standoffs (DIP type)

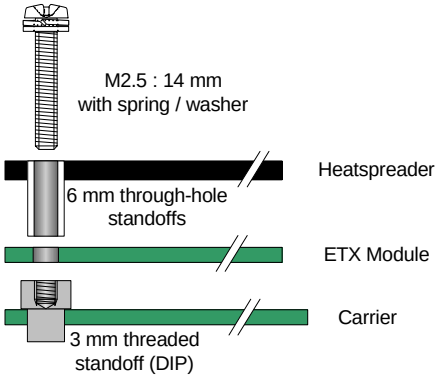
FX8C/FX8 Common Spec

- Current capacity 0.4 A per pin
- Rated voltage 100 V AC
- Insulation resistance 100 M or greater @ 250 V DC
- Withstand voltage 300 V AC r.m.s.
- Contact resistance 45 m or less @ 100 mA DC
- Insulation PPS resin (Light brown, UL94V-0)
- Contacts phosphor bronze (gold plated contacts and leads)

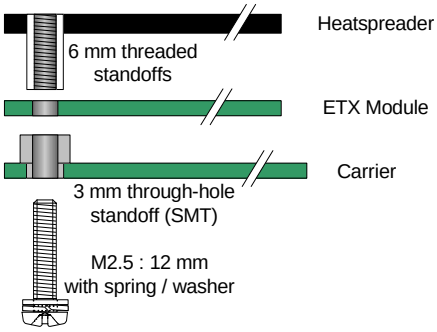
A.3 Mounting Procedures

There are several standard ways to mount an ETX board with heatspreader on a carrier board. ETX boards may be mounted with 9.5 mm ETX connectors on the carrier board or standard 3 mm connectors. There are also two different types of heatspreaders to choose from: heatspreaders with threaded standoffs which require inserting screws from under the carrier, or top mounting heatspreaders using through-hole heatspreader standoffs and threaded carrier board standoffs.

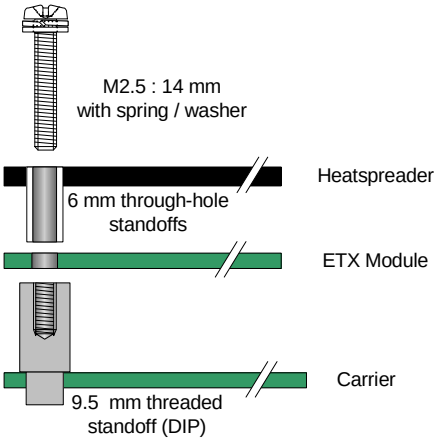
Top Mounting
3 mm Hirose FX8-100S-SV
Carrier Board Connectors



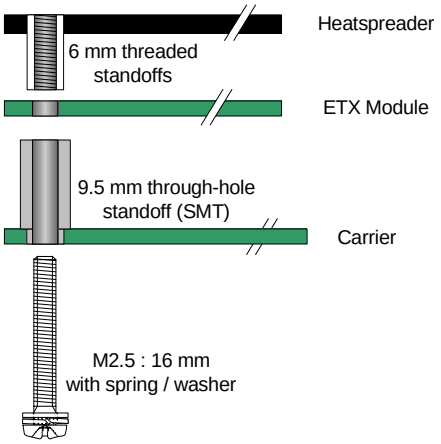
Bottom Mounting
3 mm Hirose FX8-100S-SV
Carrier Board Connectors



Top Mounting
9.5 mm Hirose FX8C-100S-SV5
Carrier Board Connectors



Bottom Mounting
9.5 mm Hirose FX8C-100S-SV5
Carrier Board Connectors



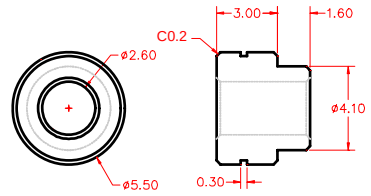
A.4 Standoff Types - Carrier Board

For different mounting procedures there are different standoffs available for the carrier board. Note that threaded standoffs are both DIP and SMT type and the through-hole types are all SMT type. Other types not listed can be made available upon request.

33-72000-0030

3 mm through-hole standoff (SMT type)

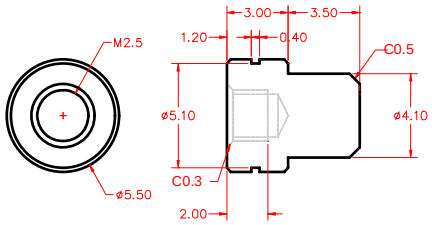
for HTS-EAT-B with 3 mm Hirose carrier board connectors



33-72011-0030

3 mm threaded standoff (DIP type)

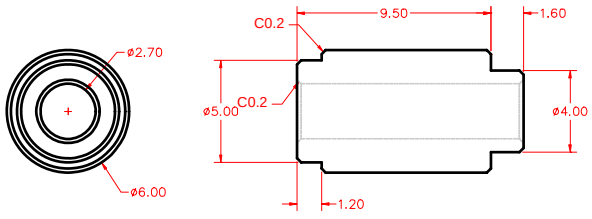
for HTS-EAT-BT with 3 mm Hirose carrier board connectors



33-72007-9P50

9.5 mm through-hole standoff (SMT type)

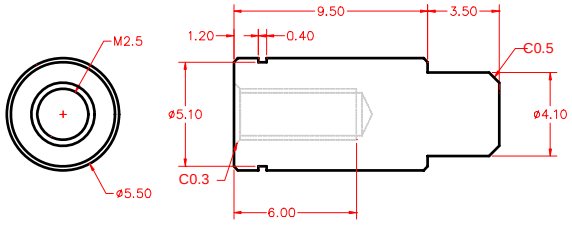
for HTS-EAT-B with 9.5 mm Hirose carrier board connectors



33-72011-9P50

9.5 mm threaded standoff (DIP type)

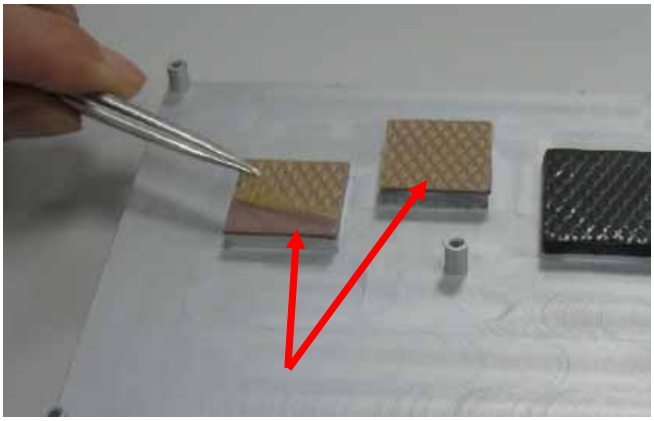
for HTS-EAT-BT with 9.5 mm Hirose carrier board connectors

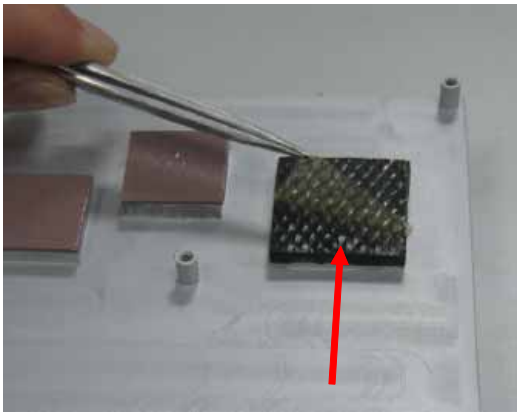


Appendix B: **Heatspreaders and Heatsinks**

B.1 **Heatspreader Introduction**

The function of the heatspreader is to ensure an identical mechanical profile for every ETX module. In this way the thermal solution, that is built on top of the heatspreader is compatible with any ETX module, not just the ETX-AT.

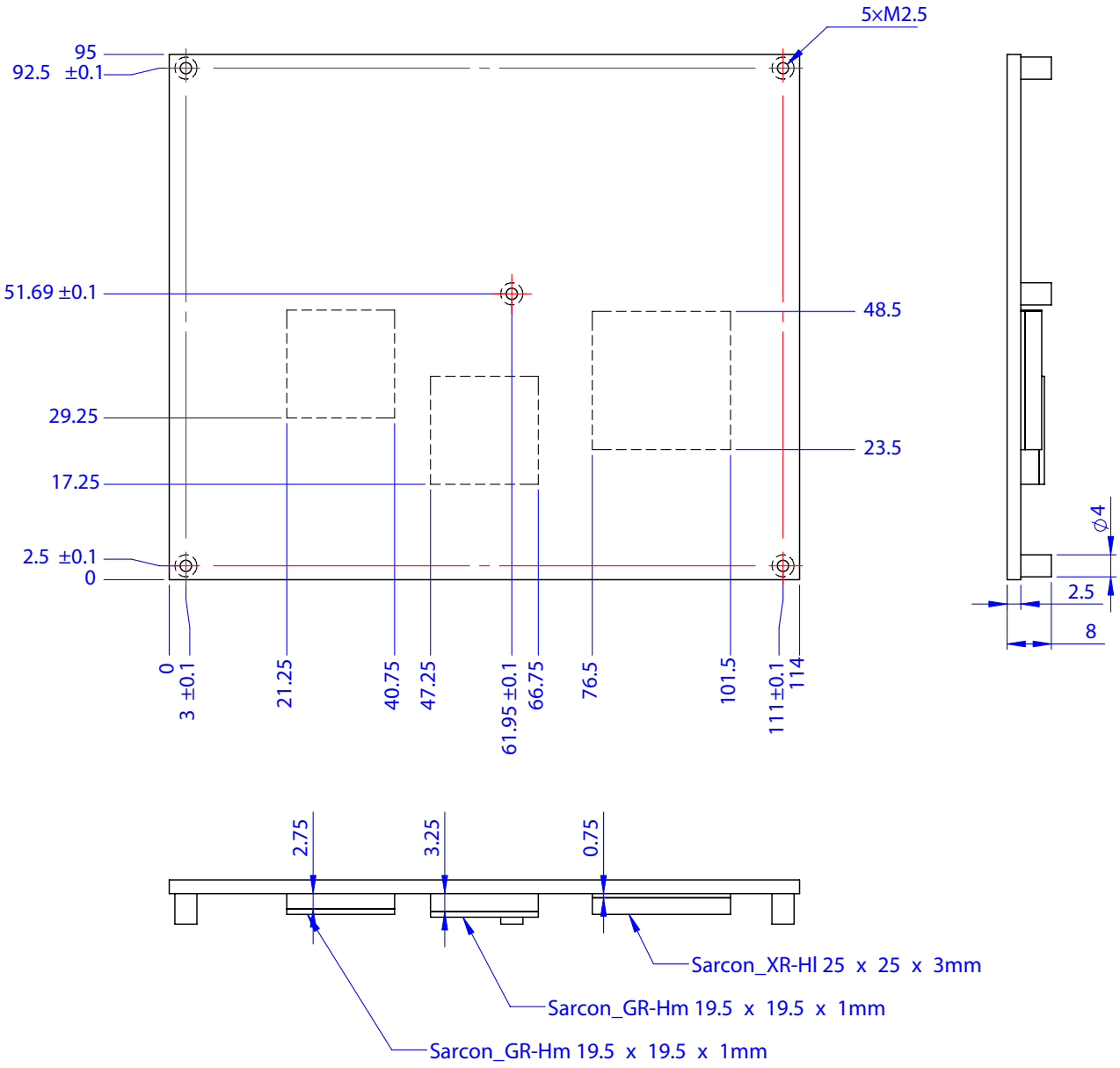




Remove the protective layer from CPU, Northbridge, and Southbridge pads before placing the heatspreader on the module.

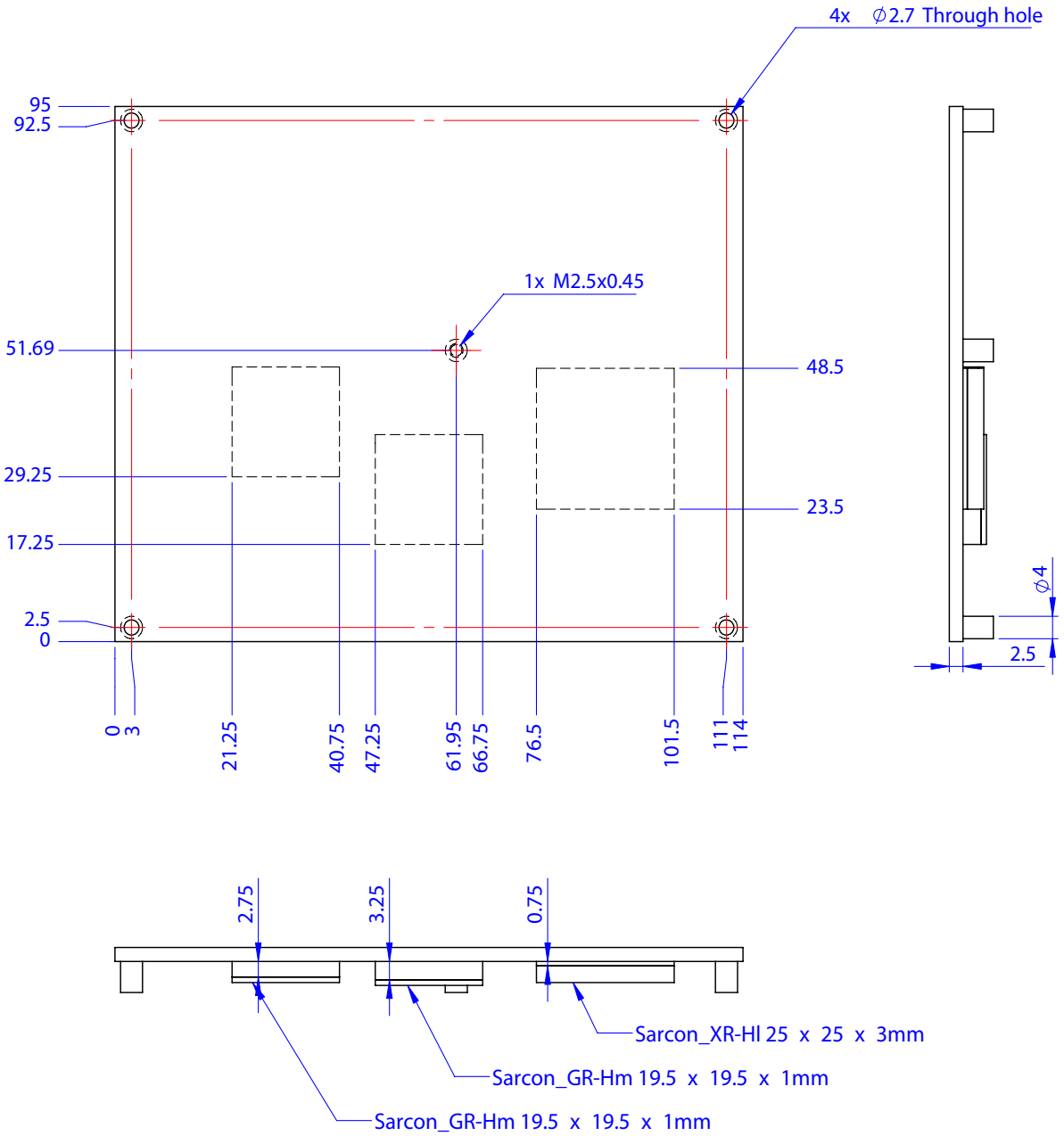
Heatspreader mounted on ETX-AT

B.2 **Heatspreader Dimensions for HTS-EAT-B** (threaded type)



- The heatspreader comes with four M2.5 x L12mm screws with washer/spring for use with 3 mm standoffs on the carrier board, and M2.5 x L16mm screws with washer/spring for use with 9.5 mm standoffs on the carrier board. (If the heatspreader is purchased separately, one M2.5 x L6mm screw is also included.)

B.3 **Heatspreader Dimensions for HTS-EAT-BT** (through-hole type)

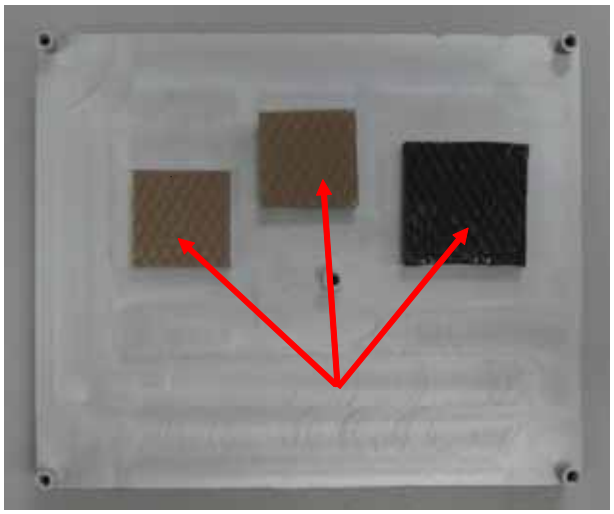


- The heatspreader comes with four M2.5 x L14mm screws with washer/spring. (If the heatspreader is purchased separately, one M2.5 x L6mm screw is also included.)

B.4 **Heatsinks:** THS-EAT-B and THSH-EAT-BL (threaded type)

The THS-EAT-B Heatsink is a low profile heatsink that is optimized for reduced height applications. The THSH-EAT-BL Heatsink is a high profile heatsink for applications without reduced height restrictions. Although the heatsinks are fanless, they still require some airflow to efficiently cool applications. The heatsinks are available in two cooling fin orientations ("vertical" shown for the THS-EAT-B and "horizontal" shown for the THSH-EAT-BL) and are bottom mounting (threaded type).

ETX-AT with THS-EAT-B heatsink ("vertically" oriented fins)



Pads for CPU, Northbridge, and Southbridge

NOTE:

Remove the protective layer from CPU, Northbridge, and Southbridge pads before placing the heatsink on the module (see Appendix B.1).

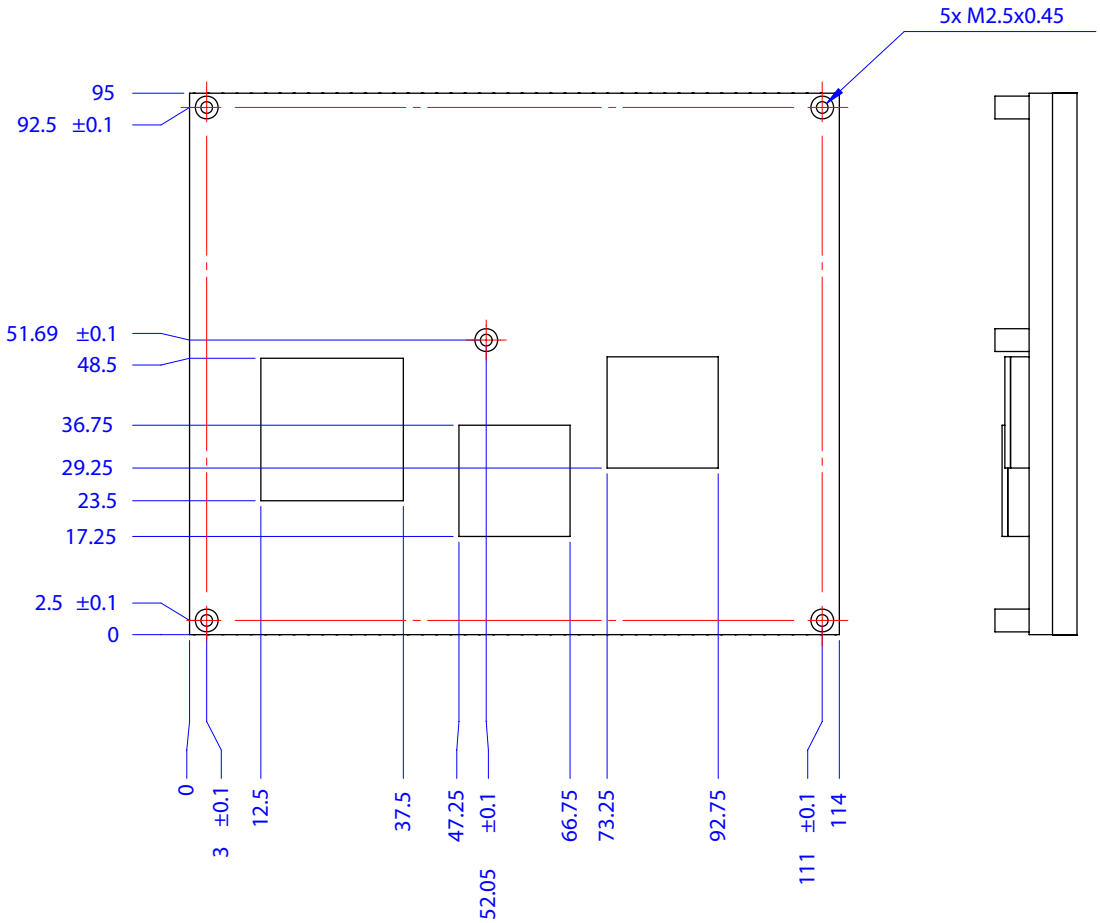
THS-EAT-B Low Profile Heatsink mounted on ETX-AT

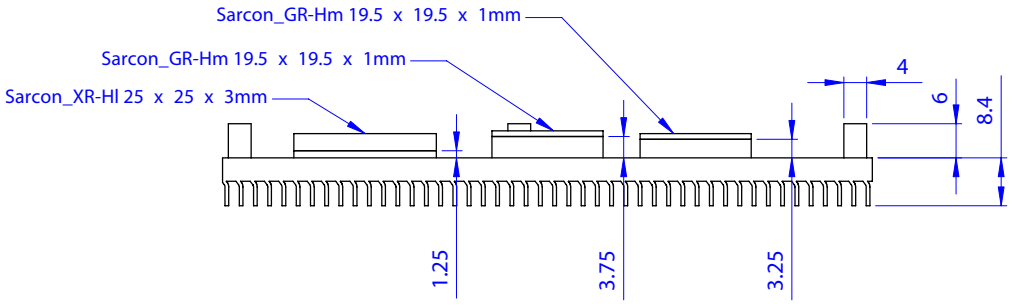
THSH-EAT-BL High Profile Heatsink (“horizontally” oriented fins)

B.5 Dimensions for THS-EAT-B Heatsink

THS-EAT-B

Low profile heatsink with “vertically” oriented fins for bottom mounting.



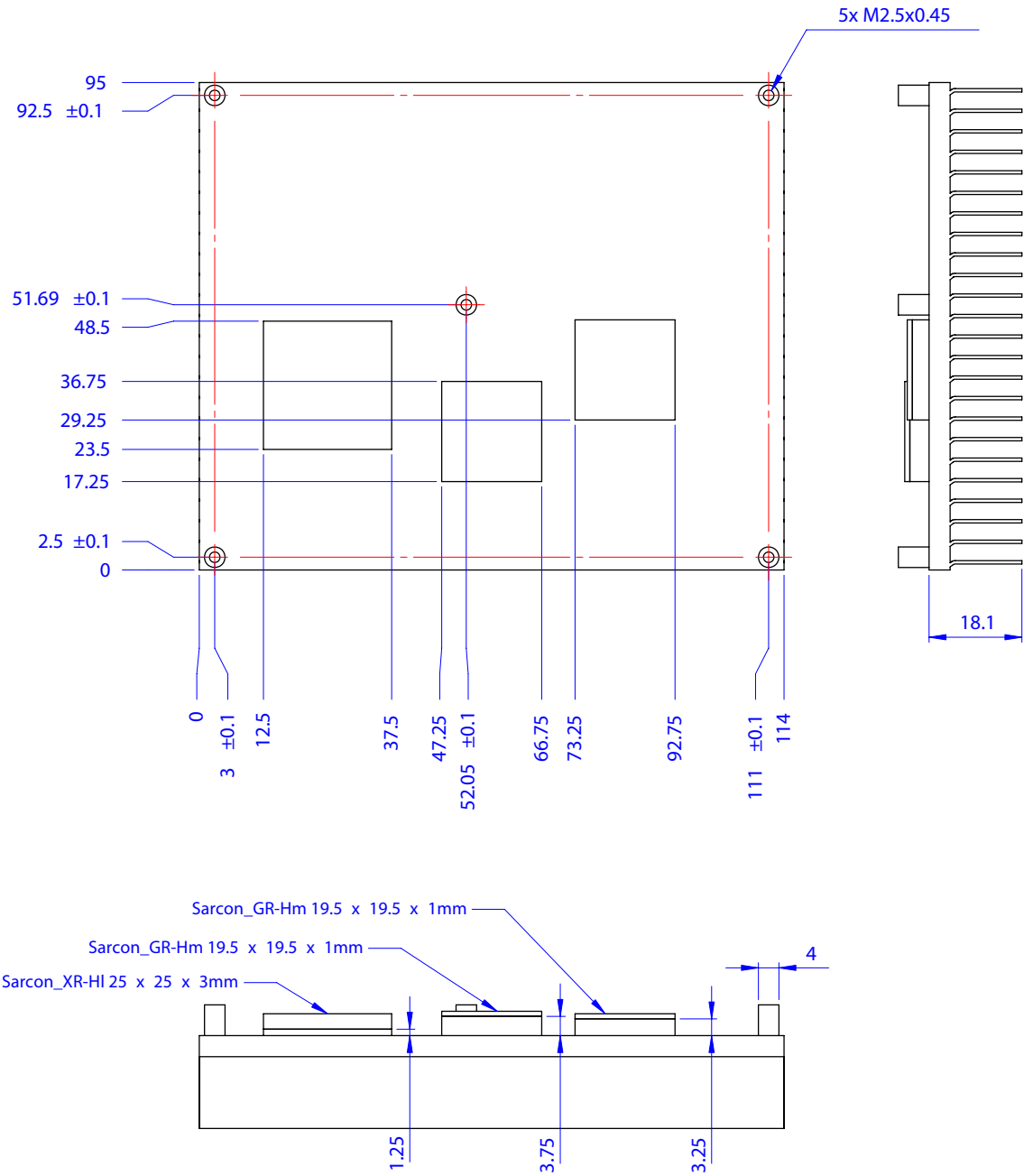


- The heatsink comes with four M2.5 x L12mm screws with washer/spring for use with 3 mm standoffs on the carrier board, and M2.5 x L16mm screws with washer/spring for use with 9.5 mm standoffs on the carrier board. (If the heatsink is purchased separately, one M2.5 x L6mm screw is also included.)

B.6 Dimensions for THSH-EAT-BL Heatsink

THSH-EAT-BL

High profile heatsink with “horizontally” oriented fins for bottom mounting.



- The heatsink comes with four M2.5 x L12mm screws with washer/spring for use with 3 mm standoffs on the carrier board, and M2.5 x L16mm screws with washer/spring for use with 9.5 mm standoffs on the carrier board. (If the heatsink is purchased separately, one M2.5 x L6mm screw is also included.)

Important Safety Instructions

For user safety, please read and follow all instructions, warnings, cautions, and notes marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:

  - Turn off power and unplug any power cords/cables.

- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.
- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.
- A Lithium-type battery may be provided for uninterrupted, backup or emergency power.

Risk of explosion if battery is replaced by an incorrect type. Dispose of used batteries according to the instructions.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

Getting Service

Contact us should you require any service or assistance.

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