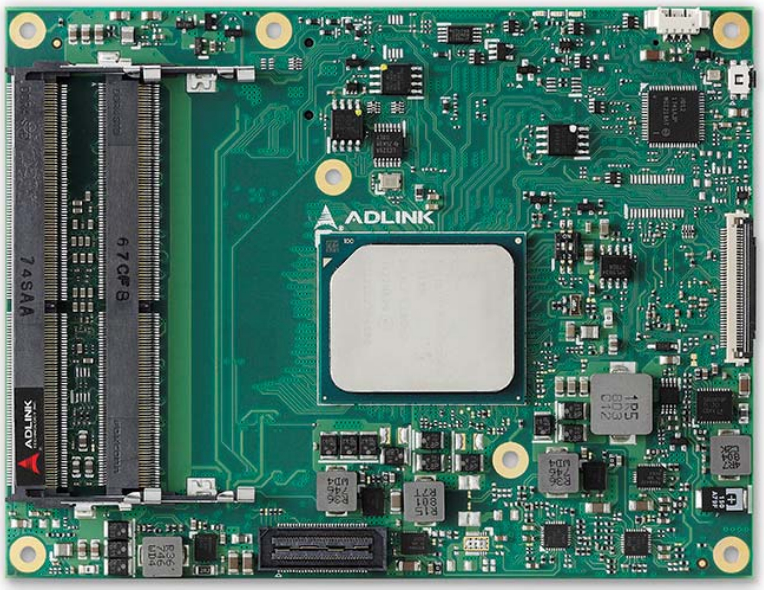
Express-DN7

User's Manual

COM Express Basic Size Type 7 Module with up to 16 cores
Intel Atom® C3000 SoC (Denverton-NS)



COM Express®

Manual Rev.: 1.2
Revision Date: October 6, 2021
Part Number: 50M-00049-1020

Leading **EDGE COMPUTING**

Preface

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Revision History

Revision	Description	Date	By
1.0	Initial release	2018-09-14	JC
1.1	Update specifications, pin descriptions, BMC codes, BIOS	2019-03-29	JC
1.2	Update BIOS, Fixed I/O Address Range Map	2021-10-06	JC

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1. Introduction

The Express-DN7 is a COM Express® COM.0 R3.0 Basic Size Type 7 module supporting the 64-bit Intel Atom® C3000 processor (formerly “Denverton-NS”) system-on-chip (SoC). 16 CPU cores with 31W TDP and integrated 10G Ethernet make the Express-DN7 especially suited for customers who need excellent computing performance with low power consumption, such as edge computing applications, in a long product life solution.

The Express-DN7 features Intel® Quick Assist Technology (cryptographic and compression acceleration), Intel® Virtualization Technology (including VT-x, VT-d), Intel® AES-NI Technology, and DDR4 ECC (or non-ECC) dual-channel memory at 1866/2133/2400 MHz (dependent on SoC SKU) to provide excellent overall performance. In addition, the Express-DN7 has up to three SODIMM sockets that are fully compliant with the COM Express mechanical specification.

An integrated Intel® 10G Ethernet controller supports a maximum of four 10GBASE-KR interfaces, relevant sideband signals and NC-SI. The Express-DN7 is designed to serve customers with optimized computing capability per watt and high speed connectivity requirements who want to outsource the custom core logic of their systems for reduced development time.

Input/output features include expanded PCIe bandwidth up to two PCIe x8 Gen3 lanes, a single onboard Gigabit Ethernet port with IEEE 1588 support suitable for real-time applications, USB 3.0/2.0 ports, and SATA 6 Gb/s ports. Support is provided for SMBus and I2C. The module is equipped with SPI AMI EFI BIOS with CMOS backup, supporting embedded features such as remote console, hardware monitor, and watchdog timer.

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2. Specifications

2.1. Core System

CPU	**Intel Atom® processor C3000 SoC, 14nm (formerly Denverton-NS)** • Intel Atom® C3808 2.0GHz 25W (12C/2133MHz, 20HSIO, eTEMP) • Intel Atom® C3708 1.7GHz 17W (8C/2133MHz, 20HSIO, eTEMP) • Intel Atom® C3508 1.6GHz 12W (4C/1866MHz, 8HSIO, eTEMP) • Intel Atom® C3308 1.6/2.1GHz 10W (2C/1866MHz, 6HSIO, eTEMP) • Intel Atom® C3958 2.0GHz 31W (16C/2400MHz, 20HSIO, by request) • Intel Atom® C3858 2.0GHz 25W (12C/2400MHz, 20HSIO, by request) • Intel Atom® C3758 2.2GHz 25W (8C/2400MHz, 20HSIO, by request) • Intel Atom® C3558 2.2GHz 16W (4C/2133MHz, 12HSIO, by request) • Intel Atom® C3538 2.1GHz 15W (4C/2133MHz, 12HSIO, by request) • Intel Atom® C3338 1.5/2.2GHz 9W (2C/1866MHz, 10HSIO, by request) Supporting: Intel® Quick Assist Technoloty (cryptographic and compression acceleration), Intel® VT (including VT-x, VT-d, VT-x with Extended Page Tables), Intel® Turbo Boost Technology 2.0, Intel® SSE4.2, Intel® 64 Architecture, Intel® ISA compatibility, Intel® Execurt Disable Bit, Intel® OS Guard, Intel® Secure Key, Intel® AES-NI, Intel® Security Hash Algorithm Extensions (SHA-1, SHA-256) **Notes:** • Availability of features may vary between processor SKUs. • SoC SKUs not listed above or marked “by request” are supported by project basis. Please contact your local ADLINK representative.
Cache	16MB for C3708/C3958/C3758, 12MB for C3808/C3858, 8MB for C3508/C3558/C3538, 4MB for C3308/C3338
Memory	Dual channel ECC (or non-ECC) 1866/2133/2400 MHz DDR4 memory up to 48GB in three SODIMM sockets (support for 96GB is under verification) **Notes:** • Supported memory frequencies may vary between processor SKUs. • The 3rd SODIMM on the module’s bottom side is supported by project basis. Please contact local sales. • C3308/C3338 only support one channel in the lower SODIMM socket on top side.
Embedded BIOS	AMI Aptio 5 EFI with CMOS backup in 16MB SPI BIOS
Chipset	Integrated in SoC

2.2. Expansion Busses

PCI Express	Up to 1 PCI Express x8 Lanes Gen3 (CD): • Lanes 16-23: four controllers/root ports, can be configured to x8, x4, x2, x1 (connected to PCIe Cluster 1 which has four root ports RP 4/5/6/7) Up to 1 PCI Express x8 Lanes Gen3 (AB & CD): • Lanes 0-7: four controllers/root ports, can be configured to x8, x4, x2, x1 (dependent on GbE support, connected to PCIe Cluster 0 which has four root ports, RP 0/1/2/3) **Notes:** • Number of PCIe lanes depends on SoC SKUs. Refer to 2.6 Multi I/O and Storage for detailed info • Root port 3 (PCIe lanes 6/7) is connected to GbE controller by default; support for PCIe lanes 6/7 is by build option. • Although the Denverton-NS platform supports four roots on Lanes 0-7, the PICMG COM.0 R3.0 specification for Lanes 0-7 states: "*Type 7 module may support eight x1 root hubs. It is expected that future generation products may limit the number of available root hubs.*"
Other	• LPC bus • SMBus (system) • I^2C (user)

2.3. 10GBASE-KR

Integrated on Processor	Intel® 10G Ethernet Controller (two controllers)
10GbE Feature Support	Four 10GBASE-KR ports (on CD connector) Sideband signals (on CD connector) for 10GbE **Notes:** • 10GBASE-KR ports 0, 1 are from LAN controller 0, 10GBASE-KR ports 2, 3 are from LAN controller 1 • Maximum combined throughput on all four ports is 20Gb/s

	C3808	C3708	C3508	C3308
LAN Controller 0 (Gb/s)	10 2.5 1		2.5 1	
LAN Controller 1 (Gb/s)	10 2.5 1		2.5 1	

	C3958	C3858	C3758	C3558	C3538	C3338
LAN Controller 0 (Gb/s)	10 2.5 1					2.5 1
LAN Controller 1 (Gb/s)	10 2.5 1			2.5 1		

Note: The default 10GbE firmware supports four ports optical fiber PHY. Support for 10GBASE-T (copper PHY) is by project basis.

2.4. Gigabit Ethernet

Intel Controller	Intel® i210 Ethernet Controller, IEEE 1588 PTP support
Interface	10/100/1000 Mbit/s connection

Note: GbE0_SDP pin (A49) is supported.

2.5. NC-SI

- **NC-SI** (on AB connector): manageability interface, connecting to IPMI BMC located on carrier board
  - Routing from Intel® i210 Ethernet Controller to row AB connector

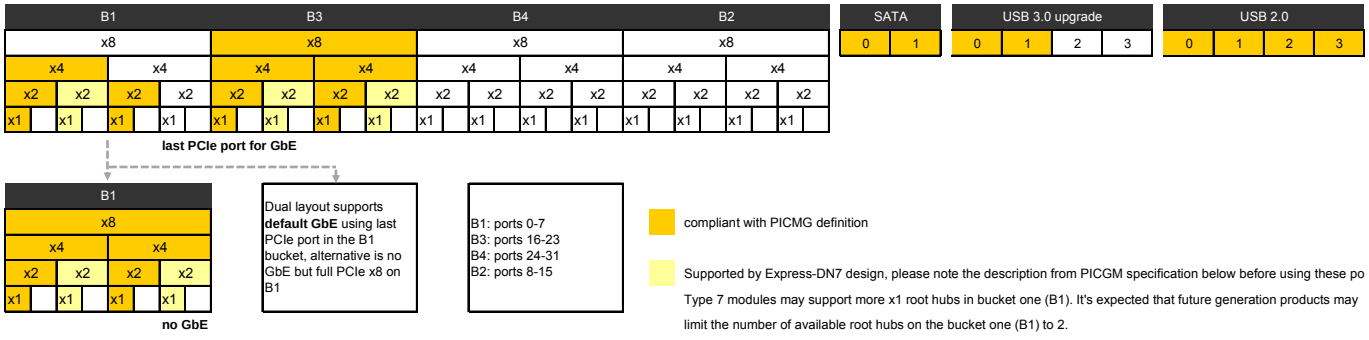
2.6. Multi I/O and Storage

I/O Hub	Integrated on SoC
USB	Up to 2x USB 3.0/2.0 (USB 0,1), 2x USB 2.0 (USB 2,3)
SATA*	Up to 2x SATA 6Gb/s (SATA 0,1)
GPIO	4 GPO and 4 GPI (GPI with interrupt)
eMMC 5.0 (build option)	8/16/32/64GB (boot-up device functionalilty supported by project basis)

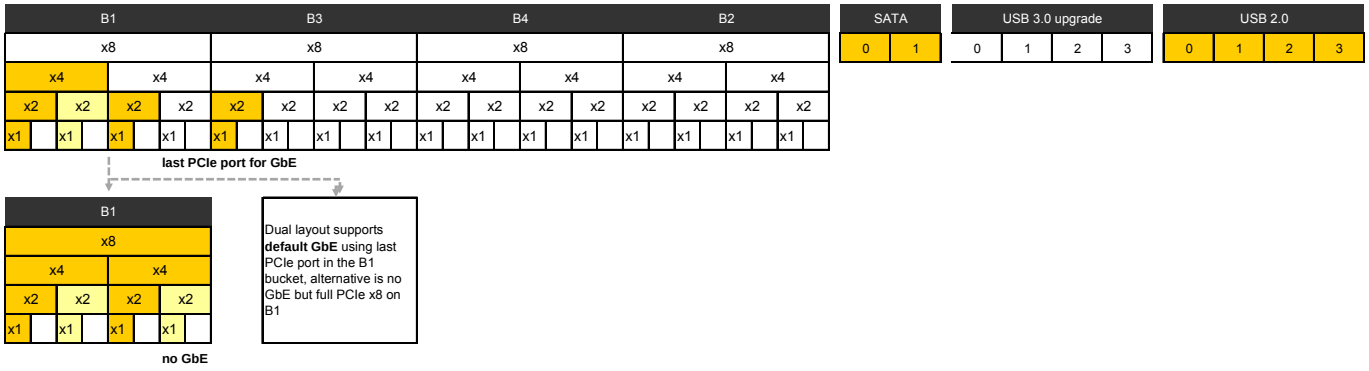
***Note:** For SATA 6Gb/s compatibility, it is strongly recommended to use a SATA redriver on the carrier board.

I/O Support of SoC SKUs

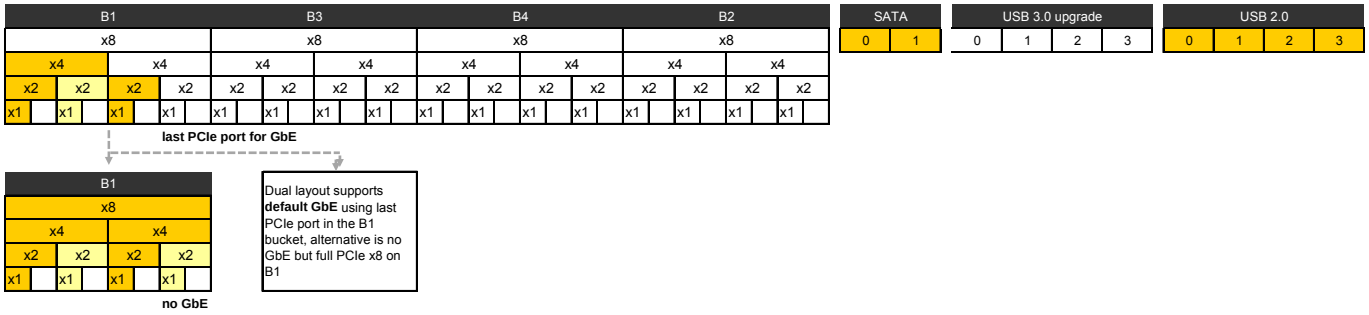
C3808, C3708, C3958, C3858, C3758
20 HSIO, 2CH DDR4 max., 48 GB DDR4



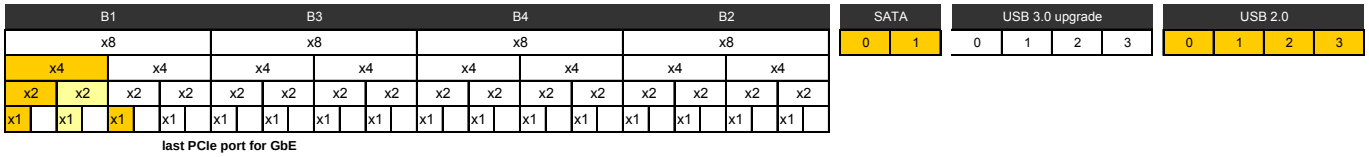
C3558, C3538
12 HSIO, 2CH DDR4, max. 48 GB DDR4



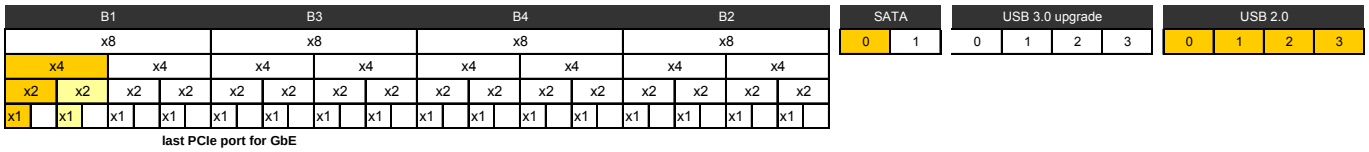
C3338
10 HSIO, 1CH DDR4, max. 16 GB DDR4



C3508
8 HSIO, 2CH DDR4, max. 48 GB DDR4



C3308
6 HSIO, 1CH DDR4, max. 16 GB DDR4



Note: PCIe configurations not listed in standard BIOS setting can be supported by project basis. Please contact your local ADLINK representative.

2.7. Serial I/O on Module

- **Chipset:** Nuvoton NCT5104D
  Note: two UART ports native from SoC instead of NCT5104D supported by build option
- **Ports:** 2x UARTs Rx/Tx only
- **Console Redirection:** COM 1 or COM 2 selectable in BIOS

COM Port	Description	IRQ	Address	Console redirection support
COM 1	Supported by module (SER0, A98/A99), via NCT5104D	4	0x3F8	YES
COM 2	Supported by module (SER1, A101/A102), via NCT5104D	3	0x2F8	YES
COM 3	Supported by Super I/O (W83627DHG) on carrier board	5	0x240	YES
COM 4	Supported by Super I/O (W83627DHG) on carrier board	7	0x248	YES

Note: NCT5104D is 16550-compatible and it supports up to 1.5Mb/s (baud rate at 24MHz)

2.8. Trusted Platform Module (TPM)

- **Chipset:** Infineon (TPM is supported by build option)
- **Type:** TPM 2.0

2.9. SEMA Board Controller

- **Type:** ADLINK Smart Embedded Management Agent (SEMA)
- **Functions:**
  - Voltage/Current monitoring
  - Power sequence debug support
  - AT/ATX mode control
  - Logistics and forensic information
  - Flat panel control (not supported on this product, as the platform has no GPU)
  - General purpose I2C
  - Failsafe BIOS (dual BIOS)
  - Watchdog timer and fan control

2.10. Debug

- 40-pin flat cable connector to be used with DB-40 debug module
  Supports: BIOS POST code LED, BMC access, SPI BIOS flashing, power testpoints, debug LEDs
- MIPI60 header for debug of SoC (build option)

2.11. Power Specifications

Power Modes	AT and ATX mode (AT mode startup controlled by SEMA Board Controller)
Standard Voltage Input	ATX @ 12V±5%,/ 5Vsb ±5% or AT @ 12V ±5%
Wide Voltage Input	ATX @ 8.5-20V, 5Vsb ±5% or AT @ 8.5-20V
Power Management	ACPI 5.0 compliant, Smart Battery support
Power States	Supports C0, C1, C2, C3, S0, S4, S5, S5 ECO mode (Wake-on-USB S4, WOL S4/S5)
ECO Mode	Supports deep S5 for 5Vsb power saving

2.12. Power Consumption

Please contact your ADLINK representative for the document “COM Express Module Power Consumption”.

2.13. Operating Temperatures

Standard Operating Temperature	0°C to +60°C (Wide Voltage Input) Storage: -20°C to +80°C
Extreme Rugged Operating Temperature (optional)	-40°C to +85°C (Standard Voltage Input, only for eTEMP SKUs, by build option, TBC) Storage: -40°C to +85°C

2.14. Environmental

Humidity	Operating: 5-90% RH, non-condensing Storage: 5-95% RH (and operating with conformal coating)
Shock and Vibration	IEC 60068-2-64 and IEC-60068-2-27 MIL-STD-202F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D
HALT	Thermal Stress, Vibration Stress, Thermal Shock and Combined Test

2.15. Specification Compliance

- PICMG COM.0: Rev 3.0 Type 7, Basic size 125 x 95 mm

2.16. Operating Systems

Standard Support	• Windows Server 2012/2016 (64-bit) • Yocto project based Linux(64-bit)
Extended Support (BSP)	• Yocto project based Linux (64-bit)

2.17. Functional Diagram

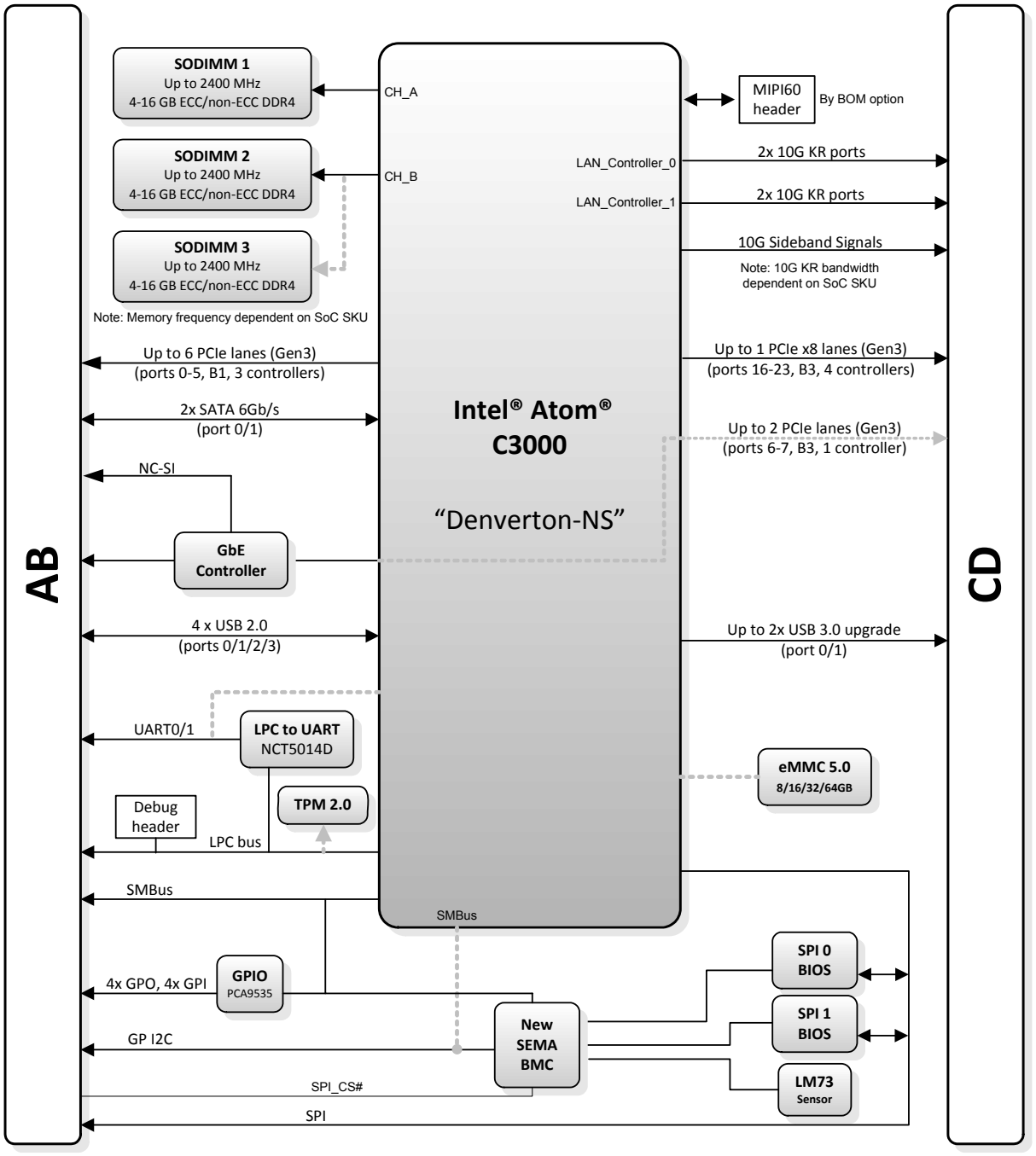
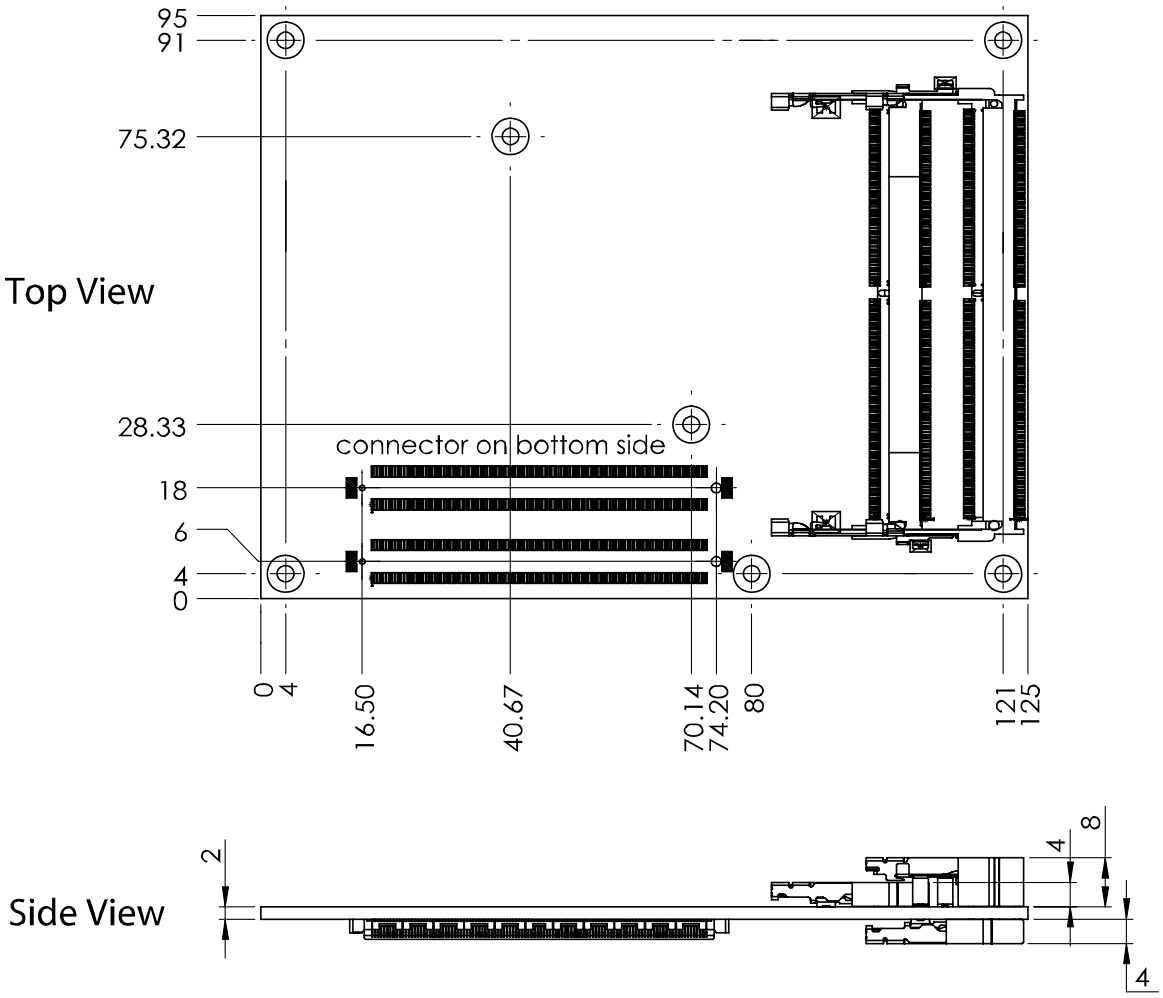


Figure 1: Express-DN7 Functional Block Diagram

Note: I/O dependent on the specific SoC SKU, described in 2.6 Multi I/O and Storage above.

2.18. Mechanical Drawing



All dimensions are shown in millimeters. Tolerances should be ± 0.25mm, unless otherwise noted.
The tolerances on the module connector locating peg holes (dimensions [16.50, 6.00] and [16.50, 18.00]) should be ± 0.10mm.

Figure 2: Express-DN7 Mechanical Drawing

3. Pinouts and Signal Descriptions

3.1. AB/CD Pin Definitions

The Express-DN7 is a Type 7 module supporting up to 16 PCIe lanes and four 10GBASE-KR ports on the CD connector and NC-SI on the AB connector. In the table below, all standard pins of the COM Express specification are described, including those not supported on the Express-DN7. Signals not supported on the Express-DN7 module are ~~crossed out~~.

Table 1: Express-DN7 AB/CD Pin Definitions

	Row A		Row B		Row C		Row D
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**
A1	GND (fixed)	**B1**	GND (fixed)	**C1**	GND (fixed)	**D1**	GND (fixed)
A2	GBE0_MDI3-	**B2**	GBE0_ACT#	**C2**	GND	**D2**	GND
A3	GBE0_MDI3+	**B3**	LPC_FRAME# ~~/ESPI_CS0#~~	**C3**	USB_SSRX0-	**D3**	USB_SSTX0-
A4	GBE0_LINK100#	**B4**	LPC_AD0 ~~/ESPI_IO_0~~	**C4**	USB_SSRX0+	**D4**	USB_SSTX0+
A5	GBE0_LINK1000#	**B5**	LPC_AD1 ~~/ESPI_IO_1~~	**C5**	GND	**D5**	GND
A6	GBE0_MDI2-	**B6**	LPC_AD2 ~~/ESPI_IO_2~~	**C6**	USB_SSRX1-	**D6**	USB_SSTX1-
A7	GBE0_MDI2+	**B7**	LPC_AD3 ~~/ESPI_IO_3~~	**C7**	USB_SSRX1+	**D7**	USB_SSTX1+
A8	GBE0_LINK#	**B8**	~~LPC_DRQ0# /ESPI_ALERT0#~~	**C8**	GND	**D8**	GND
A9	GBE0_MDI1-	**B9**	~~LPC_DRQ1# /ESPI_ALERT1#~~	**C9**	~~USB_SSRX2-~~	**D9**	~~USB_SSTX2-~~
A10	GBE0_MDI1+	**B10**	LPC_CLK ~~/ESPI_CK~~	**C10**	~~USB_SSRX2+~~	**D10**	~~USB_SSTX2+~~
A11	GND (fixed)	**B11**	GND (fixed)	**C11**	GND (fixed)	**D11**	GND (fixed)
A12	GBE0_MDI0-	**B12**	PWRBTN#	**C12**	~~USB_SSRX3-~~	**D12**	~~USB_SSTX3-~~
A13	GBE0_MDI0+	**B13**	SMB_CK	**C13**	~~USB_SSRX3+~~	**D13**	~~USB_SSTX3+~~
A14	GBE0_CTREF	**B14**	SMB_DAT	**C14**	GND	**D14**	GND
A15	SUS_S3#	**B15**	SMB_ALERT#	**C15**	10G_PHY_MDC_SCL3	**D15**	10G_PHY_MDIO_SDA3
A16	SATA0_TX+	**B16**	SATA1_TX+	**C16**	10G_PHY_MDC_SCL2	**D16**	10G_PHY_MDIO_SDA2
A17	SATA0_TX-	**B17**	SATA1_TX-	**C17**	~~10G_SDP2~~	**D17**	~~10G_SDP3~~
A18	SUS_S4#	**B18**	SUS_STAT# ~~/ESPI_RESET#~~	**C18**	GND	**D18**	GND
A19	SATA0_RX+	**B19**	SATA1_RX+	**C19**	PCIE_RX6+ *	**D19**	PCIE_TX6+ *
A20	SATA0_RX-	**B20**	SATA1_RX-	**C20**	PCIE_RX6- *	**D20**	PCIE_TX6- *
A21	GND (fixed)	**B21**	GND (fixed)	**C21**	GND (fixed)	**D21**	GND (fixed)
A22	~~PCIE_TX15+~~	**B22**	~~PCIE_RX15+~~	**C22**	PCIE_RX7+ *	**D22**	PCIE_TX7+ *
A23	~~PCIE_TX15-~~	**B23**	~~PCIE_RX15-~~	**C23**	PCIE_RX7- *	**D23**	PCIE_TX7- *
A24	SUS_S5#	**B24**	PWR_OK	**C24**	10G_INT2	**D24**	10G_INT3
A25	~~PCIE_TX14+~~	**B25**	~~PCIE_RX14+~~	**C25**	GND	**D25**	GND
A26	~~PCIE_TX14-~~	**B26**	~~PCIE_RX14-~~	**C26**	10G_KR_RX3+	**D26**	10G_KR_TX3+
A27	BATLOW#	**B27**	WDT	**C27**	10G_KR_RX3-	**D27**	10G_KR_TX3-
A28	(S)ATA_ACT#	**B28**	RSVD	**C28**	GND	**D28**	GND
A29	RSVD	**B29**	RSVD	**C29**	10G_KR_RX2+	**D29**	10G_KR_TX2+
A30	RSVD	**B30**	RSVD	**C30**	10G_KR_RX2-	**D30**	10G_KR_TX2-
A31	GND (fixed)	**B31**	GND (fixed)	**C31**	GND (fixed)	**D31**	GND (fixed)
A32	RSVD	**B32**	~~SPKR~~	**C32**	10G_SFP_SDA3	**D32**	10G_SFP_SCL3
A33	RSVD	**B33**	I2C_CK	**C33**	10G_SFP_SDA2	**D33**	10G_SFP_SCL2
A34	BIOS_DIS0# ~~/ESPI_SAFS~~	**B34**	I2C_DAT	**C34**	10G_PHY_RST_23	**D34**	10G_PHY_CAP_23
A35	THRMTRIP#	**B35**	THRM#	**C35**	10G_PHY_RST_01	**D35**	10G_PHY_CAP_01

	Row A		Row B		Row C		Row D
Pin	Name	Pin	Name	Pin	Name	Pin	Name
A36	~~PCIE_TX13+~~	B36	~~PCIE_RX13+~~	C36	10G_LED_SDA	D36	RSVD
A37	~~PCIE_TX13-~~	B37	~~PCIE_RX13-~~	C37	10G_LED_SCL	D37	RSVD
A38	GND	B38	GND	C38	10G_SFP_SDA1	D38	10G_SFP_SCL1
A39	~~PCIE_TX12+~~	B39	~~PCIE_RX12+~~	C39	10G_SFP_SDA0	D39	10G_SFP_SCL0
A40	~~PCIE_TX12-~~	B40	~~PCIE_RX12-~~	C40	~~10G_SDP0~~	D40	~~10G_SDP1~~
A41	GND (fixed)	B41	GND (fixed)	C41	GND (fixed)	D41	GND (fixed)
A42	USB2-	B42	USB3-	C42	10G_KR_RX1+	D42	10G_KR_TX1+
A43	USB2+	B43	USB3+	C43	10G_KR_RX1-	D43	10G_KR_TX1-
A44	USB_2_3_OC#	B44	USB_0_1_OC#	C44	GND	D44	GND
A45	USB0-	B45	USB1-	C45	10G_PHY_MDC_SCL1	D45	10G_PHY_MDIO_SDA1
A46	USB0+	B46	USB1+	C46	10G_PHY_MDC_SCL0	D46	10G_PHY_MDIO_SDA0
A47	VCC_RTC	B47	~~ESPI_EN~~	C47	10G_INT0	D47	10G_INT1
A48	RSVD	B48	~~USB0_HOST_PRSNT~~	C48	GND	D48	GND
A49	GBE0_SDP	B49	SYS_RESET#	C49	10G_KR_RX0+	D49	10G_KR_TX0+
A50	LPC_SERIRQ /~~ESPI_CS1#~~	B50	CB_RESET#	C50	10G_KR_RX0-	D50	10G_KR_TX0-
A51	GND (fixed)	B51	GND (fixed)	C51	GND (fixed)	D51	GND (fixed)
A52	PCIE_TX5+	B52	PCIE_RX5+	C52	PCIE_RX16+	D52	PCIE_TX16+
A53	PCIE_TX5-	B53	PCIE_RX5-	C53	PCIE_RX16-	D53	PCIE_TX16-
A54	GPI0	B54	GPO1	C54	TYPE0#	D54	RSVD
A55	PCIE_TX4+	B55	PCIE_RX4+	C55	PCIE_RX17+	D55	PCIE_TX17+
A56	PCIE_TX4-	B56	PCIE_RX4-	C56	PCIE_RX17-	D56	PCIE_TX17-
A57	GND	B57	GPO2	C57	TYPE1#	D57	TYPE2#
A58	PCIE_TX3+	B58	PCIE_RX3+	C58	PCIE_RX18+	D58	PCIE_TX18+
A59	PCIE_TX3-	B59	PCIE_RX3-	C59	PCIE_RX18-	D59	PCIE_TX18-
A60	GND (fixed)	B60	GND (fixed)	C60	GND (fixed)	D60	GND (fixed)
A61	PCIE_TX2+	B61	PCIE_RX2+	C61	PCIE_RX19+	D61	PCIE_TX19+
A62	PCIE_TX2-	B62	PCIE_RX2-	C62	PCIE_RX19-	D62	PCIE_TX19-
A63	GPI1	B63	GPO3	C63	RSVD	D63	RSVD
A64	PCIE_TX1+	B64	PCIE_RX1+	C64	RSVD	D64	RSVD
A65	PCIE_TX1-	B65	PCIE_RX1-	C65	PCIE_RX20+	D65	PCIE_TX20+
A66	GND	B66	WAKE0#	C66	PCIE_RX20-	D66	PCIE_TX20-
A67	GPI2	B67	WAKE1#	C67	~~RAPID_SHUTDOWN~~	D67	GND
A68	PCIE_TX0+	B68	PCIE_RX0+	C68	PCIE_RX21+	D68	PCIE_TX21+
A69	PCIE_TX0-	B69	PCIE_RX0-	C69	PCIE_RX21-	D69	PCIE_TX21-
A70	GND (fixed)	B70	GND (fixed)	C70	GND (fixed)	D70	GND (fixed)
A71	~~PCIE_TX8+~~	B71	~~PCIE_RX8+~~	C71	PCIE_RX22+	D71	PCIE_TX22+
A72	~~PCIE_TX8-~~	B72	~~PCIE_RX8-~~	C72	PCIE_RX22-	D72	PCIE_TX22-
A73	GND	B73	GND	C73	GND	D73	GND
A74	~~PCIE_TX9+~~	B74	~~PCIE_RX9+~~	C74	PCIE_RX23+	D74	PCIE_TX23+
A75	~~PCIE_TX9-~~	B75	~~PCIE_RX9-~~	C75	PCIE_RX23-	D75	PCIE_TX23-
A76	GND	B76	GND	C76	GND	D76	GND
A77	~~PCIE_TX10+~~	B77	~~PCIE_RX10+~~	C77	RSVD	D77	RSVD
A78	~~PCIE_TX10-~~	B78	~~PCIE_RX10-~~	C78	~~PCIE_RX24+~~	D78	~~PCIE_TX24+~~
A79	GND	B79	GND	C79	~~PCIE_RX24-~~	D79	~~PCIE_TX24-~~

	Row A		Row B		Row C		Row D
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**
A80	GND (fixed)	**B80**	GND (fixed)	**C80**	GND (fixed)	**D80**	GND (fixed)
A81	~~PCIE_TX11+~~	**B81**	~~PCIE_RX11+~~	**C81**	~~PCIE_RX25+~~	**D81**	~~PCIE_TX25~~
A82	~~PCIE_TX11-~~	**B82**	~~PCIE_RX11-~~	**C82**	~~PCIE_RX25-~~	**D82**	~~PCIE_TX25-~~
A83	GND	**B83**	GND	**C83**	RSVD	**D83**	RSVD
A84	NCSI_TX_EN	**B84**	VCC_5V_SBY	**C84**	GND	**D84**	GND
A85	GPI3	**B85**	VCC_5V_SBY	**C85**	~~PCIE_RX26+~~	**D85**	~~PCIE_TX26+~~
A86	RSVD	**B86**	VCC_5V_SBY	**C86**	~~PCIE_RX26-~~	**D86**	~~PCIE_TX26-~~
A87	RSVD	**B87**	VCC_5V_SBY	**C87**	GND	**D87**	GND
A88	PCIE0_CK_REF+	**B88**	BIOS_DIS1#	**C88**	~~PCIE_RX27+~~	**D88**	~~PCIE_TX27+~~
A89	PCIE0_CK_REF-	**B89**	~~NSCI_RX_ER~~	**C89**	~~PCIE_RX27-~~	**D89**	~~PCIE_TX27-~~
A90	GND (fixed)	**B90**	GND (fixed)	**C90**	GND (fixed)	**D90**	GND (fixed)
A91	SPI_POWER	**B91**	NCSI_CLK_IN	**C91**	~~PCIE_RX28+~~	**D91**	~~PCIE_TX28+~~
A92	SPI_MISO	**B92**	NCSI_RXD1	**C92**	~~PCIE_RX28-~~	**D92**	~~PCIE_TX28-~~
A93	GPO0	**B93**	NCSI_RXD0	**C93**	GND	**D93**	GND
A94	SPI_CLK	**B94**	NCSI_CRS_DV	**C94**	~~PCIE_RX29+~~	**D94**	~~PCIE_TX29+~~
A95	SPI_MOSI	**B95**	NCSI_TXD1	**C95**	~~PCIE_RX29-~~	**D95**	~~PCIE_TX29-~~
A96	TPM_PP	**B96**	NCSI_TXD0	**C96**	GND	**D96**	GND
A97	TYPE10#	**B97**	SPI_CS#	**C97**	RSVD	**D97**	RSVD
A98	SER0_TX	**B98**	NCSI_ARB_IN	**C98**	~~PCIE_RX30+~~	**D98**	~~PCIE_TX30+~~
A99	SER0_RX	**B99**	NCSI_ARB_OUT	**C99**	~~PCIE_RX30-~~	**D99**	~~PCIE_TX30-~~
A100	GND (fixed)	**B100**	GND (fixed)	**C100**	GND (fixed)	**D100**	GND (fixed)
A101	SER1_TX	**B101**	FAN_PWMOUT	**C101**	~~PCIE_RX31+~~	**D101**	~~PCIE_TX31+~~
A102	SER1_RX	**B102**	FAN_TACHIN	**C102**	~~PCIE_RX31-~~	**D102**	~~PCIE_TX31-~~
A103	LID#	**B103**	SLEEP#	**C103**	GND	**D103**	GND
A104	VCC_12V	**B104**	VCC_12V	**C104**	VCC_12V	**D104**	VCC_12V
A105	VCC_12V	**B105**	VCC_12V	**C105**	VCC_12V	**D105**	VCC_12V
A106	VCC_12V	**B106**	VCC_12V	**C106**	VCC_12V	**D106**	VCC_12V
A107	VCC_12V	**B107**	VCC_12V	**C107**	VCC_12V	**D107**	VCC_12V
A108	VCC_12V	**B108**	VCC_12V	**C108**	VCC_12V	**D108**	VCC_12V
A109	VCC_12V	**B109**	VCC_12V	**C109**	VCC_12V	**D109**	VCC_12V
A110	GND (fixed)	**B110**	GND (fixed)	**C110**	GND (fixed)	**D110**	GND (fixed)

Notes:

- LPC and eSPI are muxed in the standard COM Express specification. The Denverton-NS platform only supports the LPC bus.
- PCIe lanes 6 & 7 are supported by build option, in place of GbE (PCIe lanes 6/7 come from one controller)
- PCIe lanes, USB 3.0 upgrade signals, SATA ports dependent on SoC SKUs. Refer to 2.6 Multi I/O and Storage for detailed info.

3.2. Signal Description Terminology

The following terms are used in the COM Express AB/CD Signal Descriptions below.

I	Input to the Module
O	Output from the Module
I/O	Bi-directional input/output signal
OD	Open drain output
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I/O 3.3Vsb	Bi-directional 3.3V tolerant active in standby state
I 3.3Vsb	Input 3.3V tolerant active in standy state
P	Power Input/Output
REF	Reference voltage output that may be sourced from a module power plane.
PDS	Pull-down strap. This is an output pin on the module that is either tied to GND or not connected. The signal is used to indicate the PICMG module type to the Carrier Board.
PU	ADLINK implemented pull-up resistor on module
PD	ADLINK implemented pull-down resistor on module

3.3. AB Signal Descriptions

3.3.1. Network Controller Sideband Interface (NC-SI)

Signal	Pin	Description	I/O	PU/PD	Comment
NCSI_CLK_IN	B91	Clock reference for receive, transmit and control interface	I 3.3VSB	PD 10k	
NCSI_RXD[1:0]	B92 B93	Receive Data (from NC to BMC)	O 3.3VSB	PU 10k 3.3VSB	PU 10k that aligns with LAN chip specification
NCSI_TXD[1:0]	B95 B96	Transmit Data (from BMC to NC)	I 3.3VSB	PU 10k 3.3VSB	
NCSI_CRS_DV	B94	Carrier Sense/Receive Data valid to MC, indicating that the transmitted data from NC to BMC is valid	O 3.3VSB	PD 10k	PU 10k that aligns with LAN chip specification
NCSI_TX_EN	A84	Transmit enable	I 3.3VSB	PD 10k	
NCSI_RX_ER	B89	Receive error	O 3.3VSB		
NCSI_ARB_IN	B98	Network Controller hardware arbitration input	I 3.3VSB		Left floating on module, that aligns with LAN chip specification
NCSI_ARB_OUT	B99	Network Controller hardware arbitration output	O 3.3VSB		

3.3.2. Gigabit Ethernet

Gigabit Ethernet	Pin	Description	I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000BASE-T 100BASE-TX 10BASE-T MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	I/O Analog		Twisted pair signals for external transformer.
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	O 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	O 3.3VSB		
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 1 and 2 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be 250 mA or less.	REF GND min 3.3V max		NC pin
GBE0_SDP	A49	Gigabit Ethernet Controller 0 Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal.	I/O 3.3VSB		

3.3.3. SATA

Signal	Pin	Description	I/O	PU/PD	Comment
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		AC coupled on Module
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		AC coupled on Module
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	O 3.3V		

SATA on COMe Module	HSIO Function on SoC
SATA 0	SATA controller #2, 5 (Lane 16)
SATA 1	SATA controller #2, 6 (Lane 17)

Note: Maximum number of HSIO dependent on SoC SKU. C3808 is used as an example here (20 HSIO).

3.3.4. PCI Express

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		AC coupled off Module

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_TX8+ PCIE_TX8-	A71 A72	PCI Express channel 8, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX8+ PCIE_RX8-	B71 B72	PCI Express channel 8, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX9+ PCIE_TX9-	A74 A75	PCI Express channel 9, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX9+ PCIE_RX9-	B74 B75	PCI Express channel 9, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX10+ PCIE_TX10-	A77 A78	PCI Express channel 10, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX10+ PCIE_RX10-	B77 B78	PCI Express channel 10, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX11+ PCIE_TX11-	A81 A82	PCI Express channel 11, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX11+ PCIE_RX11-	B81 B82	PCI Express channel 11, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX12+ PCIE_TX12-	A39 A40	PCI Express channel 12, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX12+ PCIE_RX12-	B39 B40	PCI Express channel 12, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX13+ PCIE_TX13-	A36 A37	PCI Express channel 13, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX13+ PCIE_RX13-	B36 B37	PCI Express channel 13, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX14+ PCIE_TX14-	A25 A26	PCI Express channel 14, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX14+ PCIE_RX14-	B25 B26	PCI Express channel 14, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX15+ PCIE_TX15-	A22 A23	PCI Express channel 15, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX15+ PCIE_RX15-	B22 B23	PCI Express channel 15, Receive Input differential pair.	I PCIE		Not supported
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		

PCIe on COMe Module	HSIO Function on SoC	Note
PCIE 0	Lane 0	The behavior of this platform: Only four controllers on Lanes 0-7. It can be used as one x8, two x4 or four x2/x1. Lanes 0-7 are from PCIe Cluster 0. It supports RP 0/1/2/3: RP0 for Lane 0/1 RP1 for Lane 2/3 RP3 for Lane 4/5 RP4 for Lane 6/7
PCIE 1	Lane 1	
PCIE 2	Lane 2	
PCIE 3	Lane 3	
PCIE 4	Lane 4	
PCIE 5	Lane 5	
PCIE 6	Lane 6	
PCIE 7	Lane 7	
PCIE 16	Lane 8	The behavior of this platform: Only four controllers on Lanes 8-15. It can be used as one x8, two x4 or four x2/x1. Lanes 16-23 are from PCIe Cluster 1. It supports RP 4/5/6/7: RP4 for Lane 8/9 RP5 for Lane 10/11 RP6 for Lane 12/13 RP7 for Lane 14/15
PCIE 17	Lane 9	
PCIE 18	Lane 10	
PCIE 19	Lane 11	
PCIE 20	Lane 12	
PCIE 21	Lane 13	
PCIE 22	Lane 14	
PCIE 23	Lane 15	

Note: Maximum number of HSIO dependent on SoC SKUs. C3808 is used as an example (20 HSIO).

3.3.5. LPC Bus

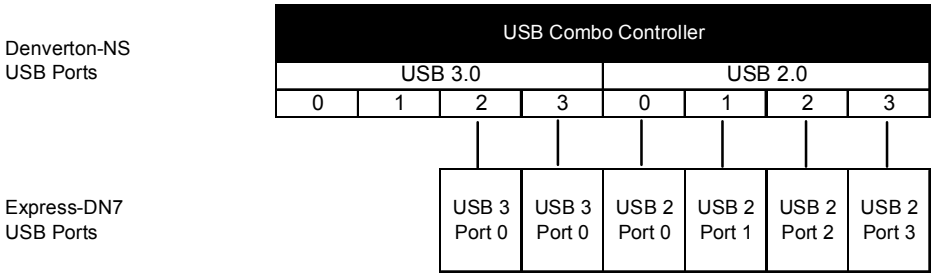
Signal	Pin	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		
LPC_DRQ0# LPC_DRQ1#	B8 B9	LPC serial DMA request	I 3.3V		Not supported
LPC_SERIRQ	A50	LPC serial interrupt	I/O OD 3.3V	PU 8.2k 3.3V	
LPC_CLK	B10	LPC clock output –33MHz nominal	O 3.3V		This platform supports 24MHz nominal

Note: eSPI and LPC buses are muxed as defined by PICMG. The Denverton-NS platform only supports LPC interface.

3.3.6. USB

Signal	Pin	Description	I/O	PU/PD	Comment
USB0+ USB0-	A46 A45	USB differential data pairs for Port 0	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB1+ USB1-	B46 B45	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB2+ USB2-	A43 A42	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB3+ USB3-	B43 B42	USB differential data pairs for Port 2	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on carrier
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on carrier
USB0_HOST_ PRSNT	A48	Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present.	I 3.3VSB		Not Supported. Limitation of this platform

3.3.7. USB Root Segmentation



Notes: Maximum number of HSIO dependent on SoC SKU. C3808 is used as an example (20 HSIO).
USB 3.0 0/1/2/3 mapping to HSIO Lane 16/17/18/19. Lane 16 & 17 are SATA and USB 3.0 muxed. On Express-DN7, the Lanes 16 & 17 are used for SATA ports support.

3.3.8. SPI (BIOS only)

Signal	Pin	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB	PU 10k 3.3VSB	
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier	O P 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I	PU 10k 3.3VSB	Carrier shall pull to GND or leave not-connected.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I	PU 10k 3.3VSB	Carrier shall pull to GND or leave not-connected

3.3.9. Miscellaneous

Signal	Pin	Description	I/O	PU/PD	Comment
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V	PU 10k 3.3V	Not Supported
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V	PU 10k 3.3V	
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3VSB		
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V	PU 10k 3.3V	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan’s RPM.	O OD 3.3V	PU 2.2K 3.3V	
FAN_TACHIN	B102	Fan tachometer input for a fan with a two pulse output.	I OD 3.3V	PU 47K 3.3V	
TPM_PP	A96	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V	PD 100k 3.3V	PD only when TPM on module

3.3.10. SMBus

Signal	Pin	Description	I/O	PU/PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line. Power sourced through 5V standby rail and main power rails.	I/O OD 3.3VSB	PU 2.2k 3.3VSB	Equivalent resistor is 2.2k
SMB_DAT#	B14	System Management Bus bidirectional data line. Power sourced through 5V standby rail and main power rails.	I/O OD 3.3VSB	PU 2.2k 3.3VSB	Equivalent resistor is 2.2k
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 5V standby rail and main power rails.	I 3.3VSB	PU 10k 3.3VSB	

3.3.11. I2C Bus

Signal	Pin	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Source SEMA BMC
I2C_DAT	B34	General purpose I²C port data I/O line	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Source SEMA BMC

3.3.12. General Purpose I/O (GPIO)

Signal	Pin	Description	I/O	PU/PD	Comment
GPO[0]	A93	General purpose output pins.	O 3.3V	PU 10K 3.3V	After hardware RESET output low
GPO[1]	B54	General purpose output pins.	O 3.3V	PU 10K 3.3V	After hardware RESET output low
GPO[2]	B57	General purpose output pins.	O 3.3V	PU 10K 3.3V	After hardware RESET output low
GPO[3]	B63	General purpose output pins.	O 3.3V	PU 10K 3.3V	After hardware RESET output low
GPI[0]	A54	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[1]	A63	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[2]	A67	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[3]	A85	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	

3.3.13. Serial Interface Signals

Signal	Pin	Description	I/O	PU/PD	Comment
SER0_TX	A98	General purpose serial port transmitter (TTL level output)	O CMOS		Power rail tolerance 5V, 12V
SER0_RX	A99	General purpose serial port receiver (TTL level input)	I CMOS	PU 10k 3.3V	Power rail tolerance 5V, 12V
SER1_TX	A101	General purpose serial port transmitter (TTL level output)	O CMOS		Power rail tolerance 5V, 12V
SER1_RX	A102	General purpose serial port receiver (TTL level input)	I CMOS	PU 10k 3.3V	Power rail tolerance 5V, 12V

3.3.14. Power and System Management

Signal	Pin	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge.	I 3.3VSB	PU 10k 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low request for module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.	I 3.3VSB	PU 10k 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow carrier based FPGAs or other configurable devices time to be programmed.	I 3.3VSB	PU 1k 3.3VSB	Should have weak pull up
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as “PS_ON”) may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10k 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 10k 3.3VSB	Connect to WAKE 1#
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3VSB	PU 10k 3.3VSB	
LID#	A103	LID button. Low active signal used by the ACPI operating system for a LID switch.	I OD 3.3VSB	PU 47k 3.3VSB	
SLEEP#	B103	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I OD 3.3VSB	PU 47k 3.3VSB	

3.3.15. Power and Ground

Signal	Pin	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109	Primary power input: +12V nominal (wide range). All available VCC_12V pins on the connector(s) shall be used.	P		8.5-20 V
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. See COM.0 Base Specification, Section 7 “Electrical Specifications“ for allowable input range. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		5Vsb ±5%
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21,B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path.	P		

3.4. CD Signal Descriptions

3.4.1. USB 3.0 Extension

Signal	Pin	Description	I/O	PU/PD	Comment
USB_SSRX0- USB_SSRX0+	C3 C4	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB0	I PCIE		AC coupled off module
USB_SSTX0- USB_SSTX0+	D3 D4	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB0	O PCIE		AC coupled on module
USB_SSRX1- USB_SSRX1+	C6 C7	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB1	I PCIE		AC coupled off module
USB_SSTX1- USB_SSTX1+	D6 D7	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB1	O PCIE		AC coupled on module
USB_SSRX2- USB_SSRX2+	C9 C10	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB2	I PCIE		Not supported
USB_SSTX2- USB_SSTX2+	D9 D10	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB2	O PCIE		Not supported
USB_SSRX3- USB_SSRX3+	C12 C13	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB3	I PCIE		Not supported
USB_SSTX3- USB_SSTX3+	D12 D13	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB3	O PCIE		Not supported

3.4.2. PCI Express x1

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair.	O PCIE		AC coupled on module
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair.	I PCIE		AC coupled off module
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair.	O PCIE		AC coupled on module
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair.	I PCIE		AC coupled off module

Note: PCIe lane 6 is supported by build option in place of GbE.

3.4.3. 10G Ethernet

10GbE port 0/1

Signal	Pin	Description	I/O	PU/PD	Comment
10G_KR_RX0+ 10G_KR_RX0- 10G_KR_RX1+ 10G_KR_RX1-	C49 C50 C42 C43	10GBASE-KR ports, Receive Input differential paris	I KR		AC coupled on Module
10G_KR_TX0+ 10G_KR_TX0- 10G_KR_TX1+ 10G_KR_TX1-	D49 D50 D42 D43	10GBASE-KR ports, Transmit Output differential paris	O KR		AC coupled on Carrier
10G_INT0 10G_INT1	C47 D47	Interrupt pin from Copper PHY or Optical SFP+ module to the 10GbE controller	I 3.3VSB	PU 2.2k 3.3VSB	
10G_PHY_MDIO_SDA0	D46	**MDIO Mode** Management Data I/O Interface mode data signal for serial data transfers between the MAC and an external PHY	O 3.3VSB		
		I^2C Mode I^2C Data signal, of the 2-wire management interface used for serial data transfers between the MAC and the external PHY	I/O OD 3.3VSB	PU 2.2k 3.3VSB	
10G_PHY_MDC_SCL0	C46	**MDIO Mode** Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY	O 3.3VSB		
		I^2C Mode I^2C Data signal, of the 2-wire management interface used for serial data transfers between the MAC and the external PHY	I/O OD 3.3VSB	PU 2.2k 3.3VSB	
10G_PHY_MDIO_SDA1	D45	**MDIO Mode** Management Data I/O Interface mode data signal for serial data transfers between the MAC and an external PHY	O 3.3VSB		
		I^2C Mode I^2C Data signal, of the 2-wire management interface used for serial data transfers between the MAC and the external PHY	I/O OD 3.3VSB	PU 2.2k 3.3VSB	
10G_PHY_MDC_SCL1	C45	**MDIO Mode** Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY	O 3.3VSB		
		I^2C Mode I^2C Data signal, of the 2-wire management interface used for serial data transfers between the MAC and the external PHY	I/O OD 3.3VSB	PU 2.2k 3.3VSB	
10G_SDP0 10G_SDP1	C40 D40	Software-Definable Pins	I/O 3.3VSB		Not supported
10G_SFP_SDA0 10G_SFP_SDA1	C39 C38	I^2C Data signal, of the 2-wire management interface used by 10GbE	I/O OD 3.3VSB	PU 2.2k 3.3VSB	

Signal	Pin	Description	I/O	PU/PD	Comment
		controller to access the management registers of an external Optical SFP+ module			
10G_SFP_SCL0 10G_SFP_SCL1	D39 D38	I^2C Clock signal, of the 2-wire management interface used by 10GbE controller to access the management registers of an external Optical SFP+ module	I/O OD 3.3VSB	PU 2.2k 3.3VSB	
10G_PHY_RST_01	C35	Output signal that resets and Optical PHY on port 0 and port 1	O 3.3VSB		This signal is not used for Copper PHY
10G_PHY_CAP_01	D35	Phy mode capability pin: Indicates if the PHY for 10G lanes 0 and1 is capable of configuration by I2C. High indicates MDIO-only configuration, and low indicates configuration capability via I2C or MDIO. The actual protocol used for PHY configuration is determined by the module, in part based on this input. The actual protocol used is indicated over the dedicated I2C interface	I 3.3VSB	PU 10k 3.3VSB	Default state is MDIO mode. For I^2C mode pull down with 1K on carrier
10G_LED_SDA	C36	I^2C Data signal, of the 2-wire that transfers all LED signals and additional Strapping signal for I^2C or MDIO mode of Optical PHY	I/O OD 3.3VSB	PU 2.2k 3.3VSB	LED signals for 10GbE port 2/3 are also transferred through this pin
10G_LED_SCL	C37	I^2C Clock signal, of the 2-wire that transfers all LED signals and additional Strapping signal for I^2C or MDIO mode of Optical PHY	I/O OD 3.3VSB	PU 2.2k 3.3VSB	LED signals for 10GbE port 2/3 are also transferred through this pin

10GbE port 2/3

Signal	Pin	Description	I/O	PU/PD	Comment
10G_KR_RX2+ 10G_KR_RX2- 10G_KR_RX3+ 10G_KR_RX3-	C29 C30 C26 C27	10GBASE-KR ports, Receive Input differential paris	I KR		AC coupled on Module
10G_KR_TX2+ 10G_KR_TX2- 10G_KR_TX3+ 10G_KR_TX3-	D29 D30 D26 D27	10GBASE-KR ports, Transmit Output differential paris	O KR		AC coupled on Carrier
10G_INT2 10G_INT3	C24 D24	Interrupt pin from Copper PHY or Optical SFP+ module to the 10GbE controller	I 3.3VSB	PU 2.2k 3.3VSB	
10G_PHY_MDIO_SDA2	D16	**MDIO Mode** Management Data I/O Interface mode data signal for serial data transfers between the MAC and an external PHY	O 3.3VSB		
		I^2C Mode I^2C Data signal, of the 2-wire management interface used for serial data transfers between the MAC and the external PHY	I/O OD 3.3VSB	PU 2.2k 3.3VSB	
10G_PHY_MDC_SCL2	C16	**MDIO Mode** Management Data I/O Interface mode clock signal for serial data transfers	O 3.3VSB		

Signal	Pin	Description	I/O	PU/PD	Comment
		between the MAC and an external PHY			
		I²C Mode I²C Data signal, of the 2-wire management interface used for serial data transfers between the MAC and the external PHY	I/O OD 3.3VSB	PU 2.2k 3.3VSB	
10G_PHY_MDIO_SDA3	D15	**MDIO Mode** Management Data I/O Interface mode data signal for serial data transfers between the MAC and an external PHY	O 3.3VSB		
		I²C Mode I²C Data signal, of the 2-wire management interface used for serial data transfers between the MAC and the external PHY	I/O OD 3.3VSB	PU 2.2k 3.3VSB	
10G_PHY_MDC_SCL3	C15	**MDIO Mode** Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY	O 3.3VSB		
		I²C Mode I²C Data signal, of the 2-wire management interface used for serial data transfers between the MAC and the external PHY	I/O OD 3.3VSB	PU 2.2k 3.3VSB	
10G_SDP2 10G_SDP3	C17 D17	Software-Definable Pins	I/O 3.3VSB		Not supported
10G_SFP_SDA2 10G_SFP_SDA3	C33 C32	I²C Data signal, of the 2-wire management interface used by 10GbE controller to access the management registers of an external Optical SFP+ module	I/O OD 3.3VSB	PU 2.2k 3.3VSB	
10G_SFP_SCL2 10G_SFP_SCL3	D33 D32	I²C Clock signal, of the 2-wire management interface used by 10GbE controller to access the management registers of an external Optical SFP+ module	I/O OD 3.3VSB	PU 2.2k 3.3VSB	
10G_PHY_RST_23	C34	Output signal that resets and Optical PHY on port 0 and port 1	O 3.3VSB		This signal is not used for Copper PHY
10G_PHY_CAP_23	D34	Phy mode capability pin: Indicates if the PHY for 10G lanes 0 and1 is capable of configuration by I2C. High indicates MDIO-only configuration, and low indicates configuration capability via I2C or MDIO. The actual protocol used for PHY configuration is determined by the module, in part based on this input. The actual protocol used is indicated over the dedicated I2C interface	I 3.3VSB	PU 10k 3.3VSB	Default state is MDIO mode. For I²C mode pull down with 1K on carrier

3.4.4. PCI Express

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_TX16+ PCIE_TX16-	D52 D53	PCI Express channel 16, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX16+ PCIE_RX16-	C52 C53	PCI Express channel 16, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX17+ PCIE_TX17-	D55 D56	PCI Express channel 17, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX17+ PCIE_RX17-	C55 C56	PCI Express channel 17, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX18+ PCIE_TX18-	D58 D59	PCI Express channel 18, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX18+ PCIE_RX18-	C58 C59	PCI Express channel 18, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX19+ PCIE_TX19-	D61 D62	PCI Express channel 19, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX19+ PCIE_RX19-	C61 C62	PCI Express channel 19, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX20+ PCIE_TX20-	D65 D66	PCI Express channel 20, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX20+ PCIE_RX20-	C65 C66	PCI Express channel 20, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX21+ PCIE_TX21-	D68 D69	PCI Express channel 21, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX21+ PCIE_RX21-	C68 C69	PCI Express channel 21, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX22+ PCIE_TX22-	D71 D72	PCI Express channel 22, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX22+ PCIE_RX22-	C71 C72	PCI Express channel 22, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX23+ PCIE_TX23-	D74 D75	PCI Express channel 23, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX23+ PCIE_RX23-	C74 C75	PCI Express channel 23, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX24+ PCIE_TX24-	D78 D79	PCI Express channel 24, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX24+ PCIE_RX24-	C78 C79	PCI Express channel 24, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX25+ PCIE_TX25-	D81 D82	PCI Express channel 25, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX25+ PCIE_RX25-	C81 C82	PCI Express channel 25, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX26+ PCIE_TX26-	D85 D86	PCI Express channel 26, Transmit Output differential pair.	O PCIE		Not supported

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_RX26+ PCIE_RX26-	C85 C86	PCI Express channel 26, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX27+ PCIE_TX27-	D88 D89	PCI Express channel 27, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX27+ PCIE_RX27-	C88 C89	PCI Express channel 27, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX28+ PCIE_TX28-	D91 D92	PCI Express channel 28, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX28+ PCIE_RX28-	C91 C92	PCI Express channel 28, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX29+ PCIE_TX29-	D94 D95	PCI Express channel 29, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX29+ PCIE_RX29-	C94 C95	PCI Express channel 29, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX30+ PCIE_TX30-	D98 D99	PCI Express channel 30, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX30+ PCIE_RX30-	C98 C99	PCI Express channel 30, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX31+ PCIE_TX31-	D101 D102	PCI Express channel 31, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX31+ PCIE_RX31-	C101 C102	PCI Express channel 31, Receive Input differential pair.	I PCIE		Not supported

3.4.5. Module Type Definition

Signal	Pin	Description	I/O	Comment
TYPE0# TYPE1# TYPE2# TYPE7#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1, these pins are don't care (X). TYPE2# TYPE1# TYPE0# X X X Pinout Type 1 NC NC NC Pinout Type 2 NC NC GND Pinout Type 3 (no IDE) NC GND NC Pinout Type 4 (no PCI) NC GND GND Pinout Type 5 (no IDE, no PCI) GND NC NC Pinout Type 6 (no IDE, no PCI) **GND NC GND Pinout Type 7 (server level with 10GbE)** The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.		Type 7

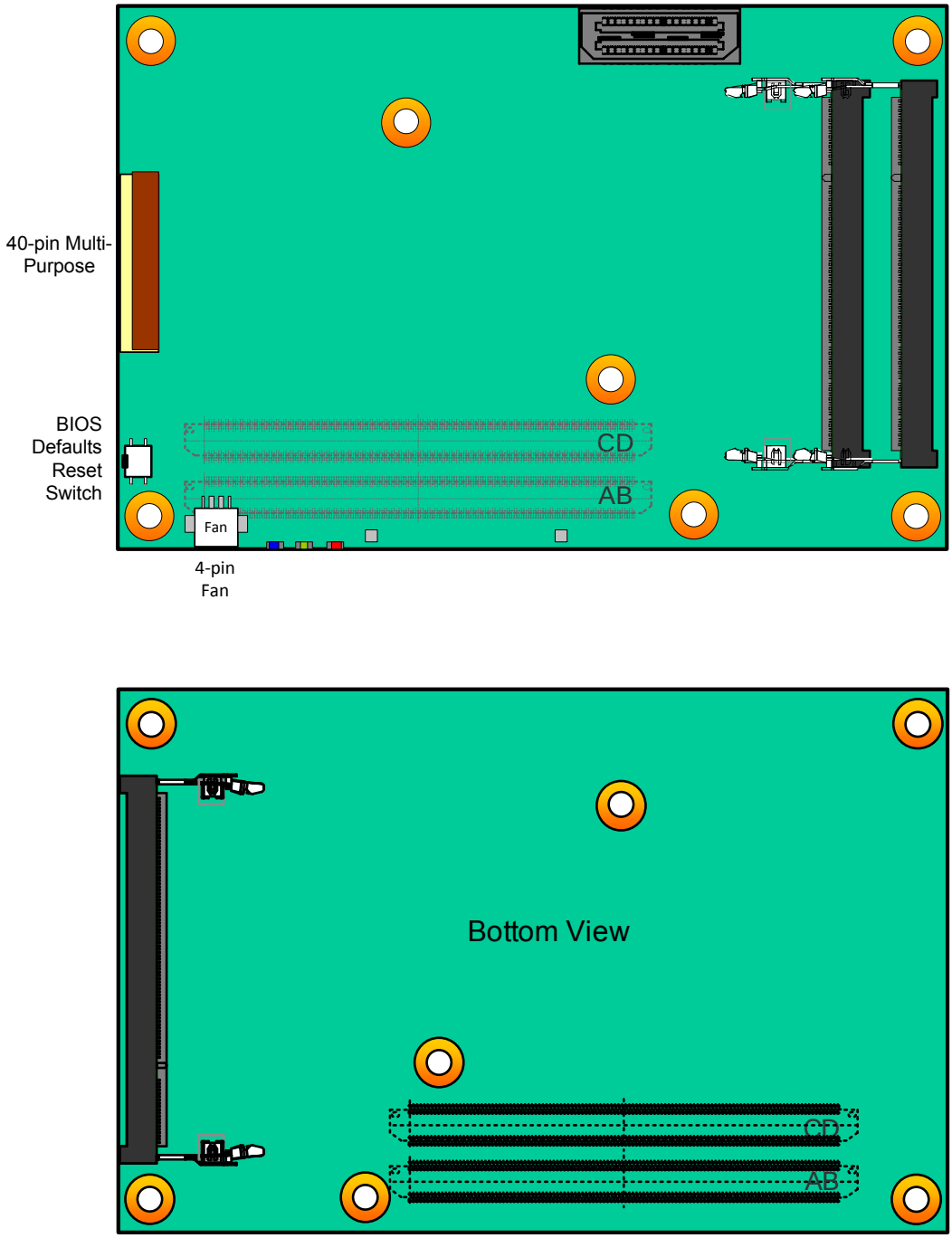
3.4.6. Power and Ground

Signal	Pin	Description	I/O	PU/PD	Comment
VCC_12V	C104-C109 D104-D109	Primary power input: +12V nominal (wide range 5-20V). All available VCC_12V pins on the connector(s) shall be used	P		8.5-20V
GND	C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70, C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73 D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane.	P		

4. Connector Pinouts on Module

This chapter describes connectors and pinouts, LEDs and switches that are used on the module but are not included in the PICMG standard specification

4.1. Connector, Switch and LED Locations



Note: 3rd SODIMM is located on back-side of module (supported by build option).

Figure 3: Express-DN7 Connector, Switch and LED Locations

COM Express module and the DB40 Debug Module

For illustration purposes only

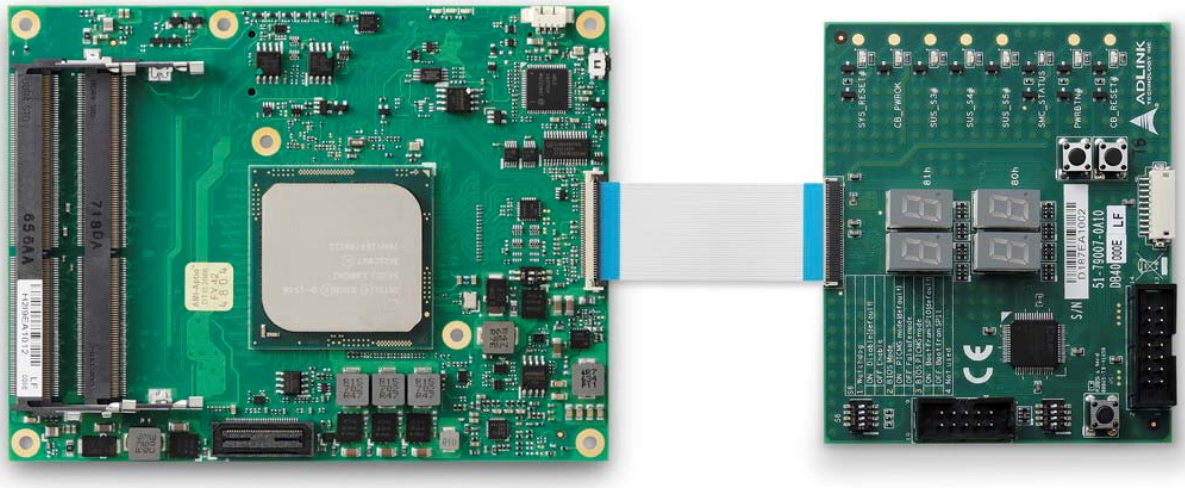


Figure 4: COM Express module and the DB40 Debug Module

4.2. 40-pin Debug Connector

FPC Connector Type: Molex 502790-4091

Pin Orientation

1 40

40-pin Debug Connector Pin Definition on the COM Express Module

Pin	Interface	Signal	Remark
40	SPI Program interface	VCC_SPI_IN	
39		GND	
38		SPI_BIOS_CS0#	
37		SPI_BIOS_CS1#	PU 10k 3.3VSB
36		SPI_BIOS_MISO	
35		SPI_BIOS_MOSI	
34		SPI_BIOS_CLK	
33	LPC Bus	3V3_LPC	
32		GND	
31		BIOS_DIS0	PU 10k 3.3VSB
30		RST#	
29		CLK33_LPC	
28		LPC_FRAME#	
27		LPC_AD3	
26		LPC_AD2	
25		LPC_AD1	
24		LPC_AD0	
23	BMC Program interface	3.3V_BMC	
22		3.3VSB	
21		GND	

Pin	Interface	Signal	Remark
20	BMC Program interface (cont'd)	TXD6	
19		RXD6	
18		FUMD0	
17		RESET_IN#	PU 10k 3.3VSB
16		DATA	PU 2.2k 3.3VSB Equivalent
15		CLK	PU 2.2k 3.3VSB Equivalent
14		OCD0A	
13		OCD0B	
12	Test points	PWRBTN#	PU 10k 3.3VSB
11		SYS_RESET#	PU 10k 3.3VSB
10		CB_RESET#	PU 1k 3.3VSB
9		CB_PWROK	
8		SUS_S3#	
7		SUS_S4#	
6		SUS_S5#	
5	BMC Debug signals	POSTWDT_DIS#	PU 100k 3.3VSB
4		SEL_BIOS	
3		BIOS_MODE	
2		BMC_STATUS	
1	Reserved		Tied to GND through 0ohm resistor

Table 2: 40-pin Debug Connector Pin Definition

Note: The pin definition on the debug module is the inverse of that on the COM Express module.

4.3. Status LEDs

To facilitate easier maintenance, status LED's are mounted on the board.

LED1 LED2 LED3

LED Descriptions

Name	Color	Connection	Function
LED1	Blue	BMC output	Power Sequence Status Code (BMC) Power Changes, RESET (see 5.1.4 Exception Codes below)
LED2	Green	Power Source 3Vcc	S0 LED ON S3/S4/S5 LED OFF ECO mode LED OFF
LED3	Red	BMC output and same signal as WDT (B27) on BtB connector	Module power up LED OFF Watchdog counting Keep last state Watchdog timed out LED ON Watchdog RESET LED ON Rebooted after WD RESET LED ON Rebooted after PWRBTN LED OFF Rebooted after RESET BTN LED OFF Note: only a RESET not initiated by the BMC can clear the WD LED (user action)

Table 3: Express-DN7 LED Descriptions

4.4. MIPI60 Debug Header

Not all pins of the Intel MIPI60 connector are connected to the CombiProbe Intel x86/x64 MIPI-C.

Pin	Signal
1	VREF_DEBUG
3	TCK0
5	TDI
7	Reset In
9	TRST_N
11	PRDY_N
13	PTI_0_CLK
15	GND
17	No Connect
19	PTI_0_DATA[0]
21	PTI_0_DATA[1]
23	PTI_0_DATA[2]
25	PTI_0_DATA[3]
27	PTI_0_DATA[4]
29	PTI_0_DATA[5]
31	PTI_0_DATA[6]
33	PTI_0_DATA[7]
35	No Connect
37	No Connect
39	No Connect
41	No Connect
43	No Connect
45	No Connect
47	No Connect
49	No Connect
51	No Connect
53	No Connect
55	No Connect
57	GND
59	No Connect

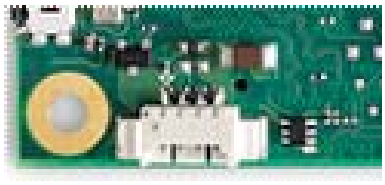
Pin	XDP Signal
2	TMS
4	TDO
6	Open Drain Reset Out
8	No Connect
10	PREQ_N
12	VREF_TRACE
14	PTI_1_CLK
16	GND
18	PTI_1_DATA[0]
20	PTI_1_DATA[1]
22	PTI_1_DATA[2]
24	PTI_1_DATA[3]
26	No Connect
28	No Connect
30	No Connect
32	No Connect
34	Reset Out
36	Boot Stall
38	CPU Boot Stall
40	Power Button
42	PWRGOOD
44	No Connect
46	No Connect
48	I2C_SCL
50	I2C_SDA
52	No Connect
54	DBG_UART_TX
56	DBG_UART_RX
58	GND
60	No Connect

Table 4: MIPI60 Debug Header Pin Definition

4.5. Fan Connector

Connector Type: JVE 24W1125A-04M00

Pin Orientation



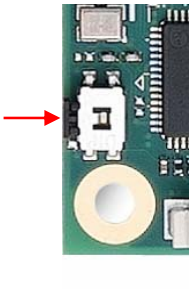
1 2 3 4

Pin Assignment

Name	Signal
1	FAN_PWMOUT
2	FAN_TACHIN
3	Ground
4	5V

Table 5: Fan Connector Pin Definition

4.6. BIOS Setup Defaults Reset Button



To perform a hardware reset of BIOS default settings, perform the following steps:

1. Shut down the system.
2. Hold down the BIOS Setup Defaults Reset Button and boot up the system. You can release the button when the BIOS prompt screen appears
3. The BIOS prompt screen will display a confirmation that BIOS defaults have been reset and request that you reboot the system.

4.7. Switch Settings

Switch Locations

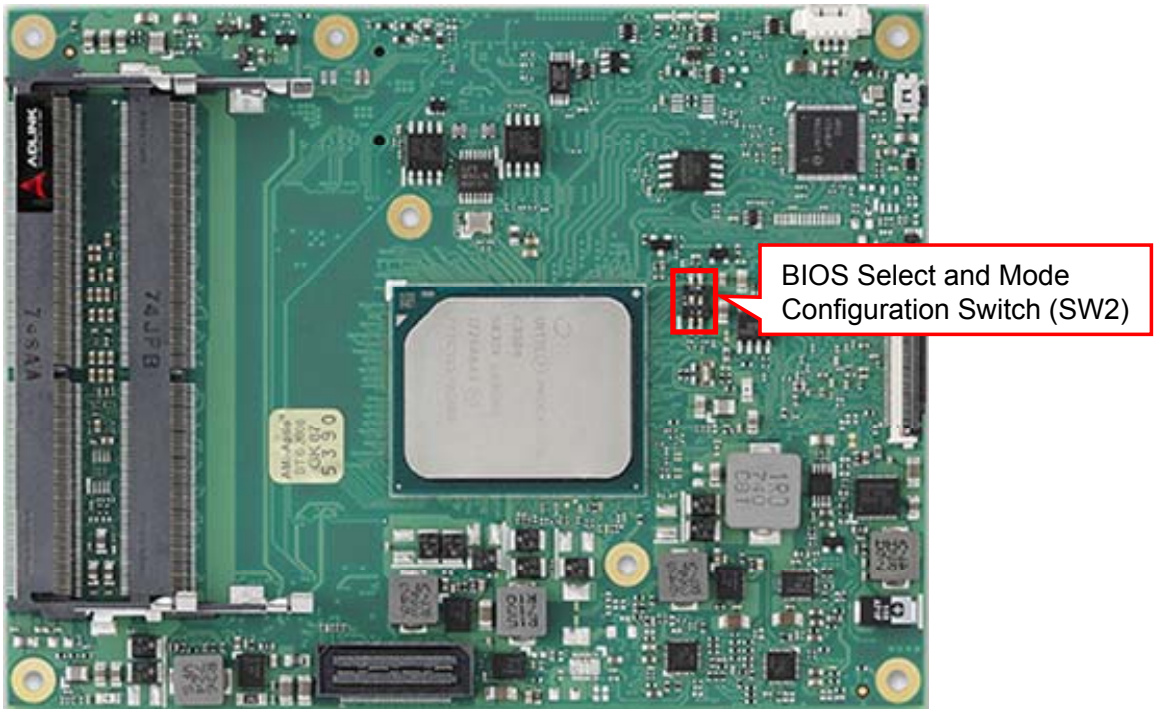


Figure 5: Express-DN7 Switch Locations

BIOS Select and Mode Configuration Switch

The module has two BIOS chips and BIOS operation can be configured to "PICMG" and dual-BIOS "Failsafe" modes using the BIOS Select and Mode Configuration Switch (SW2), Pin 2.

Setting the module to PICMG mode will configure the BIOS chips on the module as SPI0 and SPI1. In PICMG mode, a BIOS chip cannot be placed in the SPI0 slot on the carrier.

In dual-BIOS Failsafe mode, both BIOS chips on the module are configured as SPI1. Only one of the two is connected to the SPI bus at any given time. In case of failure of the primary SPI1 BIOS, the system will reboot and switch to the secondary SPI1 BIOS on the module. In Failsafe mode, the SPI0 BIOS socket on the carrier can be populated.

In either mode, Pin 1 is used to select whether to boot from SPI0 or SPI1.

Mode	Pin 1	Pin 2
Boot from SPI0 (default)	On	—
Boot from SPI1	Off	—
Set BIOS to PICMG mode	—	On
Set BIOS to Failsafe BIOS mode (default)	—	Off

Table 6: BIOS Select and Mode Configuration Switch Settings

4.8. PCIe x8-to-two-x4 Adapter Card

The Express-DN7 can be used with the PCIe x8-to-two-x4 Adapter Card on the Express-BASE7 Reference Carrier to support bifurbication of the PCIe x8 interface. The card reroutes the PCIe x8 to two x4 and allows testing of two independent PCIe add-on cards with x4/x2/x1 width. To use the card, set **BIOS > Chipset > IIO Configuration > IIO0 Configuration > IOU2 (IIO PCIe Port 1)** to "x4x4 ".

PCIex8-to-two-x4 Adapter Card
(Model: P8TO24, Part No.:)

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5. Smart Embedded Management Agent (SEMA)

The onboard microcontroller (BMC) implements power sequencing and Smart Embedded Management Agent (SEMA) functionality. The microcontroller communicates via the System Management Bus with the CPU/chipset. The following functions are implemented:

- Total operating hours counter. Counts the number of hours the module has been run in minutes.
- On-time minutes counter. Counts the seconds since last system start.
- Temperature monitoring of CPU and board temperature. Minimum and maximum temperature values of CPU and board are stored in flash.
- Power cycles counter
- Boot counter. Counts the number of boot attempts.
- Watchdog Timer. Set/Reset/Disable Watchdog Timer. Features auto-reload at power-up.
- System Restart Cause. Power loss/BIOS Fail/Watchdog/Internal Reset/External Reset
- Fail-safe BIOS support. In case of a boot failure, hardware signals tells external logic to boot from fail-safe BIOS.
- Flash area. 1kB Flash area for customer data
- 2K Bytes Protected Flash area. Keys, IDs, etc. can be stored in a write- and clear-protectable region.
- Board Identify. Vendor/Board/Serial number/Production Date
- Main-current & voltage. Monitors drawn current and main voltages

For a detailed description of SEMA features and functionality, please refer to **SEMA Technical Manual** and **SEMA Software Manual**, downloadable at: **http://www.adlinktech.com/sema/**.

5.1. Board Specific SEMA Functions (update later)

Note: To be confirmed.

5.1.1. Voltages

The BMC of the Express-DN7 implements a voltage monitor and samples several onboard voltages. The voltages can be read by calling the SEMA function “Get Voltages”. The function returns a 16-bit value divided into high-byte (MSB) and low-byte (LSB).

ADC Channel	Voltage Name	Voltage Formula [V]
0	VCORE	(MSB<<8 + LSB) x 1.0 x 3.3 / 1024
1	VMEM	(MSB<<8 + LSB) x 1.0 x 3.3 / 1024
2	RTC	(MSB<<8 + LSB) x 1.0 x 3.3 / 1024
3	3.3V	(MSB<<8 + LSB) x 1.1 x 3.3 / 1024
4	5VSB	(MSB<<8 + LSB) x 1.826 x 3.3 / 1024
5	VIN	(MSB<<8 + LSB) x 3.7 x 3.3 / 1024
6	3.3VSB	(MSB<<8 + LSB) x 1.1 x 3.3 / 1024
7	5V	(MSB<<8 + LSB) x 1.826 x 3.3 / 1024

Table 7: SEMA Onboard Voltage Monitor

5.1.2. Main Current

The BMC of the Express-DN7 implements a current monitor. The current can be read by calling the SEMA function “Get Main Current”. The function returns four 16-bit values divided in high-byte (MSB) and low-byte (LSB). These 4 values represent the last 4 currents drawn by the board. The values are sampled every 250ms. The order of the 4 values is NOT in chronological order. Access by the BMC may increase the drawn current of the whole system. In this case, there are still 3 samples not influenced by the read access.

Main Current = (MSB_n<<8 + LSB_n) x 8.06mA

5.1.3. BMC Status

This register shows the status of BMC controlled signals on the Express-DN7.

Status Bit	Signal
0	WDT_OUT
1	Reserved
2	Reserved
3	BIOS_MODE
4	POSTWDT_DISn
5	SEL_BIOS
6	BIOS_DIS0n
7	BIOS_DIS1n

Table 8: SEMA BMC Status

5.1.4. Exception Codes

In case of an error, the BMC drives a blinking code on the blue Status LED (LED1). The same error code is also reported by the BMC Flags register. The Exception Code is not stored in the Flash Storage and is cleared when the power is removed. Therefore, a “Clear Exception Code” command is not needed or supported.

Exception Code	Error Message
0	NOERROR
2	NO_SUSCLK
3	NO_SLP_S45
4	NO_SLP_S3
5	RESET_FAIL
6	BIOS_FAIL
7	NO_CB_PWROK
8	POWER_FAIL
9	VOLTAGE_FAIL
10	NO_VCC_CORE
11	NO_VDDQ
12	NO_VRTC
13	NO_V3P3_S
14	NO_V5VSB
15	NO_V12
16	NO_V3P3_A
17	NO_V5V_S
18	NO_P_5V_3P3_PG
19	NO_5V_PG
20	NO_VCCRAM_PG
21	NO_VNN_PG
22	NO_V5_DUAL
23	NO_V1P8_A_PG
24	NO_V1P05_A_PG
25	NO_ALL_SYS_PG
26	CRITICAL_TEMP
27	RESETIN_FAIL

Table 9: SEMA Exception Codes

5.1.5. BMC Flags

The BMC Flags register returns the last detected Exception Code since power-up and shows the BIOS in use and the power mode.

Bit	Description
[0 ~ 4]	Exception Code
[6]	0 = AT mode 1 = ATX mode
[7]	0 = Standard BIOS 1 = Fail-safe BIOS.

Table 10: SEMA BMC Flags

6. System Resources

6.1. System Memory Map

Memory Range	Target
0000 0000h – 000D FFFFh 0010 0000h – TOM (Top of Memory)	Main Memory
000E 0000h – 000F FFFFh	Motherboard resources
FEC0 0000h-FEC0 0fffh	IO(x) APIC
FED0 0000 – FED0 03FF	HPET
FF00 0000 h – FFFF FFFFh	IFAW (BIOS)

6.2. Direct Memory Access Channels

Channel Number	Data Width	System Resource
0	8-bits	Generic
1	8-bits	Generic
2	8-bits	Generic
3	8-bits	Generic
4		Reserved - cascade channel
5	16-bits	Generic
6	16-bits	Generic
7	16-bits	Generic

6.3. Fixed I/O Address Range Map

Hex Range	Device
020-021	Interrupt Controller
024-025	Interrupt Controller
028-029	Interrupt Controller
02C-02D	Interrupt Controller
02E-02F	LPC SIO
030-031	Interrupt Controller
034-035	Interrupt Controller
038-039	Interrupt Controller
03C-03D	Interrupt Controller
040-042	Timer/Counter
043	Timer/Counter
04E-04F	LPC SIO

Hex Range	Device
050-052	Timer/Counter
053	Timer/Counter
060	Microcontroller
061	NMI Controller
062	Microcontroller
064	Microcontroller
066	Microcontroller
070-077	RTC
080 081-083 084-086 087 088 089-08B 08C-08E 08F	DMA Controller and LPC,PCI,or PCIE
090-091	DMA Controller
093-09F	DMA Controller
092	Reset Generator
0A0-0A1 0A4-0A5 0A8-0A9 0AC-0AD	Interrupt Controller
0B0-0B1 0B4-0B5 0B8-0B9 0BC-0BD	Interrupt Controller
0B2-0B3	Power Management
0C0-0D1 0D2-0DD 0DE-0DF	DMA Controller
0F0	FERR# / Interrupt Controller
240-247	COM3
248-24F	COM4
2F8-2FF	COM2
3F8-3FF	COM1
4D0-4D1	Interrupt Controller
CA0-CB0	IPMI Usage
CF9	Reset Generator

6.4. Variable I/O Address Range Map

Hex Range	Device
Anywhere in 64 KB I/O Space	ACPI
Anywhere in 64 KB I/O Space	SATA Index/Data Pair
Anywhere in 64 KB I/O Space	SMBus
96 Bytes above ACPI Base	TCO
Anywhere in 64 KB I/O Space	GPIO
8 Ranges in 64 KB I/O Space	Serial Port 1
8 Ranges in 64 KB I/O Space	Serial Port 2
Anywhere in 64 KB I/O Space	LAN
Anywhere in 64 KB I/O Space	LPC Generic 1
Anywhere in 64 KB I/O Space	LPC Generic 2
Anywhere in 64 KB I/O Space	LPC Generic 3
Anywhere in 64 KB I/O Space	LPC Generic 4
Anywhere in 64 KB I/O Space	I/O Trapping Ranges

6.5. APIC Interrupt Mapping

IRQ#	Typical Intterupt Resource	Using SERIRQ
0	Cascade from 8259 #1	No
1		Yes
2	8254 Counter 0,HPET #0(Legacy mode)	No
3	COM2	Yes
4	COM1	Yes
5	COM3	Yes
6		Yes
7	COM4	Yes
8	RTC,HPET #1(Legacy mode)	No
9	Option for SCI,TCO	Yes
10	Option for SCI,TCO	Yes
11	HPET #2,Option for SCI,TCO	Yes
12		Yes
13	FERR# logic	No
14		
15		
16	Internal devices are routable.	PIRQA#
17	Internal devices are routable.	PIRQB#
18	Internal devices are routable.	PIRQC#

IRQ#	Typical Intterupt Resource	Using SERIRQ
19	Internal devices are routable.	PIRQD#
20	Option for SCI,TCO,HPET #0,1,2,3.Other internal device are routable.	N/A
21	Option for SCI,TCO,HPET #0,1,2,3.Other internal device are routable.	N/A
22	Option for SCI,TCO,HPET #0,1,2,3.Other internal device are routable.	N/A
23	Option for SCI,TCO,HPET #0,1,2,3.Other internal device are routable.	N/A

6.6. PCI Configuration Space Map

Bus Number	Device Number	Function Number	Description
00h	00h	00h	System Agent
00h	04h	00h	Global and Local Error Registers (GLMREG)
00h	05h	00h	Root Complex Event Collector
00h	06h	00h	RP - Intel® QuickAssist Technology
00h	09h~0Ch,0Eh~11h	00h	PCI Express Root Ports
00h	13h	00h	SATA Controllers
00h	15h	00h	USB Combo Controller
00h	18h	00h	System Management
00h	1Ah	00h	HSUART Controller
00h	1Bh	00h	Innovation Engine
00h	1Ch	00h	eMMC Controller
00h	1Fh	00h	LPC Controller
00h	1Fh	01h	Primary to Side Band Bridge
00h	1FH	02H	Power Management Controller
00h	1Fh	04h	SMBus - Legacy
00h	1Fh	05h	SPI Controller

6.7. PCI Interrupt Routing Map

INT Line	xHCI Controller	PCIE Port1	PCIE Port 2	PCIE Port 3	PCIE Port 4	PCIE Port 5	PCIE Port 6
Int0	INTD:19	INTA:16	INTB:17	INTC:18	INTD:19	INTE:20	INTH:23
Int1		INTB:17	INTC:18	INTD:19	INTA:16	INTF:21	INTE:20
Int2		INTC:18	INTD:19	INTA:16	INTB:17	INTG:22	INTF:21
Int3		INTD:19	INTA:16	INTB:17	INTC:18	INTH:23	INTG:22

INT Line	PCIE Port 7	PCIE Port 8	SATA Controller	SMBus Controller
Int0	INTG:22	INTH:23	INTE:20	
Int1	INTH:23	INTE:20		
Int2	INTE:20	INTF:21		INTH:23
Int3	INTF:21	INTG:22		

6.8. SMBus Address Table

Device	Address
BMC	50h
Extend GPIO	40h

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7. BIOS Setup

7.1. Menu Structure

This section presents the six primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. The subsections in this section describe the Submenus and setting options for each menu item. The default setting options are presented in **bold**, and the function of each setting is described in the right hand column of the respective table.

Main	IntelRCSetup	Advanced	Event Logs	Security	Boot	Save & Exit
BIOS Information System Information Board Information System Date and Time Access Level	Platform RC Revision Processor BSP Revision Microcode Revision Processor Configuration ► CPU Thermal Configuration ► CK420 Configuration ► Server ME Configuration ► Server ME Configuration ► System Event Log ► North Bridge Chipset Configuration ► South Bridge Chipset Configuration ►	Power Management ► System Management ► Thermal Management ► Watchdog Timer ► CSM Configuration ► Super IO Configuration ► Serial Console Redirection ► USB Configuration ► Network Stack Configuration ► Miscellaneous ► Driver Health ► Trusted Computing ►	Change SMBIOS Event Log Settings ► Vies SMBIOS Event Log ►	Setup Administrator Password ► User Password Secure Boot ►	Boot Configuration ► FIXED BOOT ORDER Priorities ► UEFI USB Key Drive BBS Priorities ►	Save Change and Exit ► Discard Changes and Exit ► Save Changes and Reset ► Discard Changes and Reset ► Save Options Boot Override ►

Notes:

► indicates a Submenu
Gray text indicates info only

7.2. Main

The Main Menu provides read-only information about your system and also allows you to set the System Date and Time. Refer to the tables below for details of the settings.

7.2.1. Main > BIOS Information

Feature	Options	Description
BIOS Vender	Info only	American Megatrends
BIOS Version	Info only	ADLINK BIOS version
Build Date	Info only	ADLINK BIOS Build Date
SPS Firmware Version	Info only	Display SPS Firmware Version

7.2.2. Main > System Information

Feature	Options	Description
Project Name	Info only	Display Project Name.
Hardware version	Info only	Display CPU Board Version.
CPU Brand String	Info only	Display CPU Board String.
CPU Frequency	Info only	Display CPU Frequency.
Total Memory	Info only	Display Installed Memory Size.
SOC SKU	Info only	

7.2.3. Main > Board Information

Feature	Options	Description
Board Information	Submenu	
Board Information	Info only	
Serial Number	Info only	Display SEMA serial Number.
Manufacturing Date	Info only	Display SEMA manufacturing date.
Last Repair Date	Info only	Display SEMA last repair date.
MAC ID	Info only	Display SEMA MAC ID.
Runtime Statistics	Info only	
Total Runtime	Info only	The returned value specifies the total time in minutes the system is running in S0 state.
Current Runtime	Info only	The returned value specifies the time in seconds the system is running in S0 state. This counter is cleared when the system is removed from the external power supply.
Power Cycles	Info only	The returned value specifies the number of times the external power supply has been shut down
Boot Cycles	Info only	The Boot counter is increased after a HW- or SW-Reset or after a successful power-up.
Boot Reason	Info only	The boot reason is the event which causes the reboot of the system.

7.2.4. Main >System Date/Time

Feature	Options	Description
System Date	Info only	
System Time	Info only	

7.2.5. Main >Access Level

Feature	Options	Description
Access Level	Info only	

7.3. IntelRCSetup

7.3.1. IntelRCSetup >Processor Configuration

Feature	Options	Description
Processor Configuration	Info only	
EIST (GV3)	Disabled **Enabled**	Enable/Disable EIST. GV3 and TM1 must be enabled for TM2 to be available. GV3 must be enabled for Turbo. Auto-Enable for B0 CPU stepping, all others disabled, change setting to override.
BIOS Request Frequency	Disabled **Enabled**	Two modes: Min Frequency and Max Frequency (the CPU will be instructed to provide the highest possible legal frequency to the processor).
Turbo	Disabled **Enabled**	Enable or Disable CPU Turbo capability. This option only applies to ES2 and above.
TM1	Disabled **Enabled**	Enable/Disable TM1. TM1 and GV3 must be enabled in order to support TM2
TM2 Mode	LFM Throttling **Adaptive Throttling**	Select LFM throttling or adaptive throttling for TM2 mechanisms.
Dynamic Self Refresh	Disabled **Enabled**	Enable or Disable dynamic self refresh in memory controller
PMOP Levels	Slow **Fast**	Power Mode Opcode during Self Refresh Slow/Fast
CPU C State	Disabled **Enabled**	Enables the Enhanced Cx state of the CPU, takes effect after reboot. Auto - Enable for B0 CPU stepping, all others disabled, change setting to override.
Package C State limit	No Pkg C-State No S0Ix **No Limit**	No Package C State limit
Max Core C-State	C1 **C6**	Options are: C1 and C6.
Enhanced Halt State (C1E)	Disabled **Enabled**	Enables the Enhanced C1E state of the CPU, takes effect after reboot.
Monitor/Mwait	Disabled **Enabled**	Enable or Disable the Monitor/Mwait instruction
L1 Prefetcher	Disabled **Enabled**	Enable/Disable L1 Prefetch
L2 Prefetcher	Disabled **Enabled**	Enable/Disable L2 Prefetch
ACPI 3.0 T-States	Disabled **Enabled**	Enable/Disable ACPI 3.0 T-States.
Fast String	Disabled **Enabled**	When enabled, enables fast strings for REP MOVS/STOS
Machine Check	Disabled **Enabled**	Enable or Disable the Machine Check
Max CPUID Value Limit	**Disabled** Enabled	This should be enabled in order to boot legacy OSes that cannot support CPUs with extended CPUID functions.
Execute Disable Bit	Disabled **Enabled**	When disabled, forces the XD feature flag to always return 0.

Feature	Options	Description
vmx	Disabled **Enabled**	Enables the Vanderpool Technology, takes effect after reboot.
BIST Selection	**Disabled** Enabled	Enables BIST, takes effect after reboot.
Extended APIC	**Info only**	
MSR 606 PKG_POWER_SKU_UNIT	**Info only**	
Lock PACKAGE_RAPL_LIMIT	**Disabled** Enabled	Allows the user to lock the MSR 0x610 (PACKAGE_RAPL_LIMIT) by setting the lock bit
PL1 Time Window	**45**	Defines RAPL time window 1 in miliseconds
PL1 Power Level	**25**	Defines RAPL power limit 1 in Watts
PL2 Power Level	**29**	Defines RAPL power limit 2 in Watts
Active Processor Cores	**0**	Set the number of Active Processor Cores in the SoC. A 0 indicates all Existing Processor Cores are Active.
Dump Crash Log	**Disabled** Enabled	Enable Dump Crash Lo
CPU Flex Ratio Override	**Disabled** Enabled	Enable/Disable CPU Flex Ratio Programming
CPU Core Ratio	**Info only**	
Ratio Limits	**Disabled** Enabled	Enable/Disable the configuration of the ratio limits MSRs
Ratio Limits Configuration	Submenu	
Processor DFX Configuration	Submenu	

7.3.1.1. IntelRCSetup >Processor Configuration >Ratio Limits Configuration

Feature	Options	Description
Ratio Limits Configuration	Info only	
Ratio Limit 0	0	The frequency limit corresponding to the maximum number of active cores specified in CORE_COUNT_0 in FREQ_LIMIT_CORES.
Ratio Limit 1	0	The frequency limit corresponding to the maximum number of active cores specified in CORE_COUNT_1 in FREQ_LIMIT_CORES.
Ratio Limit 2	0	The frequency limit corresponding to the maximum number of active cores specified in CORE_COUNT_2 in FREQ_LIMIT_CORES.
Ratio Limit 3	0	The frequency limit corresponding to the maximum number of active cores specified in CORE_COUNT_3 in FREQ_LIMIT_CORES.
Ratio Limit 4	0	The frequency limit corresponding to the maximum number of active cores specified in CORE_COUNT_4 in FREQ_LIMIT_CORES.
Ratio Limit 5	0	The frequency limit corresponding to the maximum number of active cores specified in CORE_COUNT_5 in FREQ_LIMIT_CORES.
Ratio Limit 6	0	The frequency limit corresponding to the maximum number of active cores specified in CORE_COUNT_6 in FREQ_LIMIT_CORES.
Ratio Limit 7	0	The frequency limit corresponding to the maximum number of active cores specified in CORE_COUNT_7 in FREQ_LIMIT_CORES.
Core Count 0	0	The number of maximum active cores corresponding to the frequency limit specified in RATIO_LIMIT_0 in FREQ_LIMIT_RATIOS.
Core Count 1	0	The number of maximum active cores corresponding to the frequency limit specified in RATIO_LIMIT_1 in FREQ_LIMIT_RATIOS.
Core Count 2	0	The number of maximum active cores corresponding to the frequency limit specified in RATIO_LIMIT_2 in FREQ_LIMIT_RATIOS.
Core Count 3	0	The number of maximum active cores corresponding to the frequency limit specified in RATIO_LIMIT_3 in FREQ_LIMIT_RATIOS.
Core Count 4	0	The number of maximum active cores corresponding to the frequency limit specified in RATIO_LIMIT_4 in FREQ_LIMIT_RATIOS.
Core Count 5	0	The number of maximum active cores corresponding to the frequency limit specified in RATIO_LIMIT_5 in FREQ_LIMIT_RATIOS.
Core Count 6	0	The number of maximum active cores corresponding to the frequency limit specified in RATIO_LIMIT_6 in FREQ_LIMIT_RATIOS.
Core Count 7	0	The number of maximum active cores corresponding to the frequency limit specified in RATIO_LIMIT_7 in FREQ_LIMIT_RATIOS.

7.3.1.2. IntelRCSetup >Processor Configuration >Processor DFX Configuration

Feature	Options	Description
Processor DFX Configuration	Info only	
Energy Performance Bias	Performance **Balanced Performance** Balanced Efficiency Energy Efficient	Selects the energy efficiency policies used in making turbo decision by the CPU. The energy policy controls turbo performance vs. power.
Lock PL3_CONTROL	**Disabled** Enabled	Allows the user to lock the MSR 0x615 (PACKAGE_RAPL_LIMIT) by setting the lock bit
PL3 Time Window	2ms 4ms **8ms** 16ms	Defines RAPL time window 3 in miliseconds
PL3 Enable	Disabled **Enabled**	Enable/Disable PL3 Algorithm
PL3 Power Level	0	Defines RAPL power limit 3 in Watts
PL3 Duty Cycle Percentage	25	Power limit excursion duty cycle control for PL3, describing what percentage of time it is allowed for the SOC to exceed the programmed PL3 power limit. This is expressed as a percentage
PMAX Power	0	The SOC guarantees it will never exceed this power limit even for very short time windows
Self Refresh Delay	30	Configures self refresh delay in microseconds. DDR-1600 up to 1300us, DDR-1867 up to 1100us, DDR-2133 up to 950us, DDR-2400 up to 850us, DDR-2666 up to 750us.

7.3.2. IntelRCSetup >CPU Thermal Configuration

Feature	Options	Description
CPU Thermal Configuration	Info only	
TJ Target	0	Offset below TJMAX to set as the PROCHOT# activation temperature. Valid range 0C to 63C.
Tcontrol Offset	0	Offset to modify Tcontrol for DTS2.0. Valid range 0C to 63C.
Tcontrol Offset Sign	**Positive** Negative	To select the the sign for the Tcontrol Offset value
TM1	Disabled **Enabled**	Enable/Disable TM1. TM1 and GV3 must be enabled in order to support TM2
TM2 Status	Info only	
TM2 Mode	LFM Throttling **Adaptive Throttling**	Select LFM throttling or adaptive throttling for TM2 mechanisms.
CPU DFX Thermal Configuration	Submenu	

7.3.3. IntelRCSetup >CPU Thermal Configuration >CPU DFX Thermal Configuration

Feature	Options	Description
CPU DFX Thermal Configuration	Info only	
Out of Spec Interrupt	**Disabled** Enabled	Enables generation of a thermal interrupt whenever Out of Spec temperature threshold is crossed.
Low Temp Interrupt	**Disabled** Enabled	Trigger an interrupt when the temperature goes from HOT to NOT_HOT.
High Temp Interrupt	**Disabled** Enabled	Triggers an interrupt when the temperature goes from NOT_HOT to HOT.
Threshold 1 Rel Temp	**5**	Degrees below TJMAX to signal an interrupt whenever the temperature crosses this threshold. Range is 0C - 127C
Threshold 2 Rel Temp	**10**	Degrees below TJMAX to signal an interrupt whenever the temperature crosses this threshold. Range is 0C - 127C
Threshold 1 Interrupt	**Disabled** Enabled	Enables generation of a thermal interrupt whenever Threshold 1 is crossed.
Threshold 2 Interrupt	**Disabled** Enabled	Enables generation of a thermal interrupt whenever Threshold 2 is crossed.
External PROCHOT Interrupt	Disabled **Enabled**	Enables generation of an interrupt when an external device drives the PROCHOT# pin.
PROCHOT RESPONSE	**Disabled** Enabled	Prochot Configurable Response Enable. INTERNAL INTEL ONLY:Ucode will copy this value to/from PCU_CR_FIRM_CONFIG(12).
Prochot Output Mode Disable	Disabled **Enabled**	Prochot output disable. INTERNAL INTEL ONLY:Prochot output disable. Ucode will copy this value to/from PCU_CR_FIRM_CONFIG(11).
VR_THERM_ALERT_DISABLE	**Disabled** Enabled	When set to 1, disables the VR_THERMAL_ALERT signaling. INTERNAL INTEL ONLY:Disable SVID during bclk overclocking mode. This bit is a mirror of PCU_CR_FIRM_CONFIG(14).
Prochot Frequency Response	**Disabled** Enabled	Control the level of PROCHOT throttling.
LOCK_THERM_INT	**Disabled** Enabled	Ties thermal interrupts from both cores. If set then thermal interrupt on one core is routed to all cores.

7.3.4. IntelRCSetup >CK420 Configuration

Feature	Options	Description
CK420 Configuration	Info only	
CK420 Spread spectrum		Spread spectrum off/on

7.3.5. IntelRCSetup >Server ME Configuration

Feature	Options	Description
Server ME Configuration	Info only	
Altitude	80000000	The altitude of the platform location above the see level, expressed in meters. The hex number is decoded as 2's complement signed integer.\nProvide the 80000000 value if the altitude is unknown.
MCTP Bus Owner	0	MCTP bus owner location on PCIe: [15:8] bus, [7:3] device, [2:0] function. If all zeros sending bus owner is disabled.
ME Shutdown Message	**Disabled** Enabled	Enable/Disable sending ME_SHUTDOWN message to ME when launching operating system

7.3.6. IntelRCSetup >System Event Log

Feature	Options	Description
System Event Log	Info only	
System Errors	Disabled **Enabled**	System Error Enable/Disable/ Auto setup options. If Auto is selected the enabling or disbling of errors in the driver is skipped.
Memory Event Log	Submenu	
PCIe Event Log	Submenu	
Whea Settings	Submenu	

7.3.6.1. IntelRCSetup >System Event Log >Memory Event Log

Feature	Options	Description
Memory ELog Support	Disabled **Enabled**	Enable/Disable Memory Error logging support
Parity Check	Disabled **Enabled**	Enable/Disable Parity Check
Log Correctable Errors	Disabled **Enabled**	Enable/Disable Correctable Memory Error logging support
Log Un-Correctable Errors	Disabled **Enabled**	Enable/Disable Un-Correctable Memory Error logging support
Enable/Disable Error Cloaking	**Disabled** Enabled	Error Cloaking Feature to Hide CE Errors to O

7.3.6.2. IntelRCSetup >System Event Log >PCIe Event Log

Feature	Options	Description
PCIe Event Log	Info only	
PCIe ELog Support	Disabled **Enabled**	Enable/Disable PCIe Error logging support
Log Fatal Error	Disabled **Enabled**	Send system event Signal on Fatal error
Log Non-Fatal Error	Disabled **Enabled**	Send system event Signal on Non Fatal error
Log Correctable Error	Disabled **Enabled**	Send system event Signal on Correctable error
PCIe System Error	Disabled **Enabled**	Enable System Error reporting on all enumerated Root ports, bridges and devices
PCIe Parity Error	Disabled **Enabled**	Enable Parity Error reporting on all enumerated Root ports, bridges and devices

7.3.6.3. IntelRCSetup >System Event Log >Whea Settings

Feature	Options	Description
Whea Settings	Info only	
WHEA Support	Disabled **Enabled**	Enable/Disable WHEA ACPI support
WHEA Error Injection 5.0 Extension	Disabled **Enabled**	Whea EINJ ACPI 5.0 support for set error type with address and vendor extensions.
Whea Logging	Disabled **Enabled**	Enable/Disable Whea logging of errors.
WHEA PCIe Error Injection	Disabled **Enabled**	Enable/Disable WHEA PCIe Error Injection

7.3.6.4. IntelRCSetup >North Bridge Chipset Configuration

Feature	Options	Description
North Bridge Chipset Configuration	Info only	
Pass Gate Setup	Submenu	
Leaky Bucket Setup	Submenu	
NonVolatile Memory Setup	Submenu	
Fast Boot	Disabled **Enabled**	Enables/Disables fast boot which skips memory training and attempts to boot using last known good configuration.
Command Mode	**Default** 1N 2N	Set tCMD to Default, 1N or 2N
Smm Size (MB)	2 **4** 8 16	Specify the size of the SMM/TSEG region 1 MB aligned

Feature	Options	Description
Command Address Parity	Info only	
Memory Frequency	DDR-1600 DDR-1867 DDR-2133 **DDR-2400**	DDR memory frequency: DDR4 up to DDR-2666 . DDR3 up to DDR-1867
Enable 32 bit bus	**Disabled** Enabled	This enables 32 bit bus memory mode
TCL performance	Disabled **Enabled**	Enable TCL increase for performance
Enable Parallel Training	**Disabled** Enabled	Memory Training Algorithms will run in parallel
Memory Channels	**Dual Channel** Single Channel	DDR Memory Channels
MRC Debug Messages	Disabled Minimum **Medium** Maximum General options	Enable to display debug output in MRC
Memory Preservation	Disabled **Enabled**	Enables memory content preservation thru Warm Reset
Fine Ddr Voltag	100	Select between -100 to 100 mV in steps of 5mv. 0 -> -100mV :: 100 -> 0mV :: 200 -> 100mV
Read Per Bit Training	Disabled **Enabled**	Enables/Disables the Read Per Bit memory training
Write Per Bit Training	Disabled **Enabled**	Enables/Disables the Write Per Bit memory training
ECC Support	Disabled **Enabled**	Select to enable/disable ECC Support
Faulty Part Tracking	**Disabled** Enabled	Select to enable/disable faulty part tracking
On Correctable Faulty Part	**Halt** Continue	On Correctable Faulty DIMM issue (single bit) halt or continue
Patrol Scrub Enable	Disabled **Enabled**	Select to enable/disable Patrol Scrub Support
Patrol Scrub Period	1 hour 4 hours 10 hours 20 hours	Select the Patrol Scrub Period
Demand Scrub Enable	Disabled **Enabled**	Select to enable/disable Demand Scrub Support
AB Segments in DRAM	**Disabled** Enabled	When this bit is set reads and writes targeting AorB-segments are routed to DRAM
E Segment in DRAM	Disabled **Enabled**	When this bit is set reads and writes targeting E segment are routed to DRAM
F Segment in DRAM	Disabled **Enabled**	When this bit is set reads and writes targeting F segment are routed to DRAM
ZQ Calibration	Disabled **Enabled**	Enables ZQ Calibration.

Feature	Options	Description
Rank Margin Tool	**Disabled** Enabled	Enable Rank Margin Tool support
RMT CPGC exp_loop_cnt	**12**	Set the CPGC exp_loop_cnt field for MRC trainings 2^(exp_loop_cnt -1)
RMT CPGC num_bursts	**6**	Set the CPGC num_bursts field for RMT execution 2^(num_bursts -1)
Out of order memory processing	Disabled **Enabled**	Enables out of order memory processing, improving performance
Read Two Clock Preamble	**Disabled** Enabled	Enables Two Clock Preamble for Reads
Write Two Clock Preamble	**Disabled** Enabled	Enables Two Clock Preamble for Writes
Write Data Early Enable	**Disabled** Enabled	Enables Write Data Early
Out of order aging threshold	**8**	Specifies the number of requests that can be processed ahead of another request sitting in the In-Progress request queue before OOO is disabled
New request bypass	Disabled **Enabled**	Enables new memory requests to be processed immediately, skipping the In-Progress queue, if the queue is empty
Select Refresh Rate	**1x/2X** 1X/2X/4X	Disable, 1x, 2x or 4x options available
CKE Power Down	**Disabled** Active Power Down Precharge Power Down	Enables/Disables the CKE Power Down
RAPL Time Window	**0**	DRAM RAPL Time Window for PL1
RAPL Power Limit Enable	**Disabled** Enabled	DRAM RAPL Power Limit[1] Enable for DDR Domain
RAPL Power Limit	**2047875**	DRAM RAPL Power Limit[1] for DDR Domain specified in mWatts
LOCK MSR 618 DDR_RAPL_LIMIT	Disabled **Enabled**	Allows user to lock the corresponding MSRs by setting the lock bit
PMOP Value for PC0	**4**	Power Mode Opcode for PC0
PMOP Value for PCX	**7**	Power Mode Opcode for PCX
Open Page Policy Timer	**Disabled** Enabled	Set Page Closure Timer to Disabled / Immediate / 30-60 ns / 60-120ns / 120-240ns / 240-480ns / 480-960ns / 1-2us
Memory Thermal Throttling	**Auto** Disabled	Enable/Disable Memory Thermal Throttling Management mode
Thermal Throttling Type	**CLTT** OLTT	Select CLTT/OLTT mode
CLTT Mode	**Normal** Passthru	Select CLTT Normal/Passthru mode
High Temperature	**105**	Set temperature level from 105C to 255C
Medium Temperature	**85**	Set temperature level from 85C to 104C
Low Temperature	**82**	Set temperature level from 0C to 84C

Feature	Options	Description
Critical BW Level	**3**	Set Bandwidth level from 0% to 9%
High BW Level	**10**	Set Bandwidth level from 10% to 50%
Medium BW Level	**100**	Set Bandwidth level from 51% to 100%
MEMHOT Level	Disabled Mid Hi **Critical**	MEMHOT disabled (no response to pin assertion), Mid Level, Hi Level, Critical Level (MEMHOT re-uses CLTT THRT MID/HI/CRIT registers or OLTT BW Level)
MEMTRIP	**Disabled** Enabled	Enable\Disable MEMTRIP
Rx Skew Control	**No Skew** +2 Ticks -2 Ticks	Selects Rx Skew Control 0: No skew, 1: +2, 2: -2 ticks
Tx Skew Control	**No Skew** +2 Ticks -2 Ticks	Selects Tx Skew Control 0: No skew, 1: +2, 2: -2 ticks
Performance Profile	**17_19_13_18** 17_19_6_18 17_19_6_7	Performance profile for DMAP
Override Checkpoints	**Auto** Disabled Enabled	Set to Auto (normal function)/Enabled(Adds a breakpoint if warm-reset can't be executed)/Disabled
Scrambler	Disabled **Enabled**	Enable / Disable the scrambler
Slow Power Down Exit	Disabled **Enabled**	Enable / Disable Slow Power Down Exit from pre-charge
Timing Configuration	Submenu	
SSA Config	Submenu	
Memory config DFX Menu	Submenu	

7.3.6.5. IntelRCSetup >North Bridge Chipset Configuration >Pass Gate Setup

Feature	Options	Description
Pass Gate Setup	Info only	
Pass Gate Test	**Disabled** Enabled	Enables/Disables the Pass Gate Test
Pass Gate Test Direction	**Lowest->Highes** Highest->Lowest	Selects if move through memory from Lowest->Highest or from Highest->Lowest
Pass Gate Test Repetition	**900**	Pass Gate Test Repetition Count Range over the same row (1000x)
Pass Gate Test Iterations	**1**	Pass Gate Test Iterations on Row (repeat the 'Pass Gate Test Repetition')
Pass Gate Swizzle	**Auto** Enabled	Forces Swizzle mode (for Samsung)
Pass Gate Pattern	**0's** 1's	Select between Pattern 1's or 0's Agressor
Pass Gate Target Pattern	0's **1's**	Select to target pattern 1's or 0's
Pass Gate Speed	1x Only 2x Only 4x Only **8x Only**	Speed of execution of the characterization test
Pass Gate Partial	**Disabled** Enabled	Enables/Disables the Pass Gate Test in an specified memory range
Row Bank Min	**0**	Select the minimum address to test. If DDR3 'Row Bank Min[2:0] -> Banks' and 'Row Bank Min[18:3] -> Rows', if DDR4 'Row Bank Min[1:0] -> Banks', 'Row Bank Min[3:2] -> Banks Groups' and 'Row Bank Min[21:4] -> Rows'
Row Bank Max	**8**	Select the maximum address to test. If DDR3 'Row Bank Max[2:0] -> Banks' and 'Row Bank Max[18:3] -> Rows', if DDR4 'Row Bank Max[1:0] -> Banks', 'Row Bank Max[3:2] -> Banks Groups' and 'Row Bank Max[21:4] -> Rows'
Channel x:	**Info only**	
Rank x	Disabled **Enabled**	Allow the Rank x to be tested
Pass Gate MonteCarlo	**Disabled** Enabled	Enable/Disable Search Algorithm in order to find PG Max
Pass Gate Max Failures	**50**	The number of failures before reducing repetition value
Pass Gate Montecarlo Start	**900**	The start repetition value for MonteCarlo
Pass Gate Montecarlo Decrement	**10**	Step Decrement value

7.3.6.6. IntelRCSetup >North Bridge Chipset Configuration >Leaky Bucket Setup

Feature	Options	Description
Leaky Bucket Setup	Info only	
Channel x	Info only	
Leak Rate Units	Microseconds **Days**	Configure Leak Rate Units for programming all Ranks
Leak Rate Configuration	Info only	
Rank x	0	Allow the Rank x to be tested
Correctable Error Threshold	Info only	
Rank x	0	Allow the Rank x to be tested

7.3.6.7. IntelRCSetup >North Bridge Chipset Configuration >NonVolatile Memory Setup

Feature	Options	Description
NonVolatile Memory Setup	Info only	
Method	**Disabled** Enabled	
SoC Pwr loss support	**Disabled** Enabled	enable internal detection of ADR entry instead of a CPLD
Cache Flushing	**MemCtrlr only** L1, L2 and MemCtrlr	Select the amount of cache that should be flushed
ADR State source	Internal **external**	Selects whether ADR State source is internal or external
Internal Pwr Loss Event Setup	Submenu	
Interleaving	**Disabled** Enabled	interleaved or separate NVDIMMs address space
Restore	Disabled **Enabled**	Enable restoring of data from the NVDIMMs
Erase & Arm	Disabled **Enabled**	Enable erasing and arming of NVDIMM after data recovery
NVDIMM battery	inactive - charging	NVDIMM not available until adequate charge is available
LBA Start Location	**Fixed LBA** C2F disk Partition	The method used to determine the C2F storage space
LBA	**0**	the starting LBA where C2F data will be saved
Size(MB)	**1024**	the amount (in megabytes) from the top of memory space to be saved, limited to memory space above 4gig
Test NonVol mode:	**Disabled** Enabled	force a NonVolatile memory flow

IntelRCSetup >North Bridge Chipset Configuration >NonVolatile Memory Setup >Internal Pwr Loss Event Setup

Feature	Options	Description
SoC Pwr loss support	**Disabled** Enabled	enable internal detection of ADR entry instead of a CPLD
PMC reset	Disabled **Enabled**	Notify when global reset because of SMBUS Slave pwr down; CF9 w/global reset; Host partition timeout w/Promote to global reset; Sx entry timeout
Power Button Override	Disabled **Enabled**	Notify when Power Button Override
ME Pwr Button Override	Disabled **Enabled**	Notify when ME initiated Power Button Override
ME WDT	Disabled **Enabled**	Notify when ME watchdog timer expire
ME reset	Disabled **Enabled**	Notify when ME initiated global reset
PMC WDT	Disabled **Enabled**	Notify when PMC watchdog timer expire
ME uncorr Error	Disabled **Enabled**	Notify when ME uncorrectable error
SYS_PWROK	**Disabled** Enabled	Notify when SYS_PWROK failure
PMC parity error	**Disabled** Enabled	Notify when PMC parity error
Return power	Disabled **Enabled**	Power up ~4 sec after ADR entry

7.3.6.8. IntelRCSetup >North Bridge Chipset Configuration >Timing Configuration

Feature	Options	Description
Timing Configuration	Info only	
tCL	**Auto**	Set tCL to Auto | 7 -> 18, 20 DRAM Clocks
tRCD	**Auto**	Set tRCD to Auto | 7 -> 18, 20 DRAM Clocks
tRP	**Auto**	Set tRP to Auto | 7 -> 18, 20 DRAM Clocks
tRAS	**Auto**	Set tRAS to Auto | 24 -> 44 DRAM clocks
tRTP	**Auto**	Set tRTP to Auto | 6 -> 10 DRAM clocks
tRRD	**Auto**	Set tRRD to Auto | 4 -> 10 DRAM clocks
tFAW	**Auto**	Set tFAW to Auto | 16 | 20 | 22 | 23 | 24 | 26 | 27 | 30 | 32 | 33 DRAM clocks
tCCD	**Auto**	Set tCCD to Auto | 4 -> 8 DRAM clocks
tWTP	**Auto**	Set tWTP to Auto / 15 / 16 / 17 / 18 / 19 / 20 / 21 / 22 / 23 / 24 / 25 / 26 / 27 / 28 / 29 / 30 DRAM clocks
tWCL	**Auto**	Set tWCL to Auto | 7 -> 12, 14, 16, 18 DRAM clocks

7.3.6.9. IntelRCSetup >North Bridge Chipset Configuration >SSA Config

Feature	Options	Description
SSA Config	Info only	
VT-d	Disabled **Enabled**	COption to Enable / Disable VT-d
VT-d Interrupt remapping	Disabled **Enabled**	Option to Enable/Disable VT-d Interrupt remapping

IntelRCSetup >North Bridge Chipset Configuration >SSA Config >DFX SSA Config

Feature	Options	Description
DFX SSA Config	Info only	
SSA Clock Gating	**Disabled** Enabled	Enable SSA Clock Gating on NorthBridge
In Order APIC	**Disabled** Enabled	Enable/Disable In Order APIC. Option applies to B0 Stepping ONLY.
Scheduler Lat	**8**	Scheduler Latency. Value programmed has 250ns resolution.
MSI algorithm	**Fixed priority** Round Robin	Allow change the MSI algorithm
COS CAT Agentx	**0**	COS Category for Agent
BestEffortMaxLat	**63**	Best Effort Max Latency
PageHitDelay	**0**	Page Hit Delay
ISOCBankPref	**0**	ISOC Bank Prefetch
BestEffortBankPref	**32**	Best Effort Bank Prefetch

7.3.6.10. IntelRCSetup >North Bridge Chipset Configuration >Memory config DFX Menu

Feature	Options	Description
Memory config DFX Menu	Info only	
Bank XOR Mapping	Disabled **Enabled**	Memory Bank XOR Mapping
Error Threshold	16384	Modify the MCI Error threshold from 1-> 32768
Rank-to-Rank	Disabled **Enabled**	Enables/Disables the Rank To Rank Switching
Memory Test Loop	**Disabled** Enabled	Enable to repeat memory test infinitely
LoopCount	**1**	Number of time CPGC will be tested 1 - 65535
Interleave Mode	Mode 0 Mode 1 **Mode 2** HVM Mode	Selects the Interleave Mode Settings
Halt on Memtest Fail	Disabled **Enabled**	Enable to halt the system if an error is observed during memory test
MRC Reset Test	**Disabled** Enabled	Enable to execute MRC Reset Test a defined number of cycles
Max Scrub Debit Count	**0**	Maximum Number of debit Patrol scrub operations
BRAM Parity	**Auto** Disabled	Enables MC Error reporting for BRAM parity errors. 'Auto' applies the safest setting for the stepping.
Training CPGC exp_loop_cnt	**10**	Set the CPGC exp_loop_cnt field for RMT execution 2^(exp_loop_cnt -1)
Training CPGC num_bursts	**8**	Set the CPGC num_bursts field for MRC trainings 2^(num_bursts -1)
Vref Override Enable	**Disabled** Enabled	Enables/Disables Vref Override Enable
MeSeg Enable	**Disabled** Enabled	Enables Memory for Manageability Engine Usage
MMIO Size / BMBOUND Base	**Auto** 1024M / 3072M 3072M / 1024M	Size of memory mapped IO space / Corresponding BMBOUND Base setting. BMBound base plus Memory map IO low will always be 4GB
BDebug1 DRAM Self Refresh	**Disabled** Enabled	Enable/Disable DRAM Self Refresh During C0

IntelRCSetup >North Bridge Chipset Configuration >Memory config DFX Menu >PPR Option 0~7

Feature	Options	Description
PPR Sequence	**Disabled** Enabled	Enables/Disables the PPR Sequence
Target Row	**0**	Selects the failure row
Target Bank	**0**	Selects the failure bank
Target Bank Group	**0**	Selects the failure bank group
Target Dram Device	**0**	Selects the failure DRAM device for max device is 7 and for x4 is 16
Target Rank	**0**	Selects the failure rank
Target Channel	**0**	Selects the failure channel

7.3.7. IntelRCSetup >South Bridge Chipset Configuration

Feature	Options	Description
South Bridge Chipset Configuration	Info only	
SATA Configuration	Submenu	
USB Configuration	Submenu	
PCIE IP Configuration	Submenu	
PPM Config	Submenu	
IQAT Configuration	Submenu	
GPIO Status	**Disabled** Enabled	GPIO Status Help
DCI Enable	Disabled **Enabled**	When DCI is Enabled, it is taken as user consent to enable the DCI which allows debug over the USB3 interface. When Disabled, the host control is not enabling DCI feature.
SMBUS Controller	Disabled **Enabled**	SMBUS Controller options
SMBusIOSFClockGating	Disabled **Enabled**	SMBusIOSFClockGating
SMBus Host Speed	**Standard (80 kHz)** Standard (100 kHz) Fast Mode (400 kHz) Fast Mode Plus (1 MHz)	SMBus Host Speed: Value to indicate what speed physical bus must operate.
IOAPIC 24-119 Entries	**Disabled** Enabled	Enables/Disables IOAPIC 24-119 Entries to expand to PIRQI-PIRQX
SouthBridge DFX Configuration	Submenu	

7.3.7.1. IntelRCSetup >South Bridge Chipset Configuration >SATA Configuration

Feature	Options	Description
SATA x	Submenu	

7.3.7.2. IntelRCSetup >South Bridge Chipset Configuration >SATA Configuration >SATA 0~1

Feature	Options	Description
Enable controller	Disabled **Enabled**	Enables/Disables SATA Controller if supported by current cpu SKU.
SATA Testmode	**Disabled** Enabled	Enable/Disable SATA test mode
LPM	**Disabled** Enabled	Enables/Disables Link Power Management
Speed limit	Gen 1 **Gen 2** Gen 3	Indicates the highest allowable speed of the interface
Port Multiplier Support	Disabled **Enabled**	Enables port multiplier support in CAP register of the controller.
Port 0	Submenu	
Port 1	Submenu	

IntelRCSetup >South Bridge Chipset Configuration >SATA Configuration >SATA 0~1 >Port 0~1

Feature	Options	Description
SATA x Port x	Info only	
Enable/disable port	Disabled **Enabled**	Enables/Disables SATA Controller port if supported by current cpu SKU.
Hot plug	Disabled **Enabled**	Hot plug
Spin up	**Disabled** Enabled	Spin up
Topology	**Unknown** ISATA Direct Connect Flex M2	Identify the SATA Topology if it is Default or ISATA or Flex or DirectConnect or M2

7.3.7.3. IntelRCSetup >South Bridge Chipset Configuration >USB Configuration

Feature	Options	Description
USB SS Configuration	Submenu	
USB HS Configuration	Submenu	
USB Precondition	**Disabled** Enabled	Precondition work on USB host controller and root ports for faster enumeration.
Inactivity Initiated L1	Disabled **1024 bb_cclk**	If programmed to non-zero, it allows L1 power managed to be enabled after the time-out period specified
XHC Initiated L1	Disabled **Enabled**	If set, allow the XHC initiated L1 power mangement to be enabled.
XHCI Compliance Mode	**Disabled** Enabled	Disable Compiance Mode

IntelRCSetup >South Bridge Chipset Configuration >USB Configuration >USB SS Configuration >Port 0~3

Feature	Options	Description
USB SS Physical Connector	Disabled **Enabled**	Enable/Disable this USB Physical Connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.

IntelRCSetup >South Bridge Chipset Configuration >USB Configuration >USB HS Configuration >Port 0~3

Feature	Options	Description
USB HS Physical Connector	Disabled **Enabled**	Enable/Disable this USB Physical Connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.

7.3.7.4. IntelRCSetup >South Bridge Chipset Configuration >PCIE IP Configuration

Feature	Options	Description
Bifurcation PCIE0	**X2X2** X4	Select and force Root Complex Bifurcation Configuration regardless board or trident detection
Bifurcation PCIE1	**X2X2** X4X4 X8	Select and force Root Complex Bifurcation Configuration regardless board or trident detection
Compliance Test Mode	**Disabled** Enabled	Enable when using Compliance Load Board
Root Port x	Submenu	
Topologies for PCIE lane by lane	Submenu	

IntelRCSetup >South Bridge Chipset Configuration >PCIE IP Configuration >Root Port x

Feature	Options	Description
Link Speed	Gen1 Gen2 **Gen3**	Select upper limit on link operational speed for PCI Express RootPort.
Clock Gating	Disabled **Enabled**	Enable / Disable Clock Gating for PCI Express RootPort.
Max Payload	128 Bytes **256 Bytes** 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set Maximum Payload of PCI Express RootPort or allow BIOS to select the value
Max Read Request	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set Maximum Read Request of PCI Express RootPort or allow BIOS to select the value
Extended Tag	Disabled **Enabled**	If Enabled allows Device to use 8-bit Tag field as a requester
Relaxed Ordering	**Disabled** Enabled	Enables or Disables PCI Express Device Relaxed Ordering.
Extended Synch	**Disabled** Enabled	If Enabled allows generation of Extended Synchronization patterns
De-Emphasis	-3.5 dB **-6.0 dB**	When the link is operating at 5 Gb/s speed, this bit selects the level of de-emphasis for an Downstream Port
Stop and Scream	**Disabled** Enabled	Stop and Scream option
ASPM Support	L1 **Disabled**	Enable PCI Express Active State Power Management settings.
Surprise link	Disabled **Enabled**	Activate surprise link
RW - Lock	**UnLock** Lock	Root Port lock option
Lane Reversal	**Disabled** Enabled	Enable / Disable Dynamic Lane Reversal on PCI Express RootPort
Completion Timeout Disabled	**Disabled** Enabled	Enable / Disable Completion Timeout
Completion Timeout Range	**65ms to 210ms**	This field indicates the Completion Timeout Range value

IntelRCSetup >South Bridge Chipset Configuration >PCIE IP Configuration >Topologies for PCIE lane by lane

Feature	Options	Description
Topology	SATA Express M2X4 M2X1 **X4** X1 Unknown	Identify PCIE Topology:x1, x4, sata express or M2
Topology	SATA Express M2X4 M2X1 **X4** X1 Unknown	Identify PCIE Topology:x1, x4, sata express or M2
Topology	SATA Express M2X4 M2X1 **X4** X1 Unknown	Identify PCIE Topology:x1, x4, sata express or M2
Topology	SATA Express M2X4 M2X1 **X4** X1 Unknown	Identify PCIE Topology:x1, x4, sata express or M2
Topology	SATA Express M2X4 M2X1 **X4** X1 Unknown	Identify PCIE Topology:x1, x4, sata express or M2
Topology	SATA Express M2X4 M2X1 **X4** X1 Unknown	Identify PCIE Topology:x1, x4, sata express or M2
Topology	SATA Express M2X4 M2X1 **X4** X1 Unknown	Identify PCIE Topology:x1, x4, sata express or M2
Topology	SATA Express M2X4 M2X1 **X4** X1 Unknown	Identify PCIE Topology:x1, x4, sata express or M2
Topology	SATA Express	Identify PCIE Topology:x1, x4, sata express or M2

Feature	Options	Description
	M2X4 M2X1 **X4** X1 Unknown	
Topology	SATA Express M2X4 M2X1 **X4** X1 Unknown	Identify PCIE Topology:x1, x4, sata express or M2
Topology	SATA Express M2X4 M2X1 **X4** X1 Unknown	Identify PCIE Topology:x1, x4, sata express or M2
Topology	SATA Express M2X4 M2X1 **X4** X1 Unknown	Identify PCIE Topology:x1, x4, sata express or M2
Topology	SATA Express M2X4 M2X1 **X4** X1 Unknown	Identify PCIE Topology:x1, x4, sata express or M2
Topology	SATA Express M2X4 M2X1 **X4** X1 Unknown	Identify PCIE Topology:x1, x4, sata express or M2
Topology	SATA Express M2X4 M2X1 **X4** X1 Unknown	Identify PCIE Topology:x1, x4, sata express or M2
Topology	SATA Express M2X4 M2X1 **X4** X1 Unknown	Identify PCIE Topology:x1, x4, sata express or M2

7.3.7.5. IntelRCSetup >South Bridge Chipset Configuration >PPM Config

Feature	Options	Description
C-state POPUP	Disabled **Enabled**	Enable/Disable C-state POPUP

7.3.7.6. IntelRCSetup >South Bridge Chipset Configuration >IQAT Configuration

Feature	Options	Description
IQAT	Disabled **Enabled**	Hides IQAT device from an OS
Set IQAT FUSECTL	**Disabled** Enabled	Enable the setting of IQAT FUSECTL Register
Set 64B MRR/MPL	Disabled **Enabled**	Enable the setting of 64B MRR/MPL in IQAT DevCtl Register

7.3.7.7. IntelRCSetup >South Bridge Chipset Configuration >SouthBridge DFX Configuration

Feature	Options	Description
SouthBridge DFX Configuration	Info only	
IQAT Configuration	Submenu	

IntelRCSetup >South Bridge Chipset Configuration >SouthBridge DFX Configuration >IQAT Configuration

Feature	Options	Description
IQAT	Disabled **Enabled**	Hides IQAT device from an OS
Set IQAT FUSECTL	**Disabled** Enabled	Enable the setting of IQAT FUSECTL Register
Set 64B MRR/MPL	Disabled **Enabled**	Enable the setting of 64B MRR/MPL in IQAT DevCtl Register

7.4. Advanced

This menu contains the settings for most of the user interfaces in the system.

7.4.1. Advanced > Power Management

Feature	Options	Description
Power Management	Info only	
Enable ACPI Auto Configuration	**Disabled** Enabled	Enable or Disables BIOS ACPI Auto Configuration.
Enable Hibernation	Disabled **Enabled**	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
Lock Legacy Resource	**Disabled** Enabled	Enables or Disables Lock of Legacy Resources
Emulation AT/ATX	Emulation AT **ATX**	Select Emulation AT or ATX function. If this option is set to [Emulation AT], BIOS will report no suspend functions to ACPI OS. In windows XP, it will make OS show shutdown
LID Function	**Disabled** Enabled	Enable/Disable LID Function
ECO Mode	**Disabled** Enabled	
Power-up Mode	**Turn On** Remain Off Last State	
Power Consumption	Submenu	Power Consumption information.

7.4.2. Advanced > Power Management->Power Consumption

Feature	Options	Description
Power Consumption	Info Only	
Current Input Current	Info Only	Display Current Input Current
Current Input Power	Info Only	Display Current Input Power
VCORE	Info Only	Display VCORE Voltage
VMEM	Info Only	Display VMEM Voltage
5VSB	Info Only	Display 5VSB Voltage
VIN	Info Only	Display VIN Voltage
3.3VSB	Info Only	Display 3.3VSB Voltage
5V	Info Only	Display 5V Voltage

7.4.3. Advanced > System Management

Feature	Options	Description
System Management	Info Only	
Version	Info Only	Display SEMA Module Version.
SEMA Firmware	Info Only	Display SEMA Firmware Version.
Build Date	Info Only	Display SEMA Firmware Build Date.
SEMA Bootloader	Info Only	Display SEMA Bootloader Version.
Build Date	Info Only	Display SEMA Bootloader Build Date.
SEMA Features	Submenu	Display SEMA Supported Features
SEMA Supported Features	Info only	Display SEMA Supported Features
Flags	Submenu	Flag
Flags	Info only	
BMC Flags	Info Only	
BIOS Select	Info Only	
ATX/AT-Mode	Info Only	
Exception Code	Info Only	

7.4.4. Advanced > Thermal Management

Feature	Options	Description
Temperatures and Fan Speed	Info Only	
CPU Temperature	Info Only	
Current	Info Only	Display Current CPU Temperature
Startup	Info Only	Display Startup CPU Temperature
Min	Info Only	Display Min CPU Temperature
Max		Display Max CPU Temperature
Board Temperature	Info Only	
Current	Info Only	Display Current Board Temperature
Startup	Info Only	Display Startup Board Temperature
Min	Info Only	Display Min Board Temperature
Max	Info Only	Display Max Board Temperature
CPU Fan Speed	Info Only	Display CPU Fan Speed
Smart Fan	Submenu	
Critical Trip Point	**Disabled** 65 C 75 C 85 C	The value is the temperature threshold of the Critical Trip Point.
Passive Cooling Trip Point	**Disabled** 80 C 90 C	The value is the temperature threshold of the Passive Cooling Trip Point.
Watchdog ACPI Event Shutdown	**Disabled** Enabled	Watchdog ACPI Event Shutdown Enabled/Disabled

7.4.4.1. Advanced > Thermal Management > Smart Fan

Feature	Options	Description
Smart Fan	Info Only	
CPU Smart Fan Temperature Source	**CPU Sensor** Board Sensor	CPU Smart Fan Temperature Source
CPU Fan Mode	**AUTO (Smart Fan)** Fan Off Fan On	CPU Fan Mode
Trigger Point 1 to 4	Info Only	Display Trigger Point 1 to 4 information
Trigger Temperature	0-100	Select Trigger Temperature
PWM Level	0-100	Select Trigger Temperature

7.4.5. Advanced > Watchdog Timer

Feature	Options	Description
Watchdog Timer	Info only	
RunTime Watchdog	**Disabled** Enabled	The RunTime Watchdog resets the system after a certain amount of time after power up.
Power-Up Watchdog	**Disabled** Enabled	The Power Up Watchdog resets the system after a certain amount of time after power up.

7.4.6. Advanced > CSM Configuration

Feature	Options	Description
Compatibility Support Module Configuration	Info only	
CSM Support	Disableed **Enabled**	Enabled / Disabled CSM Support.
CSM16 Module Version	Info only	Display CSM16 Module Version
GateA20 Active	**Upon Request** Always	UPON REQUEST – GA20 can be disabled using BIOS services. ALWAYS – do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.
Boot option filter	**UEFI and Legacy** Legacy only UEFI only	This option controls Legacy/UEFI ROMs priority
Option ROM execution	Info only	
Network	Do not launch **UEFI** Legacy	Controls the execution of UEFI and Legacy PXE OpROM
Storage	Do not launch **UEFI** Legacy	Controls the execution of UEFI and Legacy Storage OpROM
Video	Do not launch **UEFI** Legacy	Controls the execution of UEFI and Legacy Video OpROM
Other PCI devices	Do not launch **UEFI** Legacy	Determines OpROM execution policy for devices other than Network, Storage, or Video

7.4.7. Advanced > Super IO Configuration

Feature	Options	Description
Super IO Configuration	Info only	
Super IO Chip NCT5104D	Info only	
Serial Port 1 Configuration	Submenu	Set Parameters of Serial Port 1 (COMA).
Serial Port 2 Configuration	Submenu	Set Parameters of Serial Port 2 (COMB).
Super IO Chip W83627DHG	Info Only	
Serial Port 1 Configuration	Submenu	Set Parameters of Serial Port 1 (COMA).
Serial Port 2 Configuration	Submenu	Set Parameters of Serial Port 2 (COMB).

7.4.7.1. Advanced > Super IO Configuration > Serial Port 1 Configuration (NCT5104D)

Feature	Options	Description
Serial Port 1 Configuration	Submenu	Set Parameters of Serial Port 1 (COMA).
Serial Port 1 Configuration	Info only	
Serial Port	Disableed **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	Info Only	Display IO / IRQ information of COM Port.
Change Settings	**Auto** IO=240h; IRQ=10; IO=240h; IRQ=3,4,5,6,7,10,11,12 IO=248h; IRQ=3,4,5,6,7,10,11,12 IO=250h; IRQ=3,4,5,6,7,10,11,12 IO=258h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for Super IO Device.

7.4.7.2. Advanced > Super IO Configuration > Serial Port 2 Configuration (NCT5104D)

Feature	Options	Description
Serial Port 2 Configuration	Submenu	Set Parameters of Serial Port 2 (COMB).
Serial Port 2 Configuration	Info only	
Serial Port	Disableed **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	Info Only	Display IO / IRQ information of COM Port.
Change Settings	**Auto** IO=248h; IRQ=11; IO=240h; IRQ=3,4,5,6,7,10,11,12 IO=248h; IRQ=3,4,5,6,7,10,11,12 IO=250h; IRQ=3,4,5,6,7,10,11,12 IO=258h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for Super IO Device.

7.4.7.3. Advanced > Super IO Configuration > Serial Port 1 Configuration (W83627DHG)

Feature	Options	Description
Serial Port 1 Configuration	Submenu	Set Parameters of Serial Port 1 (COMA).
Serial Port 1 Configuration	Info only	
Serial Port	Disableed **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	Info Only	Display IO / IRQ information of COM Port.
Change Settings	**Auto** IO=3F8h; IRQ=4; IO=3F8h; IRQ=3,4,5,6,7,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for Super IO Device.

7.4.7.4. Advanced > Super IO Configuration > Serial Port 2 Configuration (W83627DHG)

Feature	Options	Description
Serial Port 2 Configuration	Submenu	Set Parameters of Serial Port 2 (COMB).
Serial Port 2 Configuration	Info only	
Serial Port	Disableed **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	Info Only	Display IO / IRQ information of COM Port.
Change Settings	**Auto** IO=2F8h; IRQ=3; IO=3F8h; IRQ=3,4,5,6,7,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for Super IO Device.

7.4.8. Advanced > Serial Console Redirection

Feature	Options	Description
COM1	Info only	
Console Redirection	**Enabled** Disabled	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.
COM2	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.
COM3	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.
COM4	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.
Serial Port for Out-of-Band Management Windows Emergency Management Services (EMS)	Info only	
Console Redirection	Disabled **Enabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

7.4.8.1. Advanced > Serial Console Redirection > Console Redirection Settings (If COM1 Enable)

Feature	Options	Description
COM1	Info only	
Console Redirection Settings	Info only	
Teriminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.They can be used as an additional data bit.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
VT-UTF8 Combo Key Support	**Enabled** Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With this mode enabled only text will be sent. This is to capture terminal data.
Resolution 100x31	Enabled **Disabled**	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** Intel Linux XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.

7.4.8.2. Advanced > Serial Console Redirection > Console Redirection Settings (If COM2 Enable)

Feature	Options	Description
COM2	Info only	
Console Redirection Settings	Info only	
Teriminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.They can be used as an additional data bit.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
VT-UTF8 Combo Key Support	**Enabled** Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With this mode enabled only text will be sent. This is to capture Terminal data.
Resolution 100x31	Enabled **Disabled**	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** Intel Linux XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.

7.4.8.3. Advanced > Serial Console Redirection > Console Redirection Settings (If COM3 Enable)

Feature	Options	Description
COM3	Info only	
Console Redirection Settings	Info only	
Teriminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
VT-UTF8 Combo Key Support	**Enabled** Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With this mode enabled only text will be sent. This is to capture Terminal data.
Resolution 100x31	Enabled **Disabled**	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** Intel Linux XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.

7.4.8.4. Advanced > Serial Console Redirection > Console Redirection Settings (If COM4 Enable)

Feature	Options	Description
COM4	Info only	
Console Redirection Settings	Info only	
Teriminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.They can be used as an additional data bit.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
VT-UTF8 Combo Key Support	**Enabled** Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With this mode enabled only text will be sent. This is to capture Terminal data.
Resolution 100x31	Enabled **Disabled**	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** Intel Linux XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.

7.4.9. Advanced > USB Configuration

Feature	Options	Description
USB Configuration	Info Only	
USB Module Version	Info Only	Display USB Module Version
USB Controllers:	Info Only	Display USB Controllers is XHCI or EHCI.
USB Devices:	Info Only	Display attatcment USB deviecs.
Legacy USB Support	**Enabled** Disabled Auto	Enables Legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices availiable only for EFI applications.
XHCI Hand-off	**Enabled** Disabled	This is a workaround for Oses without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
EHCI Hand-off	**Disabled** Enabled	This is a workaround for Oses without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.
USB Mass Storage Driver Support	Disableed **Enabled**	Enable / Disable USB Mass Storge Driver Support.
USB hardware delays and time-outs:	Info Only	
USB transfer rime-out	1 sec 5sec 10sec **20 sec**	The time-out value for Control, Bulk, and Interrupt transfers.
Device reset time-out	10 sec **20 sec** 30 sec 40 sec	USB mass storage device Start Unit command time-out.
Device power-up delay	**Auto** Manual	Maximum time the device will take before it properly reports itself to the Hot Controller. ‘Auto’ uses default value: for a Root po\rt it is 100 ms, for a Hub port the delay is taken form Hub descriptor.

7.4.10. Advanced > Network Stack Configuration

Feature	Options	Description
Network Stack	**Disable** Enable	Enable / Disable UEFI Network Stack.

7.4.11. Advanced > Miscellaneous

Feature	Options	Description
Miscellanous	Info Only	
NVMe Configuration	Submenu	NVMe Device Options Settings
Smart Battery Function	**Disable** Enable	Enable / Disable Battery Function
SPD write protect	Disable **Enable**	Enable:Writes to SMBus slave addresses A0h - AEh are disabled.
Onboard LAN Controller	Disabled **Enabled**	Enable/Disable onboard Intel I210LM LAN controller.
Wake On Lan from S5	Disabled **Enabled**	Enable or Disable the Wake on Lan from S5
BMC I2C Mode	**400Kbps** 100Kbps	BMC I2C Mode
eMMC SPEED	**HS400** HS200	Adjust eMMC speed HS400/HS200

7.4.11.1. Advanced > Miscellaneous> NVMe Configuration

Feature	Options	Description
NVMe controller and Drive information	Info Only	NVMe controller and Drive information.
Bus:x Dev:x Func:x	Info only	
Nvme Size	Info only	

7.4.12. Advanced > TPM Configuration

Feature	Options	Description
TPM20 Device Found	Info Only	
Security Device Support	**Disable** Enable	Enables or Disable BIOS support for security device. OS will not show Security Device. TCG EFI protocol and available.
Active PCR banks*	Info Only	
Available PCR banks*	Info Only	
SHA-1 PCR Bank*	Disabled **Enabled**	Enable or Disable SHA-1 PCR Bank
SHA256 PCR Bank*	**Disabled** Enabled	Enable or Disable SHA256 PCR Bank
Pending operation*	**None** TPM Clear	Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.

***Note:** Displayed if Security Device Support is enabled when TPM device is connected.

7.4.13. Advanced > Intel® I210 Gigabit Network Connection

Feature	Options	Description
Port Configuration Menu	Info only	
NIC Configuration	Submenu	
Link Speed	Auto Negotiated 10 Mbps Half 10Mbps Full 100Mbps Half 100Mbps Full	Specifies the port speed used for the selected boot protocol.
Wake On LAN	Disable Enable	Enables the server to be powered on using an in-band magic packet.
Blink LEDs	0	Identify the physical network port by blinking the associated LED
Port Configuration Information	Info Only	
UEFI Driver:	Info Only	
Adapter PBA:	Info Only	
Chip Type	Info Only	
PCI Device ID	Info Only	
PCI Address	Info Only	
Link Status	Info Only	
MAC Address	Info Only	
Virtual MAC Address	Info Only	

7.4.14. Advanced > Intel® Ethernet Connection X553 10 GbE SFP+

Feature	Options	Description
NIC Configuration	Submenu	
Link Speed	**Auto Negotiated** 10 Mbps Half 10Mbps Full 100Mbps Half 100Mbps Full	Specifies the port speed used for the selected boot protocol.
Wake On LAN	Disable **Enable**	Enables the server to be powered on using an in-band magic packet.
Blink LEDs	0	Identify the physical network port by blinking the associated LED
Port Configuration Information	Info Only	
UEFI Driver:	Info Only	
Adapter PBA:	Info Only	
Chip Type	Info Only	
PCI Device ID	Info Only	
PCI Address	Info Only	
Link Status	Info Only	
MAC Address	Info Only	
Virtual MAC Address	Info Only	

7.5. Event Logs

7.5.1. Event Logs >Change SMBIOS Event Log Settings

Feature	Options	Description
Enabling/Disabling Options	Info only	
SMBIOS Event Log	Disabled **Enabled**	Change this to enable or disable all features of SMBIOS Event Logging during boot.
Erasing Setting	Info only	
Erase Event Log	**No** Yes, Next reset Yes, Every reset	Choose options for erasing SMBIOS Event Log. Erasing is done prior to any logging activation during reset.
When Log is Full	**Do Nothing** Erase Immediately	
SMBIOS Event Log Standard Settings	**Info only**	
Log System Boot Event	Disabled **Enabled**	Choose option to enable/disable logging of System boot event
MECI	1	Multiple Event Count Increment: The number of occurrences of a duplicate event that must pass before the multiple-event counter of log entry is updated. The value ranges from 1 to 255.
METW	60	Multiple Event Time Window: The number of minutes which must pass between duplicate log entries which utilize a multiple-event counter. The value ranges from 0 to 99 minutes.
Custom Options	Info only	
Log OEM Codes	Disabled **Enabled**	Enable or disable the logging of EFI Status Codes as OEM Codes (if not already converted to legacy).
Convert OEM Codes	**Disabled** Enabled	Enable or disable the converting of EFI Status Codes to Standard SMBIOS Types (Not all may be translated).

7.5.2. Event Logs >View SMBIOS Event Log

Feature	Options	Description
Date Time Error Code Severity	Info only	

7.6. Security

7.6.1. Security > Password Description

Feature	Options	Description
Password Description	Info only	
Setup Administrator Password	Enter Password	Set Setup Administrator Password
User Password	Enter Password	Set User Password
Secure Boot menu	Submenu	Customizable Secure Boot settings.
System Mode	Info only	
Secure Boot	Info only	
Secure Boot Control	Disabled **Enabled**	Secure Boot activated when\n Platform Key(PK) is enrolled,\n System mode is User/Deployed,\n and CSM function is disabled

7.7. Boot

Feature	Options	Description
Boot Configuration	Info only	
Setup Prompt Timeout	**1**	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
Bootup NumLock State	**On** Off	Select the keyboard Number state.
Ouiet Boot	Disabled **Enabled**	Select the keyboard NumLock state.
Fast Boot	Disabled **Enabled**	Enable or Disable FastBoot features. Most probes are skipped to reduce time cost during boot.
SATA Support	**All SATA Devices** Last Boot HDD Only"	Last Boot HDD Only: only last boot HDD device will be available in POST. All SATA Devices: all SATA devices will be available in OS and POST.
VGA Support	**EFI Driver** Auto	Auto: only install Legacy OpRom with Legacy OS and logo will NOT be shown during POST. EFI Driver: will still be installed with EFI OS.
USB Support	Disabled **Full Initial** Partial Initial	If Disabled, all USB devices will NOT be available until after OS boot. If Partial Initial, USB Mass Storage and specific USB port/device will NOT be available before OS boot. If Full Initial, all USB devices will be available in OS and Post.
PS2 Devices Support	Disabled **Enabled**	If Disabled, PS2 devices will be skipped.
NetWork Stack Driver Support	**Disabled** Enabled	If Disabled, NetWork Stack Driver will be skipped.
Boot mode select	**UEFI** Legacy	Select boot mode LEGACY/UEFI

7.7.1. Boot > Fixed Boot Order Priorities

Feature	Options	Description
Boot Option #1	**Hardware**	Set the system boot order.
Boot Option #2	**CD/DVD**	Set the system boot order.
Boot Option #3	**USB Hard Disk**	Set the system boot order.
Boot Option #4	**USB CD/DVD**	Set the system boot order.
Boot Option #5	**USB Key**	Set the system boot order.
Boot Option #6	**USB Floppy**	Set the system boot order.
Boot Option #7	**USB Lan**	Set the system boot order.
Boot Option #8	**Network**	Set the system boot order.

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8. BIOS Checkpoints, Beep Codes

This section of this document lists checkpoints and beep codes generated by AMI Aptio BIOS. The checkpoints defined in this document are inherent to the AMIBIOS generic core, and do not include any chipset or board specific checkpoint definitions.

Checkpoints and Beep Codes Definition

A checkpoint is either a byte or word value output to I/O port 80h. The BIOS outputs checkpoints throughout bootblock and Power-On Self Test (POST) to indicate the task the system is currently executing. Checkpoints are very useful for debugging problems that occur during the preboot process.

Beep codes are used by the BIOS to indicate a serious or fatal error. They are used when an error occurs before the system video has been initialized, and generated by the system board speaker.

Aptio Boot Flow

While performing the functions of the traditional BIOS, Aptio 5.x core follows the firmware model described by the Intel Platform Innovation Framework for EFI (“the Framework”). The Framework refers the following “boot phases”, which may apply to various status code & checkpoint descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization[1]
- Driver Execution Environment (DXE) – main hardware initialization[2]
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, …)

Viewing BIOS Checkpoints

Viewing all checkpoints generated by the BIOS requires a checkpoint card, also referred to as a □OST Card or POST Diagnostic Card. These are PCI add-in cards that show the value of I/O port 80h on a LED display.

Some computers display checkpoints in the bottom right corner of the screen during POST. This display method is limited, since it only displays checkpoints that occur after the video card has been activated.

Keep in mind that not all computers using AMI Aptio BIOS enable this feature. In most cases, a checkpoint card is the best tool for viewing AMI Aptio BIOS checkpoints.

[1]Analogous to “bootblock” functionality of legacy BIOS
[2]Analogous to “POST” functionality in legacy BIOS

8.1. Status Code Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

8.2. Standard Status Codes

8.2.1. SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization

SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

8.2.2. SEC Beep Codes

None

8.2.3. PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization

Status Code	Description
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes

Status Code	Description
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

8.2.4. PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

8.2.5. DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration

Status Code	Description
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)

Status Code	Description
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

8.2.6. DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

8.2.7. ACPI/ASL Checkpoint

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state

Status Code	Description
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

8.3. OEM-Reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

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9. Mechanical Information

9.1. Board-to-Board Connectors

To allow for different stacking heights, the receptacles for COM Express carrier boards are available in two heights: 5 mm and 8 mm. When 5 mm receptacles are chosen, the carrier board should be free of components.

Tyco 3-1827253-6

Foxconn QT002206-2131-3H

- 220-pin board-to-board connector with 0.5mm for a stacking height of 5 mm.
- This connector can be used with 5 mm through-hole standoffs (SMT type).

Tyco 3-6318491-6

Foxconn QT002206-4141-3H

- 220-pin board-to-board connector with 0.5mm for a stacking height of 8 mm.
- This connector can be used with 8 mm through-hole standoffs (SMT type).

Common Specifications

- Current capacity: 0.5A per pin
- Rated voltage: 50 VAC
- Insulation resistance: 100M or greater @ 500 VDC
- Temperature rating: -40°C ~ 85°C
- UL certification (ECBT2.E28476)
- Copper alloy (contacts)
- Housing: thermo-plastic molded compound (L.C.P.)

9.2. Thermal Solution

9.2.1. Heat Spreaders

The function of the heat spreader is to ensure an identical mechanical profile for all COM Express modules. By using a heat spreader, the thermal solution that is built on top of the module is compatible with all COM Express modules.

9.2.2. Heat Sinks

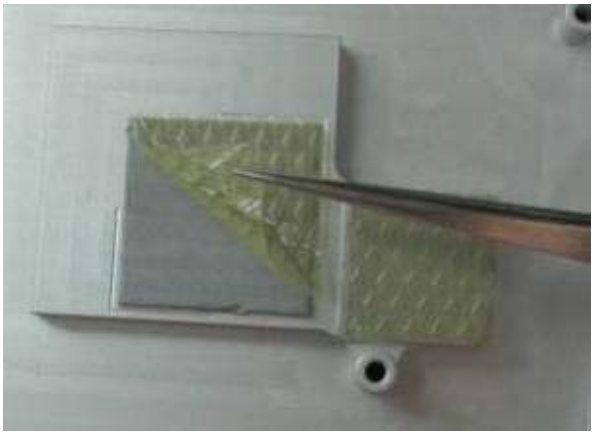
A heat sink can be used as a thermal solution for a specific COM Express module and can have a fan or be fanless, depending on the thermal requirements.

9.2.3. Installation

Install a heat spreader or heat sink using the following instructions.

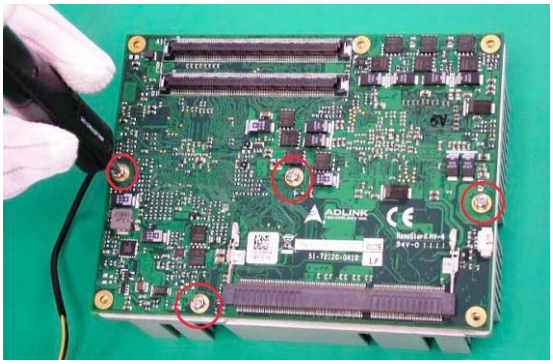
Step 1: Before mounting the heatsink, install the required memory modules onto the SODIMM socket(s) on the COM Express module.

Step 2: Remove the protective membranes from the thermal pads.

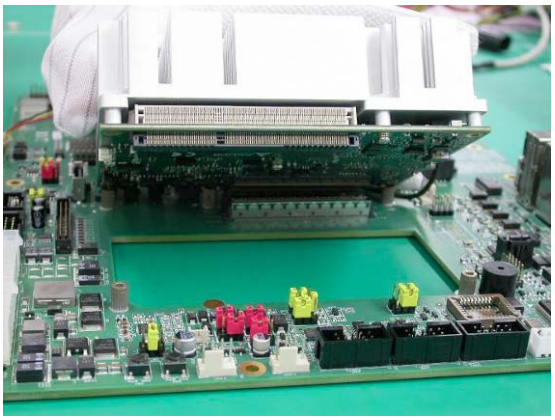


Step 3: Assemble the heatsink onto the COM Express module.

Step 4: Use the four M2.5, L=6mm screws provided to fasten the heatsink to the module.

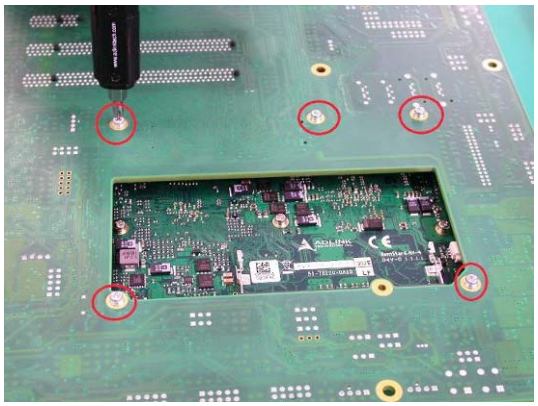


Step 5: Place the COM Express module and heatsink assembly onto the connectors on the carrier board as shown.



Then press down on the module until it is firmly seated on the carrier board.

Step 6: Use the five M2.5, L=16mm screws provided to secure the COM Express module to the carrier board from the solder side.



Step 7: If you are installing a heatsink with a fan, plug the fan connector into the carrier board as shown.

9.3. Mounting Methods

There are several standard ways to mount the COM Express module with a thermal solution onto a carrier board. In addition to the choice of 5 mm or 8mm board-to-board connectors, there is the choice of Top and Bottom mounting. In Top mounting, the threaded standoffs are on the carrier board and the thermal solution is equipped with through-hole standoffs. In Bottom mounting, the threaded standoffs are on the thermal solution and the carrier board has through-hole standoffs.

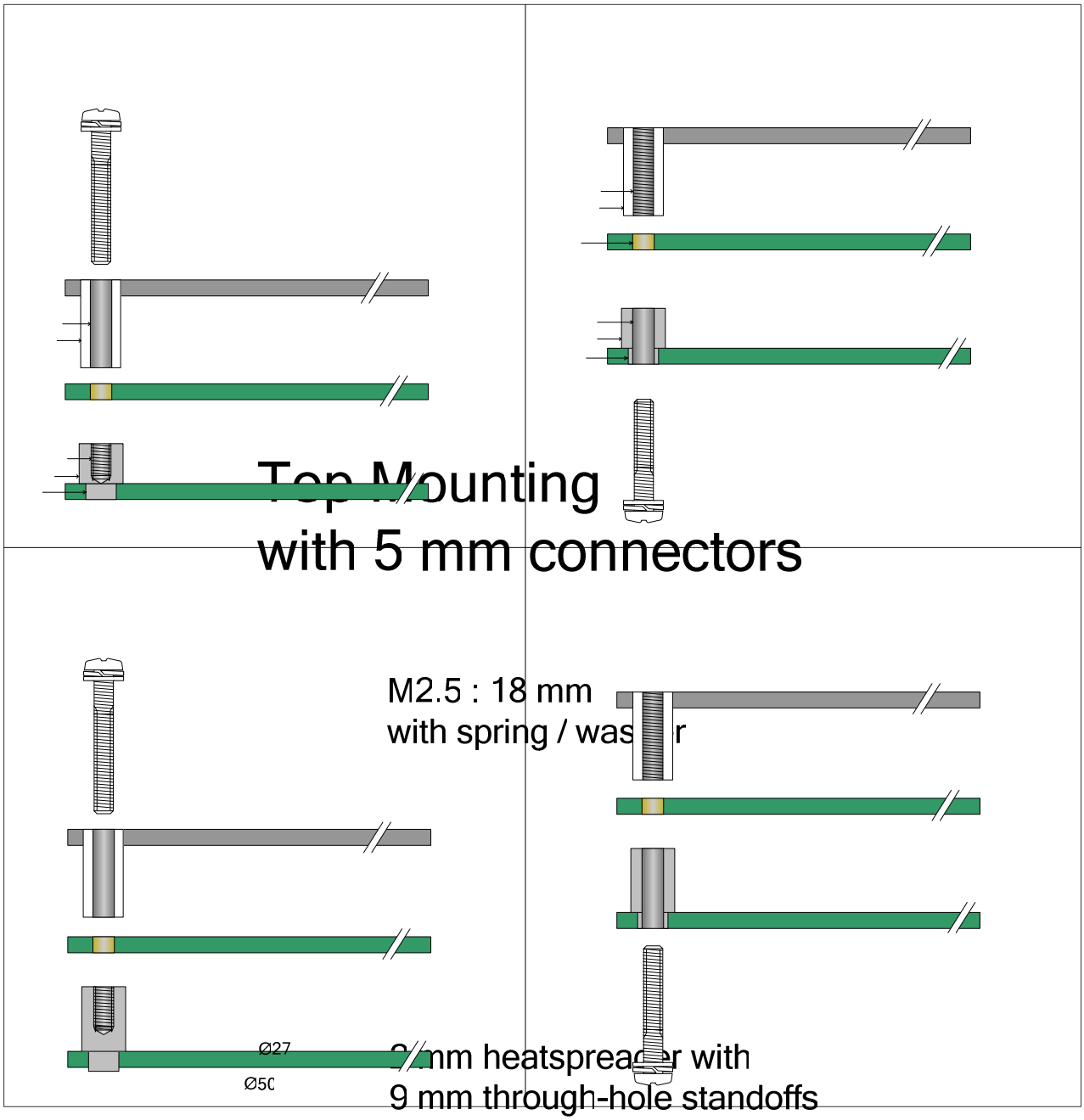


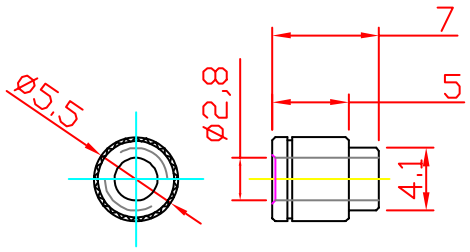
Figure 6: COM Express Mounting Methods

9.4. Standoff Types

The standoffs available for Top and Bottom mounting methods are shown below. Note that threaded standoffs are DIP type and through-hole standoffs are SMT type. Other types not listed are available upon request.

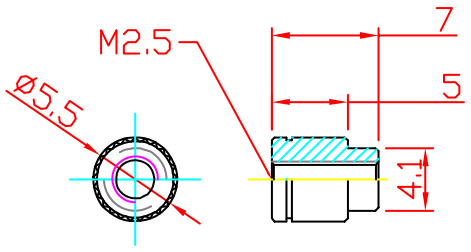
5mm through-hole standoff (SMT type)

P/N: 33-72000-0050



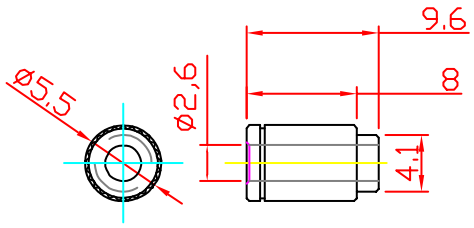
5mm threaded standoff (DIP type)

P/N: 33-72016-0050



8mm through-hole standoff (SMT type)

P/N: 33-72000-0080



8mm threaded standoff (DIP type)

P/N: 33-72015-0050

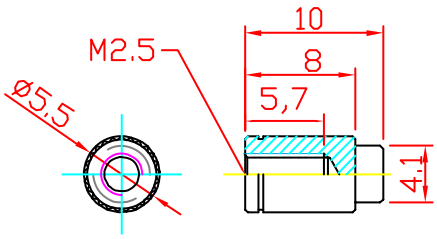


Figure 7: COM Express Standoff Types

Safety Instructions

Read and follow all instructions marked on the product and in the documentation before you operate your system. Retain all safety and operating instructions for future use.

- Please read these safety instructions carefully.
- Please keep this User‘s Manual for later reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment, turn off the power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources.
  - Keep equipment away from high heat or high humidity.
  - Keep equipment properly ventilated (do not block or cover ventilation openings).
  - Make sure to use recommended voltage and power source settings.
  - Always install and operate equipment near an easily accessible electrical socket-outlet.
  - Secure the power cord (do not place any object on/over the power cord).
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings.
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.
- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

Getting Service

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