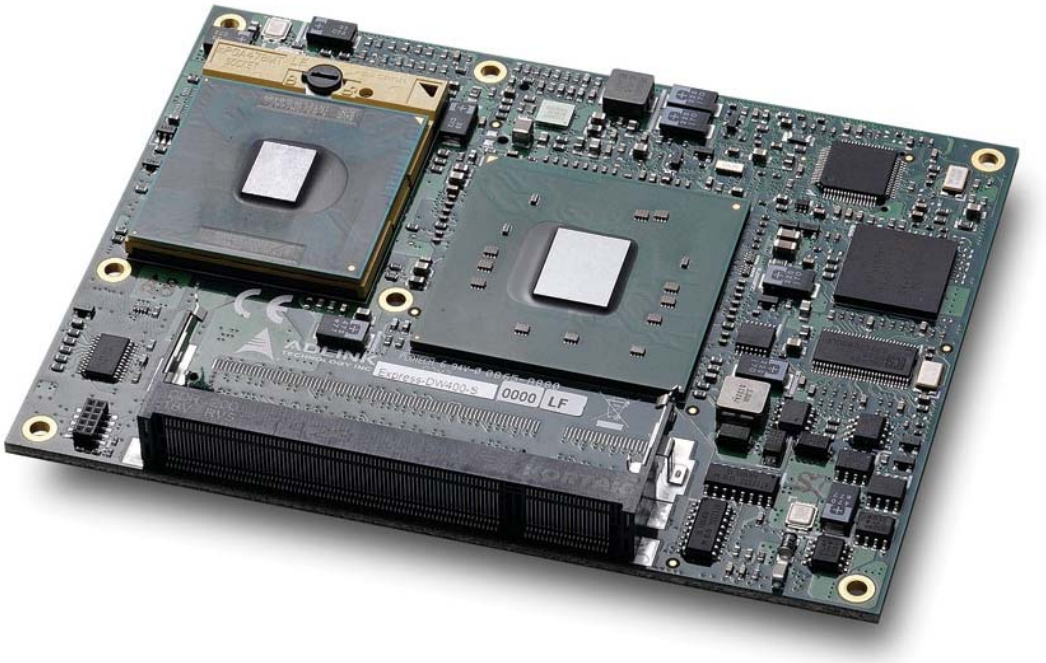
COM Express

Express-DW400

User's Manual



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ADLINK TECHNOLOGY INC.

Revision History

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2.01	2009/03/02	Correct Signal Descriptions

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Preface

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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

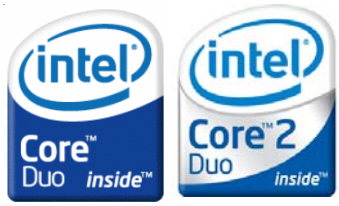
Additional information, aids, and tips that help users perform tasks.

Information to prevent *mino*r physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

Information to prevent *serious* physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

1 Introduction

1.1 Description



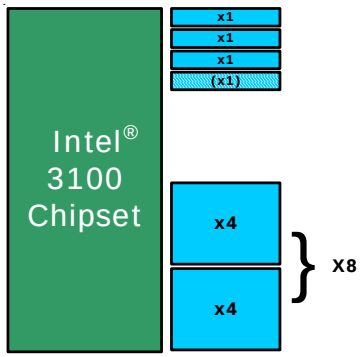
The Express-DW400 is based on the Intel® 3100 single chip, server-class chipset. The Intel® 3100 Chipset is a single integrated chip that contains the functionality of a Memory Controller Hub and an I/O Controller Hub. It can support Intel® Core™ Duo and Intel® Core™2 Duo CPUs from 1.06 GHz up to 2.1 GHz at 667MHz FSB. The Intel® 3100 chipset combines server-class memory and I/O controller functions into a single component, creating the first integrated Intel® chipset specifically optimized for embedded, communications, and storage applications. Both chipset and processors are part of the Embedded Intel® Architecture (IA) that warrants long production life for applications that need extended availability.

ECC Memory Support

The Express-DW400 supports registered ECC type, single channel DDR2 400MHz memory. The module is available with either two vertically placed SODIMM sockets or one horizontally placed SODIMM socket. A single SODIMM can support up to 2 GB of memory allowing maximum support of 4 GB memory if the two vertical socket configuration is used.

High Bandwidth PCI Express up to x8

The Intel® 3100 chipset provides one configurable x8 PCI Express interface with a maximum theoretical bandwidth of 4 GByte/s. The x8 PCI Express interface may alternatively be configured as two independent x4 PCI Express interfaces with a maximum theoretical bandwidth of 2 GBytes/s each. The Intel® 3100 Chipset also supports an additional x4 PCI Express interface with a maximum theoretical bandwidth of 2 GBytes/s which may alternatively be configured as four independent x1 PCI Express interfaces. Of these four x1 lanes, one is occupied by the Ethernet controller and three are extended to the carrier board.



EDMA on PCI Express

The IMCH includes an integrated four-channel Enhanced Direct Memory Access (EDMA) controller to perform background data transfers between locations in main memory, or from main memory to a memory-mapped I/O destination. These transfers may be individually designated to be coherent (snooped on the FSB) or non-coherent (not snooped on the FSB), providing improvements in system performance and utilization when cache coherence is managed by software rather than hardware

Other Features

The module comes with a single onboard Gigabit Ethernet port and four channel SATA. It has legacy support for Parallel IDE, 32-bit PCI and LPC bus support. The Express-DW400 comes equipped with many embedded features such as: Remote console, CMOS backup, CPU and System monitoring and a Dual Watchdog timer for NMI or RESET.

Express-DW400 is RoHS compliant and leadfree product

2 Specifications

2.1 General

- CPU:

  Merom Core socket type
  Intel® Core™ 2 Duo T7400, 2.16 GHz with 4MB L2 cache, 34 W
  Intel® Celeron® M 530, 1.73 GHz, with 1MB L2 cache 27 W

  Merom Core BGA type
  Intel® Core™ 2 Duo U7500 ULV 1.06 GHz with 2MB L2 cache, 10 W

  Yonah Core socket type
  Intel® Celeron® M 440, 1.86 GHz, with 1MB L2 cache 27 W

  Yonah Core BGA type
  Intel® Celeron M 423 ULV 1.06GHz, with 1MB L2 cache 5.5 W

- Memory:

  Single channel registered ECC DDR2 at 400MHz up to 4 GB
  Option 1: one horizontal SODIMM socket, max. 2 GB
  Option 2: two vertical SODIMM sockets, max. 4 GB

Option 1 Memory Configuration

Option 2 Memory Configuration

- Chipset: Intel® 3100 single integrated chipset containing MCH and ICH
- L2 Cache: 1 MB (Celeron® M), 2/4 MB (Core (2) Duo)
- BIOS: AMIBIOS8 with CMOS backup in 8 Mbit LPC BIOS
- Hardware Monitor: Supply Voltages and CPU temperature
- Watchdog Timer: Dual stage watchdog timer
- Expansion Busses:
  - One PCI Express® x8 lane can also be used as two PCI Express® x4 lanes
  - Four PCIe x1 lanes (one occupied by onboard GbE)
  - Four 32-bit PCI 2.3 Masters at 33/66 MHz
  - Low Pin Count (LPC) interface for Super I/O on carrier
  - SMBus interface support
  - Four GPIO input, Four GPIO output
- Power Mode Support:
  - ACPI 2.0, supports S0, S3, S4, S5 power modes

2.2 Video

- No integrated video support
- On carrier: optional VGA support can be obtained by using PCI or PCI Express® x1, X4 or X8 based VGA cards

2.3 LAN

- Chipset: Intel® 82573 PCIe-based Gigabit Ethernet connection
- Type: Triple speed 10/100/1000BASE-T IEEE 802.3 compliant which supports ASF 2.0 and Advanced Pass

2.4 Multi I/O

- Chipset: integrated in Intel® 3100
- USB: supports up to four USB 2.0 ports, supports legacy keyboard/mouse
- SATA: four integrated Serial ATA 150 ports
- PATA IDE: single channel IDE for CF card support (SATA to IDE conversion)

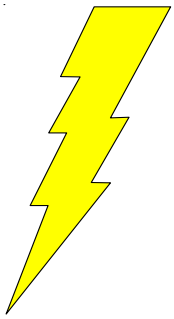
2.5 Super I/O

- Connected to LPC bus on carrier if needed

2.6 TPM (Trusted Platform Module)

- Chipset: Infineon SLB9635TT1.2
- Type: TPM 1.2

2.7 Power Specifications



- Input Power: AT mode (12 V) and ATX mode (12 V and 5 V_{SB})
- Power Management: ACPI 2.0 compliant

All power testing was done on power supply wiring leading to the Express carrier board. Although all voltages were measured, only 12 V and 5 V_{SB} are relevant because they are the only ones used by the Express module. The *Idle* power level was measured under Windows XP with no applications running (logon screen). *CPU Stress* was measured using only Kpower, and *Total System Stress* was measured under heavy burn-in conditions.

Intel® Core™2 Duo T7400, 2.16 GHz

Power State	+12V	+5V_{SB}	Power Consumption
DOS (idle)	4.21 A	N.S.	50.5 W
Windows XP logon screen (idle)	4.33 A	N.S.	52.0 W
Windows XP CPU Stress (Kpower)	4.54 A	N.S.	54.4 W
Windows XP Total System Stress (Burnin)	4.47 A	N.S.	53.6 W
S4 Mode (hibernate)	-	207.4 mA	1.02 W
S3 Mode (suspend to RAM)	-	442.9 mA	2.21 W

Intel® Celeron® M 530, 1.73 GHz

Power State	+12V	+5V_{SB}	Power Consumption
DOS (idle)	4.66 A	N.S.	55.9 W
Windows XP logon screen (idle)	4.68 A	N.S.	56.1 W
Windows XP CPU Stress (Kpower)	5.03 A	N.S.	60.4 W
Windows XP Total System Stress (Burnin)	4.74 A	N.S.	56.9 W
S4 Mode (hibernate)	-	203.1 mA	1.01 W
S3 Mode (suspend to RAM)	-	427.8 mA	2.14 W

Intel® Core™2 Duo U7500 ULV, 1.06 GHz

Power State	+12V	$+5V_{SB}$	Power Consumption
DOS (idle)	3.54 A	N.S.	42.4 W
Windows XP logon screen (idle)	3.47 A	N.S.	41.6 W
Windows XP CPU Stress (Kpower)	3.97 A	N.S.	47.6 W
Windows XP Total System Stress (Burnin)	3.74 A	N.S.	44.9 W
S4 Mode (hibernate)	-	219.7 mA	1.10 W
S3 Mode (suspend to RAM)	-	506.8 mA	2.53 W

Intel® Celeron® M 440, 1.86 GHz

Power State	+12V	$+5V_{SB}$	Power Consumption
DOS (idle)	4.63 A	N.S.	55.5 W
Windows XP logon screen (idle)	4.52 A	N.S.	54.2 W
Windows XP CPU Stress (Kpower)	4.76 A	N.S.	57.1 W
Windows XP Total System Stress (Burnin)	4.67 A	N.S.	56.1 W
S4 Mode (hibernate)	-	318.9 mA	1.59 W
S3 Mode (suspend to RAM)	-	316.9 mA	1.58 W

Intel® Celeron® M 423 ULV, 1.06 GHz

Power State	+12V	$+5V_{SB}$	Power Consumption
DOS (idle)	3.91 A	N.S.	46.9 W
Windows XP logon screen (idle)	4.10 A	N.S.	49.2 W
Windows XP CPU Stress (Kpower)	4.30 A	N.S.	51.7 W
Windows XP Total System Stress (Burnin)	4.18 A	N.S.	50.2 W
S4 Mode (hibernate)	-	105.7 mA	0.53 W
S3 Mode (suspend to RAM)	-	307.5 mA	1.54 W

CMOS/RTC Battery Power Consumption

Current	Voltage
3.5 µA	+3 V

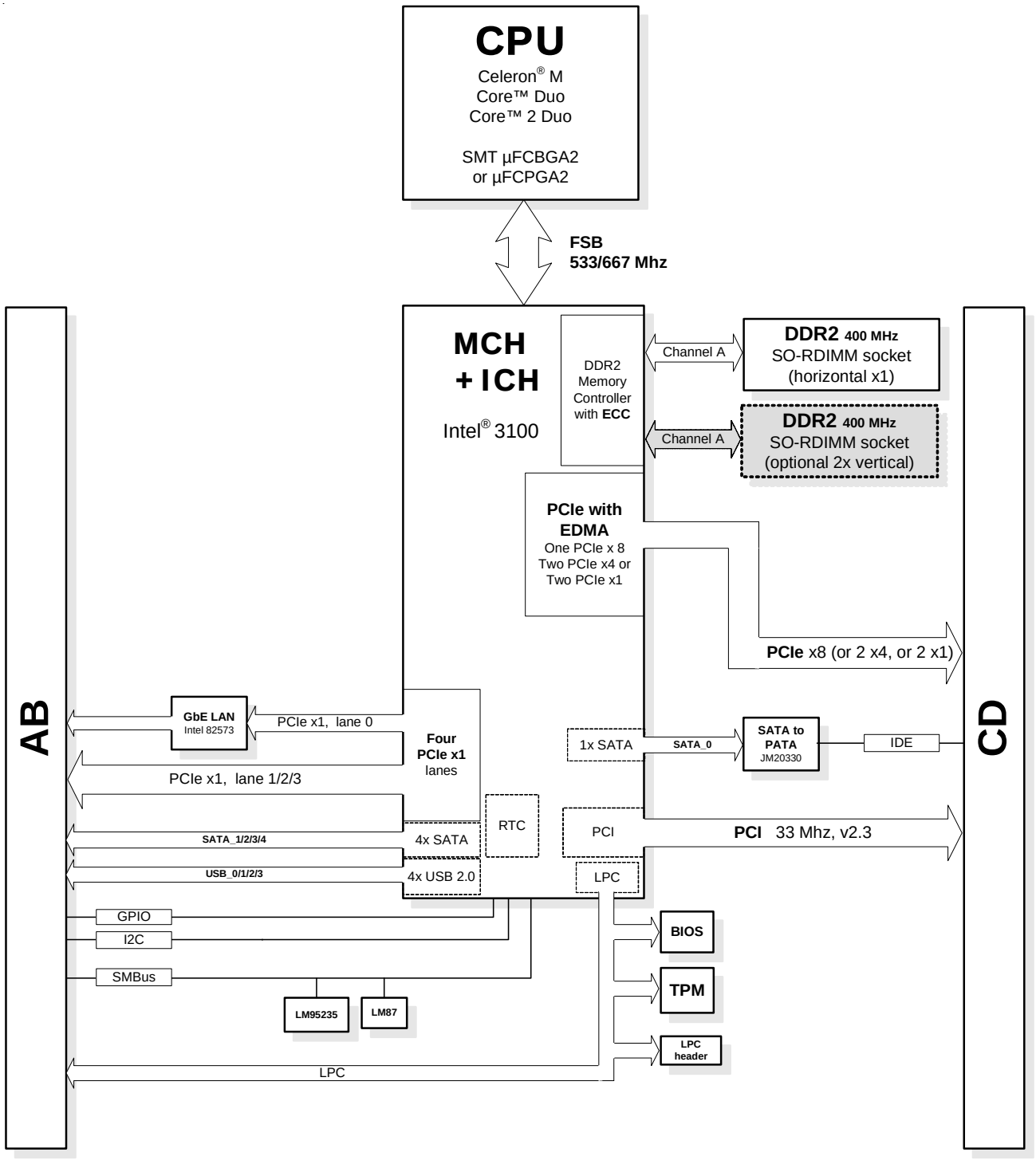
2.9 Operating Systems

- Standard Support
  - Windows XP (32/64-bit)
  - Linux 2.6.x
- Extended Support (BSP)
  - Linux 2.6.x BSP (32/64-bit)
  - AIDI I2C Library for Windows and Linux

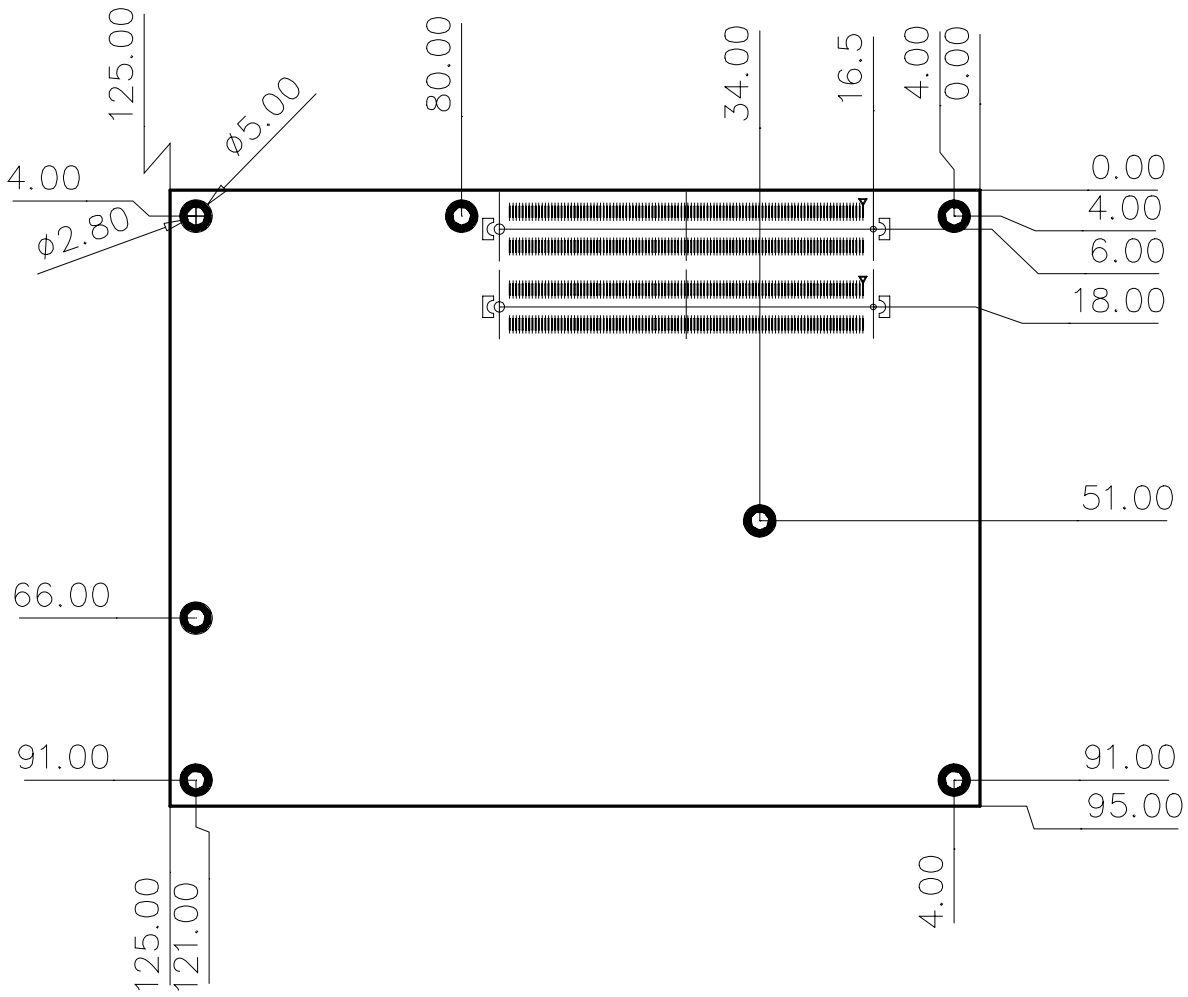
2.10 Mechanical and Environmental

- Form Factor and Type: PICMG COM.0, Standard COM Express™ Type II
- Dimensions: 95 x 125 mm
- Standard Operating Temperature: 0°C to 60°C
- Relative Humidity: up to 90% at 55°C

3 Function diagram



4 Mechanical Dimensions



All ∅ tolerances ± 0.05 mm
Other tolerances ± 0.2 mm

5 Watch Dog Timer (WDT)

5.1 Overview

The Intel® 3100 Chipset Watch Dog Timer (WDT) is a kernel mode driver designed to run on Microsoft® Windows® OS (XP, Server® 2003, Vista®, and XP Embedded) platforms. When enabled, the WDT can generate an interrupt or reboot the system in the event of a system lockup.

This WDT supports a number of IOCTL commands. These commands enable the applications to access and control all the aspects of the WDT.

The WDT is located on the LPC bus. As such, it is not detected by the Plug-n-Play (PnP) manager. To install the driver, the user must manually go through the “Add Device” wizard in the Control Panel. Installation details are covered later in this chapter.

5.2 Installing the WDT Driver

The WDT driver does not announce itself to the device manager.

To install the WDT driver:

These instructions assume that you are in the default Microsoft Windows® XP control panel view.

1. Open Control Panel and click “Printers and Other Hardware”.
2. In the “See Also” box at the top left hand corner, click “Add Hardware”.
3. Click “Next” to look for hardware.
4. Click “Yes, I have already connected the hardware” and then click “Next”.
5. Scroll to the bottom of the “Installed hardware” list and select “Add a new hardware device”.
6. Click “Install the hardware that I manually select from a list” and then Click “Next”.
7. Click “Show All Devices” and then Click “Next”.
8. Click “Have Disk…”, point to the location where the WDT driver is stored and click “OK”.
9. Click on “Intel® 3100 Chipset Watch Dog Timer” and install.

5.3 Interface with the Driver

The only supported driver communication method is through IOCTLs. The IOCTLs defined in this section allow a user-mode application to access all the capabilities of the WDT.

5.3.1 Symbolic Link

The driver creates a named device object that can be accessed through the symbolic link "\\\\.\\SAWD1". As such, the application can communicate with the driver by obtaining a handle from CreateFile() with the path, "\\\\.\\SAWD1".

```
/* Example: Getting a handle to the WDT driver */
HANDLE handle_to_wdt;
handle_to_wdt = CreateFile(
                  "\\\\.\\SAWD1",
                  GENERIC_WRITE,
                  FILE_SHARE_WRITE,
                  NULL,
                  OPEN_EXISTING,
                  0,
                  NULL);
```

Once a handle is obtained successfully, the application uses the DeviceIoControl() function to communicate with the driver.

```
/* Example: Sending an IOCTL to the driver. Here we assume
* handle_to_wdt was obtained successfully
*/
BOOL status;
int return_length;
status = DeviceIoControl(
             handle_to_wdt,     /* handle to wdt */
             IOCTL_ENABLE_WDT,  /* IOCTL to send */
             NULL,           /* no input buffer */
             0,              /* input length = 0 */
             NULL,           /* no output buffer */
             0,              /* output length = 0 */
             &return_length,/* should be 0 */
             NULL );         /* wait until I/O completes */
```

5.3.2 Supported IOCTLs

IOCTL_GET_CAPABILITIES

```
#define IOCTL_GET_CAPABILITIES                    \
          CTL_CODE( FILE_DEVICE_UNKNOWN, 0x802, \
          METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL accepts a buffer of type PSAWD_CAPABILITY_OUT_BUFF, and fills in the min and max field, indicating the minimum and maximum downcounter value. The Version field will be set to 1.

```
typedef struct _SAWD_CAPABILITY_OUT_BUFF {

unsigned    long Version;    /* version of interface used */
unsigned    long min;        /* minimum value in msecs */
unsigned    long max;        /* maximum value in msecs */

} SAWD_CAPABILITY_OUT_BUFF, *PSAWD_CAPABILITY_OUT_BUFF;
```

IOCTL_ENABLE_WDT

```
#define IOCTL_ENABLE_WDT                        \
          CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D00,    \
          METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL enables the Watch Dog Timer.

IOCTL_DISABLE_WDT

```
#define IOCTL_DISABLE_WDT                       \
          CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D01,    \
          METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL disables the Watch Dog Timer.

IOCTL_LOAD_COUNTER

```
#define IOCTL_LOAD_COUNTER                      \
          CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D02,    \
          METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This `IOCTL` accepts a buffer of type `PSAWD_CTRL`, and loads the preload counter 1 and 2 using the data in the `Preload1` and `Preload2` fields.

```
unsigned long  ConfigReg;          /* 16 bit Configuation register */
unsigned short  DeviceStatus;      /* store device status bits */
unsigned short  ReloadReg;         /* 16 bit reload register */
unsigned short  LockReg;           /* 8 bit Lock register */
unsigned long   InterruptCount;    /* # of times stage 1 INT occured */
unsigned short  IRQ;
short               BusType;
unsigned short BusNumber;
unsigned short IrqOffset;

} SAWD_CTRL, *PSAWD_CTRL;
```

IOCTL_PING_THE_WDT

```
#define IOCTL_PING_THE_WDT                    \
            CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D02,        \
            METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL reloads the Watch Dog Timer's down-counter with the preload value to prevent a timeout. If the WDT is in stage 1 of the countdown, then preload value 1 will be loaded into the main down counter. If the WDT is in stage 2 of the countdown, then preload value 2 will be loaded into the main down counter.

IOCTL_SET_PRESCALAR

```
#define IOCTL_SET_PRESCALAR                       \
            CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D04,        \
            METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL sets how the 20-bit preload value will be loaded into the 35-bit down counter. The IOCTL accepts an unsigned long integer set to 0 or 1 in the input buffer. If the input is 0, then the 20-bit preload value will be counted down at 1KHz. If the input is 1, then the 20-bit preload value will be counted down at 1MHz.

IOCTL_READ_DOWN_COUNTER

```
#define IOCTL_READ_DOWN_COUNTER                   \
            CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D05,        \
            METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL returns the current value of the down counter (in an unsigned long integer).

IOCTL_SET_EXTERNAL_OUT

```
#define IOCTL_SET_EXTERNAL_OUT                \
```

IOCTL_LOCK_DEVICE

```
#define IOCTL_LOCK_DEVICE                       \
            CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D08,        \
            METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL locks the WDT device. Once locked, the state (WDT mode vs. free running mode, and Enabled vs. Disabled) of the Watch Dog Timer cannot be changed until the system resets.

IOCTL_ROUTE_INTERRUPT

```
#define IOCTL_ROUTE_INTERRUPT                   \
            CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D09,        \
            METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL accepts an unsigned long integer, sets to 0-3, and uses it to set the type of interrupt to trigger when stage 1 timer expires.

0 sets interrupt type to PCI
1 sets interrupt type to NMI
2 sets interrupt type to SMI
3 disables stage 1 interrupt

IOCTL_USER_HANDLE

```
#define IOCTL_USER_HANDLE                       \
            CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D0D,        \
            METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This `IOCTL` accepts a buffer of type `PSAWD_CTRL`, and creates an internal reference to the function specified by the `UserEvent` field. When a stage 2 timeout occurs, the driver will call this function.

IOCTL_TEST_CALLBACK

```
#define IOCTL_TEST_CALLBACK                         \
            CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D0F,        \
            METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This `IOCTL` is used for testing the event handling code and to verify that the application thread is released when the shared UserEvent is signaled by the WDT driver. This `IOCTL` exists mainly for application developers to debug their application.

IOCTL_GET_STATUS

```
#define IOCTL_SET_MODE                          \
        CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D15,        \
        METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL accepts an unsigned long integer, sets to 0 or 1, and uses it to set the WDT mode. If the input is 0, then the WDT is set to Watch Dog Timer mode. If the input is 1, then the WDT is set to free running mode.

IOCTL_GET_TIMEOUT_STATUS

```
#define IOCTL_GET_TIMEOUT_STATUS                \
        CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D16,        \
        METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL accepts an unsigned long integer and uses it as both input and output.

As an input parameter, if the integer is set to 1, then the time out bit on the WDT device will be reset.

As an output parameter, the integer is set to 1 if both stage 1 and stage 2 timers have expired.

IOCTL_GET_STAGE_1_TIMEOUT_STATUS

```
#define IOCTL_GET_STAGE_1_TIMEOUT_STATUS        \
        CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D17,        \
        METHOD_BUFFERED, FILE_ANY_ACCESS )
```

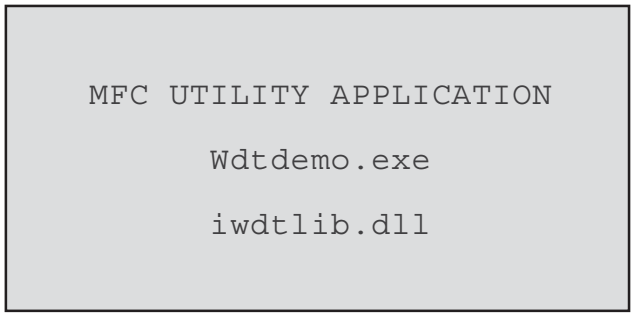
This IOCTL accepts an unsigned long integer and uses it as both input and output.

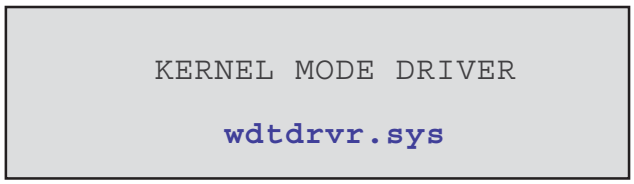
As an input parameter, if the integer is set to 1, then the time out bit on the WDT device will be reset.

As an output parameter, the integer is set to 1 if the stage 1 timer has expired.

5.4 Watch Dog Timer Windows® XP Demo Utility

This specification describes the WDT demo utility “Wdtdemo.exe”. The demo tool is a MFC based dialog application that is used to control and monitor the WDT device in the Microsoft* Windows* OS environment. Wdtdemo.exe is to be used only for demonstration of the WDT’s functionality and should not be used as a customer solution.

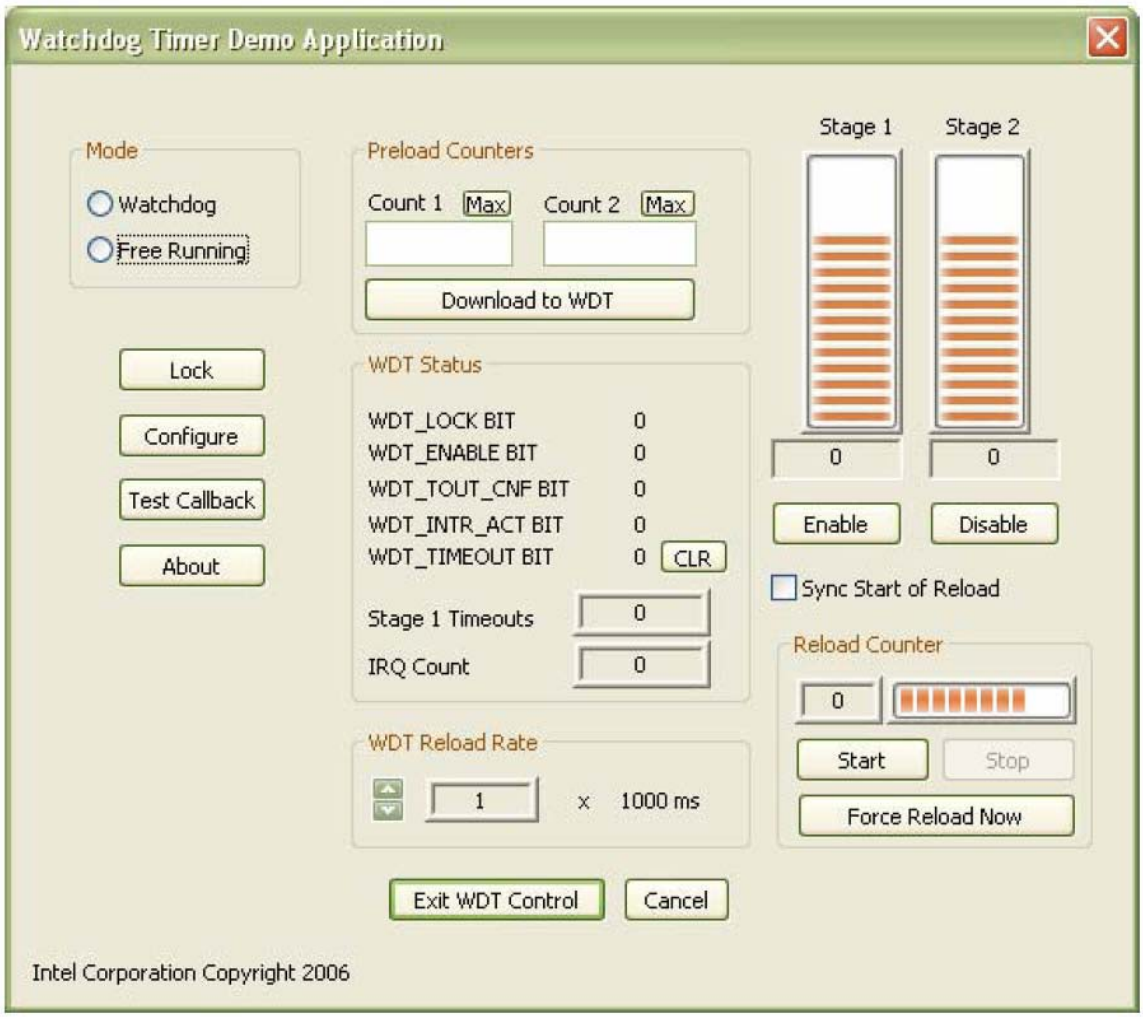




5.5 Using the Demo Application

The Wdtdemo.exe application has a number of buttons and text entry fields for configuring and controlling the Watch Dog Timer (WDT). Each of the following items has a corresponding button or entry field on the application screen.

- Setting the mode [Mode]
- Locking the WDT device [LOCK]
- Configuring the WDT device [Configure]
- Testing the user mode call function [Test Callback]
- Retrieving the driver and dynamic link version number [Lib Version]
- Downloading the Stage 1 and Stage 2 time-out values [Preload Counters]
- Information about WDT [WDT Status]
- Setting the refresh rate [WDT Reload Rate]
- Starting and Stopping the refresh of the WDT [Enable] [Disable]
- Synchronizing the start of reload [Synch Start of Reload]
- Starting and Stopping the reload counter [Reload Counter]



5.5.1 Setting the Mode

The mode can be set to either Watch Dog Mode or Free Running Mode using the radio select button at the upper left of the dialog.

5.5.2 Locking the WDT Device

The WDT can be locked by software. The LOCK button locks the WDT so that no further changes to the configuration registers are possible until a system reset. A locked WDT cannot be enabled or disabled.

5.5.3 Configuring the WDT

Click the configure button to program the following three configuration options:

Output Enable, Set Prescalar and Interrupt Routing.

[Output Enable]

Enables or disables the toggling of the external output pin if the WDT times out.

[Set Prescalar]

Specifies a prescalar value for the 35-bit, count-down counter. The default value is 34:15. See the *WDT Driver Specification* for details on pre-scalar.

[Interrupt Routing]

Select one of the three interrupt methods (SERIRQ, NMI, or SMI) or "Disabled" to disable interrupt. When SERIRQ is selected, the System BIOS designated interrupt is retrieved from the WDT.

5.5.4 Testing the User Mode Call Function

This button verifies that the interrupt handler and callback mechanism are working correctly. Clicking the Test Callback button increments the Stage 1 interrupt count.

5.5.5 Retrieving the Driver and Dynamic Link Version Number

Click the Lib Version button to retrieve the driver and dynamic link version number.

5.5.6 Downloading the Stage 1 and Stage 2 Time-out Values

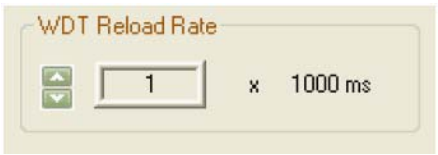
There are two edit boxes that specify Stage 1 and Stage 2 count-down values. Enter the values and then click the Download to WDT button to program the values from the application to the WDT device. Both counters are 35-bit counters that decrement using a 20-bit prescalar.

5.5.7 Information about WDT

This area shows status of the WDT.

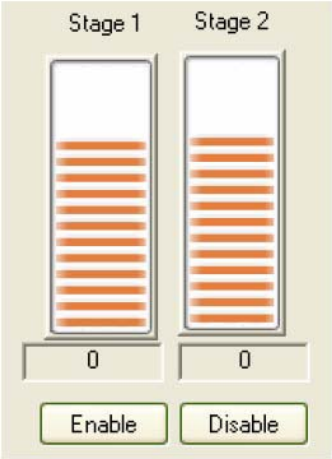
5.5.8 Setting the Reload Rate

The reload rate is set by using the button control that is in the lower center of the application. The rate can be adjusted from between 0 and 100 seconds.



5.5.9 Starting and Stopping the Refresh of the WDT

Clicking the Enable button starts the WDT counting down. Click the Disable button to stop the WDT from counting down.



5.5.10 Starting and Stopping the reload counter

Click the Start button to begin refreshing the WDT. Click the Stop button to stop refreshing the WDT. You can force an immediate refresh of the WDT by clicking the Force Reload Now button. To prevent Stage 1 or Stage 2 timeouts you must start “refresh” and have a refresh rate that ensures that the timer is refreshed before the first stage and or second stage time out.

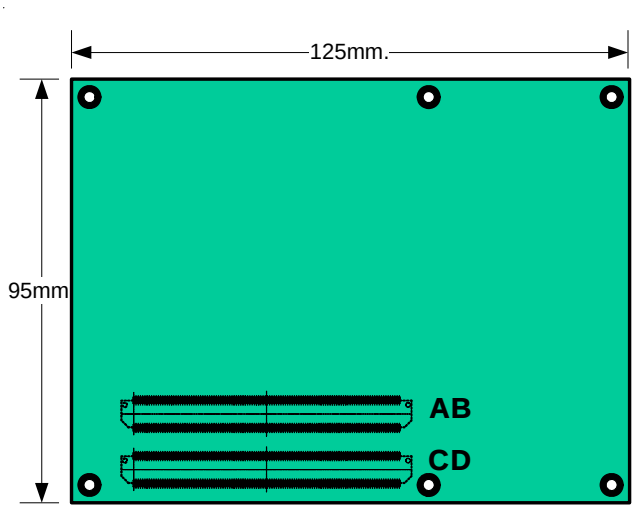
6 Connectors

6.1 COM Express® Type 2

All pin-outs on AB and CD connector of the Express-IW400 comply with pin-out and signal descriptions used in the original "PICMG® COM.0 R1.0: COM Express Module Base Specification". This document contains a description of pin-outs, signal descriptions, and mechanical characteristics of the COM Express® (Expresss®) formfactor.

An additional document, " Express® Design Guide" gives a general introduction to carrier board designs for COM Express® (Express®) modules.

AB Connector
1 Gigabit Ethernet port
LPC interface
4 Serial ATA channels
High Definition Audio
8 USB 2.0 ports
3 PCI Express Lanes x1
Dual 24-bit LVDS channels
Analog VGA
TV-out ports (SDTV/HDTV)
8 GPIO pins
+12V primary power input
+5V standby and 3V RTC

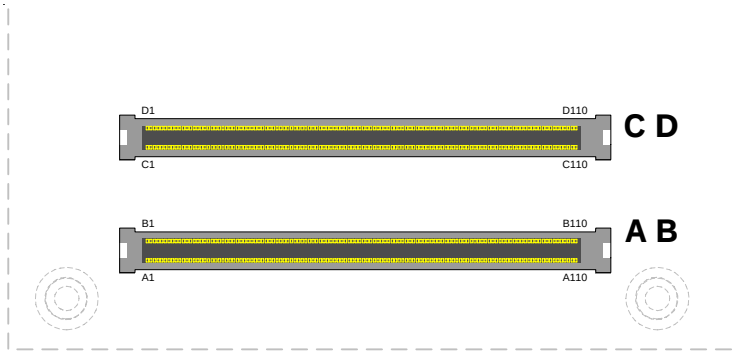


CD Connector
Parallel ATA, IDE port alternate definition assigns this to 2 additional Gigabit Ethernet ports
32-bit PCI v2.3 bus alternate definition assigns this to 10 additional PCI Express x1 lanes
PCI Express x16 for Graphics these pins can also be assigned to two SDVO extensions (multiplexed)
SMB and I^2C bus
Power / Thermal control
+12V primary power input

6.2 COM Express® Board to Board Connectors

Signals and Pin-out for:

Basic formfactor, Type 2



Row A			Row B	
Pin No.	Pin Name		Pin No.	Pin Name
A1	GND (FIXED)		B1	GND (FIXED)
A2	GBE0_MDI3-		B2	GBE0_ACT#
A3	GBE0_MDI3+		B3	LPC_FRAME#
A4	GBE0_LINK100#		B4	LPC_AD0
A5	GBE0_LINK1000#		B5	LPC_AD1
A6	GBE0_MDI2-		B6	LPC_AD2
A7	GBE0_MDI2+		B7	LPC_AD3
A8	NC		B8	LPC_DRQ1#
A9	GBE0_MDI1-		B9	LPC_DRQ1#
A10	GBE0_MDI1+		B10	LPC_CLK
A11	GND (FIXED)		B11	GND (FIXED)
A12	GBE0_MDI0-		B12	PWRBTN#
A13	GBE0_MDI0+		B13	SMB_CK
A14	GBE0_CTREF		B14	SMB_DAT
A15	SUS_S3#		B15	SMB_ALERT#
A16	SATA0_TX+		B16	SATA1_TX+
A17	SATA0_TX-		B17	SATA1_TX-
A18	SUS_S4#		B18	SUS_STAT#
A19	SATA0_RX+		B19	SATA1_RX+
A20	SATA0_RX-		B20	SATA1_RX-
A21	GND (FIXED)		B21	GND (FIXED)
A22	SATA2_TX+		B22	SATA3_TX+
A23	SATA2_TX-		B23	SATA3_TX-
A24	SUS_S5#		B24	PWR_OK
A25	SATA2_RX+		B25	SATA3_RX+
A26	SATA2_RX-		B26	SATA3_RX-
A27	BATLOW#		B27	WDT
A28	ATA_ACT#		B28	NC
A29	NC		B29	NC
A30	NC		B30	NC
A31	GND (FIXED)		B31	GND (FIXED)
A32	NC		B32	SPKR
A33	NC		B33	I2C_CK
A34	BIOS_DISABLE#		B34	I2C_DAT
A35	THRMTRIP#		B35	THRM#
A36	NC		B36	NC
A37	NC		B37	NC
A38	NC		B38	USB_4_5_OC#
A39	USB4- Client		B39	NC
A40	USB4+ Client		B40	NC
A41	GND (FIXED)		B41	GND (FIXED)
A42	USB2-		B42	USB3-
A43	USB2+		B43	USB3+
A44	USB_2_3_OC#		B44	USB_0_1_OC#
A45	USB0-		B45	USB1-
A46	USB0+		B46	USB1+
A47	VCC_RTC		B47	EXCD1_PERST#
A48	EXCD0_PERST#		B48	EXCD1_CPPE#
A49	EXCD0_CPPE#		B49	SYS_RESET#
A50	LPC_SERIRQ		B50	CB_RESET#

Row C			Row D	
Pin No.	Pin Name		Pin No.	Pin Name
C1	GND FIXED)		D1	GND FIXED)
C2	IDE_D7		D2	IDE_D5
C3	IDE_D6		D3	IDE_D10
C4	IDE_D3		D4	IDE_D11
C5	IDE_D15		D5	IDE_D12
C6	IDE_D8		D6	IDE_D4
C7	IDE_D9		D7	IDE_D0
C8	IDE_D2		D8	IDE_REQ
C9	IDE_D13		D9	IDE_IOW#
C10	IDE_D1		D10	IDE_ACK#
C11	GND (FIXED)		D11	GND (FIXED)
C12	IDE_D14		D12	IDE_IRQ
C13	IDE_IORDY		D13	IDE_A0
C14	IDE_IOR#		D14	IDE_A1
C15	PCI_PME#		D15	IDE_A2
C16	PCI_GNT2#		D16	IDE_CS1#
C17	PCI_REQ2#		D17	IDE_CS3#
C18	PCI_GNT1#		D18	IDE_RESET#
C19	PCI_REQ1#		D19	PCI_REQ3#
C20	PCI_GNT0#		D20	PCI_GNT3#
C21	GND (FIXED)		D21	GND (FIXED)
C22	PCI_REQ0#		D22	PCI_AD1
C23	PCI_RESET#		D23	PCI_AD3
C24	PCI_AD0		D24	PCI_AD5
C25	PCI_AD2		D25	PCI_AD7
C26	PCI_AD4		D26	PCI_C/BE0#
C27	PCI_AD6		D27	PCI_AD9
C28	PCI_AD8		D28	PCI_AD11
C29	PCI_AD10		D29	PCI_AD13
C30	PCI_AD12		D30	PCI_AD15
C31	GND (FIXED)		D31	GND (FIXED)
C32	PCI_AD14		D32	PCI_PAR
C33	PCI_C/BE1#		D33	PCI_SERR#
C34	PCI_PERR#		D34	PCI_STOP#
C35	PCI_LOCK#		D35	PCI_TRDY#
C36	PCI_DEVSEL#		D36	PCI_FRAME#
C37	PCI_IRDY#		D37	PCI_AD16
C38	PCI_C/BE2#		D38	PCI_AD18
C39	PCI_AD17		D39	PCI_AD20
C40	PCI_AD19		D40	PCI_AD22
C41	GND (FIXED)		D41	GND (FIXED)
C42	PCI_AD21		D42	PCI_AD24
C43	PCI_AD23		D43	PCI_AD26
C44	PCI_C/BE3#		D44	PCI_AD28
C45	PCI_AD25		D45	PCI_AD30
C46	PCI_AD27		D46	PCI_IRQC#
C47	PCI_AD29		D47	PCI_IRQD#
C48	PCI_AD31		D48	PCI_CLKRUN#
C49	PCI_IRQA#		D49	PCI_M66EN
C50	PCI_IRQB#		D50	PCI_CLK

COM Express Pin-out (cont'd)

Row A			Row B	
Pin No.	Pin Name		Pin No.	Pin Name
A51	GND (FIXED)		B51	GND (FIXED)
A52	NC		B52	NC
A53	NC		B53	NC
A54	GPI0		B54	GPO1
A55	NC		B55	NC
A56	NC		B56	NC
A57	GND		B57	GPO2
A58	NC		B58	NC
A59	NC		B59	NC
A60	GND (FIXED)		B60	GND (FIXED)
A61	PCIE_TX2+		B61	PCIE_RX2+
A62	PCIE_TX2-		B62	PCIE_RX2-
A63	GPI1		B63	GPO3
A64	PCIE_TX1+		B64	PCIE_RX1+
A65	PCIE_TX1-		B65	PCIE_RX1-
A66	GND		B66	WAKE0#
A67	GPI2		B67	WAKE1#
A68	PCIE_TX0+		B68	PCIE_RX0+
A69	PCIE_TX0-		B69	PCIE_RX0-
A70	GND (FIXED)		B70	GND (FIXED)
A71	NC		B71	NC
A72	NC		B72	NC
A73	NC		B73	NC
A74	NC		B74	NC
A75	NC		B75	NC
A76	NC		B76	NC
A77	NC		B77	NC
A78	NC		B78	NC
A79	NC		B79	NC
A80	GND (FIXED)		B80	GND (FIXED)
A81	NC		B81	NC
A82	NC		B82	NC
A83	NC		B83	NC
A84	NC		B84	VCC_5V_SBY
A85	GPI3		B85	VCC_5V_SBY
A86	KBD_RST#		B86	VCC_5V_SBY
A87	KBD_A20GATE		B87	VCC_5V_SBY
A88	PCIE0_CK_REF+		B88	RSVD
A89	PCIE0_CK_REF-		B89	NC
A90	GND (FIXED)		B90	GND (FIXED)
A91	RSVD		B91	NC
A92	RSVD		B92	NC
A93	GPO0		B93	NC
A94	RSVD		B94	NC
A95	RSVD		B95	NC
A96	GND		B96	NC
A97	VCC_12V		B97	NC
A98	VCC_12V		B98	NC
A99	VCC_12V		B99	NC
A100	GND (FIXED)		B100	GND (FIXED)
A101	VCC_12V		B101	VCC_12V
A102	VCC_12V		B102	VCC_12V
A103	VCC_12V		B103	VCC_12V
A104	VCC_12V		B104	VCC_12V
A105	VCC_12V		B105	VCC_12V
A106	VCC_12V		B106	VCC_12V
A107	VCC_12V		B107	VCC_12V
A108	VCC_12V		B108	VCC_12V
A109	VCC_12V		B109	VCC_12V
A110	GND (FIXED)		B110	GND (FIXED)

Row C			Row D	
Pin No.	Pin Name		Pin No.	Pin Name
C51	GND (FIXED)		D51	GND (FIXED)
C52	PEG_RX0+		D52	PEG_TX0+
C53	PEG_RX0-		D53	PEG_TX0-
C54	NC		D54	NC
C55	PEG_RX1+		D55	PEG_TX1+
C56	PEG_RX1-		D56	PEG_TX1-
C57	NC		D57	NC
C58	PEG_RX2+		D58	PEG_TX2+
C59	PEG_RX2-		D59	PEG_TX2-
C60	GND (FIXED)		D60	GND (FIXED)
C61	PEG_RX3+		D61	PEG_TX3+
C62	PEG_RX3-		D62	PEG_TX3-
C63	RSVD		D63	RSVD
C64	RSVD		D64	RSVD
C65	PEG_RX4+		D65	PEG_TX4+
C66	PEG_RX4-		D66	PEG_TX4-
C67	RSVD		D67	GND
C68	PEG_RX5+		D68	PEG_TX5+
C69	PEG_RX5-		D69	PEG_TX5-
C70	GND (FIXED)		D70	GND (FIXED)
C71	PEG_RX6+		D71	PEG_TX6+
C72	PEG_RX6-		D72	PEG_TX6-
C73	NC		D73	NC
C74	PEG_RX7+		D74	PEG_TX7+
C75	PEG_RX7-		D75	PEG_TX7-
C76	GND		D76	GND
C77	RSVD		D77	IDE_CBLID#
C78	NC		D78	NC
C79	NC		D79	NC
C80	GND (FIXED)		D80	GND (FIXED)
C81	NC		D81	NC
C82	NC		D82	NC
C83	RSVD		D83	RSVD
C84	GND		D84	GND
C85	NC		D85	NC
C86	NC		D86	NC
C87	GND		D87	GND
C88	NC		D88	NC
C89	NC		D89	NC
C90	GND (FIXED)		D90	GND (FIXED)
C91	NC		D91	NC
C92	NC		D92	NC
C93	GND		D93	GND
C94	NC		D94	NC
C95	NC		D95	NC
C96	GND		D96	GND
C97	RSVD		D97	NC
C98	NC		D98	NC
C99	NC		D99	NC
C100	GND (FIXED)		D100	GND (FIXED)
C101	NC		D101	NC
C102	NC		D102	NC
C103	GND		D103	GND
C104	VCC_12V		D104	VCC_12V
C105	VCC_12V		D105	VCC_12V
C106	VCC_12V		D106	VCC_12V
C107	VCC_12V		D107	VCC_12V
C108	VCC_12V		D108	VCC_12V
C109	VCC_12V		D109	VCC_12V
C110	GND (FIXED)		D110	GND (FIXED)

6.3 Signal Descriptions

Row A

Pin	Signal	Description	Type	PU/PD	Comment
A1	GND	Ground	PWR	-	-
A2	GBE0_MDI3-	Ethernet Receive Data -	I/O - DP	-	-
A3	GBE0_MDI3+	Ethernet Receive Data +	I/O - DP	-	-
A4	GBE0_LINK100#	Ethernet Speed LED (100Mb)	O-3,3	-	On at 100Mb/s
A5	GBE0_LINK1000#	Ethernet Speed LED (1000Mb)	O-3,3	-	On at 1000Mb/s
A6	GBE0_MDI2-	Ethernet Receive Data -	I/O - DP	-	-
A7	GBE0_MDI2+	Ethernet Receive Data +	I/O - DP	-	-
A8	GBE0_LINK#	LAN Link LED	NC	-	-
A9	GBE0_MDI1-	Ethernet Receive Data -	I/O - DP	-	-
A10	GBE0_MDI1+	Ethernet Receive Data +	I/O - DP	-	-
A11	GND	Ground	PWR	-	-
A12	GBE0_MDI0-	Ethernet Receive Data -	I/O - DP	-	-
A13	GBE0_MDI0+	Ethernet Receive Data +	I/O - DP	-	-
A14	GBE0_CTREF	ETHCTREF	O-2,5	-	-
A15	SUS_S3#	PM_SLP_S#3	O-3,3	-	-
A16	SATA0_TX+	SATA0_TX+ | SATA 0 Transmit Data +	O - DP	-	-
A17	SATA0_TX-	SATA0_TX- | SATA 0 Transmit Data -	O - DP	-	-
A18	SUS_S4#	PM_SLP_S#4	O-3,3	-	-
A19	SATA0_RX+	SATA0_RX+ | SATA 0 Receive Data +	I - DP	-	-
A20	SATA0_RX-	SATA0_RX - | SATA 0 Receive Data -	I - DP	-	-
A21	GND	Ground	PWR	-	-
A22	SATA2_TX+	SATA0_TX+ | SATA 2 Transmit Data +	O - DP	-	-
A23	SATA2_TX-	SATA0_TX- | SATA 2 Transmit Data -	O - DP	-	-
A24	SUS_S5#	PM_SLP_S#5	O-3,3	-	-
A25	SATA2_RX+	SATA0_RX+ | SATA 2 Receive Data +	I - DP	-	-
A26	SATA2_RX-	SATA0_RX- | SATA 2 Receive Data -	I - DP	-	-
A27	BATLOW#	PM_BATLOW# | Battery Low	I-3,3	PU 8k2 3,3VSB	-
A28	ATA_ACT#	ATA_LED# | SATA LED	O-3,3	PU 1k 3,3V	-
A29	AC_SYNC	AC_SYNC | AC'97 Sync	NC	-	-
A30	AC_RST#	AC_RST# | AC'97 Reset	NC	-	-
A31	GND	Ground	PWR	-	-
A32	AC_BITCLK	AC_BITCLK | AC'97 Clock	NC	-	-
A33	AC_SDOUT	AC_SDATAOUT | AC'97 Data	NC	-	-
A34	BIOS_DISABLE#	BIOS_DISABLE#	I-3,3	PU 4k7 3,3V	-
A35	THRMTRIP#	PM_THRMTRIP#_CON	O-3,3	PU 330 3,3V	-
A36	USB6-	USB_PN6 | USB Data – Port6	NC	-	-
A37	USB6+	USB_PP6 | USB Data + Port6	NC	-	-
A38	USB_6_7_OC#	USB_OC#_6_7 | USB OverCurrent Port 6/7	NC		-
A39	USB4-	USB_PN4 | USB Data - Port4	I/O - DP	-	-
A40	USB4+	USB_PP4 | USB Data + Port4	I/O - DP	-	-
A41	GND	Ground	PWR	-	-
A42	USB2-	USB_PN2 | USB Data - Port2	I/O - DP		-
A43	USB2+	USB_PP2 | USB Data + Port2	I/O - DP	-	-
A44	USB_2_3_OC#	USB_OC#_2_3 | USB OverCurrent Port 2/3	I-3,3	PU 10k 3,3VSB	-
A45	USB0-	USB_PN0 | USB Data - Port0	I/O - DP	-	-
A46	USB0+	USB_PP0 | USB Data + Port0	I/O - DP	-	-
A47	VCC_RTC	V_BAT	PWR	-	-
A48	EXCD0_PERST#	Express Card Support [0] |card reset	O-3,3	PU 10k 3,3VSB	-
A49	EXCD0_CPPE#	Express Card Support [0] | capable c. request	I-3,3	PU 8.2k 3,3V	-
A50	LPC_SERIRQ	INT_SERIRQ | Serial Interrupt Request	IO-3,3	-	-
A51	GND	Ground	PWR	-	-
A52	PCIE5_TX+	PCI Express lane 5 +	NC	-	-
A53	PCIE5_TX-	PCI Express lane 5 -	NC	-	-
A54	GPI0	General Purpose Input 0	I-3,3	PU 8k2 3,3V	-
A55	PCIE4_TX+	PCI Express lane 4 +	NC	-	-

Signal Descriptions (cont'd)

Row A

Pin	Signal	Description	Type	PU/PD	Comment
A56	PCIE4_TX-	PCI Express lane 4 -	NC	-	-
A57	GND	Ground	PWR	-	-
A58	PCIE3_TX+	PCI Express lane 3 + (used by LAN)	NC	-	-
A59	PCIE3_TX-	PCI Express lane 3 - (used by LAN)	NC	-	-
A60	GND	Ground	PWR	-	-
A61	PCIE2_TX+	PCI Express lane 2 +	O - DP	-	-
A62	PCIE2_TX-	PCI Express lane 2 -	O - DP	-	-
A63	GPI1	General Purpose Input 1	I-3,3	PU 8k2 3,3V	-
A64	PCIE1_TX+	PCI Express lane 1 +	O - DP	-	-
A65	PCIE1_TX-	PCI Express lane 1 -	O - DP	-	-
A66	GND	Ground	PWR	-	-
A67	GPI2	General Purpose Input 2	I-3,3	PU 8k2 3,3V	-
A68	PCIE0_TX+	PCI Express lane 0 +	O - DP	-	-
A69	PCIE0_TX-	PCI Express lane 0 -	O - DP	-	-
A70	GND	Ground	PWR	-	-
A71	LVDS_A0+	LVDS_AP0 | LVDS Channel A	NC	-	-
A72	LVDS_A0-	LVDS_AN0 | LVDS Channel A	NC	-	-
A73	LVDS_A1+	LVDS_AP1 | LVDS Channel A	NC	-	-
A74	LVDS_A1-	LVDS_AN1 | LVDS Channel A	NC	-	-
A75	LVDS_A2+	LVDS_AP2 | LVDS Channel A	NC	-	-
A76	LVDS_A2-	LVDS_AN2 | LVDS Channel A	NC	-	-
A77	LVDS_VDD_EN	LVDS_VDDEN | LVDS Panel Power	NC	-	-
A78	LVDS_A3+	LVDS_AP3 | LVDS Channel A	NC	-	-
A79	LVDS_A3-	LVDS_AN3 | LVDS Channel A	NC	-	-
A80	GND	Ground	PWR	-	-
A81	LVDS_A_CK+	LVDS_CLKAP | LVDS Channel A	NC	-	-
A82	LVDS_A_CK-	LVDS_CLKAN | LVDS Channel A	NC	-	-
A83	LVDS_I2C_CK	LVDS_DDCPCLK | JILI I2C Clock	NC	-	-
A84	LVDS_I2C_DAT	LVDS_DDCPDATA | JILI I2C Data	NC	-	-
A85	GPI3	General Purpose Input 3	I-3,3	PU 8k2 3,3V	-
A86	KBD_RST#	H_RCIN# | Keyboard Reset	I-3,3	-	-
A87	KBD_A20GATE	H_A20GATE	I-3,3	-	-
A88	PCIE_CK_REF+	CLK_PCIE_REF P	O - DP	-	-
A89	PCIE_CK_REF-	CLK_PCIE_REF N	O - DP	-	-
A90	GND	Ground	PWR	-	-
A91	RSVD	-	NC	-	-
A92	RSVD	-	NC	-	-
A93	GPO0	General Purpose Output 0	O-3,3	-	-
A94	RSVD	-	NC	-	-
A95	RSVD	-	NC	-	-
A96	GND	Ground	PWR	-	-
A97	VCC_12V	Power 12V	PWR	-	-
A98	VCC_12V	Power 12V	PWR	-	-
A99	VCC_12V	Power 12V	PWR	-	-
A100	GND	Ground	PWR	-	-
A101	VCC_12V	Power 12V	PWR	-	-
A102	VCC_12V	Power 12V	PWR	-	-
A103	VCC_12V	Power 12V	PWR	-	-
A104	VCC_12V	Power 12V	PWR	-	-
A105	VCC_12V	Power 12V	PWR	-	-
A106	VCC_12V	Power 12V	PWR	-	-
A107	VCC_12V	Power 12V	PWR	-	-
A108	VCC_12V	Power 12V	PWR	-	-
A109	VCC_12V	Power 12V	PWR	-	-
A110	GND	Ground	PWR	-	-

Signal Descriptions (cont'd)

Row B

Pin	Signal	Description	Type	PU/PD	Comment
B1	GND	Ground	PWR	-	-
B2	GBE0_ACT#	LAN_ACTLED# | Ethernet Activity LED	O-3,3	-	-
B3	LPC_FRAME#	LPC_FRAME# | LPC Frame Indicator	O-3,3	-	-
B4	LPC_AD0	LPC_AD0 | LPC Adress & DATA Bus	IO-3,3	-	-
B5	LPC_AD1	LPC_AD1 | LPC Adress & DATA Bus	IO-3,3	-	-
B6	LPC_AD2	LPC_AD2 | LPC Adress & DATA Bus	IO-3,3	-	-
B7	LPC_AD3	LPC_AD3 | LPC Adress & DATA Bus	IO-3,3	-	-
B8	LPC_DRQ0#	SIO_DRQ#0 | LPC Request 0	I-3,3	-	-
B9	LPC_DRQ1#	SIO_DRQ#1 | LPC Request 1	I-3,3	PU 8k2 3,3V	-
B10	LPC_CLK	CLK_SIOEXTPCI	O-3,3	-	-
B11	GND	Ground	I-3,3	-	-
B12	PWRBTN#	Power Button	I-3,3	PU 10k 3,3VSB	-
B13	SMB_CK	SMBUS Clock	O-3,3	PU 1k2 3,3V	-
B14	SMB_DAT	SMBUS Data	IO-3,3	PU 1k2 3,3V	-
B15	SMB_ALERT#	SMB_ALERT#	I-3,3	PU 8k2 3,3VSB	-
B16	SATA1_TX+	SATA1_TX+	O - DP	-	-
B17	SATA1_TX-	SATA1_TX-	O - DP	-	-
B18	SUS_STAT#	PM_SUS_ STAT#	O-3,3	-	-
B19	SATA1_RX+	SATA1_RX+	I - DP	-	-
B20	SATA1_RX-	SATA1_RX-	I - DP	-	-
B21	GND	Ground	PWR	-	-
B22	SATA3_TX+	SATA3_TX+	O - DP	-	-
B23	SATA3_TX-	SATA3_TX-	O - DP	-	-
B24	PWR_OK	Power OK	I-3,3	PU 10k 3,3VSB	-
B25	SATA3_RX+	SATA3_RX+	I - DP	-	-
B26	SATA3_RX-	SATA3_RX-	I - DP	-	-
B27	WDT	Watch Dog Timer	O-3,3	PU 4k7 3,3V	-
B28	AC_SDIN2	AC_SDATAIN2	NC	-	-
B29	AC_SDIN1	AC_SDATAIN1	NC	-	-
B30	AC_SDIN0	AC_SDATAIN0	NC	-	-
B31	GND	Ground	PWR	-	-
B32	SPKR	AC_SPKR	O-3,3	-	-
B33	I2C_CK	I2CLK	O-3,3	PU 1k2 3,3V	-
B34	I2C_DAT	I2DAT	IO-3,3	PU 1k2 3,3V	-
B35	THRM#	PM THRM# CON | Over Temperature	I-3,3	PU 1k 1,05V	-
B36	USB7-	USB_PN7 | USB Data – Port7	NC	-	-
B37	USB7+	USB_PP7 | USB Data + Port7	NC	-	-
B38	USB_4_5_OC#	USB_OC#_4_5 | USB OverCurrent Port	I-3,3	PU 100k 3,3VSB	-
B39	USB5-	USB_PN5 | USB Data- Port5	NC	-	-
B40	USB5+	USB_PP5 | USB Data+ Port5	NC	-	-
B41	GND	Ground	PWR	-	-
B42	USB3-	USB_PN3 | USB Data- Port3	I/O - DP	-	-
B43	USB3+	USB_PP3 | USB Data+ Port3	I/O - DP	-	-
B44	USB_0_1_OC#	USB_OC#_0_1 | USB OverCurrent Port	I-3,3	PU 10k 3,3VSB	-
B45	USB1-	USB_PN1 | USB Data- Port1	I/O - DP	-	-
B46	USB1+	USB_PP1 | USB Data+ Port1	I/O - DP	-	-
B47	EXCD1_PERST#	Express Card Support [1]|card reset	O-3,3	PU 10k 3,3VSB	-
B48	EXCD1_CPPE#	Express Card Support [1]| capable c.	I-3,3	PU 8k2 3,3V	-
B49	SYS_RESET#	ETX_SYS_RESET# | Reset Input	I-3,3	PU 10k 3,3VSB	-
B50	CB_RESET#	PCI_RST# | PCI Bus Reset	O-3,3	-	-
B51	GND	Ground	PWR	-	-
B52	PCIE5_RX+	BOM option (LAN on PCIe 5)	NC	-	-
B53	PCIE5_RX-	BOM option (LAN on PCIe 5)	NC	-	-
B54	GPO1	General Purpose Output 1	O-3,3	-	-
B55	PCIE4_RX+	PCI Express lane 4 + Recieve	NC	-	-

Signal Descriptions (cont'd)

Row B

Pin	Signal	Description	Type	PU/PD	Comment
B56	PCIE4_RX-	PCI Express lane 4 - Recieve	NC	-	-
B57	GPO2	General Purpose Output 2	O-3,3	-	-
B58	PCIE3_RX+	PCI Express lane 3 + Recieve	NC	-	-
B59	PCIE3_RX-	PCI Express lane 3 - Recieve	NC	-	-
B60	GND	Ground	PWR	-	-
B61	PCIE2_RX+	PCI Express lane 2 + Recieve	I - DP	-	-
B62	PCIE2_RX-	PCI Express lane 2 - Recieve	I - DP	-	-
B63	GPO3	General Purpose Output 3	O-3,3	-	-
B64	PCIE1_RX+	PCI Express lane 1 + Recieve	I - DP	-	-
B65	PCIE1_RX-	PCI Express lane 1 - Recieve	I - DP	-	-
B66	WAKE0#	PCIE_WAKEI#	I-3,3	PU 1k 3,3VSB	-
B67	WAKE1#	WAKE1#	I-3,3	PU 8k2 3,3VSB	-
B68	PCIE0_RX+	PCI Express lane 0 + Recieve	I - DP	-	-
B69	PCIE0_RX-	PCI Express lane 0 - Recieve	I - DP	-	-
B70	GND	Ground	PWR	-	-
B71	LVDS_B0+	LVDS_BP0 | LVDS Channel B Data0+	NC	-	-
B72	LVDS_B0-	LVDS_BN0 | LVDS Channel B Data0-	NC	-	-
B73	LVDS_B1+	LVDS_BP1 | LVDS Channel B Data1+	NC	-	-
B74	LVDS_B1-	LVDS_BN1 | LVDS Channel B Data1-	NC	-	-
B75	LVDS_B2+	LVDS_BP2 | LVDS Channel B Data2+	NC	-	-
B76	LVDS_B2-	LVDS_BN2 | LVDS Channel B Data2-	NC	-	-
B77	LVDS_B3+	LVDS_BP3 | LVDS Channel B Data3+	NC	-	-
B78	LVDS_B3-	LVDS_BN3 | LVDS Channel B Data3-	NC	-	-
B79	LVDS_BKLT_EN	Panel Backlight ON	NC	-	-
B80	GND	Ground	PWR	-	-
B81	LVDS_B_CK+	LVDS_CLKBP | LVDS Channel B	NC	-	-
B82	LVDS_B_CK-	LVDS_CLKBM | LVDS Channel B	NC	-	-
B83	LVDS_BKLT_CTRL	Backlight Brightness	NC	-	-
B84	VCC_5V_SBY	5V Standby	PWR	-	-
B85	VCC_5V_SBY	5V Standby	PWR	-	-
B86	VCC_5V_SBY	5V Standby	PWR	-	-
B87	VCC_5V_SBY	5V Standby	PWR	-	-
B88	RSVD	-	NC	-	-
B89	VGA_RED	Analog Video RGB-RED	NC	-	-
B90	GND	Ground	PWR	-	-
B91	VGA_GRN	Analog Video RGB-GREEN	NC	-	-
B92	VGA_BLU	Analog Video RGB-BLUE	NC	-	-
B93	VGA_HSYNC	Analog Video H-Sync	NC	-	-
B94	VGA_VSYNC	Analog Video V-Sync	NC	-	-
B95	VGA_I2C_CK	Display Data Channel	NC	-	-
B96	VGA_I2C_DAT	Display Data	NC	-	-
B97	TV_DAC_A	Composite CVBS	NC	-	-
B98	TV_DAC_B	TV Luminance Signal	NC	-	-
B99	TV_DAC_C	TV Chrominance Signal	NC	-	-
B100	GND	Ground	PWR	-	-
B101	VCC_12V	Power 12V	PWR	-	-
B102	VCC_12V	Power 12V	PWR	-	-
B103	VCC_12V	Power 12V	PWR	-	-
B104	VCC_12V	Power 12V	PWR	-	-
B105	VCC_12V	Power 12V	PWR	-	-
B106	VCC_12V	Power 12V	PWR	-	-
B107	VCC_12V	Power 12V	PWR	-	-
B108	VCC_12V	Power 12V	PWR	-	-
B109	VCC_12V	Power 12V	PWR	-	-
B110	GND	Ground	PWR	-	-

Signal Descriptions (cont'd)

Row C

Pin	Signal	Description	Type	PU/PD	Comment
C1	GND	Ground	PWR	-	-
C2	IDE_D7	IDE Data Bus	IO	PD 10K	-
C3	IDE_D6	IDE Data Bus	IO	-	-
C4	IDE_D3	IDE Data Bus	IO	-	-
C5	IDE_D15	IDE Data Bus	IO	-	-
C6	IDE_D8	IDE Data Bus	IO	-	-
C7	IDE_D9	IDE Data Bus	IO	-	-
C8	IDE_D2	IDE Data Bus	IO	-	-
C9	IDE_D13	IDE Data Bus	IO	-	-
C10	IDE_D1	IDE Data Bus	IO	-	-
C11	GND	Ground	PWR	-	-
C12	IDE_D14	IDE Data Bus	IO	-	-
C13	IDE_IORDY	IDE Ready	I-3,3	PU 4K7 3,3V	-
C14	IDE_IOR#	IDE IO Read	O-3,3	-	-
C15	PCI_PME#	PCI Power Management Event	IO-3,3	-	-
C16	PCI_GNT2#	PCI Bus Grant 2	O-3,3	-	-
C17	PCI_REQ2#	PCI Bus Request 2	I-3,3	-	-
C18	PCI_GNT1#	PCI Bus Grant 1	O-3,3	-	-
C19	PCI_REQ1#	PCI Bus Request 1	I-3,3	-	-
C20	PCI_GNT0#	PCI Bus Grant 0	O-3,3	-	-
C21	GND	Ground	PWR	-	-
C22	PCI_REQ0#	PCI Bus Reqest 0	I-3,3	-	-
C23	PCI_RESET#	PCI Bus Reset	O-3,3	-	-
C24	PCI_AD0	PCI Adress & Data Bus line	IO-3,3	-	-
C25	PCI_AD2	PCI Adress & Data Bus line	IO-3,3	-	-
C26	PCI_AD4	PCI Adress & Data Bus line	IO-3,3	-	-
C27	PCI_AD6	PCI Adress & Data Bus line	IO-3,3	-	-
C28	PCI_AD8	PCI Adress & Data Bus line	IO-3,3	-	-
C29	PCI_AD10	PCI Adress & Data Bus line	IO-3,3	-	-
C30	PCI_AD12	PCI Adress & Data Bus line	IO-3,3	-	-
C31	GND	Ground	PWR	-	-
C32	PCI_AD14	PCI Adress & Data Bus line	IO-3,3	-	-
C33	PCI_C/BE1#	PCI Bus Command and Byte enables	IO-3,3	-	-
C34	PCI_PERR#	PCI Bus Grant Error	IO-3,3	PU 2K7 3,3V	-
C35	PCI_LOCK#	PCI Bus Lock	IO-3,3	PU 2K7 3,3V	-
C36	PCI_DEVSEL#	PCI Bus Device Select	IO-3,3	PU 2K7 3,3V	-
C37	PCI_IRDY#	PCI Bus Bus Initiator Ready	IO-3,3	PU 2K7 3,3V	-
C38	PCI_C/BE2#	PCI Bus Command and Byte enables	IO-3,3	-	-
C39	PCI_AD17	PCI Adress & Data Bus line	IO-3,3	-	-
C40	PCI_AD19	PCI Adress & Data Bus line	IO-3,3	-	-
C41	GND	Ground	PWR	-	-
C42	PCI_AD21	PCI Adress & Data Bus line	IO-3,3	-	-
C43	PCI_AD23	PCI Adress & Data Bus line	IO-3,3	-	-
C44	PCI_C/BE3#	PCI Bus Command and Byte enables	IO-3,3	-	-
C45	PCI_AD25	PCI Adress & Data Bus line	IO-3,3	-	-
C46	PCI_AD27	PCI Adress & Data Bus line	IO-3,3	-	-
C47	PCI_AD29	PCI Adress & Data Bus line	IO-3,3	-	-
C48	PCI_AD31	PCI Adress & Data Bus line	IO-3,3	-	-
C49	PCI_IRQA#	PCI Bus Interrupt Request A	I-3,3	PU 2K7 3,3V	-
C50	PCI_IRQB#	PCI Bus Interrupt Request B	I-3,3	PU 2K7 3,3V	-
C51	GND	Ground	PWR	-	-
C52	PEG_RX0+	PCI Express Recieve + (0)	I - DP	-	-
C53	PEG_RX0-	PCI Express Recieve - (0)	I - DP	-	-
C54	TYPE0#	-	STO	-	not connected
C55	PEG_RX1+	PCI Express Recieve + (1)	I - DP	-	-

Signal Descriptions (cont'd)

Row C

Pin	Signal	Description	Type	PU/PD	Comment
C56	PEG_RX1-	PCI Express Recieve - (1)	I - DP	-	-
C57	TYPE1#	-	STO	-	not connected
C58	PEG_RX2+	PCI Express Recieve + (2)	I - DP	-	-
C59	PEG_RX2-	PCI Express Recieve - (2)	I - DP	-	-
C60	GND	Ground	PWR	-	-
C61	PEG_RX3+	PCI Express Recieve + (3)	I - DP	-	-
C62	PEG_RX3-	PCI Express Recieve - (3)	I - DP	-	-
C63	RSVD	Rx from Board Controller	NC	-	-
C64	RSVD	Tx from Board Controller	NC	-	-
C65	PEG_RX4+	PCI Express Recieve + (4)	I - DP	-	-
C66	PEG_RX4-	PCI Express Recieve - (4)	I - DP	-	-
C67	RSVD	FAN_PWR_CTRL	NC	-	-
C68	PEG_RX5+	PCI Express Recieve + (5)	I - DP	-	-
C69	PEG_RX5-	PCI Express Recieve - (5)	I - DP	-	-
C70	GND	Ground	PWR	-	-
C71	PEG_RX6+	PCI Express Recieve + (6)	I - DP	-	-
C72	PEG_RX6-	PCI Express Recieve - (6)	I - DP	-	-
C73	SDVO_DATA	SDVO_CTRLDATA	NC	-	-
C74	PEG_RX7+	PCI Express Recieve + (7)	I - DP	-	-
C75	PEG_RX7-	PCI Express Recieve - (7)	I - DP	-	-
C76	GND	Ground	PWR	-	-
C77	RSVD	FAN_TACH	NC	-	-
C78	PEG_RX8+	PCI Express Recieve + (8)	NC	-	-
C79	PEG_RX8-	PCI Express Recieve - (8)	NC	-	-
C80	GND	Ground	PWR	-	-
C81	PEG_RX9+	PCI Express Recieve + (9)	NC	-	-
C82	PEG_RX9-	PCI Express Recieve - (9)	NC	-	-
C83	RSVD	TPMPP (modify TPM address)	NC	-	-
C84	GND	Ground	NC	-	-
C85	PEG_RX10+	PCI Express Recieve + (10)	NC	-	-
C86	PEG_RX10-	PCI Express Recieve - (10)	NC	-	-
C87	GND	Ground	PWR	-	-
C88	PEG_RX11+	PCI Express Recieve + (11)	NC	-	-
C89	PEG_RX11-	PCI Express Recieve – (11)	NC	-	-
C90	GND	Ground	PWR	-	-
C91	PEG_RX12+	PCI Express Recieve + (12)	NC	-	-
C92	PEG_RX12-	PCI Express Recieve - (12)	NC	-	-
C93	GND	Ground	PWR	-	-
C94	PEG_RX13+	PCI Express Recieve + (13)	NC	-	-
C95	PEG_RX13-	PCI Express Recieve - (13)	NC	-	-
C96	GND	Ground	PWR	-	-
C97	RSVD	-	NC	-	-
C98	PEG_RX14+	PCI Express Recieve + (14)	NC	-	-
C99	PEG_RX14-	PCI Express Recieve - (14)	NC	-	-
C100	GND	Ground	PWR	-	-
C101	PEG_RX15+	PCI Express Recieve + (15)	NC	-	-
C102	PEG_RX15-	PCI Express Recieve - (15)	NC	-	-
C103	GND	Ground	PWR	-	-
C104	VCC_12V	Power 12V	PWR	-	-
C105	VCC_12V	Power 12V	PWR	-	-
C106	VCC_12V	Power 12V	PWR	-	-
C107	VCC_12V	Power 12V	PWR	-	-
C108	VCC_12V	Power 12V	PWR	-	-
C109	VCC_12V	Power 12V	PWR	-	-
C110	GND	Ground	PWR	-	-

Signal Descriptions (cont'd)

Row D

Pin	Signal	Description	Type	PU/PD	Comment
D1	GND	Ground	PWR	-	-
D2	IDE_D5	IDE Data Bus	IO	-	-
D3	IDE_D10	IDE Data Bus	IO	-	-
D4	IDE_D11	IDE Data Bus	IO	-	-
D5	IDE_D12	IDE Data Bus	IO	-	-
D6	IDE_D4	IDE Data Bus	IO	-	-
D7	IDE_D0	IDE Data Bus	IO	-	-
D8	IDE_REQ#	IDE Data Bus	I-3,3	PD 5K6	-
D9	IDE_IOW#	IDE IO Write	O-3,3	-	-
D10	IDE_ACK#	IDE DMA Acknowledge	O-3,3	-	-
D11	GND	Ground	PWR	-	-
D12	IDE_IRQ	IDE Interrupt Request	I-3,3	PD 10K	-
D13	IDE_A0	IDE Adress Bus	O-3,3	-	-
D14	IDE_A1	IDE Adress Bus	O-3,3	-	-
D15	IDE_A2	IDE Adress Bus	O-3,3	-	-
D16	IDE_CS1#	IDE Chip Select Channel 0	O-3,3	-	-
D17	IDE_CS3#	IDE Chip Select Channel 1	O-3,3	-	-
D18	IDE_RESET#	IDE Hard Drive Reset	O-3,3	-	-
D19	PCI_GNT3#	PCI Bus Grant 3	O-3,3	-	-
D20	PCI_REQ3#	PCI Bus Reqest 3	I-3,3	-	-
D21	GND	Ground	PWR	-	-
D22	PCI_AD1	PCI Adress & Data Bus line	IO-3,3	-	-
D23	PCI_AD3	PCI Adress & Data Bus line	IO-3,3	-	-
D24	PCI_AD5	PCI Adress & Data Bus line	IO-3,3	-	-
D25	PCI_AD7	PCI Adress & Data Bus line	IO-3,3	-	-
D26	PCI_C/BE0#	PCI Bus Command and Byte enables 0	IO-3,3	-	-
D27	PCI_AD9	PCI Adress & Data Bus line	IO-3,3	-	-
D28	PCI_AD11	PCI Adress & Data Bus line	IO-3,3	-	-
D29	PCI_AD13	PCI Adress & Data Bus line	IO-3,3	-	-
D30	PCI_AD15	PCI Adress & Data Bus line	IO-3,3	-	-
D31	GND	Ground	PWR	-	-
D32	PCI_PAR	PCI Bus Parity	IO-3,3	-	-
D33	PCI_SERR#	PCI Bus System Error	IO-3,3	PU 2K7 3,3V	-
D34	PCI_STOP#	PCI Bus Stop	IO-3,3	PU 2K7 3,3V	-
D35	PCI_TRDY#	PCI Bus Target Ready	IO-3,3	PU 2K7 3,3V	-
D36	PCI_FRAME#	PCI Bus Cycle Frame	IO-3,3	PU 2K7 3,3V	-
D37	PCI_AD16	PCI Adress & Data Bus line	IO-3,3	-	-
D38	PCI_AD18	PCI Adress & Data Bus line	IO-3,3	-	-
D39	PCI_AD20	PCI Adress & Data Bus line	IO-3,3	-	-
D40	PCI_AD22	PCI Adress & Data Bus line	IO-3,3	-	-
D41	GND	Ground	PWR	-	-
D42	PCI_AD24	PCI Adress & Data Bus line	IO-3,3	-	-
D43	PCI_AD26	PCI Adress & Data Bus line	IO-3,3	-	-
D44	PCI_AD28	PCI Adress & Data Bus line	IO-3,3	-	-
D45	PCI_AD30	PCI Adress & Data Bus line	IO-3,3	-	-
D46	PCI_IRQC#	PCI Bus Interrupt Request C	I-3,3	PU 2K7 3,3V	-
D47	PCI_IRQD#	PCI Bus Interrupt Request D	I-3,3	PU 2K7 3,3V	-
D48	PCI_CLKRUN#	PCI Clock Run	I-3,3	-	-
D49	PCI_M66EN#	Control PCI Speed 33/66 Mhz	I-3,3	PD 0K	Fixed to 33 Mhz
D50	PCI_CLK	PCI Clock	O-3,3	-	-
D51	GND	Ground	PWR	-	-
D52	PEG_TX0+	PCI Express Transmit + (0)	O - DP	-	-
D53	PEG_TX0-	PCI Express Transmit - (0)	O - DP	-	-
D54	PEG_LANE_RV#	PCI Express Lane Reversal	NC	-	-
D55	PEG_TX1+	PCI Express Transmit + (1)	O - DP	-	-

Signal Descriptions (cont'd)

Row D

Pin	Signal	Description	Type	PU/PD	Comment
D56	PEG_TX1-	PCI Express Transmit - (1)	O - DP	-	-
D57	TYPE2#	Connected to GND	STO	-	not connected
D58	PEG_TX2+	PCI Express Transmit + (2)	O - DP	-	-
D59	PEG_TX2-	PCI Express Transmit - (2)	O - DP	-	-
D60	GND	Ground	PWR	-	-
D61	PEG_TX3+	PCI Express Transmit + (3)	O - DP	-	-
D62	PEG_TX3-	PCI Express Transmit - (3)	O - DP	-	-
D63	RSVD	-	NC	-	-
D64	RSVD	-	NC	-	-
D65	PEG_TX4+	PCI Express Transmit + (4)	O - DP	-	-
D66	PEG_TX4-	PCI Express Transmit - (4)	O - DP	-	-
D67	GND	Ground	PWR	-	-
D68	PEG_TX5+	PCI Express Transmit + (5)	O - DP	-	-
D69	PEG_TX5-	PCI Express Transmit - (5)	O - DP	-	-
D70	GND	Ground	PWR	-	-
D71	PEG_TX6+	PCI Express Transmit + (6)	O - DP	-	-
D72	PEG_TX6-	PCI Express Transmit - (6)	O - DP	-	-
D73	SDVO_CLK	SDVO_CTRLCLK	NC	-	-
D74	PEG_TX7+	PCI Express Transmit + (7)	O - DP	-	-
D75	PEG_TX7-	PCI Express Transmit - (7)	O - DP	-	-
D76	GND	Ground	PWR	-	-
D77	IDE_CBLID#	IDE Primary ATA Detect	I-3,3	PU 8K2 3,3V	-
D78	PEG_TX8+	PCI Express Transmit + (8)	NC	-	-
D79	PEG_TX8-	PCI Express Transmit - (8)	NC	-	-
D80	GND	Ground	PWR	-	-
D81	PEG_TX9+	PCI Express Transmit + (9)	NC	-	-
D82	PEG_TX9-	PCI Express Transmit - (9)	NC	-	-
D83	RSVD	-	NC	-	-
D84	GND	Ground	PWR	-	-
D85	PEG_TX10+	PCI Express Transmit + (10)	NC	-	-
D86	PEG_TX10-	PCI Express Transmit - (10)	NC	-	-
D87	GND	Ground	PWR	-	-
D88	PEG_TX11+	PCI Express Transmit + (11)	NC	-	-
D89	PEG_TX11-	PCI Express Transmit - (11)	NC	-	-
D90	GND	Ground	PWR	-	-
D91	PEG_TX12+	PCI Express Transmit + (12)	NC	-	-
D92	PEG_TX12-	PCI Express Transmit - (12)	NC	-	-
D93	GND	Ground	PWR	-	-
D94	PEG_TX13+	PCI Express Transmit + (13)	NC	-	-
D95	PEG_TX13-	PCI Express Transmit - (13)	NC	-	-
D96	GND	Ground	PWR	-	-
D97	PEG_ENABLE#	PCI Express Enable	NC	-	-
D98	PEG_TX14+	PCI Express Transmit + (14)	NC	-	-
D99	PEG_TX14-	PCI Express Transmit - (14)	NC	-	-
D100	GND	Ground	PWR	-	-
D101	PEG_TX15+	PCI Express Transmit + (15)	NC	-	-
D102	PEG_TX15-	PCI Express Transmit - (15)	NC	-	-
D103	GND	Ground	PWR	-	-
D104	VCC_12V	Power 12V	PWR	-	-
D105	VCC_12V	Power 12V	PWR	-	-
D106	VCC_12V	Power 12V	PWR	-	-
D107	VCC_12V	Power 12V	PWR	-	-
D108	VCC_12V	Power 12V	PWR	-	-
D109	VCC_12V	Power 12V	PWR	-	-
D110	GND	Ground	PWR	-	-

Signal Descriptions (cont'd)

Signal Type Legend	
IO-2,5	Bi-directional 2,5 V Input/Output
IO-3,3	Bi-directional 3,3 V Input/Output
IO-5	Bi-directional 5 V Input/Output
I-3,3	3,3 V Input
I-5	5 V Input
O-2,5	2,5 V Output
O-3,3	3,3 V Output
O-5	5 V Output
IO	Input/Output
OA	Analog Output
I/O - DP	Differential Pair Input/Output
O - DP	Differential Pair Output
I - DP	Differential Pair Input
PWR	Power or Ground
STO	Strapping Output
PU	Pull-Up Resistor
PD	Pull-Down Resistor
NC	Not Connected / Reserved

7 System Resources

7.1 System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
(4GB-2MB)	FFE00000–FFFFFFFF	2 MB	High BIOS Area
(4GB-18MB)-(4GB-17MB-1)	FEE00000–FEEFFFFF	1 MB	FSB Interrupt Memory Space
(4GB-19MB)-(4GB-18MB-1)	FED00000–FEDFFFFF	1 MB	Chipset configuration Space
(4GB-20MB)-(4GB-19MB-1)	FEC00000–FECFFFFF	1 MB	APIC Configuration Space
15MB – 16MB	F00000–FFFFFF	1 MB	ISA Hole
960 K – 1024 K	F0000–FFFFF	64 KB	System BIOS Area
896 K – 960 K	E0000–EFFFF	64 KB	Extended System BIOS Area
768 K – 896 K	C0000–DFFFF	128 KB	PCI expansion ROM area C0000 – CEFFF: Onboard VGA BIOS CF000 – D0FFF: PXE option ROM when onboard LAN boot ROM is enabled
640 K – 768 K	A0000 – BFFFF	128 KB	Video Buffer & SMM space
0 K – 640 K	00000 – 9FFFF	640 KB	DOS Area

7.2 Direct Memory Access Channels

Channel Number	Data Width	System Resource	Available
0	8-bits	Parallel port	Note (1)
1	8-bits	Parallel port	Note (1)
2	8-bits	Diskette drive	Note (1)
3	8-bits	Parallel port	Note (1)
4		Reserved - cascade channel	
5	16-bits	Open	
6	16-bits	Open	
7	16-bits	Open	

NOTE: (1) DMA channel 0/1/3 is selected when using parallel port. DMA2 is used by Floppy.

7.3 I/O Map

Address (hex)	Size	Description
00h – 08h	9 bytes	DMA Controller
09h – 0Eh	6 bytes	DMA Controller
0Fh	1 byte	DMA Controller
10h – 18h	9 bytes	DMA Controller
19h – 1Eh	6 bytes	DMA Controller
1Fh	1 byte	DMA Controller
20h – 21h	2 bytes	Interrupt Controller
24h – 25h	2 bytes	Interrupt Controller
28h – 29h	2 bytes	Interrupt Controller
2Ch – 2Dh	2 bytes	Interrupt Controller
2Eh – 2Fh	2 bytes	LPC SIO
30h – 31h	2 bytes	Interrupt Controller
34h – 35h	2 bytes	Interrupt Controller
38h – 39h	2 bytes	Interrupt Controller
3Ch – 3Dh	2 bytes	Interrupt Controller
40h – 42h	3 bytes	Timer/Counter
43h	1 bytes	Timer/Counter
4Eh – 4Fh	2 bytes	LPC SIO
50h – 52h	3 bytes	Timer/Counter
53h	1 bytes	Timer/Counter
60h	1 byte	Microcontroller
61h	1 byte	NMI Controller
62h	1 byte	Microcontroller
63h	1 byte	NMI Controller
64h	1 byte	Microcontroller
65h	1 byte	NMI Controller
66h	1 byte	Microcontroller
67h	1 byte	NMI Controller
70h	1 byte	NMI and RTC Controller
71h	1 byte	RTC Controller
72h	1 byte	NMI and RTC Controller
73h	1 byte	RTC Controller
74h	1 byte	NMI and RTC Controller
75h	1 byte	RTC Controller
76h	1 byte	NMI and RTC Controller
77h	1 byte	RTC Controller
80h	1 byte	DMA Controller, or LPC, or PCI
81h – 83h	4 bytes	DMA Controller
84h – 86h	3 bytes	DMA Controller, or LPC, or PCI
87h	1 byte	DMA Controller
88h	1 byte	DMA Controller, or LPC, or PCI
89h – 8Bh	3 bytes	DMA Controller
8Fh	1 byte	DMA Controller, or LPC, or PCI
90h – 91h	2 bytes	DMA Controller

I/O Map (cont'd)

Address (hex)	Size	Description
92h	1 byte	Reset Generator
93h – 9Fh	13 byte	DMA Controller
84h – 86h	3 bytes	DMA Controller, or LPC, or PCI
87h	1 byte	DMA Controller
88h	1 byte	DMA Controller, or LPC, or PCI
89h – 8Bh	3 bytes	DMA Controller
8Ch– 8Eh	3 bytes	DMA Controller, or LPC, or PCI
8Fh	1 byte	DMA Controller
90h – 91h	2 bytes	DMA Controller
92h	1 byte	Reset Generator
93h – 9Fh	13 bytes	DMA Controller
A0h – A1h	2 bytes	Interrupt Controller
A4h – A5h	2 bytes	Interrupt Controller
A8h – A9h	2 bytes	Interrupt Controller
ACh – ADh	2 bytes	Interrupt Controller
B0h – B1h	2 bytes	Interrupt Controller
B2h – B3h	2 bytes	Power Management
B4h – B5h	2 bytes	Interrupt Controller
B8h – B9h	2 bytes	Interrupt Controller
BCh – BDh	2 bytes	Interrupt Controller
C0h – D1h	17 bytes	DMA Controller
D2h – DDh	12 bytes	DMA Controller
DEh – DFh	2 bytes	DMA Controller
F0h	1 byte	Interrupt Controller
170h – 177h	8 bytes	SATA or PCI
1F0h – 1F7h	8 bytes	SATA or PCI
200h – 207h	8 bytes	Gameport Low
208h – 20Fh	8 bytes	Gameport High
376h	1 byte	SATA or PCI
3F6h	1 byte	SATA or PCI
400h – 47Fh	128 bytes	ACPI Control Register
4D0h – 4D1h	2 bytes	Interrupt Controller
500h – 53Fh	64 bytes	GPIO Control Register
540h – 55Fh	32 bytes	Onboard SMBus Control Register
A79h	1 byte	ISA PnP read data port.
CF8h – CFFh*	8 bytes	PCI Configuration Register
CF9h**	1 byte	Reset Generator
4700h – 470Fh	16 bytes	TPM Control Register

NOTE:

* DWORD access only
** Byte access only

7.4 Interrupt Request (IRQ) Lines

PIC Mode

IRQ#	Typical Interrupt Resource	Connected	Available
0	Counter 0	N/A	No
1	Keyboard controller	N/A	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 2 (COM2) / PCI	IRQ3 via SERIRQ	Note (1)
4	Serial Port 1 (COM1) / PCI	IRQ4 via SERIRQ	Note (1)
5	Parallel Port 2 (LPT2) / PCI	IRQ5 via SERIRQ	Note (1)
6	Floppy Drive Controller	IRQ6 via SERIRQ	No
7	Parallel Port 1 (LPT1) / PCI	IRQ7 via SERIRQ,	Note (1)
8	Real-time clock	N/A	No
9	SCI / PCI	IRQ9 via SERIRQ	Note (1)
10	PCI	SATA controller / USB Controller / PCI	Note (1)
11	PCI	IRQ11 via SERIRQ	Note (1)
12	PS/2 Mouse / PCI	IRQ12 via SERIRQ	Note (1)
13	Math Processor	N/A	No
14	Primary IDE controller / PCI	USB Controller / PCI	Note (1)
15	Secondary IDE controller / PCI	USB Controller / PC	Note (1)

(1) These IRQs can be used for PCI devices when onboard device is disabled.

APIC Mode

IRQ#	Typical Interrupt Resource	Connected	Available
0	Counter 0	N/A	No
1	Keyboard controller	N/A	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 2 (COM2) / PC	IRQ3 via SERIRQ	Note (1)
4	Serial Port 1 (COM1) / PCI	IRQ4 via SERIRQ	Note (1)
5	Parallel Port 2 (LPT2) / PCI	IRQ5 via SERIRQ	Note (1)
6	Floppy Drive Controller	IRQ6 via SERIRQ	No
7	Parallel Port 1 (LPT1) / PCI	IRQ7 via SERIRQ	Note (1)
8	Real-time clock	N/A	No
9	SCI / PCI	IRQ9 via SERIRQ	Note (1),
10	PCI	IRQ10 via SERIRQ	Note (1)
11	PCI	IRQ11 via SERIRQ	Note (1)
12	PS/2 Mouse / PCI	IRQ12 via SERIRQ	Note (1)
13	Math Processor	N/A	No
14	Primary IDE controller / PCI	IRQ14 via SERIRQ	Note (1)
15	Secondary IDE controller / PCI	IRQ15 via SERIRQ	Note (1)
16	N/A	PCI Slot INT A,	Yes
17	N/A	PCI Slot INT B	Yes
18	N/A	PCI	Yes
19	N/A	SATA Controller, PCI	Yes
20	N/A		No
21	N/A		No
22	N/A		No
23	N/A	EHCI, USB	No

(1) These IRQs can be used for PCI devices when onboard device is disabled.

7.5 PCI Configuration Space Map

Bus No.	Device No.	Function No.	Routing	Description
00h	00h	00h	N/A	Intel 3100 Chipset Memory Controller Hub
00h	02h	00h	Internal	Intel IMCH Express Root port A1
00h	03h	00h	Internal	Intel IMCH Express Root port A1
00h	1Bh	00h	Internal	High Definition Audio controller
00h	1Ch	00h	Internal	Intel IICH Express Root port B0
00h	1Ch	01h	Internal	Intel IICH Express Root port B1
00h	1Ch	02h	Internal	Intel IICH Express Root port B2
00h	1Ch	03h	Internal	Intel IICH Express Root port B3
00h	1Dh	00h	Internal	Intel USB UHCI Controller 1
00h	1Dh	01h	Internal	Intel USB UHCI Controller 2
00h	1Dh	07h	Internal	Intel USB EHCI Controller
00h	1Eh	00h	N/A	Intel Hub Interface to PCI Bridge
00h	1Fh	00h	N/A	Intel LPC Interface Bridge
00h	1Fh	02h	Internal	Intel SATA controller
00h	1Fh	03h	Internal	Intel SMBus Controller
01h	04h	00h	PIRQA-PIRQD	External PCI Slot 1
01h	05h	00h	PIRQA-PIRQD	External PCI Slot 2
05h	00h	00h	onboard	Onboard LAN controller

7.6 PCI Interrupt Routing Map

PIRQ	INT	UCHI 1	UCHI 2	EHCI	SATA	SMBus	Audio	PCI Slot1	PCI Slot2	LAN
A	INTA						X	INTA	INTB	X
B	INTB							INTB	INTC	
C	INTC							INTC	INTD	
D	INTD		X		X	X		INTD	INTA	
E										
F										
G										
H		X		X						

7.7 System Management Bus (I²C compatible)

Internally the SMB bus and I2C bus are one and the same. The Intel® 3100 chipset supports SMBDAT and SMBCLK lines that are I2C compatible.

The connectors have pinouts for both the I2C and SMB bus. Both are connected to the same internal bus: the SMB bus. It is advisable to always connect external I2C devices to the I2C pins and SMB devices to the SMB pins to stay in line with other modules that might support two internal busses (separate I2C and SMB bus).

Address	Function	Device
A0h	Memory Address	SORDIMM2 (vertical or horizontal)
A2h	Memory Address	SORDIMM1 (vertical only)
ACh	Backup EEPROM	Backup EEPROM
AEh	Backup EEPROM	Backup EEPROM
30h	Hardware Monitor	LM95235
5Ch	Hardware Monitor	LM87
D2h	Timing	Clock Generator
DCh	Timing	Clock Buffer (SRC)

8 BIOS Setup Utility

The following chapter describes the basic navigation of the AMIBIOS®8 BIOS setup utility.

8.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keybaord when you see the following text prompt:

   < Press DEL to run Setup >

3. After you press the < Delete > key, the main BIOS setup menu diplays. You can access the other setup screens from the main BIOS setup menu, such as the Chipset and Power menus.

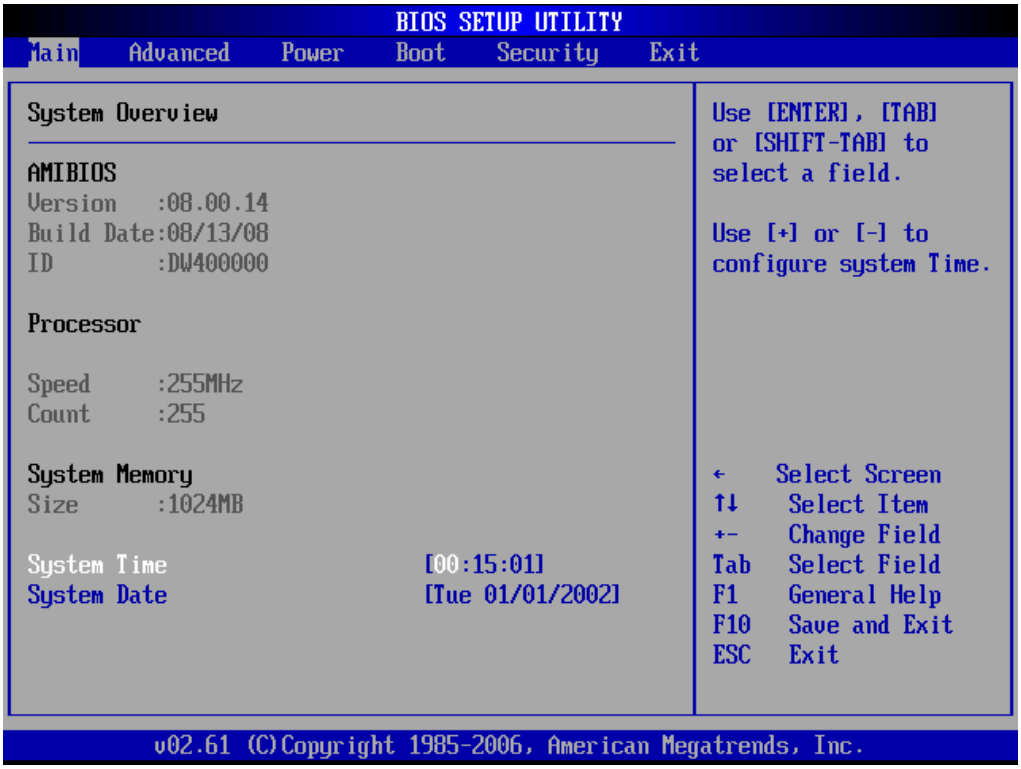
NOTE: In most cases, the <Delete> key is used to invoke the setup screen. There are a few cases that other keys are used, such as <F1>, <F2>, and so on.

8.1.1 Setup Menu

The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

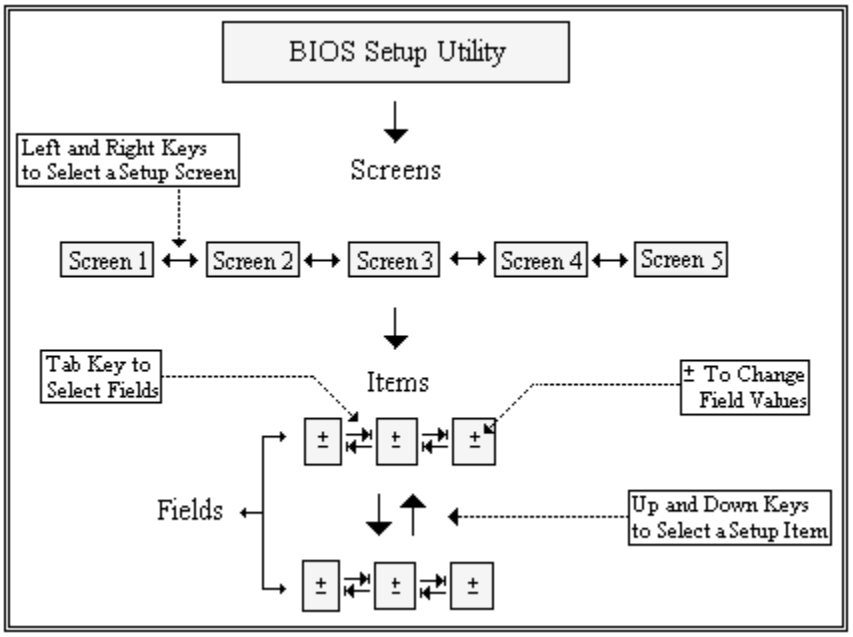
The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed-out" options cannot be configured. Options is blue can be.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.



8.1.2 Navigation

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process.
These keys include < F1 >, < F10 >, < Enter >, < ESC >, < Arrow > keys, and so on.

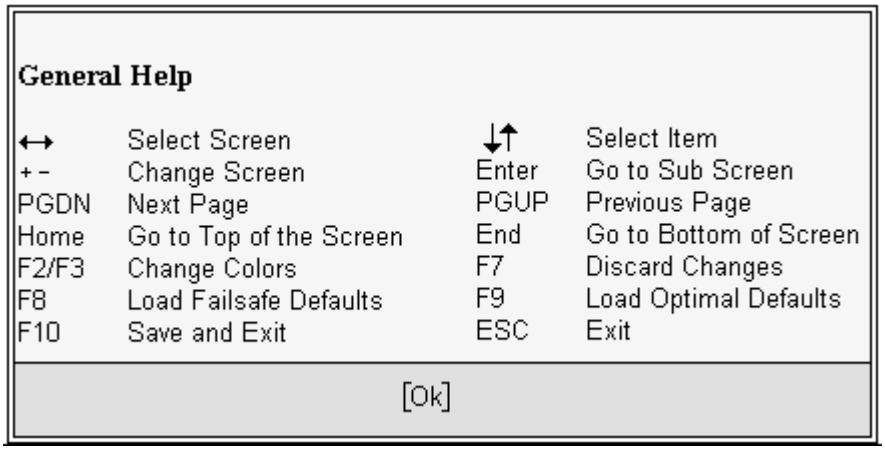


There is a hot key legend located in the right frame on most setup screens.

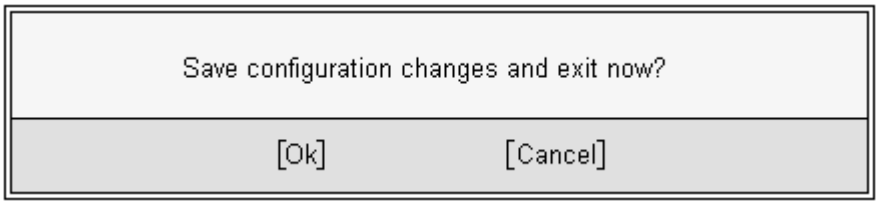
Hot Key	Description
→←	Left/Right The *Left and Right* < Arrow > keys allow you to select an setup screen. For example: Main screen, Advanced screen, Chipset screen, and so on.
↑↓	Up/Down The *Up and Down* < Arrow > keys allow you to select an setup item or sub-screen.
+ −	Plus/Minus The *Plus and Minus* < Arrow > keys allow you to change the field value of a particular setup item. For example: Date and Time.
Tab	The < Tab > key allows you to select setup fields.

NOTE: The < F8 > key on your keyboard is the Fail-Safe key. It is not displayed on the key legend by default. To set the Fail-Safe settings of the BIOS, press the < F8 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The Fail-Safe settings allow the motherboard to boot up with the least amount of options set. This can lessen the probability of conflicting settings.

Hot Key	Description
F1	The < F1 > key allows you to display the *General Help screen*. Press the < F1 > key to open the *General Help screen*.

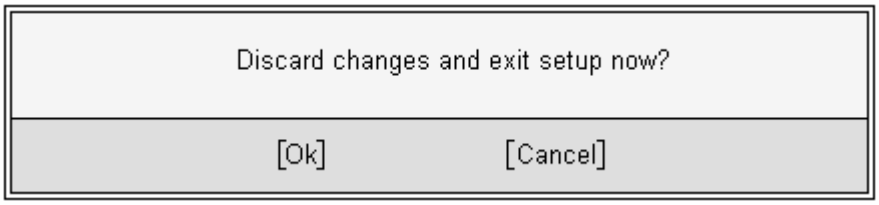


F10 >	The < F10 > key allows you to save any changes you have made and exit Setup. Press the < F10 > key to save your changes. The following screen will appear:



Press the < Enter > key to save the configuration and exit. You can also use the < Arrow > key to select *Cancel* and then press the < Enter > key to abort this function and return to the previous screen.

ESC	The < Esc > key allows you to discard any changes you have made and exit the Setup. Press the < Esc > key to exit the setup without saving your changes. The following screen will appear:

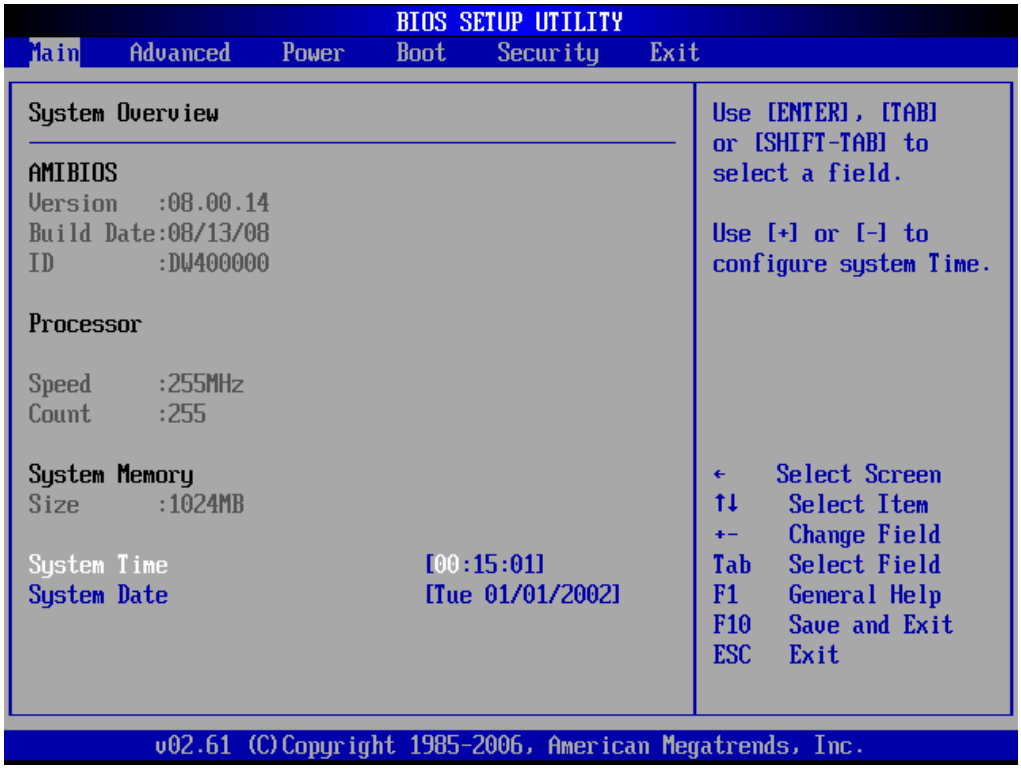


Press the < Enter > key to discard changes and exit. You can also use the < Arrow > key to select *Cancel* and then press the < Enter > key to abort this function and return to the previous screen.

Enter	The < Enter > key allows you to display or change the setup option listed for a particular setup item. The < Enter > key can also allow you to display the setup sub-screens.

8.2 Main Setup

When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the *Main* tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



8.2.1 System Time/System Date

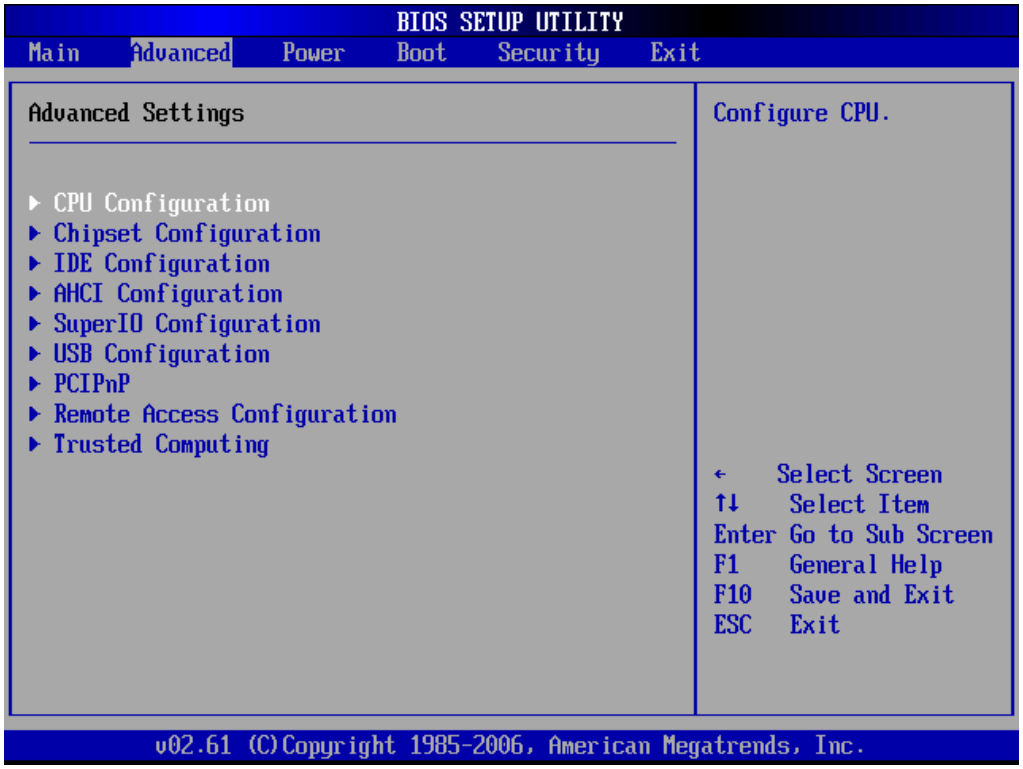
Use this option to change the system time and date. Highlight *System Time* or *System Date* using the < Arrow > keys. Enter new values through the keyboard. Press the < Tab > key or the < Arrow > keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

NOTE: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

8.3 Advanced BIOS Setup

Select the *Advanced* tab from the setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as SuperIO Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the < Arrow > keys. The Advanced BIOS Setup screen is shown below.

The sub menus are described on the following pages.

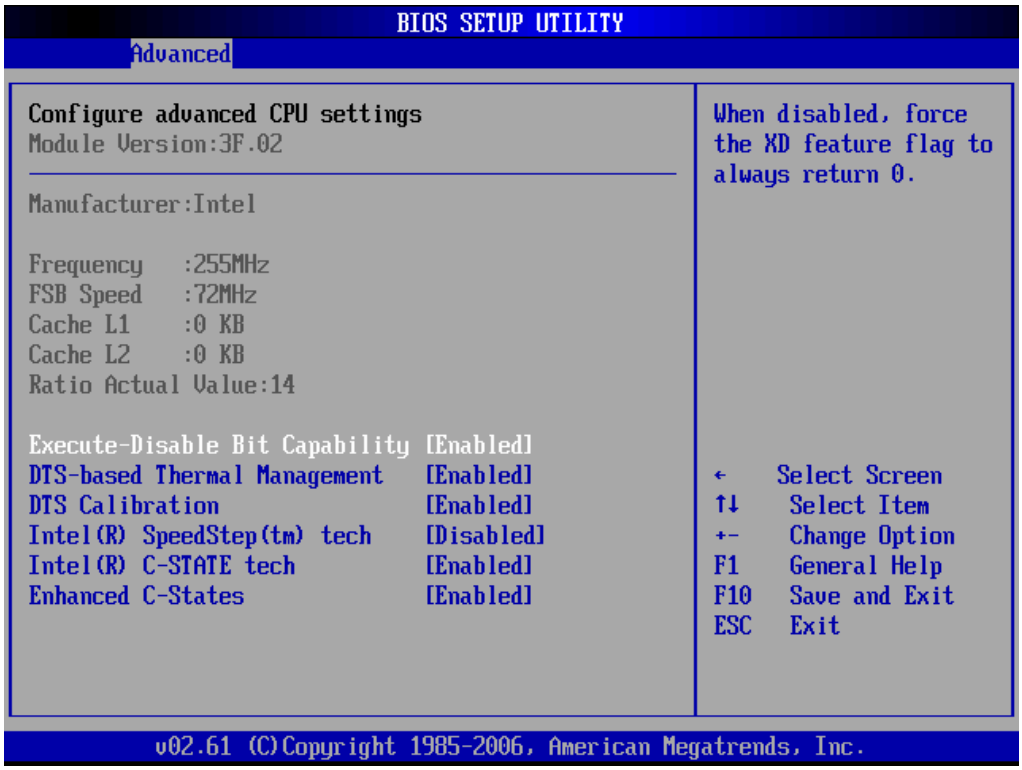


WARNING: Setting incorrect or conflicting values in Advanced BIOS Setup may cause system malfunctions.

8.3.1 CPU Configuration

CPU Configuration Settings

You can use this screen to select options for the CPU Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < Plus > and < Minus > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the *CPU Configuration* screen is shown below.



Execute Disable Bit Capability

This item allows you to enable/disable the “Execute-Disable Bit” function. Intel’s Execute Disable Bit functionality can help prevent certain classes of malicious buffer overflow attacks when combined with a supporting operating system. It allows the processor to classify areas in memory where application code can or cannot execute. When a malicious worm attempts to insert code in the buffer, the processor disables its code execution, preventing damage and worm propagation. To use Execute Disable Bit you must have a PC or server with a processor with Execute Disable Bit capability and a supporting operating system.

DTS-based Thermal Management

This item allows you to Enable/Disable the Thermal Management utilizing the CPU's Digital Thermal Sensor.

DTS Calibration

This item allows you to Enable/Disable the calibration function of the CPU's Digital Thermal Sensor.

Intel® SpeedStep™ tech

This item allows you to enable/disable Intel® SpeedStep™ Technology. This function switches both voltage and frequency in tandem between high and low levels in response to processor load.

Intel® C-STATE tech

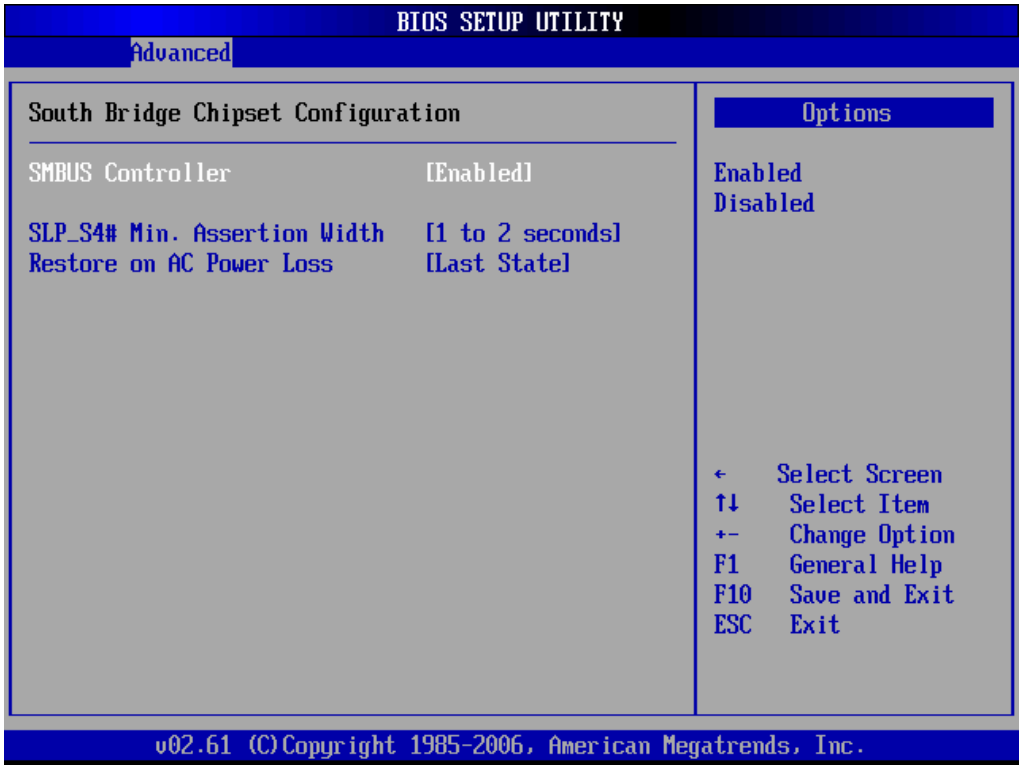
This item allows you to Enable/Disable the Intel® C-state technology. C-state technology makes the power and thermal control unit part of the core logic and not part of the chipset.

Enhanced C-STATE

This item allows you to Enable/Disable the Enhanced C- state function.

8.3.2 Chipset Setup

Select the Chipset tab from the setup screen to enter the Chipset BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. You can display a Chipset BIOS Setup option by highlighting it using the <Arrow> keys. The Chipset BIOS Setup screen is shown below.



SMBus Controller

This item allows you to Enabled/Disable the SMBus function of the chipset.

SLP_S4# Min. Assertion Width

Options: 4 to 5 seconds, 3 to 4 seconds, 2 to 3 seconds, 1 to 2 seconds.

Restore on AC Power Loss

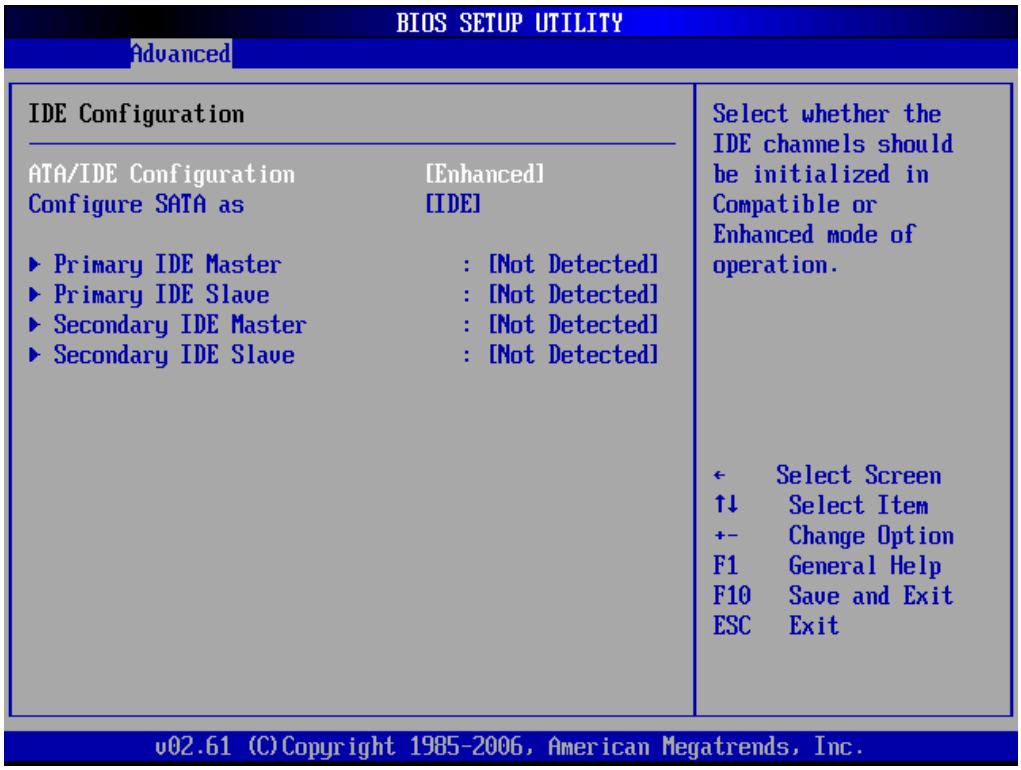
The options for this value are Last State, Power On and Power Off.

Option	Description
Power Off	The system goes into off state after an AC power loss.
Power On	The system goes on after an AC power loss.
Last State	The system goes into either off or on states, whatever the system state was before the AC power loss.

8.3.3 IDE Configuration

IDE Configuration Settings

You can use this screen to select options for the IDE Configuration Settings. Use the up and down < `Arrow` > keys to select an item. Use the < `Plus` > and < `Minus` > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the *IDE Configuration* screen is shown below.



ATA/IDE Configuration

This item specifies whether the IDE channels should be initialized in Compatible or Enhanced mode of operation. The settings are *Disabled, Compatible* and *Enhanced.*

Configure SATA as

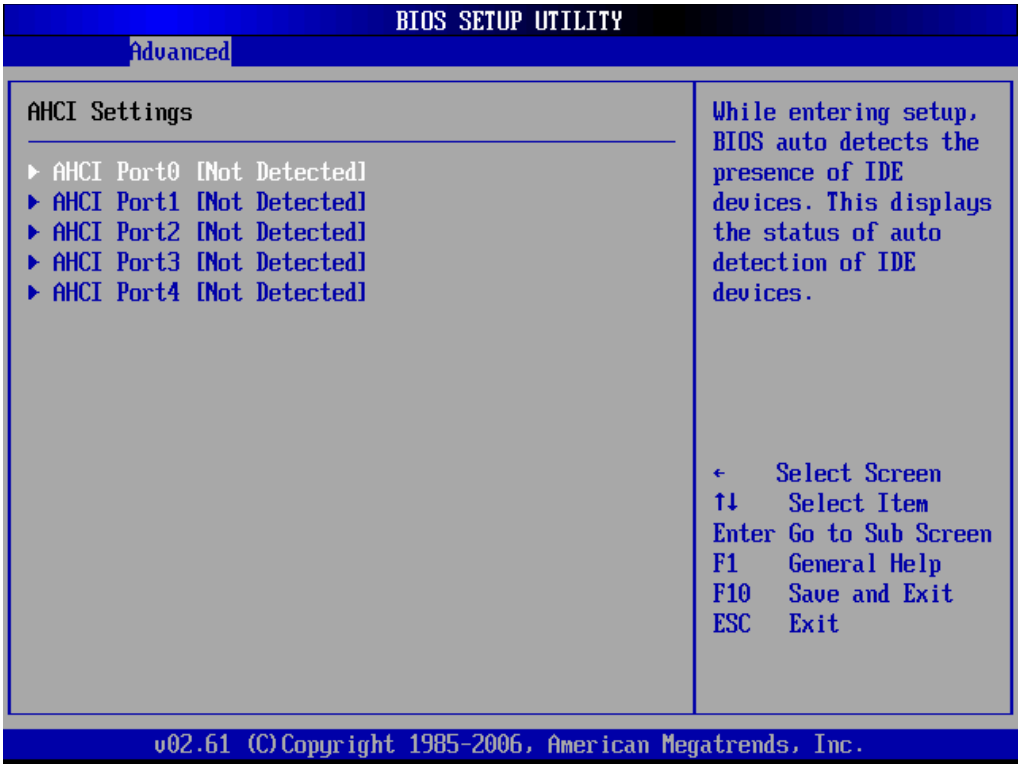
This item specifies whether the SATA interface should be legacy IDE or AHCI supported. The settings are *IDE* and *AHCI.*

Primary IDE Master/Slave, Secondary IDE Master/Slave

Select one of the hard disk drives to configure it. Press < `Enter` > to access its the sub menu.

8.3.4 AHCI Settings

You can use this screen to select options for the AHCI Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the AHCI Configuration screen is shown below.



AHCI Portx

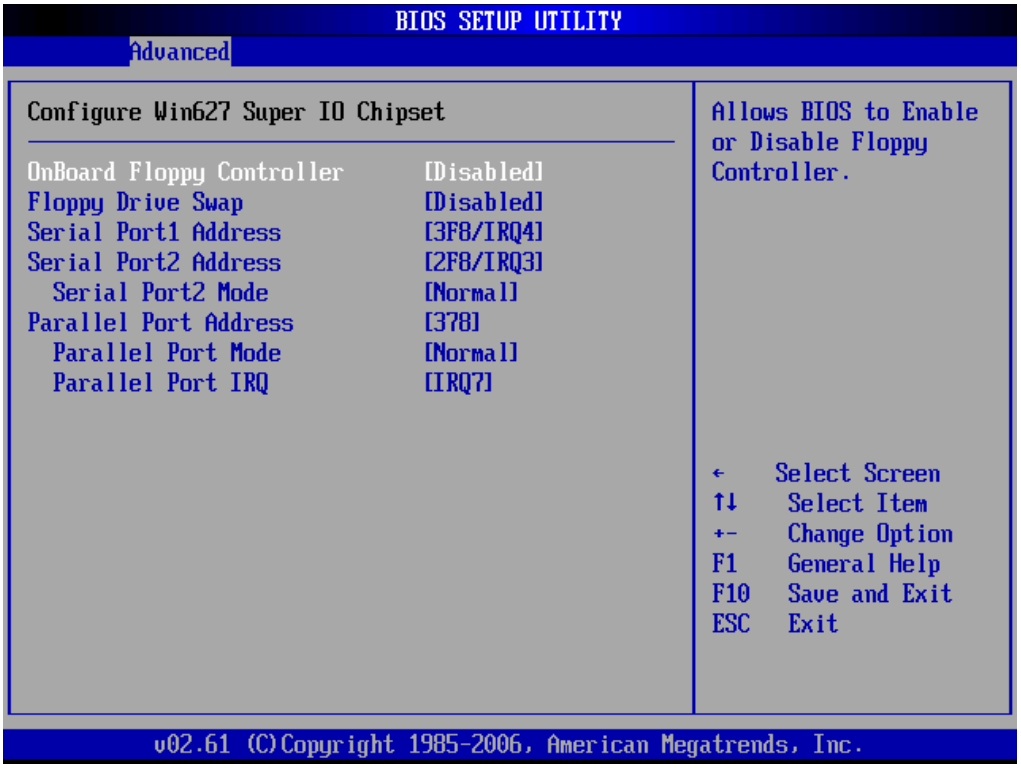
Set this value to configure the Advanced Host Controller Interface. It is an interface specification that allows the SATA controller driver to support advanced features like Native Command Queuing and Hot Plug. Each AHCI Port is automatically detected by the system.

Select one of the hard disk drives to configure the AHCI function. Press < Enter > to access its sub menu.

8.3.5 Super IO Configuration

SuperIO Configuration Screen

You can use this screen to select options for the Super IO settings. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



OnBoard Floppy Controller

Set this value to Enable/Disable the onboard floppy controller function.

Floppy Drive Swap

This option is used to logically swap the mapping of drives A: and B:. This option is dependent upon having two installed floppy drives. The settigns are Enabled and Disabled.

Serial Port1 Address

This option specifies the base I/O port address and Interrupt Request address of Serial Port 1.

Option	Description
Disabled	Set this value to prevent the serial port from accessing any system resources. When this option is set to *Disabled*, the serial port physically becomes unavailable.
3F8/IRQ4	Set this value to allow the serial port to use 3F8 as its I/O port address and IRQ 4 for the interrupt address.
3E8/IRQ4	Set this value to allow the serial port to use 3E8 as its I/O port address and IRQ 4 for the interrupt address.
2F8/IRQ3	Set this value to allow the serial port to use 2F8 as its I/O port address and IRQ 3 for the interrupt address.
2E8/IRQ3	Set this value to allow the serial port to use 2E8 as its I/O port address and IRQ 3 for the interrupt address.

Serial Port2 Address

This option specifies the base I/O port address and Interrupt Request address of serial port 2, and are identical to those for Serial Port 1 above. The option selected for Serial Port 1 will not be available for Serial Port 2

Serial Port2 Mode

This option allows installation of an Infra-red device via Serial Port2. The settings are Normal, IRDA and ASK IR.

Option	Description
Normal	The standard RS-232 Communication Port.
IrDA	Infrared Dealer's Association protocol
ASK IR	ASK IR (Ask Computer Company infrared protocol)

Parallel Port Address

This option specifies the I/O address used by the parallel port.

Option	Description
Disabled	Set this value to prevent the parallel port from accessing any system resources. When the value of this option is set to *Disabled*, the printer port becomes unavailable.
378	Set this value to allow the parallel port to use 378 as its I/O port address. The majority of parallel ports on computer systems use IRQ7 and I/O Port 378H as the standard setting.
278	Set this value to allow the parallel port to use 278 as its I/O port address.
3BC	Set this value to allow the parallel port to use 3BC as its I/O port address.

Parallel Port Mode

This option specifies the parallel port mode.

Option	Description
Normal	Set this value to allow the standard parallel port mode to be used.
EPP	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bi-directional data transfer driven by the host device.
ECP	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Megabits per second. ECP provides symmetric Bi-directional communication.
EPP+ECP	Allow the parallel port to support both the ECP and EPP modes simultaneously.

Parallel Port IRQ

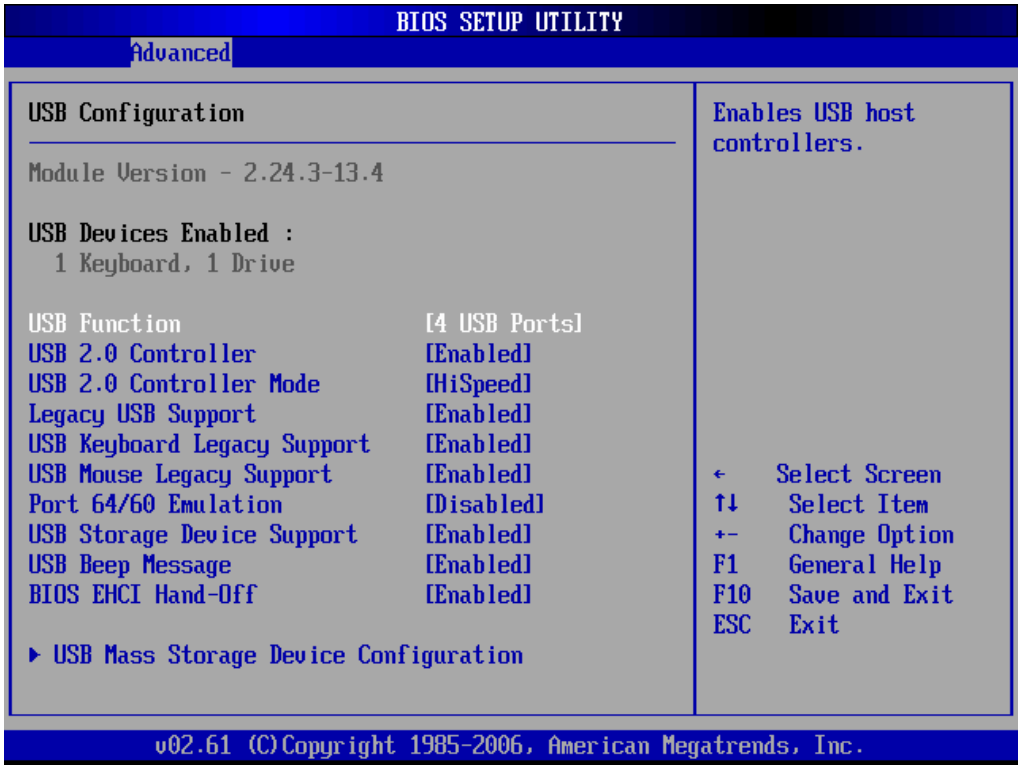
This option specifies the IRQ used by the parallel port.

Option	Description
IRQ5	Set this value to allow the serial port to use Interrupt 5.
IRQ7	Set this value to allow the serial port to use Interrupt 7. The majority of parallel ports on computer systems use IRQ7 and I/O Port 378H as the standard setting.

8.3.6 USB Configuration

USB Configuration

You can use this screen to select options for the USB Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



USB Function

Set this value to allow the system to Disable, Enable, and select a set number of onboard USB 2.0 ports. The options are Disabled, 2 USB Ports, and 4 USB Ports.

USB 2.0 Controller

This field allows you to Enable/Disable the EHCI (USB 2.0) controller.

USB 2.0 Controller Mode

This field configures the data rate of the USB port. The options are FullSpeed (12 Mbps) and HiSpeed (480 Mbps).

Legacy USB Support

Legacy USB Support refers to the USB mouse and USB keyboard support. Normally if this option is not enabled, any attached USB mouse or USB keyboard will not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there is no USB drivers loaded on the system. Set this value to enable or disable the Legacy USB Support. The Optimal and Fail-Safe default setting is Disabled.

Option	Description
Disabled	Set this value to prevent the use of any USB device in DOS or during system boot. This is the default setting.
Enabled	Set this value to allow the use of USB devices during boot and while using DOS.
Auto	This option auto detects USB Keyboards or Mice and if found, allows them to be utilized during boot and while using DOS.

Port 60/64 Emulation

This option allows you to Enable/Disable the I/O port 60h/64h emulation support for non-USB aware operating systems.

USB Storage Device Support

Allows you to enable or disable the USB storage device support.

USB Beep Message

Allows you to Enable/Disable the beep during USB device enumeration.

USB BIOS EHCI Hand-off

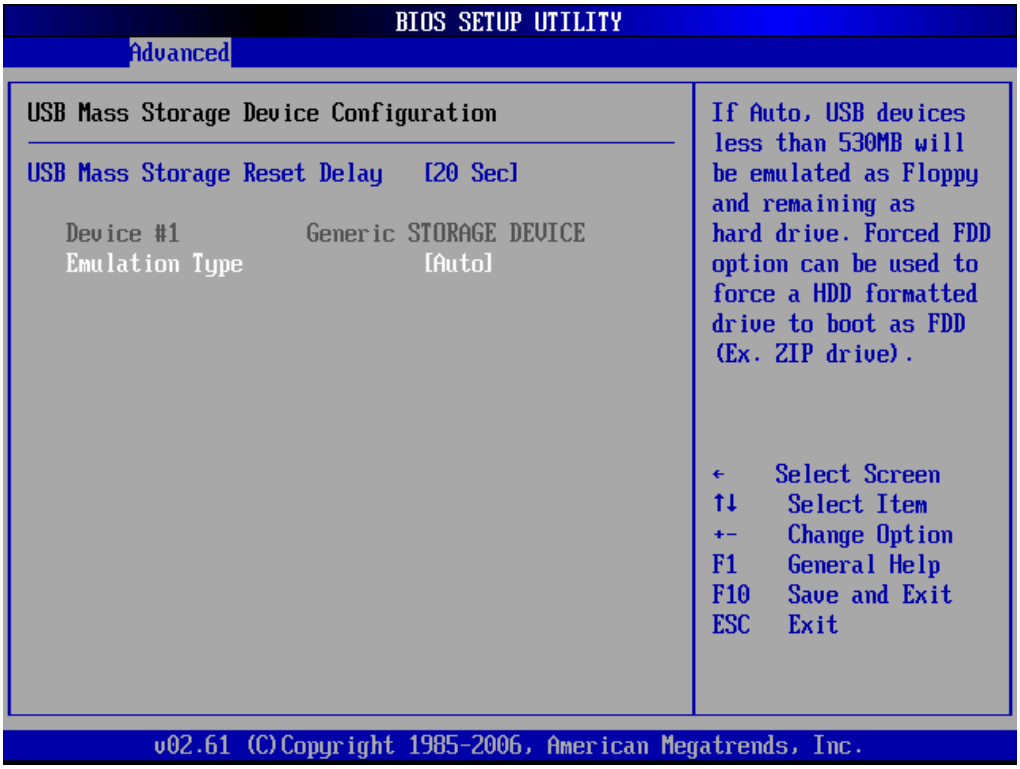
Allows you to enable the support for operating systems without EHCU hand-off feature.

USB Mass Storage Reset Delay

This item allows you to set the reset delay for USB mass storage device.

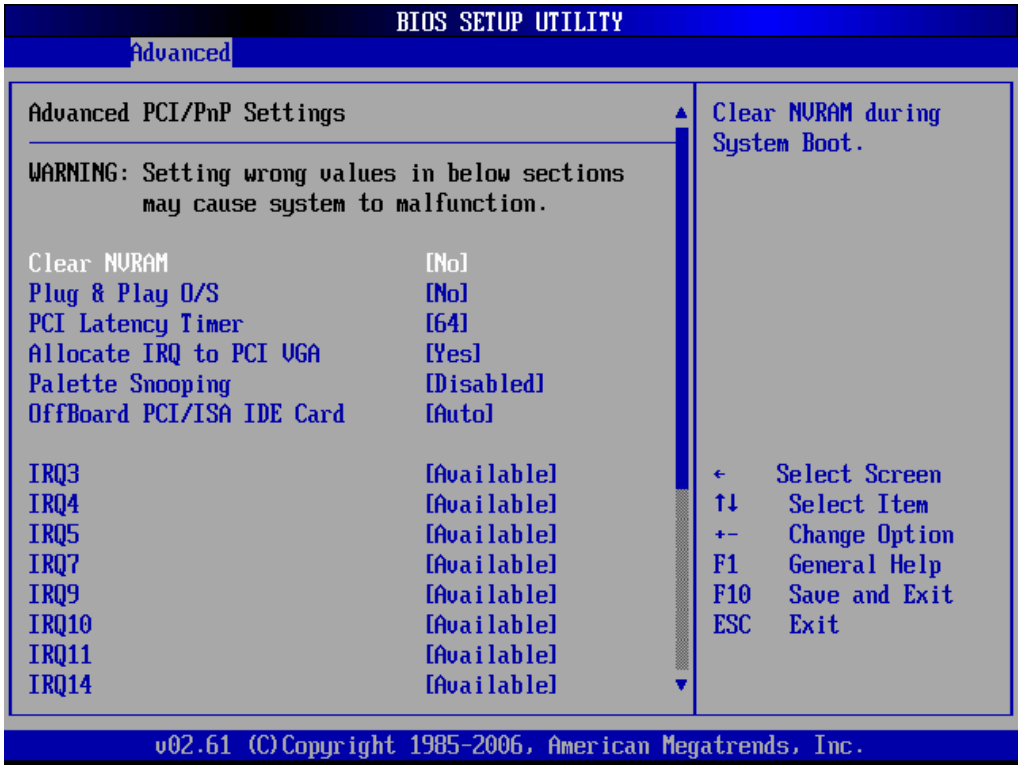
USB Mass Storage Device Configuration

This is a submenu for configuring the USB Mass Storage Class Devices when BIOS finds they are in use on USB ports. Emulation Type can be set according to the type of attached USB mass storage device(s). USB devices less than 530MB will be emulated as Floppy and those greater than 530MB will remain as hard drive. The Forced FDD option can be used to force a hard disk type drive (such as a Zip drive) to boot as FDD.



8.3.7 PCI/PnP Setup

Select the PCI/PnP tab from the setup screen to enter the Plug and Play BIOS Setup screen. You can display a Plug and Play BIOS Setup option by highlighting it using the <Arrow> keys. The Plug and Play BIOS Setup screen is shown below.



Clear NVRAM

This option clears ESCD (Extended System Configuration Data) information in NVRAM.

Plug & Play O/S

When set to "Yes" and a Plug and Play operating system is installed, the operating system configures the Plug and Play devices not required for boot.

PCI Latency Timer

Allows you to select the value in units of PCI clocks for the PCI device latency timer register.

Allocate IRQ to PCI VGA

When set to "Yes", the BIOS will assign an IRQ for a PCI VGA card.

Palette Snooping

Normally this option is always Disabled. Non standard VGA display adapters such as overlay cards or MPEG video cards may not show colors properly. Setting this option to Enabled should correct this problem. If set to Enabled, any I/O access on the ISA bus to the VGA card's palette registers will be reflected on the PCI bus. This will allow overlay cards to adapt to the changing palette colors.

OffBoard PCI/ISA IDE Card

Set this option to allow the OffBoard PCI/ISA IDE Card to be selected.

IRQ

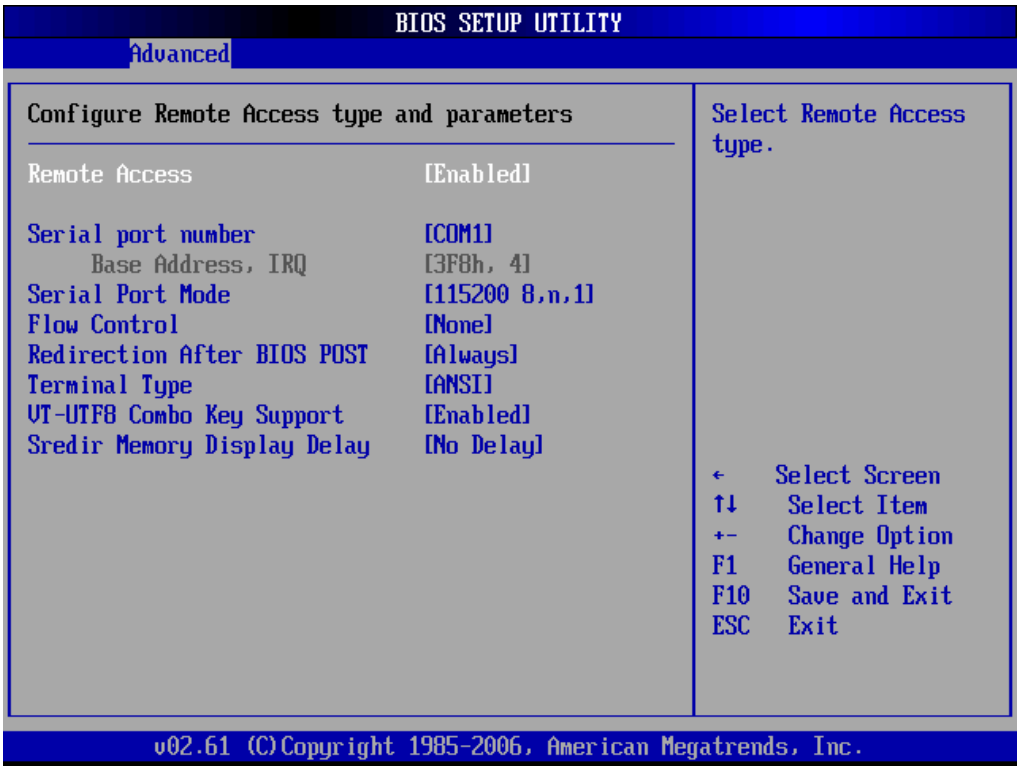
Set this value to allow the IRQ settings to be modified.

Available - This setting allows the specified IRQ to be used by a PCI/PnP device.
Reserved - This setting allows the specified IRQ to be used by a legacy ISA device.

8.3.8 Remote Access Configuration

Remote Access Configuration

You can use this screen to select options for the Remote Access Configuration, which provides the settings to allow remote access by another computer to get POST messages and issue commands through serial port access. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



Remote Access

Select this option to Enable or Disable the BIOS remote access feature.

NOTE: Enabled Remote Access requires a dedicated serial port connection. Once both serial ports are configured to disabled, you should set this value to Disabled or it may cause abnormal boot.

Serial Port Number

Select the serial port you want to use for the remote access interface. You can set the value for this option to either *COM1* or *COM2.*

If you have changed the resource assignment of the serial ports in Advanced>SuperIO Configuration, you must Save Changes and Exit, reboot the system, and enter the setup menu again in order to see those changes reflected in the available Remote Access options.

Serial Port Mode

Select the baud rate you want the serial port to use for console redirection. The options are 115200 8,n,1; 57600 8,n,1; 19200 8,n,1; and 09600 8,n,1.

Flow Control

Set this option to select Flow Control for console redirection. The settings for this value are None, Hardware, or Software.

Redirection After BIOS POST

This option allows you to set Redirection configuration after BIOS POST. The settings for this value are Disabled, Boot Loader, or Always.

Option	Description
Disabled	Set this value to turn off the redirection after POST
Boot Loader	Set this value to allow the redirection to be active during POST and Boot Loader.
Always	Set this value to allow the redirection to be always active.

Terminal Type

This option is used to select either VT100/VT-UTF8 or ANSI terminal type. The settings for this value are ANSI, VT100, or VT-UTF8.

VT-UTF8 Combo Key Support

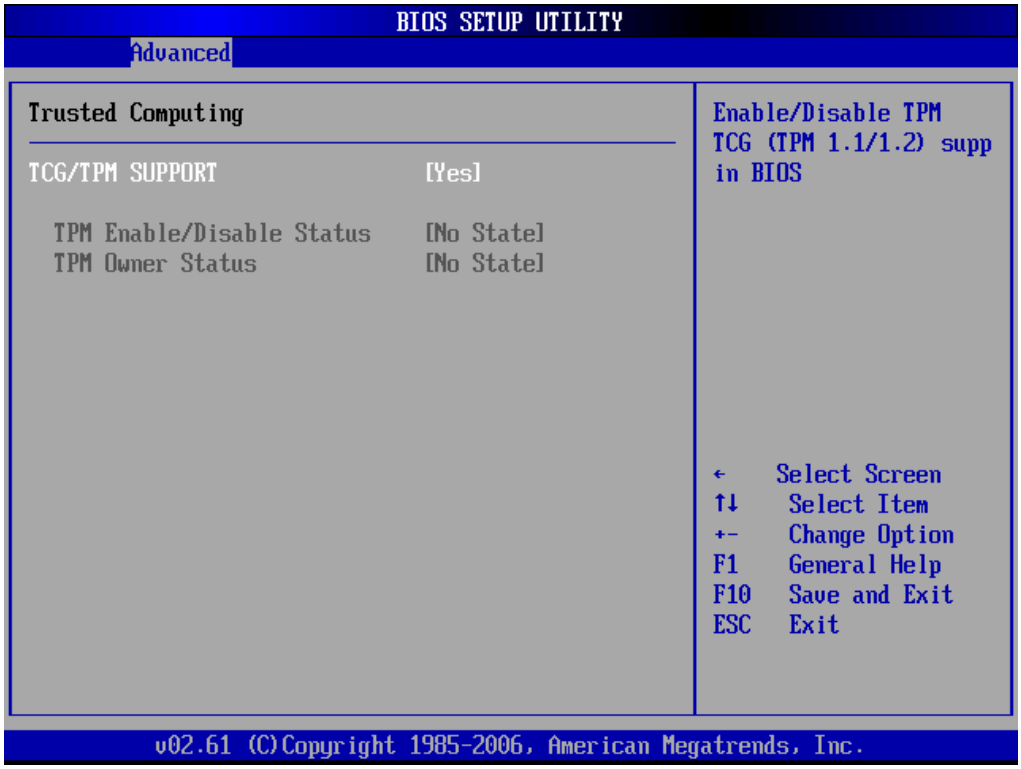
This option enables VT-UTF8 Combination Key Support for ANSI/VT100 terminals. The settings for this value are Enabled or Disabled.

Sredir Memory Display Delay

This option gives the delay in seconds to display memory information. The options for this value are No Delay, Delay 1 Sec, Delay 2 Sec, or Delay 4 Sec.

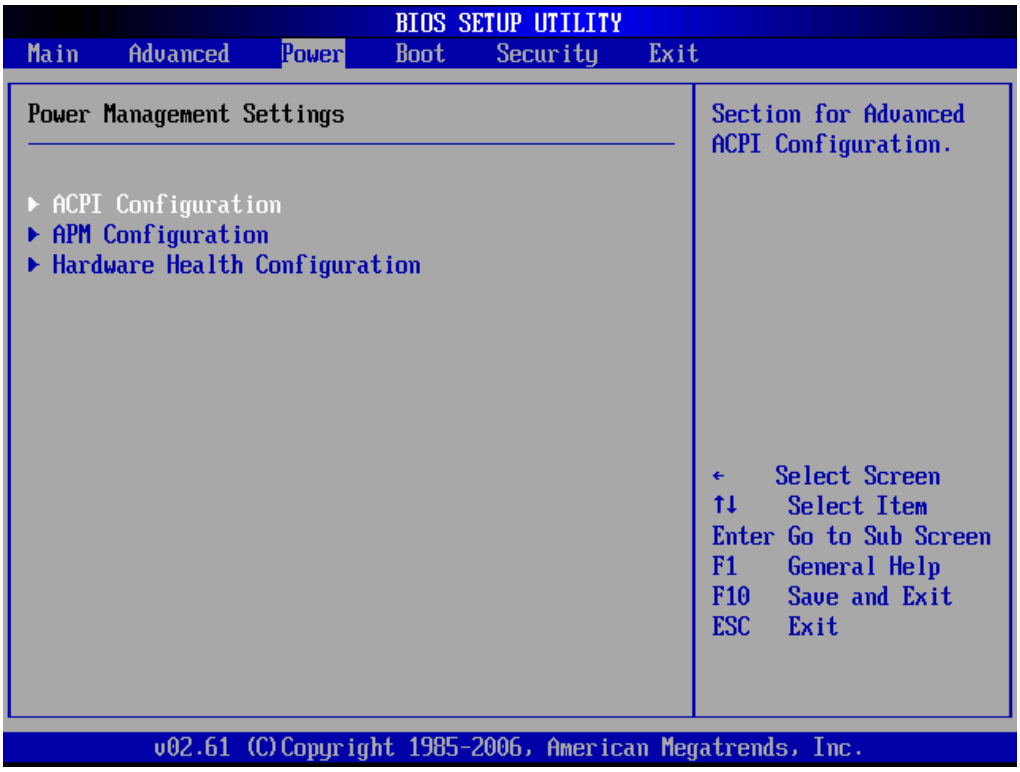
8.3.9 Trusted Computing

Trusted computing is an industry standard to make personal computers more secure through a dedicated hardware chip, called a Trusted Platform Module (TPM). This option allows you to enable or disable the TPM support.



8.4 Power Setup

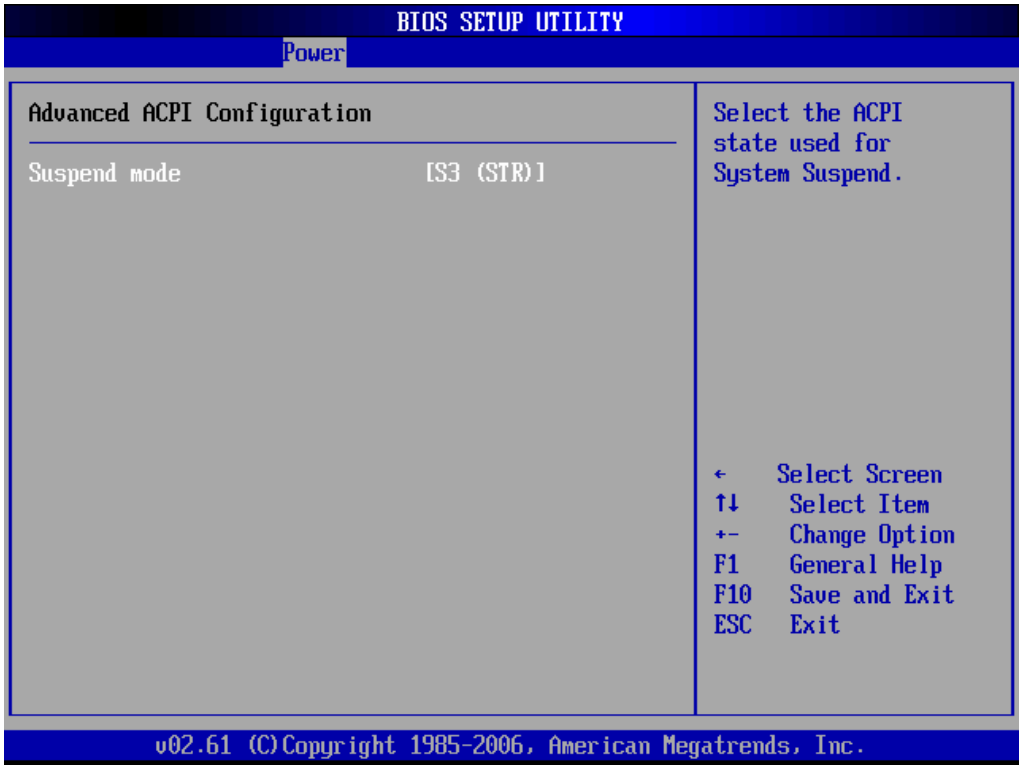
Select the Power tab from the setup screen to enter the Power Management Setting Setup screen. You can select any of the items in the left frame of the screen, such as ACPI Configuration, to go to the sub menu for that item. You can display a Power Management option by highlighting it using the < Arrow > keys. The Power Management BIOS Setup screen is shown below.



8.4.1 Advanced ACPI Configuration

Advanced ACPI Configuration

You can use this screen to select options for the Advanced ACPI Configuration settings. Use the up and down <Arrow> keys to select an item. Use the < + > and < - > keys to change the value of the selected option. The ACPI BIOS Setup screen is shown below.

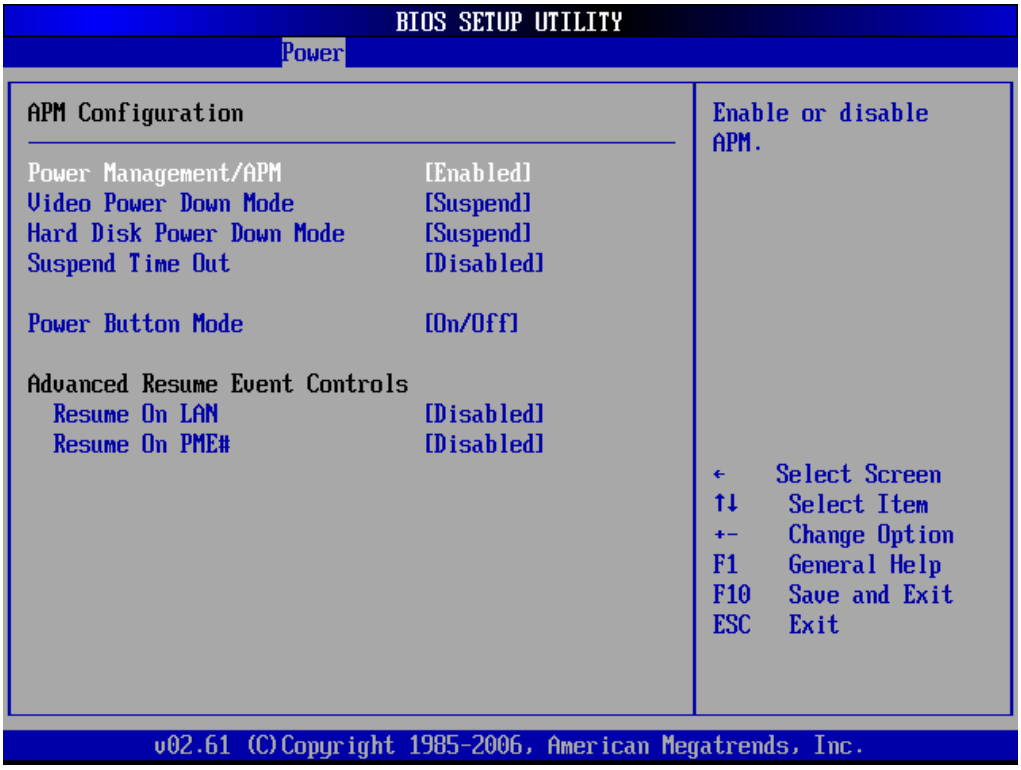


Suspend mode

This setting selects either S1 (POS) or S3 (STR) system suspend mode.

8.4.2 APM Configuration

You can use this screen to select options for the APM settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. The APM BIOS Setup screen is shown below.



Power Management/APM

Set this value to *Enable* or *Disable* Power Management/APM (Advanced Power Management) features.

Video Power Down Mode

This option specifies the power management state that the video subsystem enters when the BIOS places it in a power saving state after the period of inactivity specified in *Suspend Time Out* has expired. The options are *Disabled* and *Suspend*.

Hard Disk Drive Power Down Mode

This option specifies the power management state that the hard disk drive enters after the period of hard drive inactivity specified in *Suspend Time Out* has expired.

Suspend Time Out

This option specifies the length of time the system waits before it enters suspend mode. The options are *Disabled, 1 Min, 2 Min, 4 Min, 8 Min, 10 Min, 20 Min, 30 Min, 40 Min, 50 Min,* and *60 Min.*

Power Button Mode

This feature allows users to configure the Power Button function.

Option	Description
On/Off	Turn the system On/Off when the power button is pressed.
Suspend	The system goes into suspend mode or resumes from suspend mode when power button is pressed.

Restore on AC Power Loss

Determines what state the computer enters when AC power is restored after a power loss. The options for this value are Last State, Power On and Power Off.

Option	Description
Power Off	The system remains powered off when AC power is restored.
Power On	The system powers on after AC power is restored.
Last State	The system will power off/on depending on the last system power state when AC power is restored.

Advanced Resume Event Controls

Resume on LAN

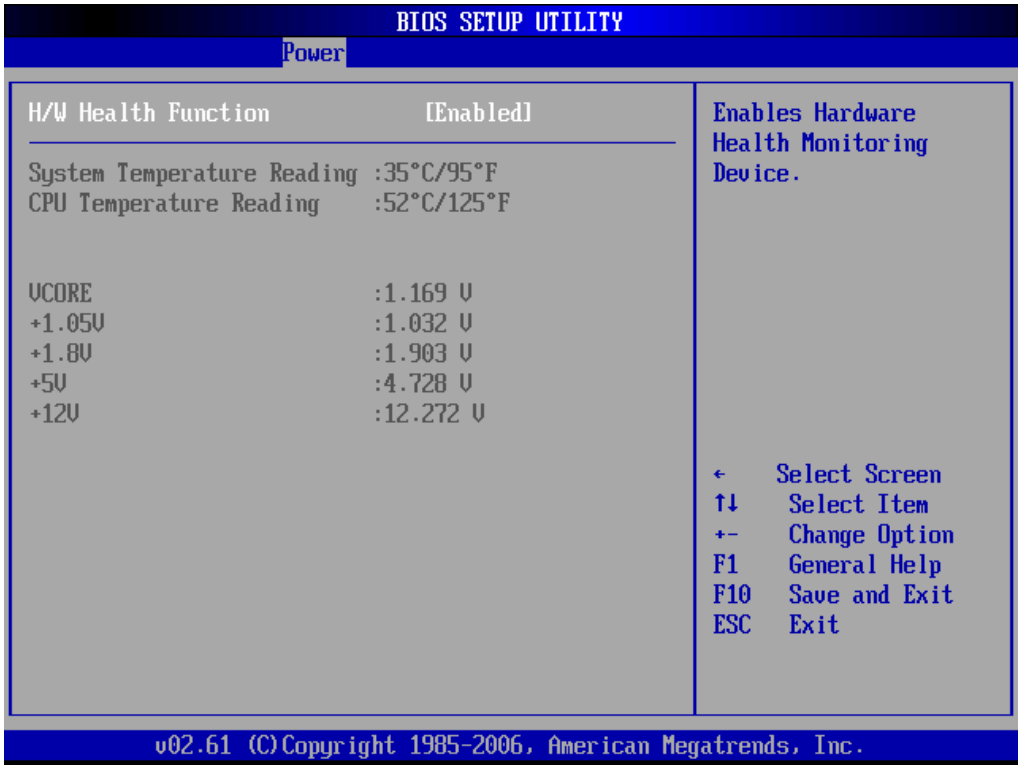
The item specifies how the system will be awakened from power saving mode by an onboard LAN device.

Resume on PME#

The item specifies how the system will be awakened from power saving mode when a PCI input signal is detected.

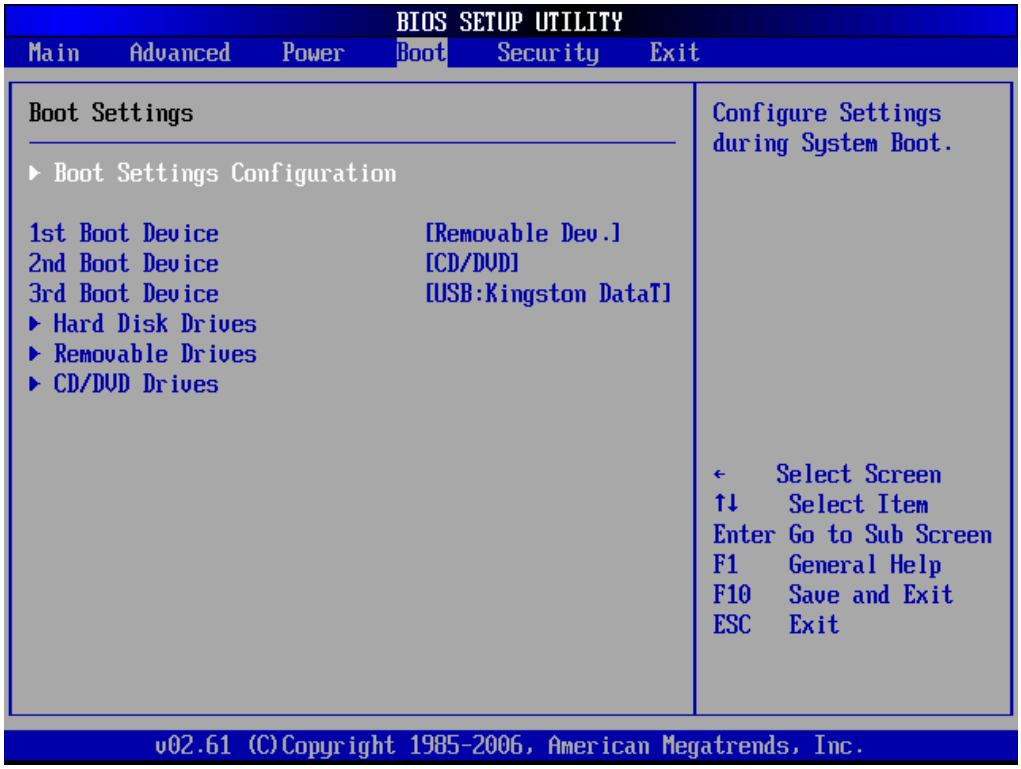
8.4.3 Hardware Health Configuration

This option displays the current status of all of the monitored hardware devices/components such as CPU voltages, temperatures and fan speeds. The options are Enabled and Disabled.



8.5 Boot Setup

Select the Boot tab from the setup screen to enter the Boot BIOS Setup screen. You can select any of the items in the left frame of the screen, such as Boot Device Priority, to go to the sub menu for that item. You can display an Boot BIOS Setup option by highlighting it using the < Arrow > keys. The Boot Settings screen is shown below:



Boot Device Priority

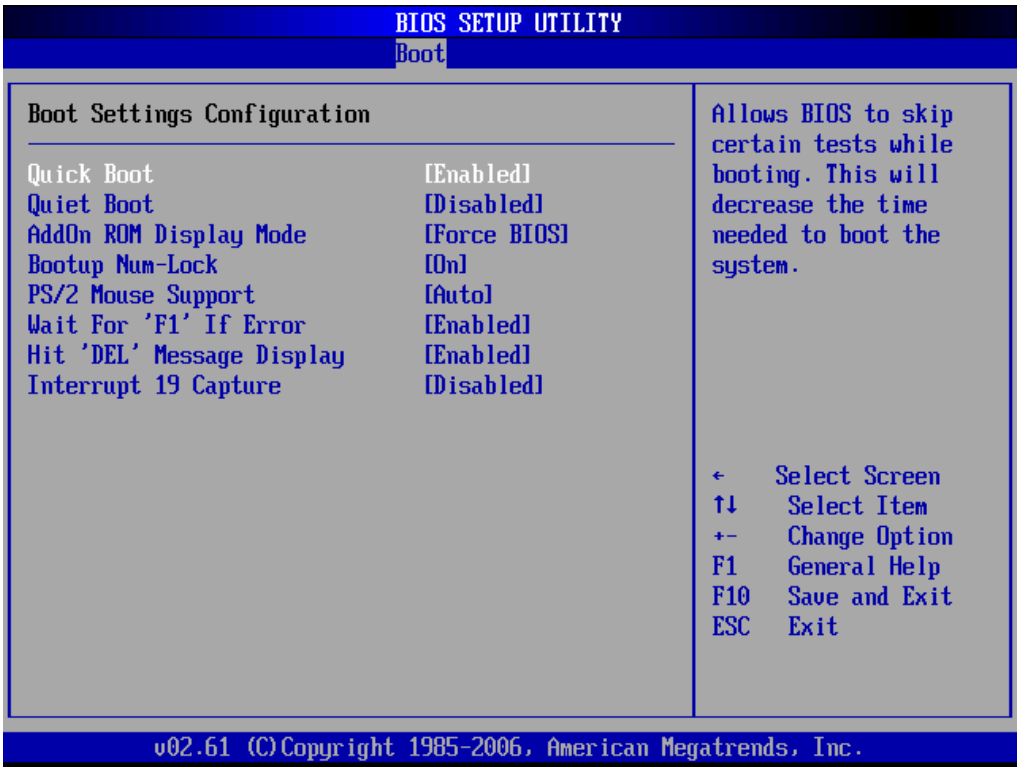
Set the boot device options to determine the sequence in which the computer checks which device to boot from.

Boot Device Groups

The Boot devices are listed in groups by device type. First press <Enter> to enter the sub-menu. Then you may use the arrow keys to select the desired device, then press <+>, <-> or <PageUp>, <PageDown> key to move it up/down in the priority list. For example, USB storage disks will be listed as “USB Drives” in the sub-menu. Only the first device in each device group will be available for selection in the Boot Device Priority option.

Boot Settings Configuration

Use this screen to select options for the Boot Settings Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The screen is shown below.



Quick Boot

Disabled - Set this value to allow the BIOS to perform all POST tests.
Enabled - Set this value to allow the BIOS to skip certain POST tests to boot faster.

Quiet Boot

Disabled - Set this value to allow the computer system to display the POST messages.
Enabled - Set this value to allow the computer system to display the OEM logo.

AddOn ROM Display Mode

This feature controls the display of ROM messages from the BIOS of add-on devices like graphics cards or SATA controllers during the boot sequence.

When set to Force BIOS, AddOn ROM messages will be forced to display during the boot sequence.

When set to Keep Current, AddOn ROM messages will only be displayed if the third-party manufacturer had set the add-on device to do so.

Bootup Num-Lock

Set this value to allow the Number Lock setting to be modified during boot up.
Off - This option does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard will light up when the Number Lock is engaged.
On - Set this value to allow the Number Lock on the keyboard to be enabled automatically when the computer system is boot up. This allows the immediate use of 10-keys numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard will be lit.

PS/2 Mouse Support

Allows you to enable/disable PS/2 mouse support.

Wait for 'F1' If Error

If this option is set to Disabled, AMIBIOS does not wait for you to press the <F1> key after an error message.

Hit 'DEL' Message Display

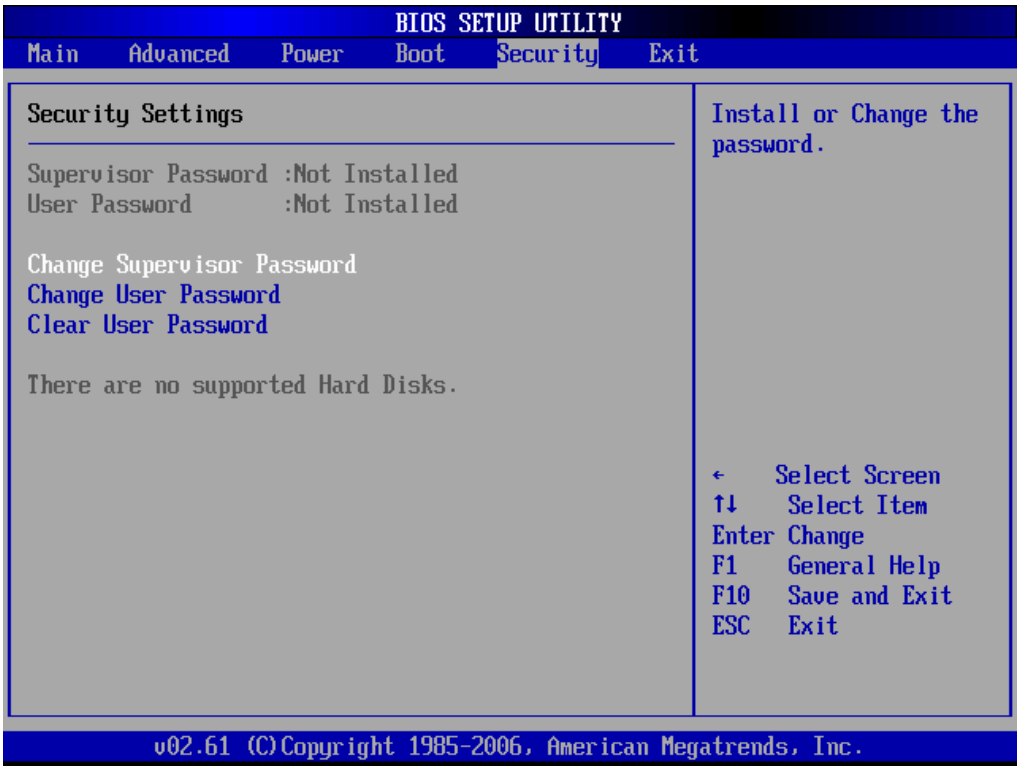
When set to Enabled, the system displays the message "Press DEL to run Setup during POST".

Interrupt 19 Capture

Interrupt 19 is the software interrupt that handles the boot disk function. When enabled, this feature allows the AddOn ROM of these host adaptors to "capture" Interrupt 19 during the boot process so that drives attached to these adaptors can function as bootable disks. In addition, it allows you to gain access to the host adaptor's AddOn ROM setup utility, if one is available.

When disabled, the AddOn ROM of these host adaptors will not be able to "capture" Interrupt 19. Therefore, you will not be able to boot operating systems from any bootable disks attached to these host adaptors. Nor will you be able to gain access to their AddOn ROM utilities.

8.6 Security Setup



8.6.1 Password Support

Two Levels of Password Protection

The BIOS provides both a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first.

The system can be configured so that all users must enter a password every time the system boots or when Setup is executed, using either or either the Supervisor password or User password.

The Supervisor and User passwords activate two different levels of password security. If you select password support, you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed. Make sure you write it down. If you forget it, you must drain NVRAM and re-configure.

Remember the Password

Keep a record of the new password when the password is changed. If you forget the password, you must erase the system configuration information in NVRAM.

Select Security Setup from the Setup main BIOS setup menu. Security Setup options, such as password protection and virus protection, are described in this section. To access the sub menu for the following items, select the item and press < Enter >:

- Change Supervisor Password
- Change User Password
- Clear User Password

Supervisor Password

Indicates whether a supervisor password has been set.

User Password

Indicates whether a user password has been set.

Change Supervisor Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to change the supervisor password.

Change User Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to change the user password.

Clear User Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to clear the user password.

8.6.2 Change Supervisor Password

Select Change Supervisor Password from the Security Setup menu and press < Enter >.

```
Enter New Password:
```

Type the password and press < Enter >. The screen does not display the characters entered. Retype the password as prompted and press < Enter >. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after setup completes.

8.6.3 Change User Password

Select Change User Password from the Security Setup menu and press < Enter >.

```
Enter New Password:
```

Type the password and press < Enter >. The screen does not display the characters entered. Retype the password as prompted and press < Enter >. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after setup completes.

8.6.4 Clear User Password

Select Clear User Password from the Security Setup menu and press < Enter >.

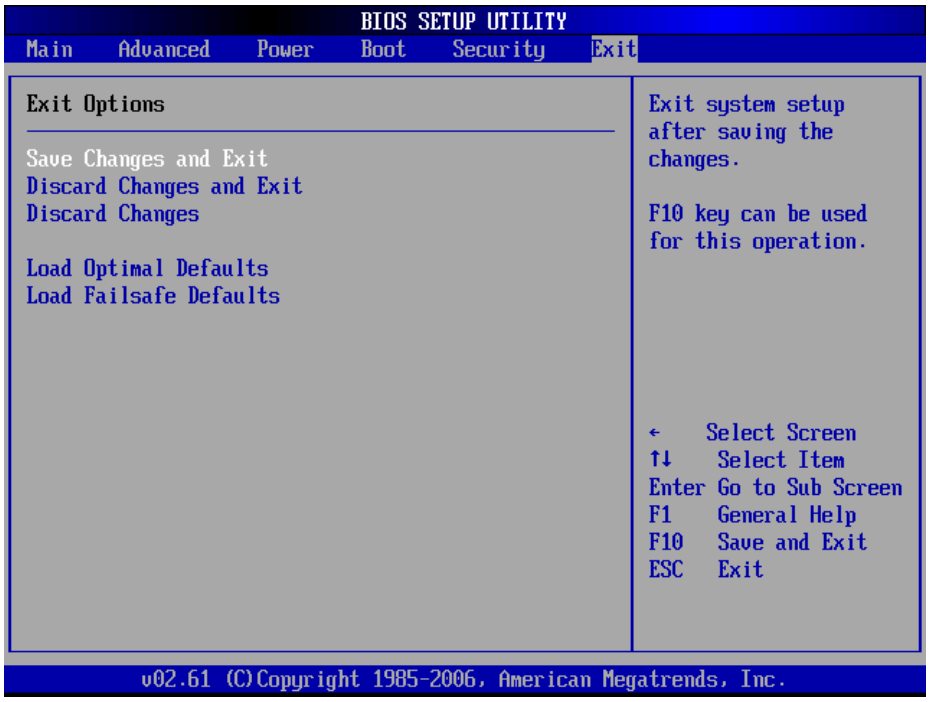
```
Clear New Password

[Ok] [Cancel]
```

Type the password and press < Enter >. The screen does not display the characters entered. Retype the password as prompted and press < Enter >. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after setup completes.

8.7 Exit Menu

Select the *Exit* tab from the setup screen to enter the Exit BIOS Setup screen. You can display an Exit BIOS Setup option by highlighting it using the <Arrow> keys. The Exit BIOS Setup screen is shown below.



Save Changes and Exit

When you have completed the system configuration changes, select this option to leave Setup and reboot the computer so the new system configuration parameters can take effect. Select Exit Saving Changes from the Exit menu and press < `Enter` >.

`Save Configuration Changes and Exit Now?`

`[Ok]  [Cancel]`

appears in the window. Select Ok to save changes and exit.

Discard Changes and Exit

Select this option to quit Setup without making any permanent changes to the system configuration. Select Exit Discarding Changes from the Exit menu and press <Enter>.

`Discard Changes and Exit Setup Now?`

`[Ok]  [Cancel]`

appears in the window. Select *Ok* to discard changes and exit.

Discard Changes

Select Discard Changes from the Exit menu and press < Enter >.

Select *Ok* to discard changes.

Load Optimal Defaults

Automatically sets all Setup options to a complete set of default settings when you Select this option. The Optimal settings are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Optimal Setup options if your computer is experiencing system configuration problems.

Select Load Optimal Defaults from the Exit menu and press < Enter >.

Select *Ok* to load optimal defaults.

Load Failsafe Defaults

Automatically sets all Setup options to a complete set of default settings when you Select this option. The Failsafe settings are designed for maximum system stability, but not maximum performance. Select the Fail-Safe Setup options if your computer is experiencing system configuration problems.

Select Load Fail-Safe Defaults from the Exit menu and press < Enter >.

```
Load Fail-Safe Defaults?

[Ok]   [Cancel]
```

appears in the window. Select Ok to load Fail-Safe defaults.

9 BIOS Checkpoints, Beep Codes

This section of this document lists checkpoints and beep codes generated by AMIBIOS. The checkpoints defined in this document are inherent to the AMIBIOS generic core, and do not include any chipset or board specific checkpoint definitions.

Checkpoints and Beep Codes Definition

A checkpoint is either a byte or word value output to I/O port 80h. The BIOS outputs checkpoints throughout bootblock and Power-On Self Test (POST) to indicate the task the system is currently executing. Checkpoints are very useful for debugging problems that occur during the preboot process.

Beep codes are used by the BIOS to indicate a serious or fatal error. They are used when an error occurs before the system video has been initialized, and generated by the system board speaker.

Viewing BIOS Checkpoints

Viewing all checkpoints generated by the BIOS requires a checkpoint card, also referred to as a "POST Card" or "POST Diagnostic Card". These are ISA or PCI add-in cards that show the value of I/O port 80h on a LED display.

Some computers display checkpoints in the bottom right corner of the screen during POST. This display method is limited, since it only displays checkpoints that occur after the video card has been activated.

Keep in mind that not all computers using AMIBIOS enable this feature. In most cases, a checkpoint card is the best tool for viewing AMIBIOS checkpoints.

9.1 Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS:

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs from add-in PCI devices.

Checkpoint	Description
Before D0	If boot block debugger is enabled, CPU cache-as-RAM functionality is enabled at this point. Stack will be enabled from this point.
D0	Early Boot Strap Processor (BSP) initialization like microcode update, frequency and other CPU critical initialization. Early chipset initialization is done.
D1	Early super I/O initialization is done including RTC and keyboard controller. Serial port is enabled at this point if needed for debugging. NMI is disabled. Perform keyboard controller BAT test. Save power-on CPUID value in scratch CMOS. Go to flat mode with 4GB limit and GA20 enabled.
D2	Verify the boot block checksum. System will hang here if checksum is bad.
D3	Disable CACHE before memory detection. Execute full memory sizing module. If memory sizing module not executed, start memory refresh and do memory sizing in Boot block code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM. Copies compressed boot block code to memory in right segments. Copies BIOS from ROM to RAM for faster access. Performs main BIOS checksum and updates recovery status accordingly.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. If BIOS recovery is necessary, control flows to checkpoint E0. See Bootblock Recovery Code Checkpoints section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See POST Code Checkpoints section of document for more information.
DC	System is waking from ACPI S3 state
E1-E8, EC-EE	OEM memory detection/configuration error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.

9.2 Bootblock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS:

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs From add-in PCI devices.

Checkpoint	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.
FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

9.3 POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS preboot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

Checkpoints may differ between different platforms based on system configuration.
Checkpoints may change due to vendor requirements, system chipset or option ROMs
From add-in PCI devices.

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer.Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
07	Fixes CPU POST interface calling pointer.
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache – Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor
C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
20	Relocate System Management Interrupt vector for all CPU in the system.
24	Uncompress and initialize any platform specific BIOS modules. GPNV is initialized at this checkpoint.
2A	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.

POST Code Checkpoints cont'd:

Checkpoint	Description
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information. USB controllers are initialized at this point.
39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, ... etc.) successfully installed in the system and update the BDA, EBDA…etc.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory. Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed / requested. Check boot password if installed.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disable NMI as selected
90	Initialization of system management interrupt by invoking all handlers. *Please note this checkpoint comes right after checkpoint 20h*
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module. Display boot option popup menu.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector.
AB	Prepare BBS for Int 19 boot. Init MP tables.
AC	End of POST initialization of chipset registers. De-initializes the ADM module.
B1	Save system context for ACPI. Prepare CPU for OS boot including final MTRR values.
00	Passes control to OS Loader (typically INT19h).

9.4 OEM POST Error Checkpoints

Checkpoints from the range 61h to 70h are reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.

9.5 DIM Code Checkpoints

The Device Initialization Manager (DIM) gets control at various times during BIOS POST to initialize different system busses. The following table describes the main checkpoints where the DIM module is accessed:

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs from add-in PCI devices.

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI- PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.

While control is in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two fields. The details of the high byte of these checkpoints are as follows:

HIGH BYTE XY

The upper nibble 'X' indicates the function number that is being executed. 'X' can be from 0 to 7.

0 = func#0, disable all devices on the BUS concerned.
1 = func#1, static devices initialization on the BUS concerned.
2 = func#2, output device initialization on the BUS concerned.
3 = func#3, input device initialization on the BUS concerned.
4 = func#4, IPL device initialization on the BUS concerned.
5 = func#5, general device initialization on the BUS concerned.
6 = func#6, error reporting for the BUS concerned.
7 = func#7, add-on ROM initialization for all BUSes.
8 = func#8, BBS ROM initialization for all BUSes.

The lower nibble 'Y' indicates the BUS on which the different routines are being executed. 'Y' can be from 0 to 5.

0 = Generic DIM (Device Initialization Manager).
1 = Onboard System devices.
2 = ISA devices.
3 = EISA devices.
4 = ISA PnP devices.
5 = PCI devices.

9.6 ACPI Runtime Checkpoints

ACPI checkpoints are displayed when an ACPI capable operating system either enters or leaves a sleep state. The following table describes the type of checkpoints that may occur during ACPI sleep or wake events:

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs from add-in PCI devices.

9.7 Boot Block Beep Codes

No. of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
3	Base Memory error
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

9.8 POST BIOS Beep Codes

No. of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
3	Base memory read/write test error
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

9.9 Troubleshooting POST BIOS Beep Codes

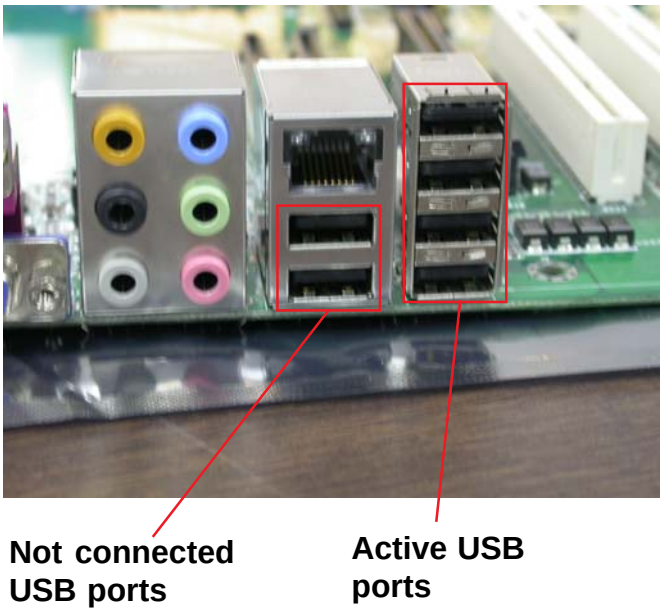
No. of Beeps	Description
1, 2 or 3	Reseat the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. - If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. - If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning card.
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

Appendix A: Available USB Ports

A.1 Description

The Intel® 3100 chipset supports 4 USB ports.

The figure on the right indicates which USB ports can be used on the Express-BASE carrier.



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Important Safety Instructions

For user safety, please read and follow all instructions, warnings, cautions, and notes marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:

  - Turn off power and unplug any power cords/cables.

- To avoid electrical shock and/or damage to equipment:

  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.
- A Lithium-type battery may be provided for uninterrupted, backup or emergency power.

Risk of explosion if battery is replaced by an incorrect type. Dispose of used batteries according to the instructions.

- Equipment must be serviced by authorized technicians when:

  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

Getting Service

Contact us should you require any service or assistance.

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