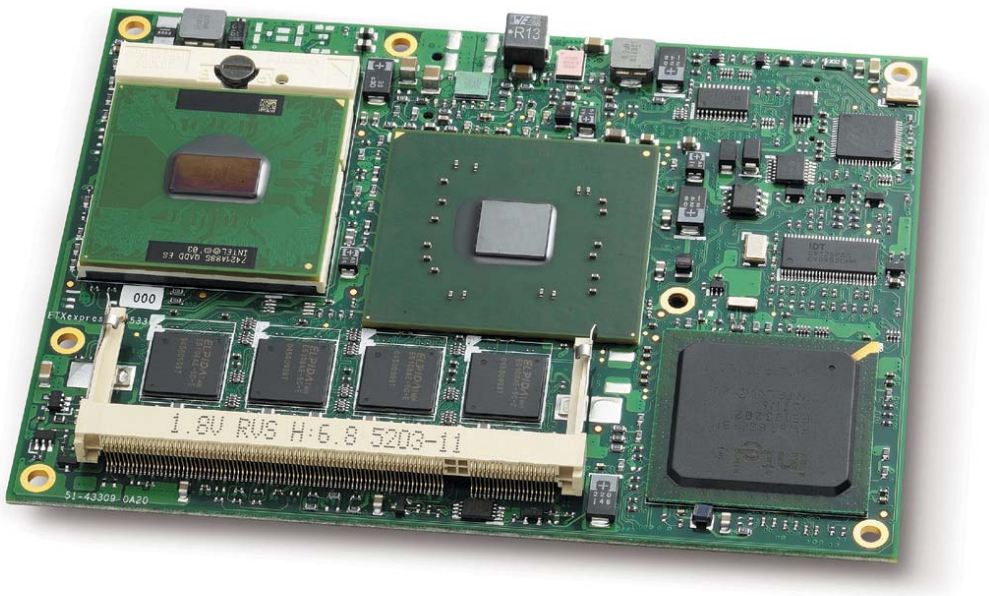
COM Express

Express-IA533

User's Manual



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ADLINK TECHNOLOGY INC.

Revision History

Release	Date	Change
2.10	2007/10/19	Initial Release
2.20	2007/11/12	Layout Revision Added Preface Section
2.21	2007/11/28	Revised BIOS information, Power Management Setup and PEG/VGA control
2.22	2007/12/17	Revised Intel Chipset specifications for Southbridge, removed TV-out support and revised functional diagram specs
2.30	2008/10/31	Correct pin definitions, add Signal Descriptions Correct address

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Preface

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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

Additional information, aids, and tips that help users perform tasks.

Information to prevent *mino*r physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

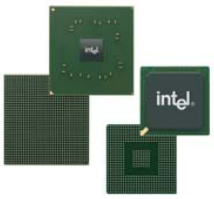
Information to prevent *serious* physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

1 Introduction

1.1 Description

Express modules are based on the new PICMG® form factor called COM Express™, the convergence of the latest technology standards based on serial differential signaling such as PCI Express®, USB 2.0, SATA, LVDS and Serial DVO. These standards are implemented on a compact, 95 mm x 125 mm, Computer on Module. Signals are brought out through two 220-pin board-to-board connectors that permit data transmission rates of up to 5 GHz. Six mounting holes connect the module with a custom-made, application specific carrier boards which provide protection from shock and vibration.

The Express-IA533 is based on Intel® 915GME with ICH6-M Southbridge with Enhanced Intel® Speedstep® support. It can support Intel Celeron® M and Pentium® M CPU's in the range of 600 MHz to 2.1 GHz at FSB400/533. Both chipsets and processors are part of the Embedded Intel® Architecture (IA) that warrants long production life for applications that need extended availability.



The Express-IA533 supports dual-channel DDR2 533 MHz memory, one bank soldered and one bank on the SODIMM. The 915GME GCMH has integrated graphic support for CRT, and single/dual-channel LVDS. In addition to the onboard integrated graphics, a Graphic PCI Express® x16 slot is available for connection to high end PCI Express® x16 Graphic chipsets. The PCI Express® Graphics (PEG) x16 bus can also be used to connect to SDVO devices for DVI or TMDS. The board allows connection of up to four additional PCI Express® x1 devices.

The module comes with a single onboard Gigabit Ethernet port and Dual-channel SATA. It has legacy support for Parallel IDE, 32-bit PCI™ and ISA through LPC. The Express-IA533 comes equipped with many embedded features such as: Remote console, CMOS backup in EEPROM, CPU and System monitoring and a Dual-Watchdog timer for NMI or RESET.

Express-IA533 is RoHS compliant and lead free product

2 Specifications

2.1 General

- CPU: Intel® Pentium® M or Intel® Celeron® M Processor with 400 or 533 MHz FSB with Enhanced Intel® Speedstep® Technology
- Memory: Channel A: SO-DIMM socket for DDR2 memory, max 1 GB
  Channel B: soldered DDR2 memory, max 1 GB
  both types non-ECC, unbuffered, 400/533 MHz DDR2
- Chipset: Intel® 915GME Express Graphic Memory Controller Hub
  Intel® I/O Controller Hub 6 Mobile (ICH6-M)
- L2 Cache: Banias type processors: 512 KB (Celeron® M), 1 MB (Pentium® M)
  Dothan type processors: 1 MB (Celeron® M), 2 MB (Pentium® M)
- BIOS: Phoenix BIOS in 1 MB FWH with console redirection and CMOS EEPROM backup
- Hardware Monitor: Supply Voltages and CPU temperature
- Watchdog Timer: Programmable timer ranges to generate RESET
- Expansion Busses:
  - Four PCI Express® x1 lanes (one occupied by onboard GbE)
  - Six 32-bit PCI 2.3 Masters at 33/66 MHz
  - Low Pin Count (LPC) interface for Super I/O on carrier
  - SMBus 2.0 interface support

2.2 Video

- Chipset: 915GME GMCH integrated chipset supports dual independent displays
- VGA Interface: Analog VGA support up to 2048 x1536 resolution
- LVDS Interface: Dual channel LVDS interface support up to 2x18 bpp
- Graphic Expansion busses
  - One x16 PCI Express® Graphics port
  - Two Serial DVO ports (multiplexed with PCI Express® x16)

2.3 Audio

- Chipset: Integrated in Intel® I/O Controller Hub 6 Mobile (ICH6-M)
- Audio Codec: On carrier, either High Definition Audio ("Azalia") interface or AC'97 v2.3 controller

2.4 LAN

- Chipset: Yukon®-EC 88E8053 PCI Express® Gigabit Ethernet Controller
- Type: Triple speed 10/100/1000BASE-T IEEE 802.3 compliant with fully integrated ASF 2.0 functionality

2.5 Multi I/O

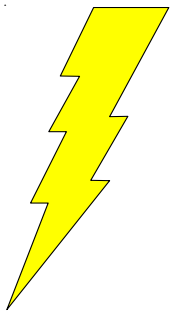
- Chipset: integrated in Intel® I/O Controller Hub 6 Mobile (ICH6-M)
- Keyboard / Mouse: through USB ports
- USB: supports up to eight USB 2.0 ports, supports legacy KB / Mouse
- SATA: two integrated Serial ATA 150 ports
- IDE (PATA): one Ultra ATA 100/66/33 IDE port

OPTIONAL

2.6 Super I/O

- Chipset: Winbond W83627HF (onboard Express-BASE reference carrier)
- Serial: Two high speed RS-232C ports (COM1/COM2)
- Parallel: SPP, EPP and ECP mode
- FDD: Two 3.5” Floppy drives
- IrDA: Supports SIR IrDA 1.1 compliant
- Keyboard & Mouse: One PS/2 keyboard and one PS/2 mouse

2.7 Module Power Consumption



All power testing was done on power supply wiring leading to the Express carrier board. Although all voltages were measured, only 12 V and 5 VSB are relevant because they are the only ones used by the Express module. The typical power level was measured under Windows 2000 without applications running. Maximum level was measured under 100% system stress generate by HCT and Kpower loading.

Testing was done with 512 MB DDR2 533 on installed SODIMM.

Express-IA533-373/0 (BGA type Celeron M 373 at 1 GHz)	
Standby	TBD
Typical	12 W
Max	16 W

Express-IA533-738/0 (BGA type Pentium M 738 at 1.4 GHz)	
Standby	TBD
Typical	14 W
Max	20 W

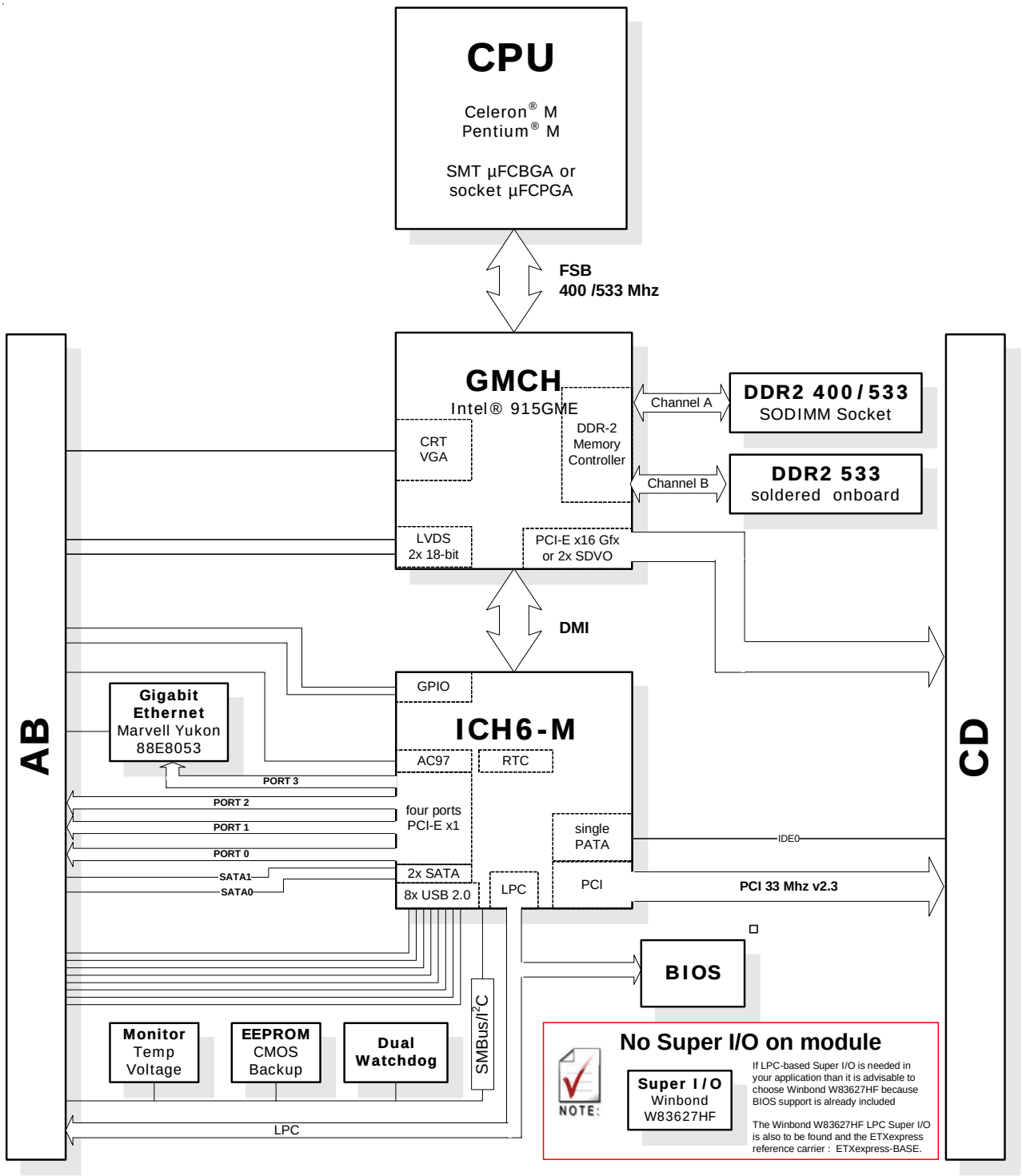
Express-IA533-S/0 with socket type Pentium M 745 at 1.8 GHz	
Standby	TBD
Typical	19 W
Max	29 W

Express-IA533-S/0 with socket type Pentium M 760 at 2.0 GHz	
Standby	TBD
Typical	20 W
Max	32 W

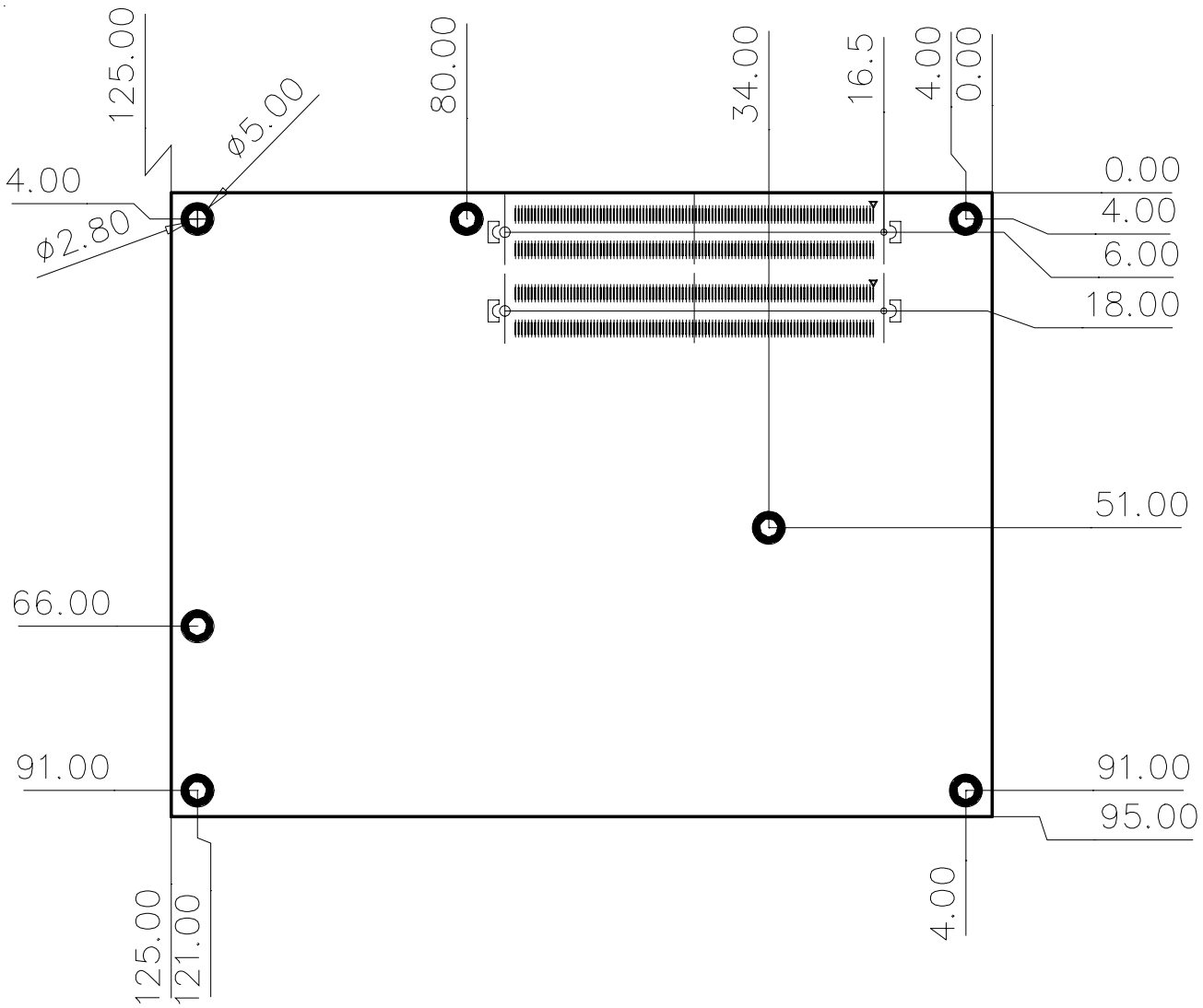
2.8 Mechanical and Environmental

- Form factor: Standard COM Express Type II
- Dimensions: 95 x 125 mm
- Operating Temperature: 0 to 55°C
- Relative Humidity: up to 90% @ 55°C
- Weight: 87 grams

3 Function diagram



4 Mechanical Dimensions



5 Watchdog Timer

Express-IA533 implements an on module external I²C Watchdog timer. The Watchdog timer consists of a one-second/ minute resolution down counter. If the counter ever reaches 1, before the software restarts it, the software is presumed to be malfunctioning and the processor's RESET signal is asserted.

The WDT has the following configuration registers:

- STS_WD_TMOUT Register 36h, bit 6
  Watchdog timeout indicator. 1 means the watchdog has timed out. This register can only be reset to 0 by writing a 1 to it.
- WD_ENABLE Register 36h, bit 5
  Write 1 to enable the Watchdog, and write 0 to disable.
- WD_PULSE Register 36h, bit 4
  Watchdog level/pulse upon timeout.
  Write 1 to enable pulse, and write 0 to enable level.
- WD_UNIT Register 36h, bit 3
  Watchdog units selection. Write 1 to enable minutes, and write 0 to enable seconds.
- WD_HACTIVE Register 36h, bit 2
  Watchdog timeout output level. Write 1 to enable high, and write 0 to enable low.
- WD_PSWIDTH Register 36h, bit 1-0
  Watchdog timeout pulse width. 00b = 1ms, 01b=20ms, 10b=100ms, 11b=4s
- WD_TIME Register 37h, bit 7-0
  Watchdog timeout value. Range from 0 to 255 in either seconds or minutes (WD_UNIT)

The example in C shown on the next pages offers an interactive way to test the Watchdog timer under DOS.

```
#include<CONIO.H>
#include<DOS.H>
#include<stdio.h>
#include<stdlib.h>

#define TEXTBOX_Y 10
#define SMBus_Port 0x500
#define I2C_Decode_Adr  0x9c

void DisplayString(void);
void Ct_Chk_I2C_Ready(void);
void Ct_I2C_WWord(int Dev_id,int Reg_index,int Value);
int Ct_I2C_RByte(int Dev_id,int Reg_index);
int value=0,temp=0,unit=0;

int main(argc,argv)
int argc;
unsigned char *argv[];
{
   unit=atoi(argv[1]);
   value=atoi(argv[2]);
//   printf("Argc=%d\n",argc);
//   printf("Argv=%d\n",value);
      if(argc!= 3 || value>255 )
      {
            printf("\nInvalid switch !!\a\n");
            printf("\nUsage= I2CWDT %1 %2 ( Ex. I2CWDT 1 5 ) ");
            printf("\n   %1= Unit select – 0:Minutes / 1:Seconds ");
            printf("\n   %2= Timer Range");
            printf("\nWDT Timer supports 0~255 Minute/Sec ");
            printf("\n");
            return 1;
      }

      clrscr(); //Clear the whole screen
      //Display Utility information and how to use is
      DisplayString();

      //Reset all registers
      temp=Ct_I2C_RByte(I2C_Decode_Adr,0x01);
      temp=temp | 0x88;
      Ct_I2C_WWord(I2C_Decode_Adr,0x01,temp);

      //Set Pin 10 to WDT Function
      temp=Ct_I2C_RByte(I2C_Decode_Adr,0x03);    //read the original status
value
      temp=temp | 0x03;                                  //OR back to temp
      Ct_I2C_WWord(I2C_Decode_Adr,0x03,temp);    //write back all

      //Set GPIO16(Pin 4) to LED Function
      temp=Ct_I2C_RByte(I2C_Decode_Adr,0x04);
      temp=temp | 0x01;
      Ct_I2C_WWord(I2C_Decode_Adr,0x04,temp);
```

```
        //Set GPIO(Pin 4) to LED Function 1Hz
        temp=Ct_I2C_RByte(I2C_Decode_Adr,0x07);
        temp=temp & 0xCF;
        temp=temp | 0x20;
        Ct_I2C_WWord(I2C_Decode_Adr,0x07,temp);

        //Set Timer Value (Minute/Second)
        Ct_I2C_WWord(I2C_Decode_Adr,0x37,value);

        //Bit6   Write will clear this bit
        //Bit5   Enable watchdog timer
        //Bit4   WDT Output Plus
        //Bit3   WDT Unit select second
        //Bit2   This pin will drive low
        //Bit1/0 WDT Plus width 4 Second
        temp=Ct_I2C_RByte(I2C_Decode_Adr,0x36);

        if(unit==0)
        {temp=temp | 0x7b;} //Minute
        else
        {temp=temp | 0x73;} //Second

        Ct_I2C_WWord(I2C_Decode_Adr,0x36,temp);

        return 1;
}

void DisplayString(void)
{
        gotoxy(15,2);
        textcolor(WHITE);
        printf("ADLINK Express-IA533 I2C Bus WDT Test Utility");
        gotoxy(15,4);
        printf("This will enable WDT and reset the system in ?? seconds");
}

void Ct_I2C_WWord(int Dev_id,int Reg_index,int Value)
{
        outportb(SMBus_Port+4,Dev_id); //Select I2C Device
        delay(1);

        Ct_Chk_I2C_Ready();

        outportb(SMBus_Port+3,Reg_index); //Set control register
        delay(1);
        outportb(SMBus_Port+5,(Value & 0x00FF)); //Write value to I2C device
        delay(1);
        outportb(SMBus_Port+6,((Value & 0xFF00)>>8)); //Write value to I2C device
        delay(1);
        outportb(SMBus_Port+2,0x4C); //SMBus Control byte write command
        delay(5);
        Ct_Chk_I2C_Ready(); //Check SMBus ready?
}
```

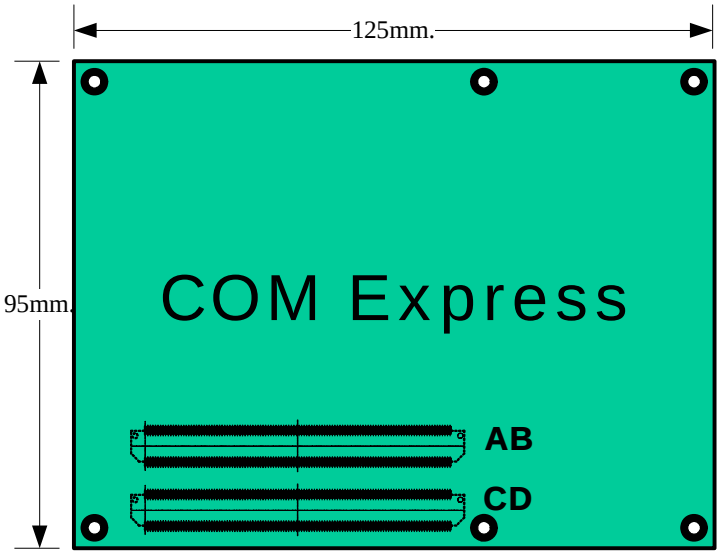
```
int Ct_I2C_RByte(int Dev_id,int Reg_index)
{
      int Get_value;

      outportb(SMBus_Port+3,Reg_index); //Set Index Byte to Read
      delay(1);

      outportb(SMBus_Port+4,Dev_id|0x01); //0x1A=SMBus DAC Address
      delay(1);

      Ct_Chk_I2C_Ready();

      outportb(SMBus_Port+2,0x48); //Start I2C Read Operation
      delay(1);

      Ct_Chk_I2C_Ready();

      Get_value=inportb(SMBus_Port+5);
      return Get_value;
}

void Ct_Chk_I2C_Ready(void)
{
      int status,flag=0;

      status=inport(SMBus_Port); //SMBus Status control
      while((status | status) !=0)   //Status = 0 -> Not busy
      {
          while((status & 0x04) !=0) //Status = 4 -> Has error
            {
                  flag=1;
                  outportb(SMBus_Port,status); //Clear error bit
                  delay(1);
                  status=inportb(SMBus_Port);
            }
          if(flag==1)
            break;
          else
            {
                  delay(5);
                  outportb(SMBus_Port,status);
            }
          status=inportb(SMBus_Port);
      }
}
```

6 Connectors

6.1 COM Express Type 2

All pinouts on AB and CD connector of the Express-IA533 comply with pin-out and signal descriptions used in the original "PICMG® COM.0 R1.0: COM Express™ Module Base Specification". This document contains a description of pinouts, signal descriptions, and mechanical characteristics of the COM Express® (Express®) form factor.

An additional document, " Express® Design Guide" gives a general introduction to carrier board designs for COM Express™ (Express®) modules.



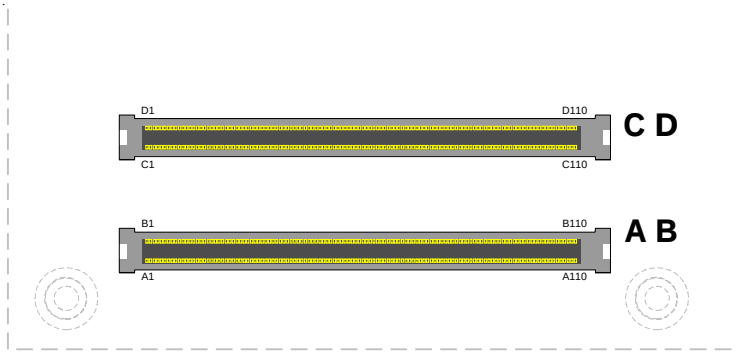
AB Connector
1 Gigabit Ethernet port
LPC interface
4 Serial ATA channels
High Definition Audio
8 USB 2.0 ports
6 PCI Express Lanes x1
Dual 24-bit LVDS channels
Analog VGA
TV-out ports (SDTV/HDTV)
8 GPIO pins
+12V primary power input
+5V standby and 3V RTC

CD Connector
Parallel ATA, IDE port alternate definition assigns this to 2 additional Gigabit Ethernet ports
32-bit PCI v2.3 bus alternate definition assigns this to 10 additional PCI Express x1 lanes
PCI Express x16 for Graphics these pins can also be assigned to two SDVO extensions (multiplexed)
SMB and I^2C bus
Power / Thermal control
+12V primary power input

6.2 COM Express™ Board to Board Connectors

Signals and Pin-out for:

Basic form factor, Type 2.



	Row A			Row B
Pin No.	Pin Name		Pin No.	Pin Name
A1	GND (FIXED)		B1	GND (FIXED)
A2	GBE0_MDI3-		B2	GBE0_ACT#
A3	GBE0_MDI3+		B3	LPC_FRAME#
A4	GBE0_LINK100#		B4	LPC_AD0
A5	GBE0_LINK1000#		B5	LPC_AD1
A6	GBE0_MDI2-		B6	LPC_AD2
A7	GBE0_MDI2+		B7	LPC_AD3
A8	GBE0_LINK#		B8	LPC_DRQ0#
A9	GBE0_MDI1-		B9	LPC_DRQ1#
A10	GBE0_MDI1+		B10	LPC_CLK
A11	GND (FIXED)		B11	GND (FIXED)
A12	GBE0_MDI0-		B12	PWRBTN#
A13	GBE0_MDI0+		B13	SMB_CK
A14	GBE0_CTREF		B14	SMB_DAT
A15	SUS_S3#		B15	SMB_ALERT#
A16	SATA0_TX+		B16	SATA1_TX+
A17	SATA0_TX-		B17	SATA1_TX-
A18	SUS_S4#		B18	SUS_STAT#
A19	SATA0_RX+		B19	SATA1_RX+
A20	SATA0_RX-		B20	SATA1_RX-
A21	GND (FIXED)		B21	GND (FIXED)
A22	NC		B22	NC
A23	NC		B23	NC
A24	SUS_S5#		B24	PWR_OK
A25	NC		B25	NC
A26	NC		B26	NC
A27	BATLOW#		B27	WDT
A28	ATA_ACT#		B28	AC_SDIN2
A29	AC_SYNC		B29	AC_SDIN1
A30	AC_RST#		B30	AC_SDIN0
A31	GND (FIXED)		B31	GND (FIXED)
A32	AC_BITCLK		B32	SPKR
A33	AC_SDOUT		B33	NC
A34	BIOS_DISABLE#		B34	NC
A35	THRMTRIP#		B35	THRM#
A36	USB6-		B36	USB7-
A37	USB6+		B37	USB7+
A38	USB_6_7_OC#		B38	USB_4_5_OC#
A39	USB4-		B39	USB5-
A40	USB4+		B40	USB5+
A41	GND (FIXED)		B41	GND (FIXED)
A42	USB2-		B42	USB3-
A43	USB2+		B43	USB3+
A44	USB_2_3_OC#		B44	USB_0_1_OC#
A45	USB0-		B45	USB1-
A46	USB0+		B46	USB1+
A47	VCC_RTC		B47	EXCD1_PERST#
A48	EXCD0_PERST#		B48	EXCD1_CPPE#
A49	EXCD0_CPPE#		B49	SYS_RESET#
A50	LPC_SERIRQ		B50	CB_RESET#

	Row C			Row D
Pin No.	Pin Name		Pin No.	Pin Name
C1	GND FIXED)		D1	GND FIXED)
C2	IDE_D7		D2	IDE_D5
C3	IDE_D6		D3	IDE_D10
C4	IDE_D3		D4	IDE_D11
C5	IDE_D15		D5	IDE_D12
C6	IDE_D8		D6	IDE_D4
C7	IDE_D9		D7	IDE_D0
C8	IDE_D2		D8	IDE_REQ
C9	IDE_D13		D9	IDE_IOW#
C10	IDE_D1		D10	IDE_ACK#
C11	GND (FIXED)		D11	GND (FIXED)
C12	IDE_D14		D12	IDE_IRQ
C13	IDE_IORDY		D13	IDE_A0
C14	IDE_IOR#		D14	IDE_A1
C15	PCI_PME#		D15	IDE_A2
C16	NC		D16	IDE_CS1#
C17	NC		D17	IDE_CS3#
C18	PCI_GNT1#		D18	IDE_RESET#
C19	PCI_REQ1#		D19	NC
C20	PCI_GNT0#		D20	NC
C21	GND (FIXED)		D21	GND (FIXED)
C22	PCI_REQ0#		D22	PCI_AD1
C23	PCI_RESET#		D23	PCI_AD3
C24	PCI_AD0		D24	PCI_AD5
C25	PCI_AD2		D25	PCI_AD7
C26	PCI_AD4		D26	PCI_C/BE0#
C27	PCI_AD6		D27	PCI_AD9
C28	PCI_AD8		D28	PCI_AD11
C29	PCI_AD10		D29	PCI_AD13
C30	PCI_AD12		D30	PCI_AD15
C31	GND (FIXED)		D31	GND (FIXED)
C32	PCI_AD14		D32	PCI_PAR
C33	PCI_C/BE1#		D33	PCI_SERR#
C34	PCI_PERR#		D34	PCI_STOP#
C35	PCI_LOCK#		D35	PCI_TRDY#
C36	PCI_DEVSEL#		D36	PCI_FRAME#
C37	PCI_IRDY#		D37	PCI_AD16
C38	PCI_C/BE2#		D38	PCI_AD18
C39	PCI_AD17		D39	PCI_AD20
C40	PCI_AD19		D40	PCI_AD22
C41	GND (FIXED)		D41	GND (FIXED)
C42	PCI_AD21		D42	PCI_AD24
C43	PCI_AD23		D43	PCI_AD26
C44	PCI_C/BE3#		D44	PCI_AD28
C45	PCI_AD25		D45	PCI_AD30
C46	PCI_AD27		D46	PCI_IRQC#
C47	PCI_AD29		D47	PCI_IRQD#
C48	PCI_AD31		D48	PCI_CLKRUN#
C49	PCI_IRQA#		D49	PCI_M66EN#
C50	PCI_IRQB#		D50	PCI_CLK

Signals and Pin-outs (cont'd)

Row A			Row B	
Pin No.	Pin Name		Pin No.	Pin Name
A51	GND (FIXED)		B51	GND (FIXED)
A52	NC		B52	NC
A53	NC		B53	NC
A54	GPI0		B54	GPO1
A55	NC		B55	NC
A56	NC		B56	NC
A57	GND		B57	GPO2
A58	NC		B58	NC
A59	NC		B59	NC
A60	GND (FIXED)		B60	GND (FIXED)
A61	PCIE_TX2+		B61	PCIE_RX2+
A62	PCIE_TX2-		B62	PCIE_RX2-
A63	GPI1		B63	GPO3
A64	PCIE_TX1+		B64	PCIE_RX1+
A65	PCIE_TX1-		B65	PCIE_RX1-
A66	GND		B66	WAKE0#
A67	GPI2		B67	WAKE1#
A68	PCIE_TX0+		B68	PCIE_RX0+
A69	PCIE_TX0-		B69	PCIE_RX0-
A70	GND (FIXED)		B70	GND (FIXED)
A71	LVDS_A0+		B71	LVDS_B0+
A72	LVDS_A0-		B72	LVDS_B0-
A73	LVDS_A1+		B73	LVDS_B1+
A74	LVDS_A1-		B74	LVDS_B1-
A75	LVDS_A2+		B75	LVDS_B2+
A76	LVDS_A2-		B76	LVDS_B2-
A77	LVDS_VDD_EN		B77	NC
A78	NC		B78	NC
A79	NC		B79	LVDS_BKLT_EN
A80	GND (FIXED)		B80	GND (FIXED)
A81	LVDS_A_CK+		B81	LVDS_B_CK+
A82	LVDS_A_CK-		B82	LVDS_B_CK-
A83	LVDS_I2C_CK		B83	LVDS_BKLT_CTRL
A84	LVDS_I2C_DAT		B84	VCC_5V_SBY
A85	GPI3		B85	VCC_5V_SBY
A86	KBD_RST#		B86	VCC_5V_SBY
A87	KBD_A20GATE		B87	VCC_5V_SBY
A88	PCIE0_CK_REF+		B88	RSVD
A89	PCIE0_CK_REF-		B89	VGA_RED
A90	GND (FIXED)		B90	GND (FIXED)
A91	RSVD		B91	VGA_GRN
A92	RSVD		B92	VGA_BLU
A93	GPO0		B93	VGA_HSYNC
A94	RSVD		B94	VGA_VSYNC
A95	RSVD		B95	VGA_I2C_CK
A96	GND		B96	VGA_I2C_DAT
A97	VCC_12V		B97	TV_DAC_A
A98	VCC_12V		B98	TV_DAC_B
A99	VCC_12V		B99	TV_DAC_C
A100	GND (FIXED)		B100	GND (FIXED)
A101	VCC_12V		B101	VCC_12V
A102	VCC_12V		B102	VCC_12V
A103	VCC_12V		B103	VCC_12V
A104	VCC_12V		B104	VCC_12V
A105	VCC_12V		B105	VCC_12V
A106	VCC_12V		B106	VCC_12V
A107	VCC_12V		B107	VCC_12V
A108	VCC_12V		B108	VCC_12V
A109	VCC_12V		B109	VCC_12V
A110	GND (FIXED)		B110	GND (FIXED)

Row C			Row D	
Pin No.	Pin Name		Pin No.	Pin Name
C51	GND (FIXED)		D51	GND (FIXED)
C52	PEG_RX0+		D52	PEG_TX0+
C53	PEG_RX0-		D53	PEG_TX0-
C54	TYPE0# (NC)		D54	PEG_LANE_RV#
C55	PEG_RX1+		D55	PEG_TX1+
C56	PEG_RX1-		D56	PEG_TX1-
C57	TYPE1# (NC)		D57	TYPE2# (NC)
C58	PEG_RX2+		D58	PEG_TX2+
C59	PEG_RX2-		D59	PEG_TX2-
C60	GND (FIXED)		D60	GND (FIXED)
C61	PEG_RX3+		D61	PEG_TX3+
C62	PEG_RX3-		D62	PEG_TX3-
C63	RSVD		D63	RSVD
C64	RSVD		D64	RSVD
C65	PEG_RX4+		D65	PEG_TX4+
C66	PEG_RX4-		D66	PEG_TX4-
C67	RSVD		D67	GND
C68	PEG_RX5+		D68	PEG_TX5+
C69	PEG_RX5-		D69	PEG_TX5-
C70	GND (FIXED)		D70	GND (FIXED)
C71	PEG_RX6+		D71	PEG_TX6+
C72	PEG_RX6-		D72	PEG_TX6-
C73	SDVO_DATA		D73	SDVO_CLK
C74	PEG_RX7+		D74	PEG_TX7+
C75	PEG_RX7-		D75	PEG_TX7-
C76	GND		D76	GND
C77	RSVD		D77	IDE_CBLID#
C78	PEG_RX8+		D78	PEG_TX8+
C79	PEG_RX8-		D79	PEG_TX8-
C80	GND (FIXED)		D80	GND (FIXED)
C81	PEG_RX9+		D81	PEG_TX9+
C82	PEG_RX9-		D82	PEG_TX9-
C83	RSVD		D83	RSVD
C84	GND		D84	GND
C85	PEG_RX10+		D85	PEG_TX10+
C86	PEG_RX10-		D86	PEG_TX10-
C87	GND		D87	GND
C88	PEG_RX11+		D88	PEG_TX11+
C89	PEG_RX11-		D89	PEG_TX11-
C90	GND (FIXED)		D90	GND (FIXED)
C91	PEG_RX12+		D91	PEG_TX12+
C92	PEG_RX12-		D92	PEG_TX12-
C93	GND		D93	GND
C94	PEG_RX13+		D94	PEG_TX13+
C95	PEG_RX13-		D95	PEG_TX13-
C96	GND		D96	GND
C97	RSVD		D97	PEG_ENABLE#
C98	PEG_RX14+		D98	PEG_TX14+
C99	PEG_RX14-		D99	PEG_TX14-
C100	GND (FIXED)		D100	GND (FIXED)
C101	PEG_RX15+		D101	PEG_TX15+
C102	PEG_RX15-		D102	PEG_TX15-
C103	GND		D103	GND
C104	VCC_12V		D104	VCC_12V
C105	VCC_12V		D105	VCC_12V
C106	VCC_12V		D106	VCC_12V
C107	VCC_12V		D107	VCC_12V
C108	VCC_12V		D108	VCC_12V
C109	VCC_12V		D109	VCC_12V
C110	GND (FIXED)		D110	GND (FIXED)

6.3 Signal Descriptions

Row A

Pin	Signal	Description	Type	PU/PD	Comment
A1	GND	Ground	PWR	-	-
A2	GBE0_MDI3-	Ethernet Receive Data -	I/O - DP	-	-
A3	GBE0_MDI3+	Ethernet Receive Data +	I/O - DP	-	-
A4	GBE0_LINK100#	Ethernet Speed LED (100Mb)	O-3,3	-	On at 100Mb/s
A5	GBE0_LINK1000#	Ethernet Speed LED (1000Mb)	O-3,3	-	On at 1000Mb/s
A6	GBE0_MDI2-	Ethernet Receive Data -	I/O - DP	-	-
A7	GBE0_MDI2+	Ethernet Receive Data +	I/O - DP	-	-
A8	GBE0_LINK#	LAN Link LED	O-3,3	-	-
A9	GBE0_MDI1-	Ethernet Receive Data -	I/O - DP	-	-
A10	GBE0_MDI1+	Ethernet Receive Data +	I/O - DP	-	-
A11	GND	Ground	PWR	-	-
A12	GBE0_MDI0-	Ethernet Receive Data -	I/O - DP	-	-
A13	GBE0_MDI0+	Ethernet Receive Data +	I/O - DP	-	-
A14	GBE0_CTREF	ETHCTREF	O-1,8	-	-
A15	SUS_S3#	PM_SLP_S#3	O-3,3	-	-
A16	SATA0_TX+	SATA0_TX+ | SATA 0 Transmit Data +	O - DP	-	-
A17	SATA0_TX-	SATA0_TX- | SATA 0 Transmit Data -	O - DP	-	-
A18	SUS_S4#	PM_SLP_S#4	O-3,3	-	-
A19	SATA0_RX+	SATA0_RX+ | SATA 0 Receive Data +	I - DP	-	-
A20	SATA0_RX-	SATA0_RX - | SATA 0 Receive Data -	I - DP	-	-
A21	GND	Ground	PWR	-	-
A22	SATA2_TX+	SATA2_TX+ | SATA 2 Transmit Data +	NC	-	-
A23	SATA2_TX-	SATA2_TX- | SATA 2 Transmit Data -	NC	-	-
A24	SUS_S5#	PM_SLP_S#5	O-3,3	-	-
A25	SATA2_RX+	SATA2_RX+ | SATA 2 Receive Data +	NC	-	-
A26	SATA2_RX-	SATA2_RX- | SATA 2 Receive Data -	NC	-	-
A27	BATLOW#	PM_BATLOW# | Battery Low	I-3,3	PU 8k2 3,3VSB	-
A28	ATA_ACT#	ATA_LED# | SATA LED	O-3,3	PU 10k 3,3V	int. PU 15k to 3.3V in ICH6
A29	AC_SYNC	AC_SYNC | AC'97 Sync	O-3,3	-	int. PD 20k in ICH6
A30	AC_RST#	AC_RST# | AC'97 Reset	O-3,3	-	int. PD 20k in ICH6
A31	GND	Ground	PWR	-	
A32	AC_BITCLK	AC_BITCLK | AC'97 Clock	O-3,3	-	int. PD 20k in ICH6
A33	AC_SDOUT	AC_SDATAOUT | AC'97 Data	O-3,3	-	int. PD 20k in ICH6
A34	BIOS_DISABLE#	BIOS_DISABLE#	I-3,3	-	-
A35	THRMTRIP#	PM_THRMTRIP#_CON	IO-3,3		-
A36	USB6-	USB_PN6 | USB Data – Port6	I/O - DP	-	int. PD 15k in ICH6
A37	USB6+	USB_PP6 | USB Data + Port6	I/O - DP	-	int. PD 15k in ICH6
A38	USB_6_7_OC#	USB_OC#_6_7 | USB OverCurrent Port 6/7	I-3,3	PU 10k 3,3VSB	-
A39	USB4-	USB_PN4 | USB Data - Port4	I/O - DP	-	int. PD 15k in ICH6
A40	USB4+	USB_PP4 | USB Data + Port4	I/O - DP	-	int. PD 15k in ICH6
A41	GND	Ground	PWR	-	-
A42	USB2-	USB_PN2 | USB Data - Port2	I/O - DP	-	int. PD 15k in ICH6
A43	USB2+	USB_PP2 | USB Data + Port2	I/O - DP	-	int. PD 15k in ICH6
A44	USB_2_3_OC#	USB_OC#_2_3 | USB OverCurrent Port 2/3	I-3,3	PU 10k 3,3VSB	
A45	USB0-	USB_PN0 | USB Data - Port0	I/O - DP	-	int. PD 15k in ICH6
A46	USB0+	USB_PP0 | USB Data + Port0	I/O - DP	-	int. PD 15k in ICH6
A47	VCC_RTC	V_BAT	PWR	-	-
A48	EXCD0_PERST#	Express Card Support [0]|card reset	O-3,3	PU 10k 3,3VSB	-
A49	EXCD0_CPPE#	Express Card Support [0]| capable c. request	I-3,3	PU 8k2 3,3V	-
A50	LPC_SERIRQ	INT_SERIRQ | Serial Interrupt Request	IO-3,3	PU 8k2 3,3V	-
A51	GND	Ground	PWR	-	-
A52	PCIE5_TX+	BOM option (LAN on PCIe 5)	NC	-	-
A53	PCIE5_TX-	BOM option (LAN on PCIe 5)	NC	-	-
A54	GPI0	General Purpose Input 0	I-3,3	PU 8k2 3,3V	-
A55	PCIE4_TX+	PCI Express 4 Transmit +	NC	-	-

Signal Descriptions (cont'd)

Row A

Pin	Signal	Description	Type	PU/PD	Comment
A56	PCIE4_TX-	PCI Express 4 Transmit -	NC	-	-
A57	GND	Ground	PWR	-	-
A58	PCIE3_TX+	PCI Express 3 Transmit +	NC	-	Opt. for PCIE3_TX+
A59	PCIE3_TX-	PCI Express 3 Transmit -	NC	-	Opt. for PCIE3_TX-
A60	GND	Ground	PWR	-	-
A61	PCIE2_TX+	PCI Express 2 Transmit +	O - DP	-	-
A62	PCIE2_TX-	PCI Express 2 Transmit -	O - DP	-	-
A63	GPI1	General Purpose Input 1	PWR	PU 8k2 3,3V	-
A64	PCIE1_TX+	PCI Express 1 Transmit +	O - DP	-	-
A65	PCIE1_TX-	PCI Express 1 Transmit -	O - DP	-	-
A66	GND	Ground	PWR	-	-
A67	GPI2	General Purpose Input 2	I-3,3	PU 8k2 3,3V	-
A68	PCIE0_TX+	PCI Express 0 +	O - DP	-	-
A69	PCIE0_TX-	PCI Express 0 -	O - DP	-	-
A70	GND	Ground	PWR	-	-
A71	LVDS_A0+	LVDS_AP0 | LVDS Channel A	O - DP	-	-
A72	LVDS_A0-	LVDS_AN0 | LVDS Channel A	O - DP	-	-
A73	LVDS_A1+	LVDS_AP1 | LVDS Channel A	O - DP	-	-
A74	LVDS_A1-	LVDS_AN1 | LVDS Channel A	O - DP	-	-
A75	LVDS_A2+	LVDS_AP2 | LVDS Channel A	O - DP	-	-
A76	LVDS_A2-	LVDS_AN2 | LVDS Channel A	O - DP	-	-
A77	LVDS_VDD_EN	LVDS_VDDEN | LVDS Panel Power	O-2,5	PU 2k2 3,3V	-
A78	LVDS_A3+	LVDS_AP3 | LVDS Channel A	NC	-	-
A79	LVDS_A3-	LVDS_AN3 | LVDS Channel A	NC	-	-
A80	GND	Ground	PWR	-	-
A81	LVDS_A_CK+	LVDS_CLKAP | LVDS Channel A	O - DP	-	-
A82	LVDS_A_CK-	LVDS_CLKAN | LVDS Channel A	O - DP	-	-
A83	LVDS_I2C_CK	LVDS_DDCPCLK | JILI I2C Clock	IO-3,3	PU 2k2 3,3V	-
A84	LVDS_I2C_DAT	LVDS_DDCPDATA | JILI I2C Data	IO-3,3	PU 2k2 3,3V	-
A85	GPI3	General Purpose Input 3	I-3,3	PU 8k2 3,3V	-
A86	KBD_RST#	H_RCIN# | Keyboard Reset	I-3,3	PU 10k 3,3V	-
A87	KBD_A20GATE	H_A20GATE	I-3,3	PU 10k 3,3V	-
A88	PCIE_CK_REF+	CLK_PCIE_REF P	O - DP	-	-
A89	PCIE_CK_REF-	CLK_PCIE_REF N	O - DP	-	-
A90	GND	Ground	PWR	-	-
A91	RSVD		NC	-	-
A92	RSVD		NC	-	-
A93	GPO0	General Purpose Output 0	O-3,3		-
A94	RSVD		NC	-	-
A95	RSVD		NC	-	-
A96	GND	Ground	PWR	-	-
A97	VCC_12V	Power 12V	PWR	-	-
A98	VCC_12V	Power 12V	PWR	-	-
A99	VCC_12V	Power 12V	PWR	-	-
A100	GND	Ground	PWR	-	-
A101	VCC_12V	Power 12V	PWR	-	-
A102	VCC_12V	Power 12V	PWR	-	-
A103	VCC_12V	Power 12V	PWR	-	-
A104	VCC_12V	Power 12V	PWR	-	-
A105	VCC_12V	Power 12V	PWR	-	-
A106	VCC_12V	Power 12V	PWR	-	-
A107	VCC_12V	Power 12V	PWR	-	-
A108	VCC_12V	Power 12V	PWR	-	-
A109	VCC_12V	Power 12V	PWR	-	-
A110	GND	Ground	PWR	-	-

Signal Descriptions (cont'd)

Row B

Pin	Signal	Description	Type	PU/PD	Comment
B1	GND	Ground	PWR	-	-
B2	GBE0_ACT#	LAN_ACTLED# | Ethernet Activity LED	O-3,3	PU 150 3,3V	-
B3	LPC_FRAME#	LPC_FRAME# | LPC Frame Indicator	O-3,3	-	-
B4	LPC_AD0	LPC_AD0 | LPC Adress & DATA Bus	IO-3,3	-	int. PU 20k in ICH6
B5	LPC_AD1	LPC_AD1 | LPC Adress & DATA Bus	IO-3,3	-	int. PU 20k in ICH6
B6	LPC_AD2	LPC_AD2 | LPC Adress & DATA Bus	IO-3,3	-	int. PU 20k in ICH6
B7	LPC_AD3	LPC_AD3 | LPC Adress & DATA Bus	IO-3,3	-	int. PU 20k in ICH6
B8	LPC_DRQ0#	SIO_DRQ#0 | LPC Serial DMA Request 0	I-3,3	-	int. PU 20k in ICH6
B9	LPC_DRQ1#	SIO_DRQ#1 | LPC Serial DMA Request 1	I-3,3	-	int. PU 20k in ICH6
B10	LPC_CLK	CLK_SIOEXTPCI	O-3,3	-	-
B11	GND	Ground	I-3,3	-	-
B12	PWRBTN#	Power Button	I-5	-	-
B13	SMB_CK	SMBUS Clock	O-3,3	PU 2k2 3,3V	-
B14	SMB_DAT	SMBUS Data	IO-3,3	PU 2k2 3,3V	-
B15	SMB_ALERT#	SMB_ALERT#	I-3,3	PU 8k2 3,3VSB	-
B16	SATA1_TX+	SATA1_TX+ | SATA 1 Transmit Data +	O - DP	-	-
B17	SATA1_TX-	SATA1_TX- | SATA 1 Transmit Data -	O - DP	-	-
B18	SUS_STAT#	PM_SUS_STAT#	O-3,3	-	-
B19	SATA1_RX+	SATA1_RX+ | SATA 1 Receive Data +	I - DP	-	-
B20	SATA1_RX-	SATA1_RX - | SATA 1 Receive Data -	I - DP	-	-
B21	GND	Ground	PWR	-	-
B22	SATA3_TX+	SATA3_TX+ | SATA 3 Transmit Data +	NC	-	-
B23	SATA3_TX-	SATA3_TX- | SATA 3 Transmit Data -	NC	-	-
B24	PWR_OK	Power OK	I,5	-	-
B25	SATA3_RX+	SATA3_RX+ | SATA 3 Receive Data +	NC	-	-
B26	SATA3_RX-	SATA3_RX - | SATA 3 Receive Data -	NC	-	-
B27	WDT	Watch Dog Timer	O-3,3	-	-
B28	AC_SDIN2	AC_SDATAIN2	I-3,3	-	int. PD 20k in ICH6
B29	AC_SDIN1	AC_SDATAIN1	I-3,3	-	int. PD 20k in ICH6
B30	AC_SDIN0	AC_SDATAIN0	I-3,3	-	int. PD 20k in ICH6
B31	GND	Ground	PWR	-	
B32	SPKR	AC_SPKR	O-3,3	-	int. PD 20k in ICH6
B33	I2C_CK	I2CLK	NC		Connect to SMB_CK if req'd
B34	I2C_DAT	I2DAT	NC		Connect to SMB_DAT if req'd
B35	THRM#	PM THRM# CON | Over Temperature	I-3,3	PU 8k2 3,3V	-
B36	USB7-	USB_PN7 | USB Data – Port7	I/O - DP	-	int. PD 15k in ICH6
B37	USB7+	USB_PP7 | USB Data + Port7	I/O - DP	-	int. PD 15k in ICH6
B38	USB_4_5_OC#	USB_OC#_4_5 | USB OverCurrent Port	I-3,3	PU 10k 3,3VSB	
B39	USB5-	USB_PN5 | USB Data- Port5	I/O - DP	-	int. PD 15k in ICH6
B40	USB5+	USB_PP5 | USB Data+ Port5	I/O - DP	-	int. PD 15k in ICH6
B41	GND	Ground	I-3,3	-	-
B42	USB3-	USB_PN3 | USB Data- Port3	I/O - DP	-	int. PD 15k in ICH6
B43	USB3+	USB_PP3 | USB Data+ Port3	I/O - DP	-	int. PD 15k in ICH6
B44	USB_0_1_OC#	USB_OC#_0_1 | USB OverCurrent Port	I-3,3	PU 10k 3,3VSB	-
B45	USB1-	USB_PN1 | USB Data- Port1	I/O - DP	-	int. PD 15k in ICH6
B46	USB1+	USB_PP1 | USB Data+ Port1	I/O - DP	-	int. PD 15k in ICH6
B47	EXCD1_PERST#	Express Card Support [1] | card reset	O-3,3	PU 10k 3,3VSB	-
B48	EXCD1_CPPE#	Express Card Support [1] | capable c.	I-3,3	PU 10k 3,3VSB	-
B49	SYS_RESET#	ETX_SYS_RESET# | Reset Input	I-3,3	PU 4k7 3,3VSB	-
B50	CB_RESET#	PCI_RST# | PCI Bus Reset	O-3,3	-	-
B51	GND	Ground	PWR	-	-
B52	PCIE5_RX+	BOM option (LAN on PCIe 5)	NC	-	-
B53	PCIE5_RX-	BOM option (LAN on PCIe 5)	NC	-	-
B54	GPO1	General Purpose Output 1	O-3,3		-
B55	PCIE4_RX+	PCI Express 4 Recieve +	NC	-	-

Signal Descriptions (cont'd)

Row B

Pin	Signal	Description	Type	PU/PD	Comment
B56	PCIE4_RX-	PCI Express 4 Receive -	NC	-	-
B57	GPO2	General Purpose Output 2	O-3,3		-
B58	PCIE3_RX+	PCI Express 3 Receieve +	NC	-	Opt. for PCIE3_TX+
B59	PCIE3_RX-	PCI Express 3 Receive -	NC	-	Opt. for PCIE3_TX-
B60	GND	Ground	PWR	-	-
B61	PCIE2_RX+	PCI Express 2 Receive +	I - DP	-	-
B62	PCIE2_RX-	PCI Express 2 Receive -	I - DP	-	-
B63	GPO3	General Purpose Output 3	O-3,3		-
B64	PCIE1_RX+	PCI Express 1 Receive +	I - DP	-	-
B65	PCIE1_RX-	PCI Express 1 Receive -	I - DP	-	-
B66	WAKE0#	PCIE_WAKEI#	I-3,3	PU 1k 3,3VSB	-
B67	WAKE1#	WAKE1#	I-3,3	PU 1k 3,3VSB	-
B68	PCIE0_RX+	PCI Express 0 Receive +	I - DP	-	-
B69	PCIE0_RX-	PCI Express 0 Receive -	I - DP	-	-
B70	GND	Ground	PWR	-	-
B71	LVDS_B0+	LVDS_BP0 | LVDS Channel B Data0+	O - DP	-	-
B72	LVDS_B0-	LVDS_BN0 | LVDS Channel B Data0-	O - DP	-	-
B73	LVDS_B1+	LVDS_BP1 | LVDS Channel B Data1+	O - DP	-	-
B74	LVDS_B1-	LVDS_BN1 | LVDS Channel B Data1-	O - DP	-	-
B75	LVDS_B2+	LVDS_BP2 | LVDS Channel B Data2+	O - DP	-	-
B76	LVDS_B2-	LVDS_BN2 | LVDS Channel B Data2-	O - DP	-	-
B77	LVDS_B3+	LVDS_BP3 | LVDS Channel B Data3+	NC	-	-
B78	LVDS_B3-	LVDS_BN3 | LVDS Channel B Data3-	NC	-	-
B79	LVDS_BKLT_EN	Panel Backlight ON	O-3,3	PD 100k	-
B80	GND	Ground	PWR	-	-
B81	LVDS_B_CK+	LVDS_CLKBP | LVDS Channel B	O - DP	-	-
B82	LVDS_B_CK-	LVDS_CLKBM | LVDS Channel B	O - DP	-	-
B83	LVDS_BKLT_CTRL	Backlight Brightness	O-3,3	-	-
B84	VCC_5V_SBY	5V Standby	PWR	-	-
B85	VCC_5V_SBY	5V Standby	PWR	-	-
B86	VCC_5V_SBY	5V Standby	PWR	-	-
B87	VCC_5V_SBY	5V Standby	PWR	-	-
B88	RSVD	NC	NC	-	-
B89	VGA_RED	Analog Video RGB-RED	OA	PD 150	-
B90	GND	Ground	PWR	-	-
B91	VGA_GRN	Analog Video RGB-GREEN	OA	PD 150	-
B92	VGA_BLU	Analog Video RGB-BLUE	OA	PD 150	-
B93	VGA_HSYNC	Analog Video H-Sync	O-3,3	-	-
B94	VGA_VSYNC	Analog Video V-Sync	O-3,3	-	-
B95	VGA_I2C_CK	Display Data Channel	O-3,3	PU 2k2 3,3V	-
B96	VGA_I2C_DAT	Display Data	IO-3,3	PU 2k2 3,3V	-
B97	TV_DAC_A	Composite CVBS	OA	PD 150	-
B98	TV_DAC_B	TV Luminance Signal	OA	PD 150	-
B99	TV_DAC_C	TV Chrominance Signal	OA	PD 150	-
B100	GND	Ground	PWR	-	-
B101	VCC_12V	Power 12V	PWR	-	-
B102	VCC_12V	Power 12V	PWR	-	-
B103	VCC_12V	Power 12V	PWR	-	-
B104	VCC_12V	Power 12V	PWR	-	-
B105	VCC_12V	Power 12V	PWR	-	-
B106	VCC_12V	Power 12V	PWR	-	-
B107	VCC_12V	Power 12V	PWR	-	-
B108	VCC_12V	Power 12V	PWR	-	-
B109	VCC_12V	Power 12V	PWR	-	-
B110	GND	Ground	PWR	-	-

Signal Descriptions (cont'd)

Row C

Pin	Signal	Description	Type	PU/PD	Comment
C1	GND	Ground	PWR	-	-
C2	IDE_D7	IDE Data Bus	IO	-	int. PD 11.5k in ICH6
C3	IDE_D6	IDE Data Bus	IO	-	-
C4	IDE_D3	IDE Data Bus	IO	-	-
C5	IDE_D15	IDE Data Bus	IO	-	-
C6	IDE_D8	IDE Data Bus	IO	-	-
C7	IDE_D9	IDE Data Bus	IO	-	-
C8	IDE_D2	IDE Data Bus	IO	-	-
C9	IDE_D13	IDE Data Bus	IO	-	-
C10	IDE_D1	IDE Data Bus	IO	-	-
C11	GND	Ground	PWR	-	-
C12	IDE_D14	IDE Data Bus	IO	-	-
C13	IDE_IORDY	IDE I/O Ready	I-3,3	PU 4K7 3,3V	-
C14	IDE_IOR#	I/O read line to IDE device	O-3,3		-
C15	PCI_PME#	PCI Power Management Event	IO-3,3		int. PU 20k in ICH6
C16	PCI_GNT2#	PCI Bus Grant 2	O-3,3		int. PU 20k in ICH6
C17	PCI_REQ2#	PCI Bus Request 2	I-3,3	PU 8K2 3,3V	-
C18	PCI_GNT1#	PCI Bus Grant 1	O-3,3		int. PU 20k in ICH6
C19	PCI_REQ1#	PCI Bus Request 1	I-3,3	PU 8K2 3,3V	-
C20	PCI_GNT0#	PCI Bus Grant 0	O-3,3		int. PU 20k in ICH6
C21	GND	Ground	PWR		-
C22	PCI_REQ0#	PCI Bus Reqest 0	I-3,3	PU 8K2 3,3V	-
C23	PCI_RESET#	PCI Bus Reset	O-3,3	-	-
C24	PCI_AD0	PCI Adress & Data Bus line	IO-3,3	-	-
C25	PCI_AD2	PCI Adress & Data Bus line	IO-3,3	-	-
C26	PCI_AD4	PCI Adress & Data Bus line	IO-3,3	-	-
C27	PCI_AD6	PCI Adress & Data Bus line	IO-3,3	-	-
C28	PCI_AD8	PCI Adress & Data Bus line	IO-3,3	-	-
C29	PCI_AD10	PCI Adress & Data Bus line	IO-3,3	-	-
C30	PCI_AD12	PCI Adress & Data Bus line	IO-3,3	-	-
C31	GND	Ground	PWR	-	-
C32	PCI_AD14	PCI Adress & Data Bus line	IO-3,3	-	-
C33	PCI_C/BE1#	PCI Bus Command and Byte enables	IO-3,3	-	-
C34	PCI_PERR#	PCI Bus Grant Error	IO-3,3	PU 8K2 3,3V	-
C35	PCI_LOCK#	PCI Bus Lock	IO-3,3	PU 8K2 3,3V	-
C36	PCI_DEVSEL#	PCI Bus Device Select	IO-3,3	PU 8K2 3,3V	-
C37	PCI_IRDY#	PCI Bus Bus Initiator Ready	IO-3,3	PU 8K2 3,3V	-
C38	PCI_C/BE2#	PCI Bus Command and Byte enables	IO-3,3		-
C39	PCI_AD17	PCI Adress & Data Bus line	IO-3,3	-	-
C40	PCI_AD19	PCI Adress & Data Bus line	IO-3,3	-	-
C41	GND	Ground	PWR	-	-
C42	PCI_AD21	PCI Adress & Data Bus line	IO-3,3	-	-
C43	PCI_AD23	PCI Adress & Data Bus line	IO-3,3	-	-
C44	PCI_C/BE3#	PCI Bus Command and Byte enables	IO-3,3	-	-
C45	PCI_AD25	PCI Adress & Data Bus line	IO-3,3	-	-
C46	PCI_AD27	PCI Adress & Data Bus line	IO-3,3	-	-
C47	PCI_AD29	PCI Adress & Data Bus line	IO-3,3	-	-
C48	PCI_AD31	PCI Adress & Data Bus line	IO-3,3		-
C49	PCI_IRQA#	PCI Bus Interrupt Request A	I-3,3	PU 8K2 3,3V	-
C50	PCI_IRQB#	PCI Bus Interrupt Request B	I-3,3	PU 8K2 3,3V	-
C51	GND	Ground	PWR		-
C52	PEG_RX0+	PCI Express 0 Recieve +	I - DP		-
C53	PEG_RX0-	PCI Express 0 Recieve -	I - DP	-	-
C54	TYPE0#	Module type ID pin 0	NC	-	-
C55	PEG_RX1+	PCI Express 1 Recieve +	I - DP	-	-

Signal Descriptions (cont'd)

Row C

Pin	Signal	Description	Type	PU/PD	Comment
C56	PEG_RX1-	PCI Express 1 Recieve -	I - DP	-	-
C57	TYPE1#	Module type ID pin 1	NC	-	-
C58	PEG_RX2+	PCI Express 2 Recieve +	I - DP	-	-
C59	PEG_RX2-	PCI Express 2 Recieve -	I - DP	-	-
C60	GND	Ground	PWR	-	-
C61	PEG_RX3+	PCI Express 3 Recieve +	I - DP	-	-
C62	PEG_RX3-	PCI Express 3 Recieve -	I - DP	-	-
C63	RSVD	Rx from Board Controller	I-3.3	-	-
C64	RSVD	Tx from Board Controller	O-3.3	-	-
C65	PEG_RX4+	PCI Express 4 Recieve +	I - DP	-	-
C66	PEG_RX4-	PCI Express 4 Recieve -	I - DP	-	-
C67	RSVD	FAN_PWR_CTRL	I-5	-	-
C68	PEG_RX5+	PCI Express 5 Recieve +	I - DP	-	-
C69	PEG_RX5-	PCI Express 5 Recieve -	I - DP	-	-
C70	GND	Ground	PWR	-	-
C71	PEG_RX6+	PCI Express 6 Recieve +	I - DP	-	-
C72	PEG_RX6-	PCI Express 6 Recieve -	I - DP	-	-
C73	SDVO_DATA	SDVO_CTRLDATA	IO-2,5	PU 2K2 2,5V	-
C74	PEG_RX7+	PCI Express 7 Recieve +	I - DP	-	-
C75	PEG_RX7-	PCI Express 7 Recieve -	I - DP	-	-
C76	GND	Ground	PWR	-	-
C77	RSVD	FAN_TACH	O-5	-	-
C78	PEG_RX8+	PCI Express 8 Recieve +	I - DP	-	-
C79	PEG_RX8-	PCI Express 8 Recieve -	I - DP	-	-
C80	GND	Ground	PWR	-	-
C81	PEG_RX9+	PCI Express 9 Recieve +	I - DP	-	-
C82	PEG_RX9-	PCI Express 9 Recieve -	I - DP	-	-
C83	RSVD	Physical Presence	I-3,3		-
C84	GND	Ground	PWR	-	-
C85	PEG_RX10+	PCI Express 10 Recieve +	I - DP	-	-
C86	PEG_RX10-	PCI Express 10 Recieve -	I - DP	-	-
C87	GND	Ground	PWR	-	-
C88	PEG_RX11+	PCI Express 11 Recieve +	I - DP	-	-
C89	PEG_RX11-	PCI Express 11 Recieve –	I - DP	-	-
C90	GND	Ground	PWR	-	-
C91	PEG_RX12+	PCI Express 12 Recieve +	I - DP	-	-
C92	PEG_RX12-	PCI Express 12 Recieve -	I - DP	-	-
C93	GND	Ground	PWR	-	-
C94	PEG_RX13+	PCI Express 13 Recieve +	I - DP	-	-
C95	PEG_RX13-	PCI Express 13 Recieve -	I - DP	-	-
C96	GND	Ground	PWR	-	-
C97	RSVD	NC	NC	-	-
C98	PEG_RX14+	PCI Express 14 Recieve +	I - DP	-	-
C99	PEG_RX14-	PCI Express 14 Recieve -	I - DP	-	-
C100	GND	Ground	PWR	-	-
C101	PEG_RX15+	PCI Express 15 Recieve +	I - DP	-	-
C102	PEG_RX15-	PCI Express 15 Recieve -	I - DP	-	-
C103	GND	Ground	PWR	-	-
C104	VCC_12V	Power 12V	PWR	-	-
C105	VCC_12V	Power 12V	PWR	-	-
C106	VCC_12V	Power 12V	PWR	-	-
C107	VCC_12V	Power 12V	PWR	-	-
C108	VCC_12V	Power 12V	PWR	-	-
C109	VCC_12V	Power 12V	PWR	-	-
C110	GND	Ground	PWR	-	-

Signal Descriptions (cont'd)

Row D

Pin	Signal	Description	Type	PU/PD	Comment
D1	GND	Ground	PWR	-	-
D2	IDE_D5	IDE Data Bus	IO	-	-
D3	IDE_D10	IDE Data Bus	IO	-	-
D4	IDE_D11	IDE Data Bus	IO	-	-
D5	IDE_D12	IDE Data Bus	IO	-	-
D6	IDE_D4	IDE Data Bus	IO	-	-
D7	IDE_D0	IDE Data Bus	IO	-	-
D8	IDE_REQ#	IDE Device DMA Request.	IO	-	int. PD 11.5k in ICH6
D9	IDE_IOW#	IDE IO Write	O-3,3	-	-
D10	IDE_ACK#	IDE DMA Acknowledge	O-3,3	-	-
D11	GND	Ground	PWR	-	-
D12	IDE_IRQ	IDE Interrupt Request	I-3,3	PU 10K 3,3V	-
D13	IDE_A0	IDE Address Bus	O-3,3	-	-
D14	IDE_A1	IDE Address Bus	O-3,3	-	-
D15	IDE_A2	IDE Address Bus	O-3,3	-	-
D16	IDE_CS1#	IDE Chip Select for 1F0h to 1FFh range	O-3,3	-	-
D17	IDE_CS3#	IDE Chip Select for 3F0h to 3FFh range	O-3,3	-	-
D18	IDE_RESET#	IDE Reset Output to Device	O-3,3	-	-
D19	PCI_GNT3#	PCI Bus Grant 3	O-3,3	-	int. PU 20k in ICH6
D20	PCI_REQ3#	PCI Bus Reqest 3	I-3,3	PU 8K2 3,3V	-
D21	GND	Ground	PWR	-	-
D22	PCI_AD1	PCI Address & Data Bus line	IO-3,3	-	-
D23	PCI_AD3	PCI Address & Data Bus line	IO-3,3	-	-
D24	PCI_AD5	PCI Address & Data Bus line	IO-3,3	-	-
D25	PCI_AD7	PCI Address & Data Bus line	IO-3,3	-	-
D26	PCI_C/BE0#	PCI Bus Command and Byte enables 0	IO-3,3	-	-
D27	PCI_AD9	PCI Address & Data Bus line	IO-3,3	-	-
D28	PCI_AD11	PCI Address & Data Bus line	IO-3,3	-	-
D29	PCI_AD13	PCI Address & Data Bus line	IO-3,3	-	-
D30	PCI_AD15	PCI Address & Data Bus line	IO-3,3	-	-
D31	GND	Ground	PWR	-	-
D32	PCI_PAR	PCI Bus Parity	IO-3,3	-	-
D33	PCI_SERR#	PCI Bus System Error	IO-3,3	PU 8K2 3,3V	-
D34	PCI_STOP#	PCI Bus Stop	IO-3,3	PU 8K2 3,3V	-
D35	PCI_TRDY#	PCI Bus Target Ready	IO-3,3	PU 8K2 3,3V	-
D36	PCI_FRAME#	PCI Bus Cycle Frame	IO-3,3	PU 8K2 3,3V	-
D37	PCI_AD16	PCI Address & Data Bus line	IO-3,3	-	-
D38	PCI_AD18	PCI Address & Data Bus line	IO-3,3	-	-
D39	PCI_AD20	PCI Address & Data Bus line	IO-3,3	-	-
D40	PCI_AD22	PCI Address & Data Bus line	IO-3,3	-	-
D41	GND	Ground	PWR	-	-
D42	PCI_AD24	PCI Address & Data Bus line	IO-3,3	-	-
D43	PCI_AD26	PCI Address & Data Bus line	IO-3,3	-	-
D44	PCI_AD28	PCI Address & Data Bus line	IO-3,3	-	-
D45	PCI_AD30	PCI Address & Data Bus line	IO-3,3	-	-
D46	PCI_IRQC#	PCI Bus Interrupt Request C	I-3,3	PU 8K2 3,3V	-
D47	PCI_IRQD#	PCI Bus Interrupt Request D	I-3,3	PU 8K2 3,3V	-
D48	PCI_CLKRUN#	PCI Clock Run	I-3,3	PU 8K2 3,3V	-
D49	PCI_M66EN#	Control PCI Speed 33/66 Mhz	O-3,3	PD	Fixed to 33 Mhz
D50	PCI_CLK	PCI Clock	O-3,3	-	-
D51	GND	Ground	PWR	-	-
D52	PEG_TX0+	PCI Express 0 Transmit +	O - DP	-	-
D53	PEG_TX0-	PCI Express 0 Transmit -	O - DP	-	-
D54	PEG_LANE_RV#	PCI Express Lane Reversal	O-3,3	-	-
D55	PEG_TX1+	PCI Express 1 Transmit +	O - DP	-	-

Signal Descriptions (cont'd)

Row D

Pin	Signal	Description	Type	PU/PD	Comment
D56	PEG_TX1-	PCI Express 1 Transmit -	O - DP	-	-
D57	TYPE2#	Module type ID pin 2	NC	-	-
D58	PEG_TX2+	PCI Express 2 Transmit +	O - DP	-	-
D59	PEG_TX2-	PCI Express 2 Transmit -	O - DP	-	-
D60	GND	Ground	PWR	-	-
D61	PEG_TX3+	PCI Express 3 Transmit +	O - DP	-	-
D62	PEG_TX3-	PCI Express 3 Transmit -	O - DP	-	-
D63	RSVD		NC	-	-
D64	RSVD		NC	-	-
D65	PEG_TX4+	PCI Express 4 Transmit +	O - DP	-	-
D66	PEG_TX4-	PCI Express 4 Transmit -	O - DP	-	-
D67	GND	Ground	PWR	-	-
D68	PEG_TX5+	PCI Express 5 Transmit +	O - DP	-	-
D69	PEG_TX5-	PCI Express 5 Transmit -	O - DP	-	-
D70	GND	Ground	PWR	-	-
D71	PEG_TX6+	PCI Express 6 Transmit +	O - DP	-	-
D72	PEG_TX6-	PCI Express 6 Transmit -	O - DP	-	-
D73	SDVO_CLK	SDVO_CTRLCLK	IO-2,5	PU 2K2 2,5V	-
D74	PEG_TX7+	PCI Express 7 Transmit +	O - DP	-	-
D75	PEG_TX7-	PCI Express 7 Transmit -	O - DP	-	-
D76	GND	Ground	PWR	-	-
D77	IDE_CBLID#	IDE Cable Indicator Signal	I-3,3	PD 10k	-
D78	PEG_TX8+	PCI Express 8 Transmit +	O - DP	-	-
D79	PEG_TX8-	PCI Express 8 Transmit -	O - DP	-	-
D80	GND	Ground	PWR	-	-
D81	PEG_TX9+	PCI Express 9 Transmit +	O - DP	-	-
D82	PEG_TX9-	PCI Express 9 Transmit -	O - DP	-	-
D83	RSVD		NC	-	-
D84	GND	Ground	PWR	-	-
D85	PEG_TX10+	PCI Express 10 Transmit +	O - DP	-	-
D86	PEG_TX10-	PCI Express 10 Transmit -	O - DP	-	-
D87	GND	Ground	PWR	-	-
D88	PEG_TX11+	PCI Express 11 Transmit +	O - DP	-	-
D89	PEG_TX11-	PCI Express 11 Transmit -	O - DP	-	-
D90	GND	Ground	PWR	-	-
D91	PEG_TX12+	PCI Express 12 Transmit +	O - DP	-	-
D92	PEG_TX12-	PCI Express 12 Transmit -	O - DP	-	-
D93	GND	Ground	PWR	-	-
D94	PEG_TX13+	PCI Express 13 Transmit +	O - DP	-	-
D95	PEG_TX13-	PCI Express 13 Transmit -	O - DP	-	-
D96	GND	Ground	PWR	-	-
D97	PEG_ENABLE#	PCI Express Enable	I-3,3	PU 10K 3,3V	-
D98	PEG_TX14+	PCI Express 14 Transmit +	O - DP	-	-
D99	PEG_TX14-	PCI Express 14 Transmit -	O - DP	-	-
D100	GND	Ground	PWR	-	-
D101	PEG_TX15+	PCI Express 15 Transmit +	O - DP	-	-
D102	PEG_TX15-	PCI Express 15 Transmit -	O - DP	-	-
D103	GND	Ground	PWR	-	-
D104	VCC_12V	Power 12V	PWR	-	-
D105	VCC_12V	Power 12V	PWR	-	-
D106	VCC_12V	Power 12V	PWR	-	-
D107	VCC_12V	Power 12V	PWR	-	-
D108	VCC_12V	Power 12V	PWR	-	-
D109	VCC_12V	Power 12V	PWR	-	-
D110	GND	Ground	PWR	-	-

Signal Descriptions (cont'd)

Signal Type Legend	
IO-2,5	Bi-directional 2,5 V Input/Output
IO-3,3	Bi-directional 3,3 V Input/Output
IO-5	Bi-directional 5 V Input/Output
I-3,3	3,3 V Input
I-5	5 V Input
O-2,5	2,5 V Output
O-3,3	3,3 V Output
O-5	5 V Output
IO	Input/Output
OA	Analog Output
DP	Differential Pair Input/Output
O	Differential Pair Output
I	Differential Pair Input
PU	Pull-Up Resistor
PD	Pull-Down Resistor
PWR	Power or Ground
NC	Not Connected / Reserved

7 System Resources

7.1 Interrupt Assignment

PCI™ and LPC interrupts supported by the Intel® FW82801FBM South Bridge are as follows:

ISA IRQ	Edge/ Level	Polarity	Interrupt Source	Notes
NMI	Edge	High	SERR_L asserted	
IRQ0	Edge	High	Timer0	(1)
IRQ1	Edge	High	PCI PnP IRQ	(2)
IRQ2	Edge	High	Cascade Interrupt from Slave Interrupt Controller	
IRQ3	Edge	High	PCI PnP IRQ	(2)
IRQ4	Edge	High	PCI PnP IRQ	(2)
IRQ5	Edge	Low	PCI PnP IRQ	
IRQ6	Edge	High	PCI PnP IRQ	(2)
IRQ7	Edge	High	PCI PnP IRQ	(2)
IRQ8_L	Edge	Low	Real Time Clock	(2)
IRQ9	Edge	Low	PCI PnP IRQ	(2)
IRQ10	Level	Low	PCI PnP IRQ	
IRQ11	Level	Low	PCI PnP IRQ	(2)
IRQ12	Edge	High	PCI PnP IRQ	(2)
IRQ13	Edge	High	FERR_L asserted	
IRQ14	Edge	High	Primary IDE	(3)
IRQ15	Edge	High	PCIP~PIRQ	

NOTE:

[1]Internally generated by the FW82801FBM.

[2]Some of these interrupts may be claimed by any LPC based Super I/O residing on the carrier board.

[3]This interrupt is routed to the IRQ14 input of the FW82801DA.

7.2 PCI™ Bus Arbitration Assignment

PCI Bus Request	PCI Master(s)	IDSEL
Request 0	Routed to CD connector	*
Request 1	Routed to CD connector	*
Request 2	Routed to CD connector	*
Request 3	Routed to CD connector	*

NOTE: IDSEL routing depends on the design of the carrier board.

7.3 PCI™ Interrupt Routing

Device	Net PIRQ0_L	Net PIRQ1_L	Net PIRQ2_L	Net PIRQ3_L
CD connector	PIRQA#	PIRQB#	PIRQC#	PIRQD#

7.4 Memory Map

Address	Size	Description
00000000~0009FFFF	640K	DOS Application Area
000A0000~000BFFFF	128K	Video Buffer Area
000C0000~000DFFFF	128K	Expansion Area
000E0000~000EFFFF	64K	Extended System BIOS Area
000F0000~000FFFFF	64K	System BIOS Area
00100000~DRAM Top	---	System memory area
DRAM Top ~FFFRFFFF	---	Bus area
FFFEFFFF ~ FFFFFFFF	64K	Initialization area

7.5 Direct Memory Access Channels

DMA#	Available	Description
0	Yes	
1	Yes	Unavailable if Sound Blaster is enabled with default configuration
2	Yes	Unavailable if Floppy disk is used
3	Yes	Unavailable when LPT is in ECP mode
4	No	Used for Cascade
5	Yes	
6	Yes	
7	Yes	

7.6 I/O Address Map

Address	Size	Description
0000 - 001F	32 bytes	Master DMA controller
0020 - 002D	14 bytes	Master Interrupt Controller
0040 - 005F	32 bytes	Timer/Counter
0060 - 006F	32 bytes	Keyboard Controller / NMI Controller
60h	1 byte	KBC data
61h	1 byte	Misc function and Speaker control
64h	1 byte	KBC command / status
0070 - 0077	8 bytes	RTC/CMOS/NMI Controller
0078 - 007F	8 bytes	Available for system use
0080	1 byte	Reserved (Debug port)
0081 - 008F	16 bytes	DMA page registers
0090 - 0091	2 bytes	Available for system use
0092	1 byte	System Control
0093 - 009F	13 bytes	Available for system use
00A0 - 00BF	32 bytes	Slave Interrupt Controller
00C0 - 00DF	32 bytes	Slave DMA Controller
00E0 - 00FF	32 bytes	Available for system use
0100 - 0CF7		Available for system use
0CF8 -0CFB	4 bytes	PCI configuration address
0CFC - 0CFF	4 bytes	PCI configuration data
0D00 - FFFF		Available for system use

7.7 System Management Bus (I²C compatible)

Internally the SMB bus and I2C bus are one and the same. The ICH4 Southbridge supports SMBDAT and SMBCLK lines that are I2C compatible.

The X4 connector has pinouts for both the I2C and SMB bus. Both are connected to the same internal bus: the SMB bus. It is advisable to always connect external I2C devices to the I2C pins and SMB devices to the SMB pins to stay in line with other modules that might support two internal busses (separate I2C and SMB bus)

Address	Function	Device
A0h ~ A6h	Identification Info	SODIMM0 EEPROM
ACh	CMOS setting backup	EEPROM
AEh	Sound	AC'97 codec
D2h	Timing	Clock generator
9Ch	Watchdog Timer	F75111R
5Ah	Hardware Monitor	F75375

8 Phoenix Award™ BIOS

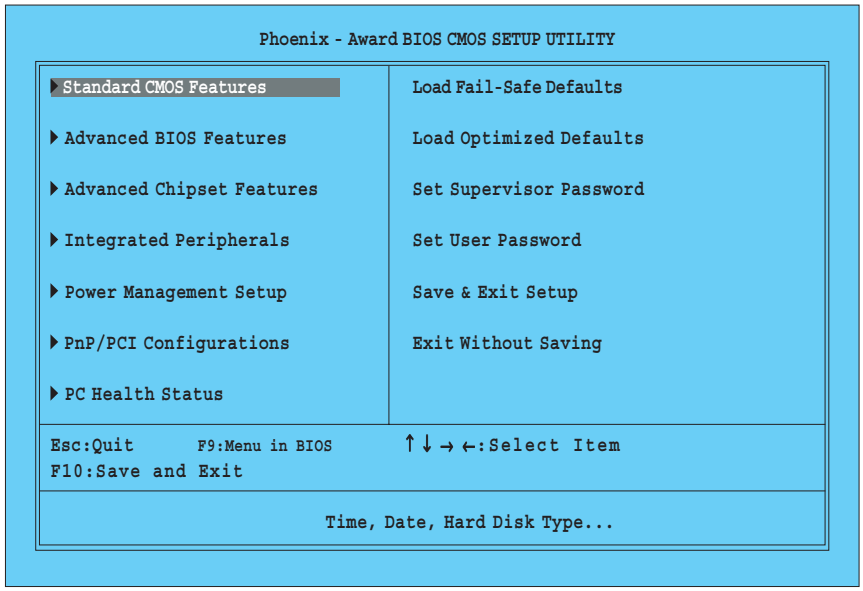
8.1 Description

The module has a Phoenix Award™ PCI/ISA BIOS ver 6.0 for the system configuration. The Award BIOS setup program is designed to provide maximum flexibility in configuring the system by offering various options which could be selected for end-user requirements. This chapter is written to assist you in the proper usage of these features.

To access the Phoenix AWARD™ PCI/ISA BIOS Setup program,

press <Del> key.

The Main Menu will then be displayed.



NOTE:

Although the BIOS supports and lists several Super I/O options and functions (Keyboard, Mouse, COM/Parallel ports and FDD), the Super I/O chip itself is located on the reference carrier (Express-BASE) and is an optional device.

The super I/O BIOS chip used on the reference carrier is the Winbond W83627HF. It is advisable when designing your own carrier board, if you need Super I/O to stick to this part, avoid needless BIOS modifications and accompanied verification testing.

8.2 Main Menu Setup Items

The main menu includes the following main setup categories. Recall that some systems may not include all entries.

Standard CMOS Features (see paragraph 9.3)

Use this menu for basic system configuration.

Advanced BIOS Features (see paragraph 9.4)

Use this menu to set the Advanced Features available on your system.

Advanced Chipset Features (see paragraph 9.5)

Change values in the chipset registers and optimize your system's performance.

Integrated Peripherals (see paragraph 9.6)

Use this menu to specify your settings for integrated peripherals.

Power Management Setup (see paragraph 9.7)

Use this menu to specify your settings for power management.

PnP / PCI Configuration (see paragraph 9.8)

This entry will only appear if your system supports PnP / PCI.

PC Health Status (see paragraph 9.9)

Use this menu to monitor CPU and system temperatures.

Frequency/Voltage Control

Use this menu to specify your settings for frequency/voltage control.

Load Fail-Safe Defaults

Load the BIOS default values for the minimal/stable performance for your system to operate.

Load Optimized Defaults

Load the BIOS default values that are factory settings for optimal system performance.

Supervisor/User Password

Use this menu to set User and Supervisor Passwords.

Save & Exit Setup

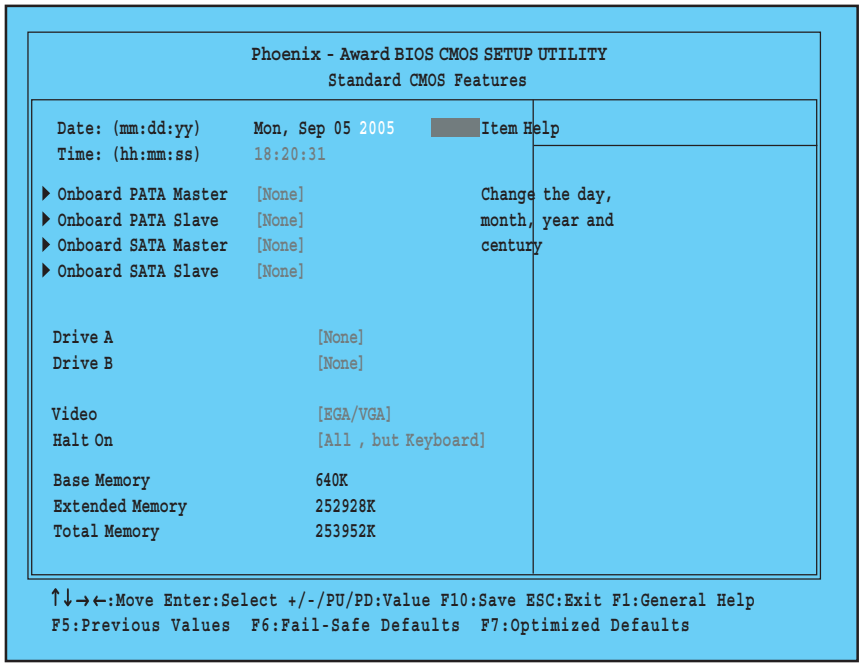
Save CMOS value changes to CMOS and exit setup.

Exit Without Saving

Abandon all CMOS value changes and exit setup.

8.3 Standard CMOS Features

The main menu includes the following main setup categories. Recall that some systems may not include all entries.



Date

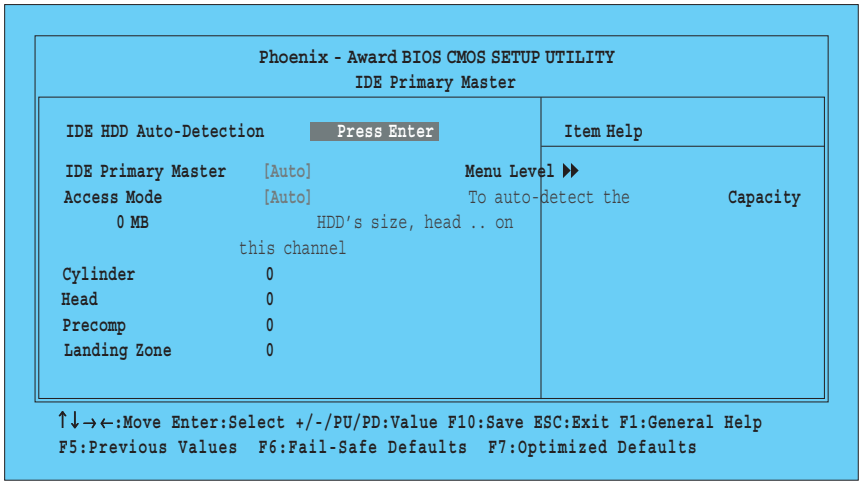
The BIOS determines the day of the week from other date information; this field is for information only.

Time

The time format is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Press the « or (key to move to the desired field Press the PgUp or PgDn key to increment the setting, or directly type the desired value into the field.

IDE Primary and Secondary Master/Slave Items

This selection brings up a configuration menu of the designated Drive (see next page)



IDE HDD Auto-detection	Press Enter	Press Enter to auto-detect the HDD on this channel. If detection is successful, it automatically fills the remaining fields on this menu.
IDE Primary Master	None/Auto/Manual	Selecting 'manual' allows the user to set the remaining fields on this screen. Selects the type of fixed disk. "User Type" will let you select the number of cylinders, heads, etc.

NOTE: PRECOMP=65535 means NONE.

Capacity	Auto Display disk size	Disk drive capacity (Approximated). Note that this size is usually slightly greater than the size of a formatted disk given by a disk checking program.
Access Mode	CHS/LBA/Large/Auto	Choose the access mode for this hard disk

The following options are selectable only if the 'IDE Primary Master' item is set to 'Manual'

Cylinder	Min = 0 Max = 65535	Set the number of cylinders for this hard disk.
Head	Min = 0 Max = 255	Set the number of read/write heads
Precomp	Min = 0 Max = 65535	

Setting a value of 65535 means no hard disk

Landing zone	Min = 0 Max = 65535	

Setting a value of 65535 means no hard disk

Sector	Min = 0 Max = 255	Number of sectors per track

Drive A, B

Select the correct specifications for the diskette drive(s) installed in the computer.

None:	No diskette drive installed
360K:	5.25 in5-1/4 inch PC-type standard drive
1.2M:	5.25 in5-1/4 inch AT-type high-density drive
720K:	3.5 in3-1/2 inch double-sided drive
1.44M:	3.5 in3-1/2 inch double-sided drive
2.88M:	3.5 in3-1/2 inch double-sided drive

Video

Select the type of primary video subsystem in your computer. The BIOS usually detects the correct video type automatically. The BIOS supports a secondary video subsystem, but this is not selected in Setup.

Halt On

During the Power On Self Test (POST), the computer stops if the BIOS detects a hardware error. The BIOS can be instructed to ignore certain errors during POST and continue the boot-up process. The options are as follows:

No errors:	POST does not stop for any errors.
All errors:	POST stops for any nonfatal error and will prompt the user to take any corrective measures.
All, But Keyboard:	POST does not stop for a keyboard error, but stops for all other errors
All, But Diskette:	POST does not stop for diskette errors, but stops for all other errors
All, But Disk/Key:	POST does not stop for keyboard/disk errors, but stops for all other errors

Base Memory

Displays the amount of base (or conventional) memory installed in the system. The value of the base memory is typically 512K for systems with 512K memory installed on the motherboard or 640K for systems with 640K or more memory installed on the motherboard.

Extended Memory

Displays the amount of extended memory detected during boot-up.

Total Memory

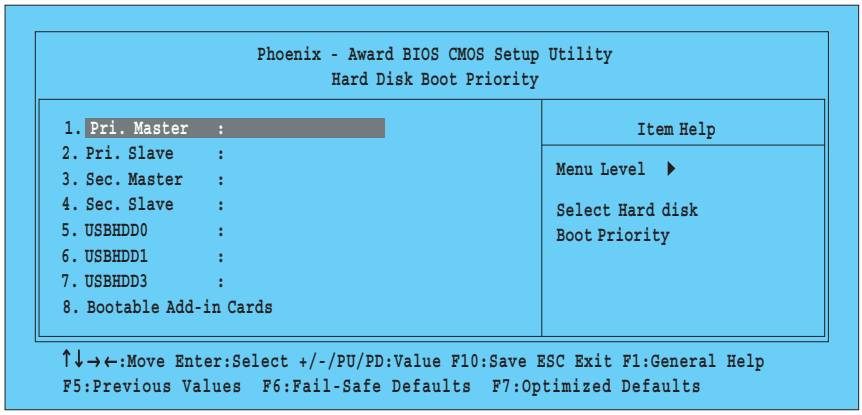
Displays the total memory available in the system.

8.4 Advanced BIOS Features

This section allows the user to configure the system for basic operation. The following features can be selected here: system default speed, boot-up sequence, keyboard operation, shadowing, security, and CPU Internal Cache/CPU External Cache.

Hard Disk Boot Priority

This field is used to select the boot sequence of the hard drives. Move the cursor to the “Hard Disk Boot Priority” field then press <Enter>. The following menu will appear:



Use the Up or Down arrow keys to select a device then press <+> to move it up or <-> to move it down the list.

CPU L1 & L2 Cache

These fields speed up the memory access. The default value is enabled. Enable the external cache for better performance.

CPU L3 Cache

These fields speed up the memory access. The default value is enabled. Enable the external cache for better performance.

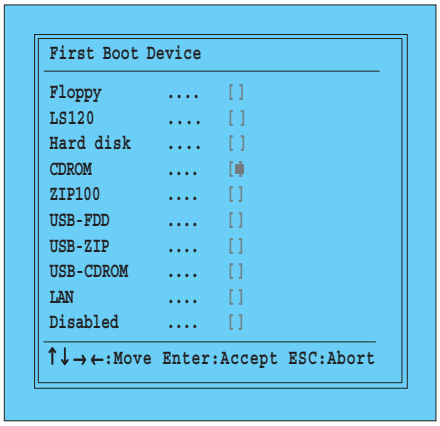
Quick Power On Self Test

This category speeds up the Power On Self Test (POST). If enabled, BIOS will shorten or skip some check items during POST. Options: Enabled: enables quick POST. Disabled: normal POST.

First/Second/Third Boot Device

Pressing <Enter> brings up the Boot Device Menu. The BIOS attempts to load the operating system from the selected device.

See menu for possible options



NOTE:

Any hard disk, either SATA, PATA or USB is first selected as “Hard disk” in this submenu and its boot order can later be assigned in the “Hard Disk Boot Priority” submenu.

Boot Other Device

When enabled, the BIOS will try to boot from the second or third option if booting from the first device fails. When disabled, the BIOS will not use alternative devices.

Swap Floppy Drive

When this field is enabled and the system is booting from the floppy drive, the system will boot from drive B instead of drive A. When this field is disabled and the system is booting from the floppy drive, the system will boot from drive A. You must have two floppy drives to use this function.

Boot Up Floppy Seek

When enabled, the BIOS will check whether the floppy disk drive installed has 40 or 80 tracks. When disabled, the BIOS will not search for the type of floppy disk drive by track number.

Boot Up NumLock Status

Select power on state for NumLock. Options: On/Off

Gate A20 Option

Select if the chipset or keyboard controller should control GateA20.
Normal: A pin in the keyboard controller controls GateA20
Fast: Lets chipset control GateA20

Typematic Rate Setting

Key strokes repeat at a rate determined by the keyboard controller. When enabled, the typematic rate and typematic delay can be selected. Options: Enabled/Disabled.

Typematic Rate (Chars/Sec)

Sets the number of times per second to repeat a key stroke when holding down the key. Options: 6, 8, 10, 12, 15, 20, 24, and 30.

Typematic Delay (Msec)

Sets the delay time after the key is held down before it begins to repeat the keystroke. Options: 250, 500, 750, and 1000.

Security Option

Select whether the password is required every time the system boots or only when you enter setup. Choices:

System: The system will not boot and access to Setup will be denied if an incorrect password is entered at the prompt.

Setup: The system will boot, but access to Setup will be denied if an incorrect password is not entered at the prompt.

To disable security, select PASSWORD SETTING in Main Menu. The user will then be prompted to enter the password. Do not type anything and press <Enter> to disable security. Once security is disabled, the system will boot and Setup can be entered freely.

APIC Mode

APIC mode (Advanced Programmable Interrupt Controller) is a BIOS setting that increases the number of IRQ (Interrupt Request) lines available to the processor. APIC is responsible for multiprocessor support, more IRQs, and faster interrupt handling. APIC is only supported by newer operating systems like Linux, Microsoft Windows NT, Windows 2000 and Windows XP. Older operating systems like DOS or Windows 95/98 do not support this feature.

Enable it if you use an OS that can support it, otherwise disable it.

MPS Version Control for OS

This option is only valid for multiprocessor motherboards as it specifies the version of the Multiprocessor Specification (MPS) that the motherboard will use. The MPS is a specification by which PC manufacturers design and build Intel architecture systems with two or more processors.

Console Redirection

Award's Preboot Agent provides you with console redirection to let you control a remote PC or embedded system via modem or direct serial connection at boot time.
Choice: Enable, Disable.

Baud Rate

Select baud rate: 9600, 19200, 38400, 57600 and 115200.

Agent Connect via

Fixed to NULL (Null modem cable), no selection possible.

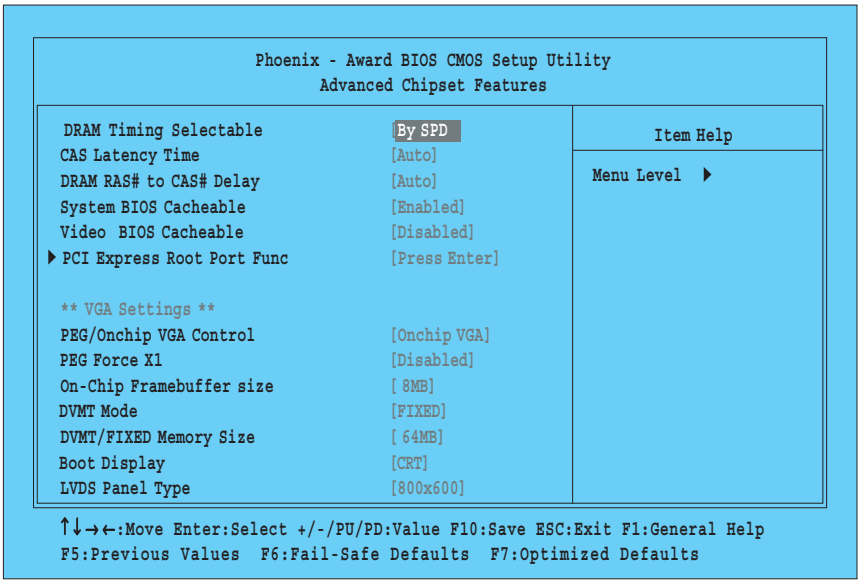
Agent after boot

Enable this option to keep the Agent running after OS boot.

Summary Screen Show

Suppress the summary screen. Choice:Enable, Disable

8.5 Advanced Chipset Features



DRAM Timing Selectable

This field is used to select the timing of the DRAM.

By SPD:
The EEPROM on a DIMM has SPD (Serial Presence Detect) data structure that stores information about the module such as the memory type, memory size, memory speed, etc. When this option is selected, the system will run according to the information in the EEPROM. This option is the default setting because it provides the most stable condition for the system. The “CAS Latency Time” to “System Memory Frequency” fields will show the default settings by SPD.

Manual:
For better performance for your system other than the one “by SPD”, select “Manual” then select the best option in the “CAS Latency Time” to “System Memory Frequency” fields.

CAS Latency Time

This feature allows you to manually set the amount of time the memory controller is allowed to write to the memory module. The shorter the Write CAS Latency, the faster the writes occur.

For DDR2 SDRAM, it is recommended to set the Write CAS Latency to 2 Bus Clocks. Increase it only if faced with stability issues.

DRAM RAS# to CAS# delay

When the DRAM Timing Control is set to [Manual], this field is adjustable. When DRAM is refreshed, both rows and columns are addressed separately. This setup item allows you to determine the timing of the transition from RAS (row address strobe) to CAS (column address strobe). The fewer the clock cycles, the faster the DRAM performance. Using value too low for your memory module can result in an unstable system. If your system becomes unstable after you reduce the RAS-to-CAS delay, increase the delay or reset it to the rated delay.

System BIOS Cacheable

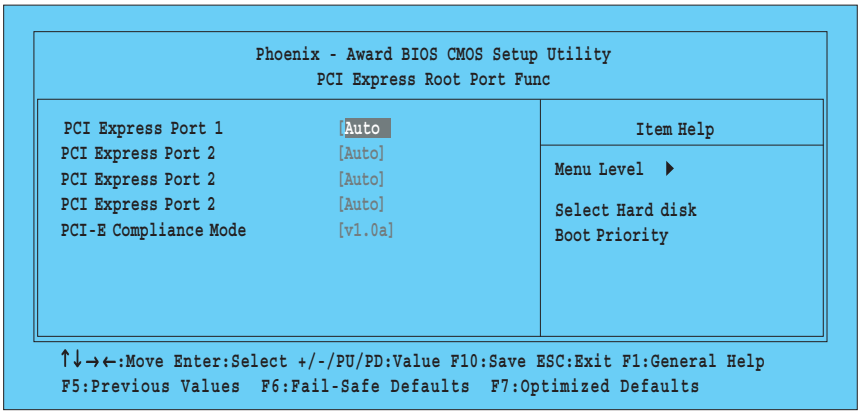
Selecting Enabled allows caching of the system BIOS ROM at F0000h-FFFFFh, resulting in better system performance. However, if any program writes to this memory area, a system error may occur.

Video RAM Cacheable

Select Enabled allows caching of the video RAM, resulting in better system performance. However, if any program writes to this memory area, a system error may result.
Options: Enabled, Disabled, Fast R-W Turn Around.

PCI Express Root Port Func

This field is used to select the boot sequence of the hard drives. Move the cursor to the “PCI Express Root Port Func” field then press <Enter>. The following menu appears:



PCI Express Port 1,2,3,4

This option is used to enable or disable PCI Express port 1. The available setting values are: Auto, Enabled, Disabled. Note that PCI Express Port 4 is occupied by the onboard LAN controller.

PCI-E Compliance Mode

This BIOS option determines compatibility between PCI-Express specification v1.0 and PCI-Express specification v1.0a.

PEG/Ochip VGA Control

This field is found in motherboards that have a built-in graphics processor as well as a PCI Express port. It allows you to select whether to use the onboard graphics processor or the PCI Express card.

Onchip VGA: The motherboard boots up using the onboard graphics processor, even when a PCI Express graphics card is installed.

PEG Port: The motherboard boots up using the PCI Express graphics card, if one is installed. Otherwise, it defaults to the onboard graphics processor.

Auto: The BIOS checks to see if a PCI Express graphics card is installed. If it detects that a PCI Express graphics card is present, the motherboard boots up using that card. Otherwise, it defaults to the onboard graphics processor.

PEG Force X1

When using a PCI Express x16 graphic card, disable this function. When using a 1x board on this interface enable this function.

Onchip Framebuffer size

This determines the amount of system memory that is pre-allocated to the graphics processor during the boot process or while running MS-DOS or other legacy operating systems. Once allocated here, it can only be used as graphics memory even when later the DVMT option is set. Additional system memory (DVMT) is only allocated after the graphics drivers are loaded.

Do not assign more memory than absolutely required by the current VGA mode.
For example, a resolution of 1600x1200 and color depth of 32-bit,
amounts to 1600 x 1200 x 32-bits = 61,440,000 bits or 7.68MB.
Set to 8MB in this example.

DVMT Mode

Dynamic Video Memory Technology (DVMT) allows dynamic allocation of system memory resources for the integrated VGA controller depending on system demand at the time.

Fixed: when set to fixed, the graphics driver will reserve a fixed portion of the system memory as graphics memory.

DVMT: When set to DVMT, the graphics chip will dynamically allocate system memory as graphics memory, according to system and graphics requirements.

Both: when set to Both, a minimum amount of memory is allocated and the system is allowed to dynamically allocated more memory resources when necessary.

DVMT/FIXED Memory Size

Only two choices: either 64 MB or 128 MB memory can be assigned as either absolute assignment (FIXED mode) or maximum assignment in DVMT mode.

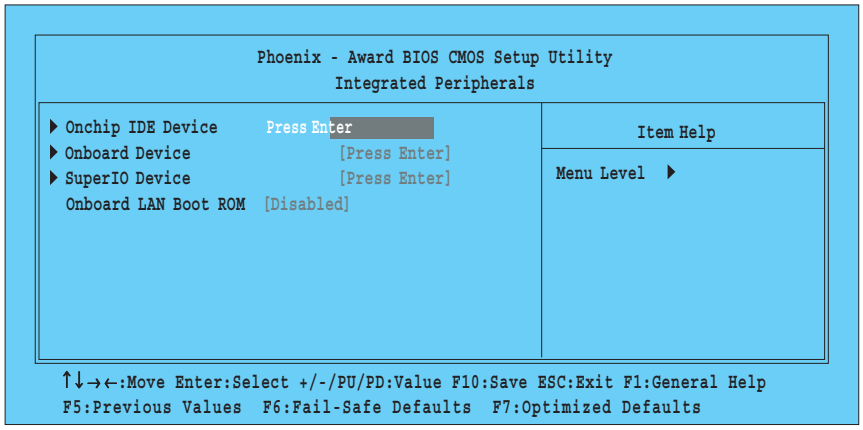
Boot Display

This item allows the user to configure the type of external display used.
Options: CRT, LVDS (displays cannot be used concurrently)

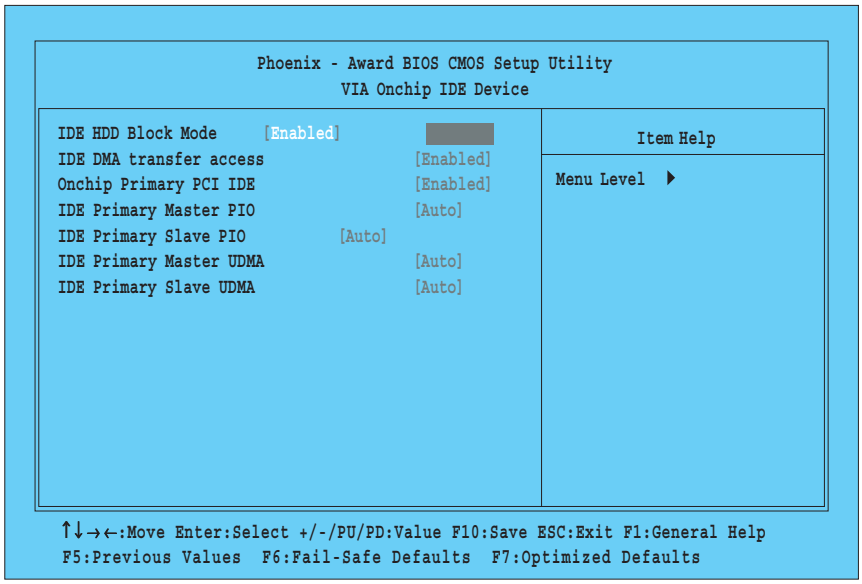
LVDS Panel Type

When LVDS is selected in “Display Feature”, the flat panel resolution can be selected.
Options: 640x480, 800x600, 1024x768, and 1280x1024.

8.6 Integrated Peripherals



Onchip IDE Device (submenu)



IDE HDD Block Mode

This feature enhances disk performance by allowing multi-sector data transfers and eliminates the interrupt handling time for each sector.

IDE DMA transfer access

This BIOS feature allows you to enable or disable DMA (Direct Memory Access) support for all IDE devices.

Onchip Primary PCI IDE

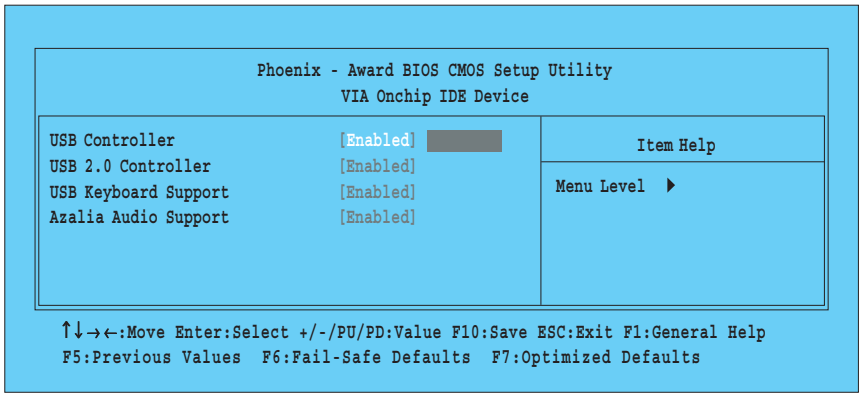
The chipset contains a PCI IDE interface with support for two IDE channels. Select Enabled to activate the primary/secondary IDE interface. Select Disabled to deactivate these interfaces.

Primary Master/Slave PIO

The four IDE PIO (Programmed Input/Output) fields allows the user to set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device. Options: Auto, Mode 0, Mode 1, Mode 2, Mode 3, Mode 4.

IDE Primary Master/Slave UDMA

Ultra DMA implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver. If your hard drive and your system software both support Ultra DMA, select Auto to enable BIOS support.



Onchip PCI Device (submenu)

USB Controller

This should be enabled to use the internal USB function. Enabling only results in USB 1.1 functionality. To also obtain USB 2.0 functionality the “USB 2.0 Controller” setting will also have to be enabled. Options: Enabled, Disabled.

USB 2.0 Controller

This enables USB 2.0 support on the USB controller. Options: Enabled, Disabled.

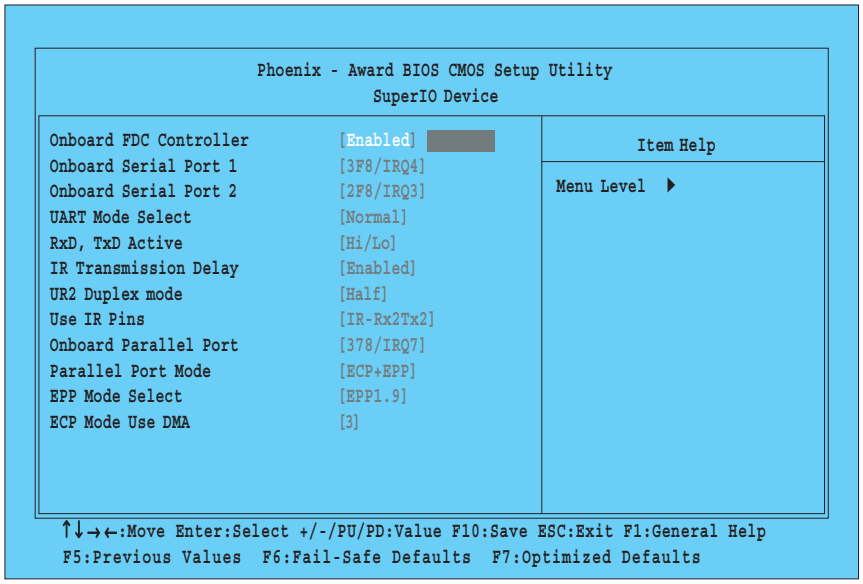
USB Keyboard Support

Select Enabled if your system contains a Universal Serial Bus (USB) controller and you have a USB keyboard. Options: Enabled, Disabled.

Azalia Audio Support

Auto Select this option when using the onboard audio CODEC. Option to disable this option when using a PCI sound card.

Super I/O Device



Onboard FDC Controller

Enable or disable Floppy Drive support

Onboard Serial Port 1/2

Select address and interrupt for the serial ports.

UART Mode Select

The serial port 2 on your system offers a variety of infrared modes. There are two different IR (Infra-Red) modes - IrDA and ASK IR. Select the IR mode that is supported by your external IR device. Choosing the wrong IR mode will prevent your computer from communicating with the external IR device.

RxD, TxD Active

This BIOS feature allows you to set the infrared reception (RxD) and transmission (TxD) polarity.

IR Transmission Delay

When UART Mode is selected in IrDA or ASKIR mode, it allows the user to enable / disable IR Transmission Delay.

UR2 Duplex Mode

This options controls the operating mode between receiving and transmitting of IrDA or ASKIR. The operating mode will be synchronous bidirectional transmission and reception when Full mode is selected. The operating mode will be asynchronous bidirectional transmission and reception when Half mode is selected. Options: Half; Full

LPT1 Setting / FDD

This setting allows the user to assign resources to LPT1 or disable the function and allow using an FDD drive. Since share LPT1 and FDD share the same pins on the X3 connector, only one of them can be used at a time.

EPP Mode Select

There are two versions of the EPP transfer protocol - EPP 1.7 and EPP 1.9. This BIOS feature allows the user to select the version of EPP that the parallel port should use.

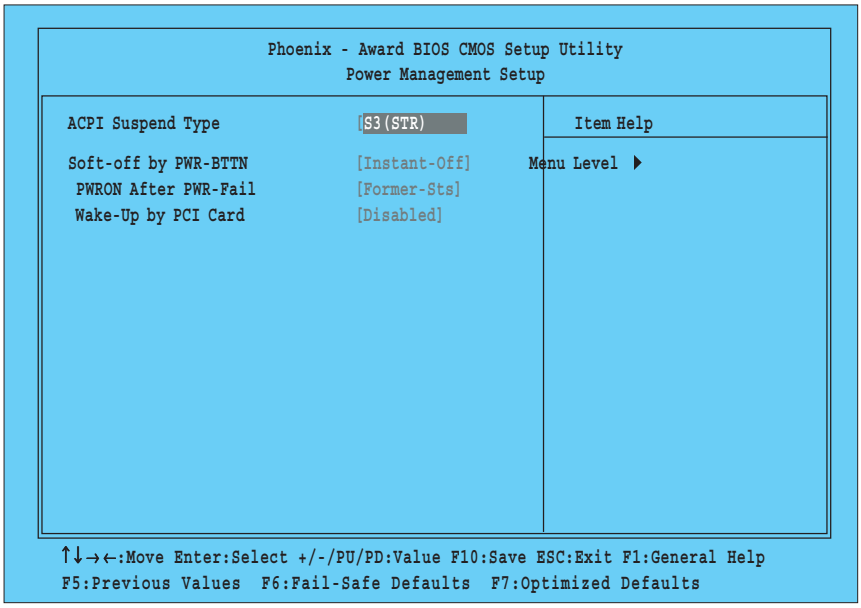
Generally, EPP 1.9 is the preferred setting because it supports the newer EPP 1.9 devices and most EPP 1.7 devices, while offering other advantages such as support for longer cables. However, because certain EPP 1.7 devices cannot work properly with an EPP 1.9 port, this BIOS feature was implemented to allow the user to set the EPP mode to EPP 1.7 when this situation occurs.

Therefore, it is recommended that you sets this BIOS feature to EPP 1.9. However, if there are problems connecting to the parallel port devices, switch to EPP 1.7.

ECP Mode Use DMA

This BIOS feature determines which DMA channel the parallel port should use when it is in ECP mode. The ECP mode uses the DMA protocol to achieve data transfer rates of up to 2.5 Mbits/s and provides symmetric bidirectional communications. For all this, it requires the use of a DMA channel.

8.7 Power Management Setup



ACPI Suspend Type

S1/Power On Suspend (POS): A low power state in which no system context (CPU or chipset) is lost and hardware maintains all system contexts.

S3/Suspend to RAM (STR): A power-down state in which power is supplied only to essential components such as main memory and wake-capable devices. The system context is saved to main memory, and context is restored from the memory when a "wake" event occurs. (Default)

S1&S3: Depends on Operating System capabilities/software support to select both.

Soft-Off By PWR-BTTN

The field defines the power-off mode when using an ATX power supply. The Instant-Off mode means the system will be powered off immediately when pressing the power button. In the Delay 4 Sec mode, the system powers off when the power button is held down for more than four seconds or places the system in a very low-power-usage state, with only enough circuitry receiving power to detect power button activity or resume by ring activity when the power button is held down for less than four seconds. The default is 'Instant-Off'.

PWRON After PWR-Fail

On: After a power failure, the system automatically reboots when power is restored.

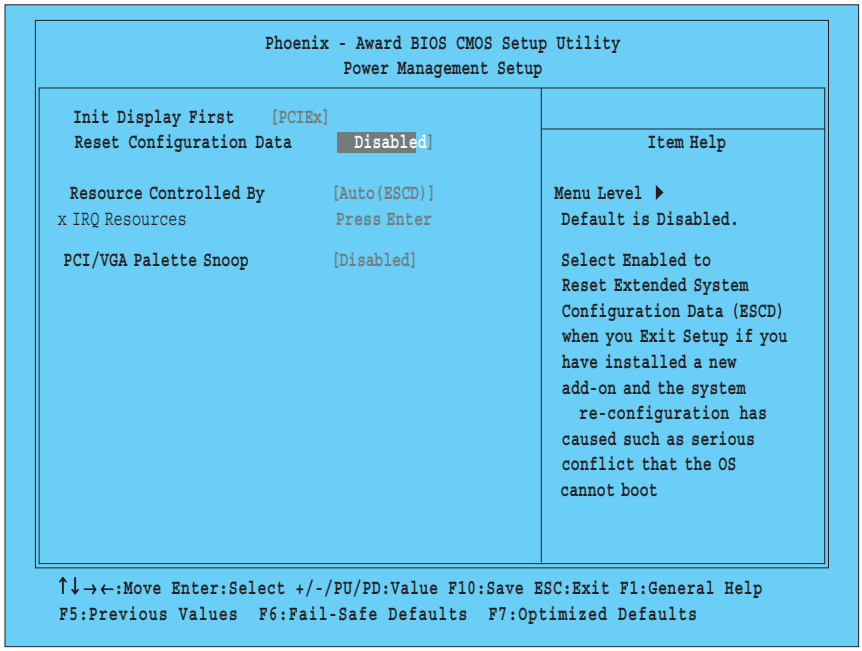
Off: After a power failure, the system will not reboot when power is restored. The system needs to be turned on again manually.

Former-Sts: After a power failure, the system automatically reboots when power is restored ONLY if the PC was turned on when the power failed.
After a power failure, the system will NOT automatically reboots when power is restored If the PC was shutdown before the power failed.

Wake-Up by PCI Card

This field should be set to Enabled only if your PCI card (e.g. LAN or modem card) uses the PCI PME (Power Management Event) signal to remotely wake up the system. Accessing the PCI card will cause the system to wake up. Refer to the card's documentation for more information. If set to Disabled, the system will not wake up if the PCI card accessed.

8.8 PnP/PCI Configurations



This section describes the configuring of the PCI bus system. PCI, or Personal Computer Interconnect, is a system which allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own special components.

Init Display First

This BIOS feature allows you to select whether to boot the system using the onboard integrated graphics, the external PEG x16 card or a possible PCI graphics card.

Reset Configuration Data

Normally, this field is left Disabled. Select Enabled to reset ESCD (Extended System Configuration Date) upon exiting Setup if a new add-on has been installed and the system re-configuration has caused such a serious conflict that the operating system cannot boot.

Resource Controlled By

The Award Plug and Play BIOS can automatically configure all the boot and Plug-and-Play compatible devices. If Auto is selected, all interrupt requests (IRQ) and DMA assignment fields disappear, as the BIOS automatically assigns them.

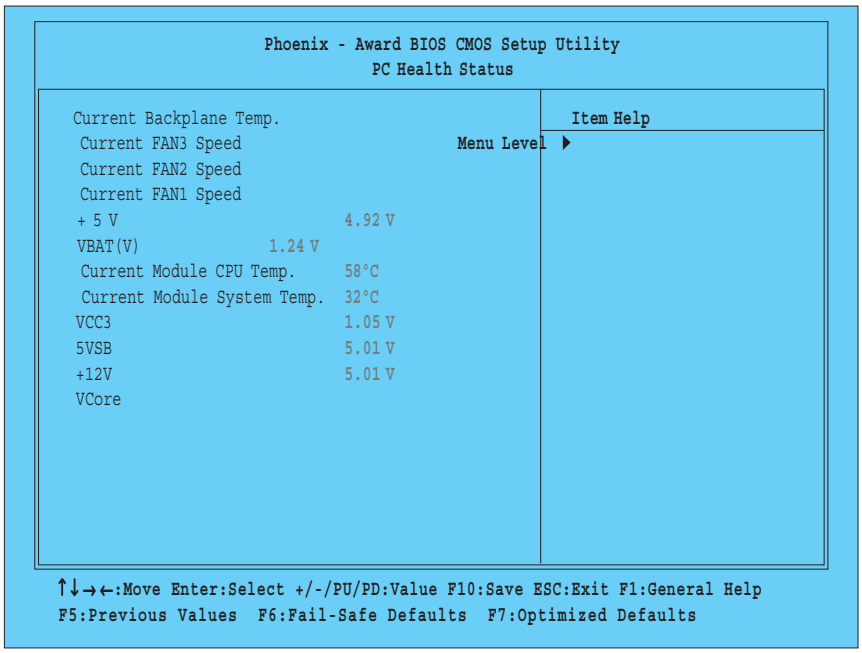
IRQ Resources

When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt:

Legacy ISA
Devices compliant with the original PC/AT bus specification, requiring a specific interrupt (such as IRQ4 for serial port 1).

PCI/ISA PnP
Device complies with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

8.9 PC Health Status



Current Backplane Temperature

Displays

Current FAN3 Speed

Displays

Current FAN2 Speed

Displays

Current FAN1 Speed

Displays

+5 V

Displays

Current Module CPU Temp

Displays

Current Module System Temp

Displays

VCC3

Displays

5VSB

Displays

+12V

Displays

VCore

Displays

8.10 BIOS POST Messages

If BIOS detects an error during the Power On Self-Test (POST), it will prompt the user by either sounding a beep code or displaying a message. If a message is displayed, it will be accompanied by:

PRESS F1 TO CONTINUE, OR DEL TO ENTER SETUP

POST Beep

Currently there are two kinds of beep codes in BIOS:

- This first beep code indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps.
- The second beep code indicates that a DRAM error has occurred. This beep code consists of a repeated single long beep.

Error Messages

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

- CMOS CHECKSUM ERROR - DEFAULTS LOADED
  Checksum of CMOS is incorrect.This may indicate that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.
- DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER
  No boot device was found. This could mean that either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Reboot the system.
- DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP
  Type of diskette drive installed in the system is different from the CMOS definition. Run Setup to re-configure the drive type correctly.
- DISPLAY SWITCH IS SET INCORRECTLY
  Display switch on the motherboard can be set to either monochrome or color. This indicates the switch; is set to a different setting than indicated in Setup. Determine which setting is correct, then either turn off the system and change the jumper, or enter Setup and change the VIDEO selection.

- FLOPPY DISK CNTRLR ERROR OR NO CNTRLR PRESENT
  Cannot find or initialize the floppy drive controller. Make sure the controller is installed correctly and firmly. If there are no floppy drives installed, be sure the Diskette Drive selection in Setup is set to NONE.

- KEYBOARD ERROR OR NO KEYBOARD PRESENT
  Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot. If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue the boot.

- OFFENDING ADDRESS NOT FOUND
  This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

- OFFENDING SEGMENT:
  This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem has been isolated.

- PRESS A KEY TO REBOOT
  This will be displayed at the bottom screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

- PRESS F1 TO DISABLE NMI, F2 TO REBOOT
  When BIOS detects a Non-Maskable Interrupt condition during boot, you can choose to disable the NMI and continue to boot, or you can reboot the system with NMI enabled.

- RAM PARITY ERROR - CHECKING FOR SEGMENT
  Indicates a parity error in Random Access Memory.

- SYSTEM HALTED, (CTRL-ALT-DEL) TO REBOOT
  Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the CTRL and ALT keys and press DEL.

- MEMORY TEST FAIL
  BIOS reports the memory test as failed if the onboard memory test results in an error.

8.11 BIOS POST Codes

Normal POST Codes

POST (hex)	Name	Description
C0	Turn Off Chipset And CPU test	OEM Specific-Cache control cache Processor Status (1FLAGS) Verification. Tests the following processor status flags: Carry, zero, sign, overflow, The BIOS sets each flag, verifies they are set, then turns each flag off and verifies it is off. Read/Write/Verify all CPU registers except SS, SP, and BP with data pattern FF and 00. RAM must be periodically refreshed to keep the memory from decaying. This function ensures that the memory refresh function is working properly.
C1	Memory Presence	First block memory detect OEM Specific-Test to size onboard memory. Early chip set initialization Memory presence test OEM chip set routines Clear low 64K of memory Test first 64K memory.
C2	Early Memory Initialization	OEM Specific- Board Initialization
C3	Extend Memory DRAM select	OEM Specific- Turn on extended memory
		Initialization Cyrix CPU Initialization Cache initialization
C4	Special Display Handling	OEM Specific- Display/Video Switch Handling so that Switch Handling display switch errors never occurs
C5	Early Shadow	OEM specific- Early shadow enable for fast boot
C6	Cache presence test	External cache size detection
CF	CMOS Check	CMOS checkup
B0	Spurious	If interrupt occurs in protected mode
B1	Unclaimed NMI	If unmasked NMI occurs, display Press F1 to disable NMI, F2 reboot
BF	Program Chip Set	To program chipset from default values
E1-EF	Setup Pages	E1- Page 1, E2 - Page 2, etc.

POST (hex)	Name	Description
1	Force load Default	Chipset defaults program to chipset
2	Reserved	
3	Early Superio Init	Early Initialized the Super I/O
4	Reserved	
5	Blank video	Reset Video controller
6	Reserved	
7	Init KBC	Keyboard controller init
8	KB test	Test the Keyboard
9	Reserved	
A	Mouse Init	Initialized the mouse
B	Onboard Audio init	Onboard audio controller initialize if exist
C	Reserved	
D	Reserved	
E	CheckSum Check	Check the integrity of the ROM, BIOS and message
F	Reserved	
10	Auto detect EEPROM	Check Flash type and copy flash write/erase routines to 0F000h segments
11	Reserved	
12	Cmos Check	Check Cmos Circuitry and reset CMOS
13	Reserved	
14	Chipset Default load	Program the chipset registers with CMOS values
15	Reserved	
16	Clock Init	Init onboard clock generator
17	Reserved	
18	Identify the CPU	Check the CPU ID and init L1/L2 cache
19	Reserved	
1A	Reserved	
1B	Setup Interrupt	Initialize first 120 interrupt Vector Table vectors with SPURIOUS_INT_HDLR and initialize INT 00h-1Fh according to INT_TBL
1C	Reserved	
1D	Early PM Init	First step initialize if single CPU onboard
1E	Reserved	
1F	Re-initial KB	Re-init KB
20	Reserved	
21	HPM init	If support HPM, HPM get initialized here
22	Reserved	
23	Test CMOS Interface and Battery Status	Verifies CMOS is working correctly, detects bad battery. If failed, load CMOS defaults and load into chipset
24	Reserved	
25	Reserved	
26	Reserved	
27	KBC final Init	Final Initial KBC and setup BIOS data area
28	Reserved	
29	Initialize Video Interface	Read CMOS location 14h to find out type of video in use. Detect and Initialize Video Adapter.

POST (hex)	Name	Description
2A	Reserved	
2B	Reserved	
2C	Reserved	
2D	Video memory test	Test video memory, write sign-on message to screen Setup shadow RAM - Enable shadow according to Setup.
2E	Reserved	
2F	Reserved	
30	Reserved	
31	Reserved	
32	Reserved	
33	PS2 Mouse setup	Setup PS2 Mouse and reset KB
34	Reserved	
35	Test DMA Controller 0	Test DMA channel 0
36	Reserved	
37	Test DMA Controller 1	Test DMA channel 1
38	Reserved	
39	Test DMA Page Registers	Test DMA Page Registers.
3A	Reserved	
3B	Reserved	
3C	Test Timer Counter 2	Test 8254 Timer 0 Counter 2.
3D	Reserved	
3E	Test 8259-1 Mask Bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.
3F	Reserved	
40	Test 8259-2 Mask Bits	Verify 8259 Channel 2 masked interrupts by alternately turning off and on the interrupt lines.
41	Reserved	
42	Reserved	
43	Test Stuck 8259's Interrupt Bits	Turn off interrupts then verify no interrupt mask register is on.
	Test 8259 Interrupt Functionality	Force an interrupt and verify the interrupt occurred.
44	Reserved	
45	Reserved	
46	Reserved	
47	Set EISA Mode	If EISA nonvolatile memory checksum is good, execute EISA initialization. If not, execute ISA tests and clear EISA mode flag.
48	Reserved	
49	Size Base and Extended Memory	Size base memory from 256K to 640K and extended memory above 1 MB.

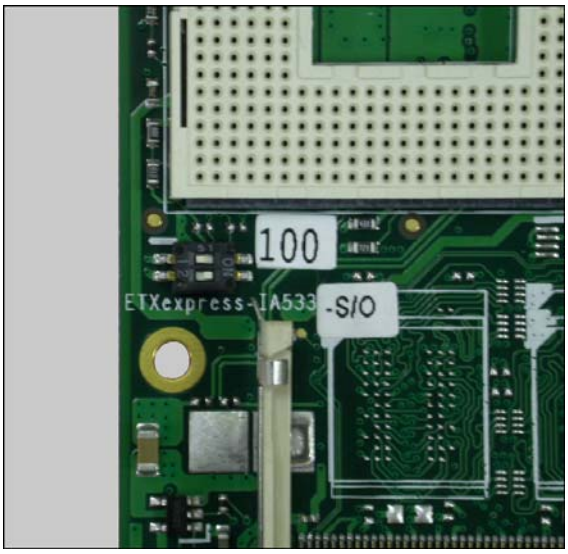
POST (hex)	Name	Description
4A	Reserved	
4B	Reserved	
4C	Reserved	
4D	Reserved	
4E	Test Base and Extended Memory	Test base memory from 256K to 640K and extended memory above 1 MB. using various patterns. NOTE: This test is skipped in EISA mode and can be skipped with ESC key in ISA mode.
4F	Reserved	
50	USB init	Initialize USB controller
51	Reserved	
52	Memory Test	Test all memory of memory above 1 MB. using Virtual 8086 mode, page mode and clear the memory
53	Reserved	
54	Reserved	
55	CPU display	Detect CPU speed and display CPU vendor specific version string and turn on all necessary CPU features
56	Reserved	
57	PnP Init	Display PnP logo and PnP early init
58	Reserved	
59	Setup Virus Protect	Setup virus protect according to Setup
5A	Reserved	
5B	Awdflash Load	If required, will auto load Awdflash.exe in POST
5C	Reserved	
5D	Onboard I/O Init	Initializing onboard Super I/O
5E	Reserved	
5F	Reserved	
60	Setup enable	Display setup message and enable setup functions
61	Reserved	
62	Reserved	
63	Initialize & Install Mouse	Detect if mouse is present, initialize mouse, install interrupt vectors.
64	Reserved	
65	PS2 Mouse special	Special treatment to PS2 Mouse port
66	Reserved	
67	ACPI init	ACPI subsystem initializing
68	Reserved	
69	Setup Cache Controller	Initialize cache controller.
6A	Reserved	
6B	Setup Entering	Enter setup check and auto configuration check up
6C	Reserved	
6D	Initialize Floppy Drive & Controller	Initialize floppy disk drive controller and any drives.
6E	Reserved	

POST (hex)	Name	Description
6F	FDD install	Install FDD and setup BIOS data area parameters
70	Reserved	
71	Reserved	
72	Reserved	
73	Initialize Hard Drive & Controller	Initialize hard drive controller and any drives.
74	Reserved	
75	Install HDD	IDE device detection and install
76	Reserved	
77	Detect & Initialize Serial/Parallel Ports	Initialize any serial and parallel ports (also game port).
78	Reserved	
79	Reserved	
7A	Detect & Initialize Math Co-processor	Initialize math co-processor.
7B	Reserved	
7C	HDD Check for Write protection	HDD check out
7D	Reserved	
7E	Reserved	
7F	POST error check	Check POST error and display them and ask for user intervention
80	Reserved	
81	Reserved	
82	Security Check	Ask password security (optional).
83	Write CMOS	Write all CMOS values back to RAM and clear screen.
84	Preboot Enable	Enable parity checker Enable NMI, Enable cache before boot.
85	Initialize Option ROMs	Initialize any option ROMs present from C8000h to EFFFFh. NOTE: When FSCAN option is enabled, ROMs initialize from C8000h to F7FFFh.
86-91	Reserved	
92	Reserved	
93	Boot Medium detection	Read and store boot partition head and cylinders values in RAM
94	Final Init	Final init for last micro details before boot
95	Special KBC patch	Set system speed for boot Setup NumLock status according to Setup
96	Boot Attempt	Set low stack Boot via INT 19h.
FF	Boot	

Appendix A: FSB Speed Setup

A.1 Socket CPU FSB speed

Express-IA533 that accepts socket type CPUs, includes a 2-port switch to set the correct FSB for different type of Intel Pentium M CPUs. This setting is only meant for socket type CPU, BGA type CPUs are fixed at production .



Switch	1	2
533	ON	ON
400	OFF	ON

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Important Safety Instructions

For user safety, please read and follow all instructions, warnings, cautions, and notes marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:

  - Turn off power and unplug any power cords/cables.

- To avoid electrical shock and/or damage to equipment:

  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.
- A Lithium-type battery may be provided for uninterrupted, backup or emergency power.

Risk of explosion if battery is replaced by an incorrect type. Dispose of used batteries according to the instructions.

- Equipment must be serviced by authorized technicians when:

  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

Getting Service

Contact us should you require any service or assistance.

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