COM Express

Express-IW400

User's Manual

Manual Revision: 2.00

Revision Date: October 22, 2007

Part Number: 50-1J010-1000

Preliminary Release

ADLINK TECHNOLOGY INC.

Revision History

Release	Date	Change
2.0	2007/10/22	Initial release

Preface

Copyright 2007 ADLINK Technology, Inc.

Disclaimer

The information in this document is subject to change without prior notice in order to improve reliability, design, and function and does not represent a commitment on the part of the manufacturer.

In no event will the manufacturer be liable for direct, indirect, special, incidental, or consequential damages arising out of the use or inability to use the product or documentation, even if advised of the possibility of such damages.

Trademarks

AT, XT, CGA, PC, VGA, OS/2 and PS/2 are registered trademarks of International Business Machines Corporation. AMIBIOS8™ is a trademark of American Megatrends, Inc. Microsoft®, DOS®, MS-DOS®, Windows®, Windows® 3.x, Windows® 95, Windows® 98, Windows® 2000, Windows® NT®, and Windows® Vista® are registered trademarks of Microsoft Corporation. Intel®, Pentium®, Celeron®, and SpeedStep® are registered trademarks of Intel Corporation. PCI Express®, COM Express® and Express® are registered trademarks of the Peripheral Component Interconnect Special Interest Group (PCI-SIG).

Product names mentioned herein are used for identification purposes only and may be trademarks and/or registered trademarks of their respective companies.

Warranty Policy

Thank you for choosing ADLINK. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1) Before using ADLINK's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from:

   http://rma.adlinktech.com/policy/

2) All ADLINK products come with a limited two-year warranty, one year for products bought in China:

- The warranty period starts on the day the product is shipped from ADLINK's factory.
- Peripherals and third-party products not manufactured by ADLINK will be covered by the original manufacturers' warranty.
- For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ADLINK is not responsible for any loss of data.
- Please ensure the use of properly licensed software with our systems. ADLINK does not condone the use of pirated software and will not service systems using such software. ADLINK will not be held legally responsible for products shipped with unlicensed software installed by the user.
- For general repairs, please do not include peripheral accessories. If peripherals need to be included, be certain to specify which items you sent on the RMA Request & Confirmation Form. ADLINK is not responsible for items not listed on the RMA Request & Confirmation Form.

3) Repair service is not covered by ADLINK's two-year guarantee in the following situations:

- Damage caused by not following instructions in the User's Manual.
- Damage caused by carelessness on the user's part during product transportation.
- Damage caused by fire, earthquakes, floods, lightening, pollution, other acts of God, and/or incorrect usage of voltage transformers.
- Damage caused by inappropriate storage environments such as high temperatures, high humidity, or volatile chemicals.
- Damage caused by leakage of battery fluid during or after change of batteries by customer/user.

- Damage from improper repair by unauthorized technicians.
- Products with altered and/or damaged serial numbers are not entitled to our service.
- This warranty is not transferable or extendable.
- Other categories not protected under our warranty.

4) Customers are responsible for all fees necessary to transport damaged products to ADLINK.

5) To ensure the speed and quality of product repair, please download an RMA application form from our company website: http://rma.adlinktech.com/policy/ Products with attached RMA forms receive priority.

For further questions, please e-mail our FAE staff:

service@adlinktech.com

Using this Manual

Audience and Scope

The Express-IW400 User's Manual is intended for hardware technicians and systems operators with knowledge of installing, configuring and using COM Express® modules. This document is specifically inteded to describe implementing ADLINK Express-IW400 modules to a wide array of user applications.

Manual Organization

This manual is organized as follows:

Preface: Presents important copyright notifications, disclaimers, trademarks, warranty, safety, and associated information on the proper understanding and usage of this document and its associated product(s).

Chapter 1, Introduction: Introduces the ADLINK Express-IW400, its features and applications.

Chapter 2, Specifications: The physical atributes of the module, operating environment and power consumption.

Chapter 3, Function Diagram: Module functional layout.

Chapter 4, Mechanical Dimensions: Physical dimensions of the module.

Chapter 5, Watch Dog Timer: Presents Watch Dog Timer driver and demo application specifications.

Chapter 6, Connectors: A full description of the module pin-outs, signal descripitons and mechanical characteristics.

Chapter 7, System Resources: A detailed presentation of module memory and I/O resources.

Chapter 8, AMIBIOS8™: Describes system BIOS settings and configurations.

Appendix A, USB Client Port: Explains how to get a console port to the Express-IW400 module.

Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

Additional information, aids, and tips that help users perform tasks.

Information to prevent *minor* physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

Information to prevent *serious* physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

Important Safety Instructions

For user safety, please read and follow all instructions, WARNINGS, CAUTIONS, and NOTES marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.
- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.
- A Lithium-type battery may be provided for uninterrupted, backup or emergency power.

Risk of explosion if battery is replaced by an incorrect type. Dispose of used batteries according to the instructions.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

Acronyms & Terminology

The following terms are used throughout this document. This list is prepared in alphabetical order for clarity.

10/100/1000BASE-T - A standard for gigabit Ethernet over copper wiring as specified in Clause 28 of IEEE 802.3-2002.

ACPI - Advanced Configuration and Power Interface

ASF - Alert Standard Format

BIOS - Basic Input/Output System

CF - CompactFlash®

CMOS - Complementary metal–oxide–semiconductor

COM Express® - Computer-On-Module Express

CPU - Central Processing Unit

DDR2 (DDR2 SDRAM) - double-data-rate two synchronous dynamic random access memory

DRAM - Dynamic random access memory

ECC - Error-Correcting Code

ECP - Extended Capability Port

EDMA (DMA) - Enhanced Direct Memory Access

EEPROM (E2PROM) - Electrically Erasable Programmable Read-Only Memory

FSB - Front Side Bus

FWH - Firmware Hub

GB (GByte) - Gigabyte (1,073,741,824 bytes)

GHz - Gigahertz (one billion hertz)

Gigabit Ethernet (GbE or GigE) - A term describing various technologies for transmitting Ethernet frames at a rate of a gigabit per second, as defined by the IEEE 802.3-2005 standard.

HCT - Hardware Compatibility Tests

HD - Hard Drive

I/O (IO) - Input / Output

IA - Embedded Intel® Architecture

ICH - I/O Controller Hub

IDE - Integrated Drive Electronics

IEEE - Institute of Electrical and Electronics Engineers

IMCH - Integrated Memory Controller Hub

IRQ / SERIRQ - Interrupt Request / Serial Interrupt Request

kb - Kilobit (1,024 bits)

kB - Kilobyte (1,024 bytes)

LAN - Local Area Network

LPC - Low Pin Count

MB - Megabyte (1,048,576 bytes)

MCH - Memory Controller Hub

MHz - Megahertz (one million hertz)

N/A (N.A.) - Not Applicable

NMI - Non-maskable Interrupt

OS - Operating System

PC - Personal Computer

PCI Express® (PCIe® or PCI-E®) - An I/O interconnect bus standard (which includes a protocol and a layered architecture) that expands on and doubles the data transfer rates of original PCI

PnP - Plug and Play

POST - Power-On Self Test

PXE - Pre-Boot Execution Environment

RAM - Random Access Memory

RoHS - Restriction of Hazardous Substances Directive. The Directive on the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment

ROM - Read Only Memory

RS-232 (Recommended Standard 232) - is a standard for serial binary data signals

S-ATA - Serial - Advanced Technology Attachment

SCI - System Control Interrupt

SODIMM - small outline dual in-line memory module

Super I/O - a class of I/O controller integrated circuits that combines interfaces for a variety of low-bandwidth devices.

TBD - To Be Determined

TOM - Top of Memory

USB - Universal Serial Bus

VGA - Video Graphics Accelerator

X86 - A generic term that refers to the CISC (complex instruction set computer) architecture, the most commercially successful central processing unit (CPU) architecture in modern computing.

Reference Documentation

The following list of documents may be used as reference materials to support installation and using the ADLINK Express-IW400. This list is prepared in alphabetical order (by vendor name, then by document title) for clarity.

Vendor	Title
American Megatrends	AMIBIOS8™ Check Point and Beep Code List
American Megatrends	Setup for AMIBIOS8™
Intel®	Watch Dog Timer (WDT) Driver Specification, Rev. 1.0
Intel®	Watch Dog Timer (WDT) Demo Application Specification, Rev. 1.0
PICMG®	PICMG® COM.0 R1.0: COM Express® Module Base Specification

Getting Service

Contact us should you require any service or assistance.

ADLINK TECHNOLOGY INC. (HEADQUARTERS)

Web Site:	http://www.adlinktech.com
Sales & Service:	service@adlinktech.com
Telephone No.:	+886-2-8226-5877
Fax No.:	+886-2-8226-5717
Mailing Address:	9F No. 166 Jian Yi Road, Chungho City, Taipei 235, Taiwan, ROC

ADLINK TECHNOLOGY AMERICA INC.

Sales & Service:	info@adlinktech.com
Toll-Free:	+1-866-423-5465
Fax No.:	+1-949-727-2099
Mailing Address:	8900 Research Drive, Irvine, CA 92618, USA

ADLINK TECHNOLOGY CO. LTD. (BEIJING)

Sales & Service:	market@adlinkchina.com.cn
Telephone No.:	+86-10-5885-8666
Fax No.:	+86-10-5885-8625
Mailing Address:	Rm. 801, Power Creative E, No. 1, B/D Shang Di East Rd. Beijing, 100085 China

ADLINK TECHNOLOGY CO. LTD. (SHANGHAI)

Sales & Service:	market@adlinkchina.com.cn
Telephone No.:	+86-21-6495-5210
Fax No.:	+86-21-5450-0414
Mailing Address:	4F, Bldg. 39, No.333 Qinjiang Road, Chao He Jing Hi Tech Park Shanghai, 200233 China

ADLINK TECHNOLOGY CO. LTD. (SHENZHEN)

Sales & Service:	market@adlinkchina.com.cn
Telephone No.:	+86-755-2643-4858
Fax No.:	+86-755-2664-6353
Mailing Address:	2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7, High-Tech Industrial Park S., Shenzhen, 518057 China

ADLINK TECHNOLOGY INC. (EUROPE)

Sales & Service: emea@adlinktech.com
Toll-Free: +49-211-495-5552
Fax No.: +49-211-495-5557
Mailing Address: Nord Carree 3, 40477
Düsseldorf, Germany

ADLINK TECHNOLOGY INC. (INDIA)

Sales & Service: india@adlinktech.com
Telephone No.: +91-80-6560-5817
Fax No.: +91-80-2244-3548
Mailing Address: No. 1357, Ground Floor, “Anupama”, Aurobindo Marg JP Nagar (Ph-1)
Bangalore, Karnataka 560078, India

ADLINK TECHNOLOGY JAPAN CORP.

Sales & Service: japan@adlinktech.com
Telephone No.: +81-3-4455-3722
Fax No.: +81-3-5333-6040
Mailing Address: Asahiseimei Hatagaya Bldg. 1-1-2 Hatagaya Shibuya-ku,
Tokyo, Japan

ADLINK TECHNOLOGY INC. (SOUTH KOREA)

Sales & Service: korea@adlinkchina.com.cn
Telephone No.: +82-2-2057-0565
Fax No.: +82-2-2057-0563
Mailing Address: 4F, Kostech Building, 262-2, Yangjae-Dong, Seocho-Gu,
Seoul, 137-130, South Korea

ADLINK TECHNOLOGY SINGAPORE PTE. LTD.

Sales & Service: singapore@adlinktech.com
Telephone No.: +65-6844-2261
Fax No.: +65-6844-2263
Mailing Address: 84 Genting Lane #07-02A, Cityneon Design Center,
Singapore 349584

Table of Contents

This page intentionally left blank.

1 Introduction

1.1 Description

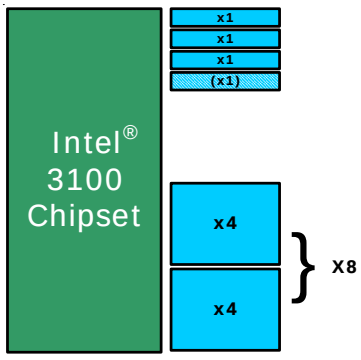
The Express-IW400 is based on the Intel® 3100 single chip, server level chipset with enhanced Intel® SpeedStep® support. The Intel® 3100 Chipset is a single integrated chip that contains the functionality of a Memory Controller Hub and an I/O Controller Hub. It can support Intel® Celeron® M and Pentium® M CPU's in the range of 1 GHz to 1.8 GHz at FSB400. The Intel® 3100 chipset combines server-class memory and I/O controller functions into a single component, creating the first integrated Intel® chipset specifically optimized for embedded, communications, and storage applications. Both chipset and processors are part of the Embedded Intel® Architecture (IA) that warrants long production life for applications that need extended availability.

ECC Memory Support

The Express-IW400 supports registered ECC type, single channel DDR2 400 MHz memory. Either available as two vertically postioned SODIMM sockets or one horizonatally positioned SODIMM socket.

High Bandwidth PCI Express® up to x8

The Intel® 3100 Chipset provides one configurable x8 PCI Express® interface with a maximum theoretical bandwidth of 4 GByte/s. The x8 PCI Express® interface may alternatively be configured as two independent x4 PCI Express® interfaces with a maximum theoretical bandwidth of 2 GBytes/s each. The Intel® 3100 Chipset also supports an additional x4 PCI Express® interface with a maximum theoretical bandwidth of 2 GBytes/s which may alternatively be configured as four independent x1 PCI Express® interfaces.



EDMA on PCI Express®

The IMCH includes an integrated four-channel Enhanced Direct Memory Access (EDMA) controller to perform background data transfers between locations in main memory, or from main memory to a memory-mapped I/O destination. These transfers may be individually designated to be coherent (snooped on the FSB) or non-coherent (not snooped on the FSB), providing improvements in system performance and utilization when cache coherence is managed by software rather than hardware.

The module comes with a single onboard Gigabit Ethernet port and four channel SATA. It has legacy support for Parallel IDE, 32-bit PCI and LPC bus support. The Express-IW400 comes equipped with many embedded features such as: Remote console, CMOS backup, CPU and System monitoring and a Dual Watchdog timer for NMI or RESET.

Express-IW400 is an RoHS compliant and lead-free product.

2 Specifications

2.1 General

- CPU: Intel® Pentium® M 745 at 1.8 Ghz,
  LV Intel® Pentium® M 738 at 1.4 Ghz, soldered only
  Intel® Celeron® M 370 at 1.5 Ghz,
  ULV Intel® Celeron® M 373 at 1.0 Ghz, soldered only
- Memory: Single channel registered ECC DDR2 at 400 MHz up to 4 GB
  Option 1: one horizontal SODIMM socket max 2 GB
  Option 2: two vertical SODIMM sockets max 4 GB
- Chipset: Intel® 3100 single integrated chipset containing MCH and ICH
- L2 Cache: Dothan type processors: 1 MB (Celeron® M), 2 MB (Pentium® M)
- BIOS: AMIBIOS8™ in 1 MB FWH with console redirection and CMOS EEPROM backup
- Hardware Monitor: Supply Voltages and CPU temperature
- Watchdog Timer: Dual stage watchdog timer

Option 1 Memory Configuration

Option 2 Memory Configuration

- Expansion Busses :
  - One x8 PCI Express lane can also be used as two x4 PCI Express® lanes
  - Four PCI Express® x1 lanes (one claimed by onboard GbE)
  - Four 32-bit PCI 2.3 Masters at 33/66 MHz
  - Low Pin Count (LPC) interface for Super I/O on carrier
  - SMBus interface support
  - Four GPIO input, Four GPIO output
- Power Mode Support :
  - ACPI v2.0, supports S0 - S3 - S4 - S5 power modes

2.2 Video

- On carrier: optional VGA support can be located on carrier board using PCI or PCI Express® x1, X4 or X8 bus interface

2.3 LAN

- Chipset: Intel® 82573 PCI Express®-based Gb Ethernet connection
- Type: Triple speed 10/100/1000BASE-T IEEE 802.3 compliant witch supports ASF 2.0 and Advanced Pass

2.4 Multi I/O

- Chipset: integrated in Intel® 3100
- USB: supports up to four USB 2.0 ports, supports legacy keyboard/mouse
- Serial: accessible via dedicated USB port (client USB)
- SATA: four integrated Serial ATA 150 ports
- PATA IDE: single channel IDE for CF card support (SATA to IDE conversion)

2.5 Module Power Consumption

All power testing was done on power supply wiring leading to the Express® carrier board. Although all voltages were measured, only 12 V and 5 VSB are relevant because they are the only ones used by the Express® module. The typical power level was measured under Windows® XP without applications running. Maximum level was measured under 100% system stress generate by HCT and Kpower loading.

Testing was done with 512 MB DDR2 533 on installed SODIMM.

Express-IA533-373/0 (BGA type Celeron® M 373 at 1 GHz)	
Standby	TBD
Typical	12 Watt
Max	16 Watt

Express-IA533-738/0 (BGA type Pentium® M 738 at 1.4 GHz)	
Standby	TBD
Typical	14 Watt
Max	20 Watt

Express-IA533-S/0 with socket type Pentium® M 745 at 1.8 GHz	
Standby	TBD
Typical	19 Watt
Max	29 Watt

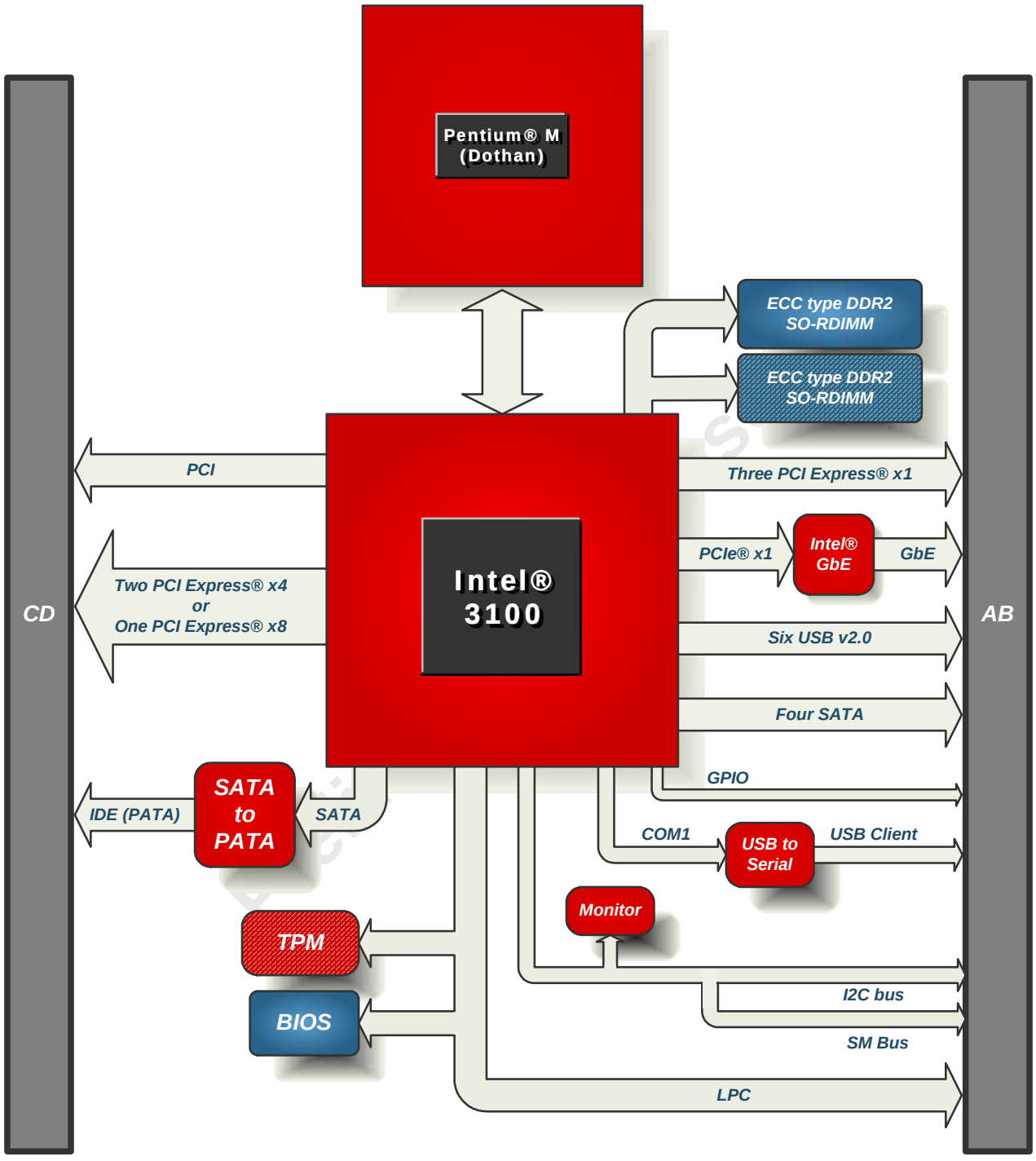
Express-IA533-S/0 with socket type Pentium® M 760 at 2.0 GHz	
Standby	TBD
Typical	20 Watt
Max	32 Watt

2.6 Mechanical and Environmental

- Formfactor and Type: Standard COM Express® Type II
- Dimensions: 95 x 125 mm
- Operating Temperature: 0°C to 60°C
- Relative Humidity: up to 90% at 55°C

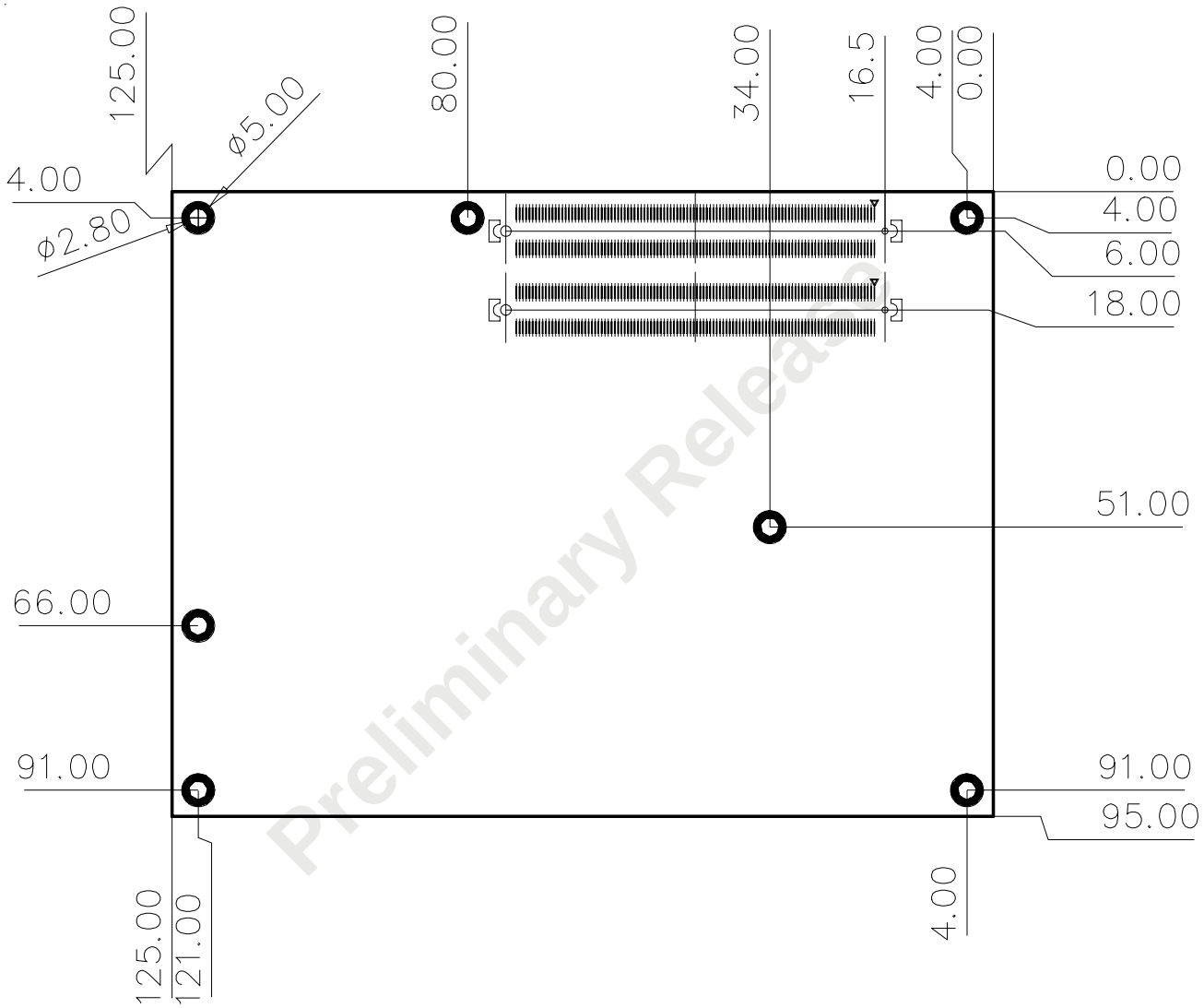
This page intentionally left blank.

3 Function diagram



This page intentionally left blank.

4 Mechanical Dimensions



This page intentionally left blank.

5 Watch Dog Timer (WDT)

5.1 Overview

The Intel® 3100 Chipset Watch Dog Timer (WDT) is a kernel mode driver designed to run on Microsoft® Windows® OS (XP, Server® 2003, Vista®, and XP Embedded) platforms. When enabled, the WDT can generate an interrupt or reboot the system in the event of a system lockup.

This WDT supports a number of IOCTL commands. These commands enable the applications to access and control all the aspects of the WDT.

The WDT is located on the LPC bus. As such, it is not detected by the Plug-n-Play (PnP) manager. To install the driver, the user must manually go through the "Add Device" wizard in the Control Panel. Installation details are covered later in this chapter.

5.2 Installing the WDT Driver

The WDT driver does not announce itself to the device manager.

To install the WDT driver:

These instructions assume that you are in the default Microsoft Windows® XP control panel view.

1. Open Control Panel and click "Printers and Other Hardware".
2. In the "See Also" box at the top left hand corner, click "Add Hardware".
3. Click "Next" to look for hardware.
4. Click "Yes, I have already connected the hardware" and then click "Next".
5. Scroll to the bottom of the "Installed hardware" list and select "Add a new hardware device".
6. Click "Install the hardware that I manually select from a list" and then Click "Next".
7. Click "Show All Devices" and then Click "Next".
8. Click "Have Disk…", point to the location where the WDT driver is stored and click "OK".
9. Click on "Intel® 3100 Chipset Watch Dog Timer" and install.

5.3 Interface with the Driver

The only supported driver communication method is through IOCTLs. The IOCTLs defined in this section allow a user-mode application to access all the capabilities of the WDT.

5.3.1 Symbolic Link

The driver creates a named device object that can be accessed through the symbolic link "\\\\.\\SAWD1". As such, the application can communicate with the driver by obtaining a handle from CreateFile() with the path, "\\\\.\\SAWD1".

```
/* Example: Getting a handle to the WDT driver */

HANDLE handle_to_wdt;

handle_to_wdt = CreateFile(
                    "\\\\.\\SAWD1",
                    GENERIC_WRITE,
                    FILE_SHARE_WRITE,
                    NULL,
                    OPEN_EXISTING,
                    0,
                    NULL);
```

Once a handle is obtained successfully, the application uses the DeviceIoControl() function to communicate with the driver.

```
/* Example: Sending an IOCTL to the driver. Here we assume
* handle_to_wdt was obtained successfully
*/

BOOL status;
int return_length;
status = DeviceIoControl(
               handle_to_wdt,      /* handle to wdt */
               IOCTL_ENABLE_WDT,   /* IOCTL to send */
               NULL,               /* no input buffer */
               0,                  /* input length = 0 */
               NULL,               /* no output buffer */
               0,                  /* output length = 0 */
               &return_length,     /* should be 0 */
               NULL );             /* wait until I/O completes */
```

5.3.2 Supported IOCTLs

IOCTL_GET_CAPABILITIES

```
#define IOCTL_GET_CAPABILITIES                          \
            CTL_CODE( FILE_DEVICE_UNKNOWN, 0x802, \
            METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL accepts a buffer of type PSAWD_CAPABILITY_OUT_BUFF, and fills in the min and max field, indicating the minimum and maximum downcounter value. The Version field will be set to 1.

```
typedef struct _SAWD_CAPABILITY_OUT_BUFF {

unsigned    long Version;   /* version of interface used */
unsigned    long min;       /* minimum value in msecs */
unsigned    long max;       /* maximum value in msecs */

} SAWD_CAPABILITY_OUT_BUFF, *PSAWD_CAPABILITY_OUT_BUFF;
```

IOCTL_ENABLE_WDT

```
#define IOCTL_ENABLE_WDT                                \
            CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D00,\
            METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL enables the Watch Dog Timer.

IOCTL_DISABLE_WDT

```
#define IOCTL_DISABLE_WDT                               \
            CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D01,\
            METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL disables the Watch Dog Timer.

IOCTL_LOAD_COUNTER

```
#define IOCTL_LOAD_COUNTER                              \
            CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D02,\
            METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This `IOCTL` accepts a buffer of type `PSAWD_CTRL`, and loads the preload counter 1 and 2 using the data in the `Preload1` and `Preload2` fields.

```
typedef struct _SAWD_CTRL {

HANDLE        UserEvent;  /* Handle to a Ring 3 user event */
unsigned long Version;    /* version of interface used */
unsigned long Flags;      /* flags defined below */
unsigned long Preload1;   /* Preload register # 1 */
unsigned long Preload2;   /* Preload Register # 2 */
unsigned long DownCount;  /* Holds current down count */
```

```
unsigned long     ConfigReg;        /* 16 bit Configuation register */
unsigned short    DeviceStatus;     /* store device status bits */
unsigned short    ReloadReg;        /* 16 bit reload register */
unsigned short    LockReg;          /* 8 bit Lock register */
unsigned long     InterruptCount;   /* # of times stage 1 INT occured */
unsigned short    IRQ;
short             BusType;
unsigned short    BusNumber;
unsigned short    IrqOffset;

} SAWD_CTRL, *PSAWD_CTRL;
```

IOCTL_PING_THE_WDT

```
#define IOCTL_PING_THE_WDT                              \
          CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D02,        \
          METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL reloads the Watch Dog Timer's down-counter with the preload value to prevent a timeout. If the WDT is in stage 1 of the countdown, then preload value 1 will be loaded into the main down counter. If the WDT is in stage 2 of the countdown, then preload value 2 will be loaded into the main down counter.

IOCTL_SET_PRESCALAR

```
#define IOCTL_SET_PRESCALAR                             \
          CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D04,        \
          METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL sets how the 20-bit preload value will be loaded into the 35-bit down counter. The IOCTL accepts an unsigned long integer set to 0 or 1 in the input buffer. If the input is 0, then the 20-bit preload value will be counted down at 1KHz. If the input is 1, then the 20-bit preload value will be counted down at 1MHz.

IOCTL_READ_DOWN_COUNTER

```
#define IOCTL_READ_DOWN_COUNTER                         \
          CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D05,        \
          METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL returns the current value of the down counter (in an unsigned long integer).

IOCTL_SET_EXTERNAL_OUT

```
#define IOCTL_SET_EXTERNAL_OUT                          \
          CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D07,        \
          METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL enables or disables the external out pin when stage 2 time out occurs. This function accepts an unsigned long integer set to 0 (enable) or 1 (disable).

IOCTL_LOCK_DEVICE

```
#define IOCTL_LOCK_DEVICE                                   \
          CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D08,            \
          METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL locks the WDT device. Once locked, the state (WDT mode vs. free running mode, and Enabled vs. Disabled) of the Watch Dog Timer cannot be changed until the system resets.

IOCTL_ROUTE_INTERRUPT

```
#define IOCTL_ROUTE_INTERRUPT                               \
          CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D09,            \
          METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL accepts an unsigned long integer, sets to 0-3, and uses it to set the type of interrupt to trigger when stage 1 timer expires.

0 sets interrupt type to PCI
1 sets interrupt type to NMI
2 sets interrupt type to SMI
3 disables stage 1 interrupt

IOCTL_USER_HANDLE

```
#define IOCTL_USER_HANDLE                                   \
          CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D0D,            \
          METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This `IOCTL` accepts a buffer of type `PSAWD_CTRL`, and creates an internal reference to the function specified by the `UserEvent` field. When a stage 2 timeout occurs, the driver will call this function.

IOCTL_TEST_CALLBACK

```
#define IOCTL_TEST_CALLBACK                                 \
          CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D0F,            \
          METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This `IOCTL` is used for testing the event handling code and to verify that the application thread is released when the shared UserEvent is signaled by the WDT driver. This `IOCTL` exists mainly for application developers to debug their application.

IOCTL_GET_STATUS

```
#define IOCTL_GET_STATUS                                    \
          CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D13,            \
          METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This `IOCTL` accepts a buffer of type `PSAWD_CTRL`, and fills the `ConfigReg` and `LockReg` fields with the current values of those two registers.

IOCTL_GET_STATUS

```
#define IOCTL_SET_MODE                                  \
          CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D15,        \
          METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL accepts an unsigned long integer, sets to 0 or 1, and uses it to set the WDT mode. If the input is 0, then the WDT is set to Watch Dog Timer mode. If the input is 1, then the WDT is set to free running mode.

IOCTL_GET_TIMEOUT_STATUS

```
#define IOCTL_GET_TIMEOUT_STATUS                        \
          CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D16,        \
          METHOD_BUFFERED, FILE_ANY_ACCESS )
```

This IOCTL accepts an unsigned long integer and uses it as both input and output.

As an input parameter, if the integer is set to 1, then the time out bit on the WDT device will be reset.

As an output parameter, the integer is set to 1 if both stage 1 and stage 2 timers have expired.

IOCTL_GET_STAGE_1_TIMEOUT_STATUS

```
#define IOCTL_GET_STAGE_1_TIMEOUT_STATUS                \
          CTL_CODE( FILE_DEVICE_UNKNOWN, 0x0D17,        \
          METHOD_BUFFERED, FILE_ANY_ACCESS )
```

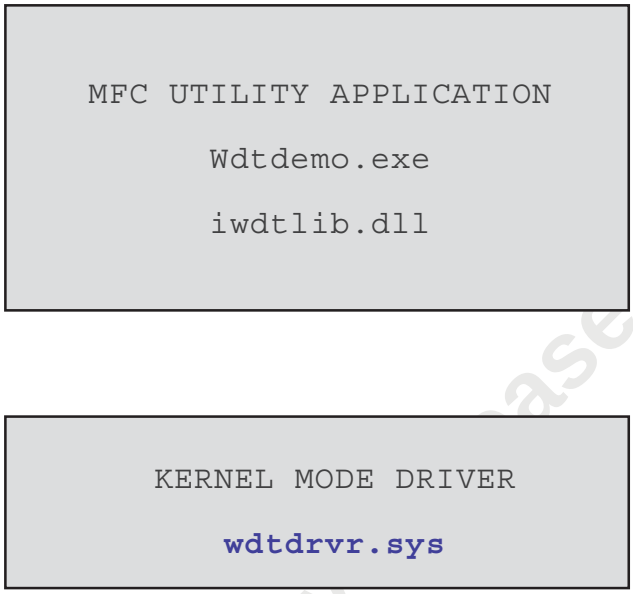
This IOCTL accepts an unsigned long integer and uses it as both input and output.

As an input parameter, if the integer is set to 1, then the time out bit on the WDT device will be reset.

As an output parameter, the integer is set to 1 if the stage 1 timer has expired.

5.4 Watch Dog Timer Windows® XP Demo Utility

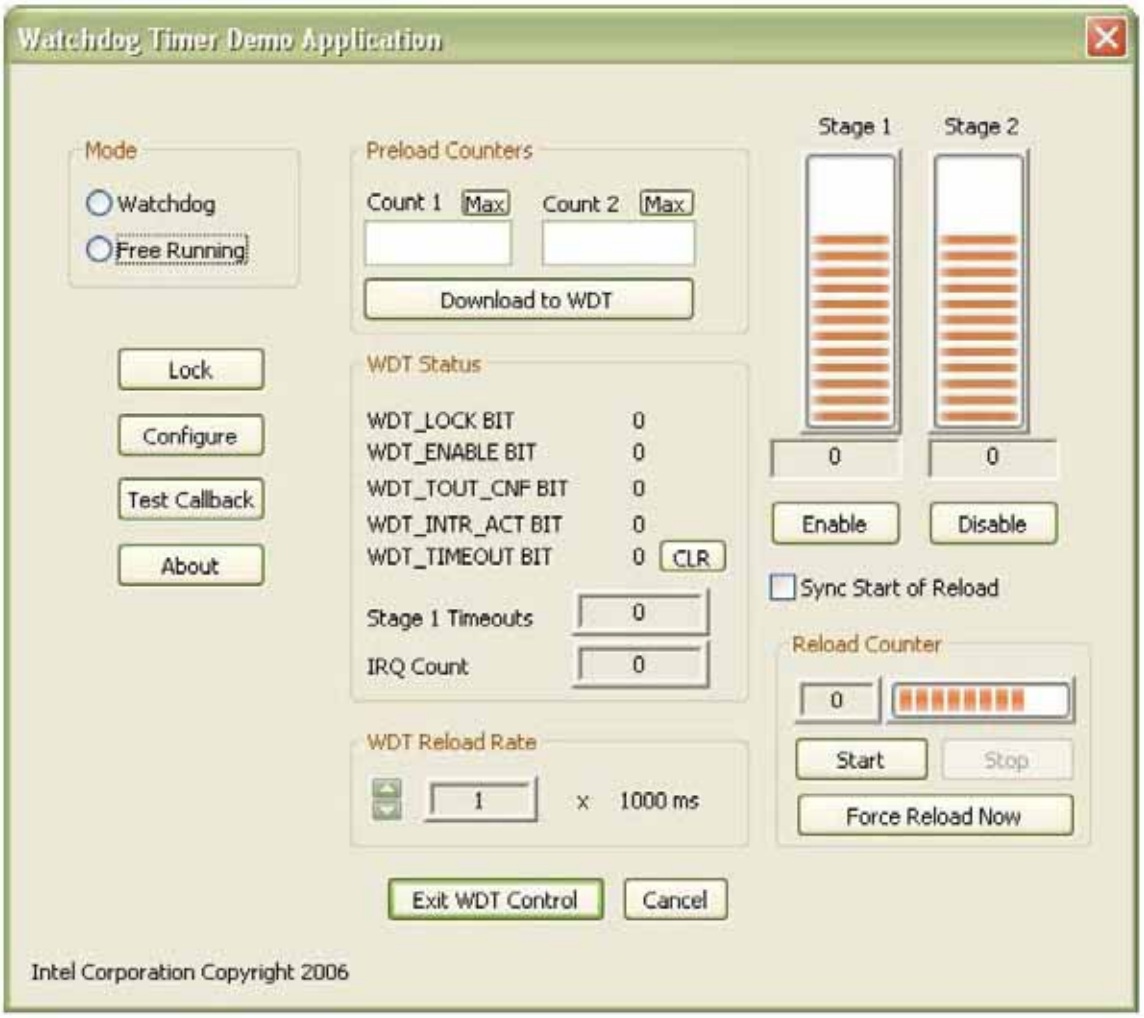
This specification describes the WDT demo utility “Wdtdemo.exe”. The demo tool is a MFC based dialog application that is used to control and monitor the WDT device in the Microsoft* Windows* OS environment. Wdtdemo.exe is to be used only for demonstration of the WDT’s functionality and should not be used as a customer solution.



5.5 Using the Demo Application

The Wdtdemo.exe application has a number of buttons and text entry fields for configuring and controlling the Watch Dog Timer (WDT). Each of the following items has a corresponding button or entry field on the application screen.

- Setting the mode [Mode]
- Locking the WDT device [LOCK]
- Configuring the WDT device [Configure]
- Testing the user mode call function [Test Callback]
- Retrieving the driver and dynamic link version number [Lib Version]
- Downloading the Stage 1 and Stage 2 time-out values [Preload Counters]
- Information about WDT [WDT Status]
- Setting the refresh rate [WDT Reload Rate]
- Starting and Stopping the refresh of the WDT [Enable] [Disable]
- Synchronizing the start of reload [Synch Start of Reload]
- Starting and Stopping the reload counter [Reload Counter]



5.5.1 Setting the Mode

The mode can be set to either Watch Dog Mode or Free Running Mode using the radio select button at the upper left of the dialog.

5.5.2 Locking the WDT Device

The WDT can be locked by software. The LOCK button locks the WDT so that no further changes to the configuration registers are possible until a system reset. A locked WDT cannot be enabled or disabled.

5.5.3 Configuring the WDT

Click the configure button to program the following three configuration options:

Output Enable, Set Prescalar and Interrupt Routing.

[Output Enable]

Enables or disables the toggling of the external output pin if the WDT times out.

[Set Prescalar]

Specifies a prescalar value for the 35-bit, count-down counter. The default value is 34:15. See the *WDT Driver Specification* for details on pre-scalar.

[Interrupt Routing]

Select one of the three interrupt methods (SERIRQ, NMI, or SMI) or "Disabled" to disable interrupt. When SERIRQ is selected, the System BIOS designated interrupt is retrieved from the WDT.

5.5.4 Testing the User Mode Call Function

This button verifies that the interrupt handler and callback mechanism are working correctly. Clicking the Test Callback button increments the Stage 1 interrupt count.

5.5.5 Retrieving the Driver and Dynamic Link Version Number

Click the Lib Version button to retrieve the driver and dynamic link version number.

5.5.6 Downloading the Stage 1 and Stage 2 Time-out Values

There are two edit boxes that specify Stage 1 and Stage 2 count-down values. Enter the values and then click the Download to WDT button to program the values from the application to the WDT device. Both counters are 35-bit counters that decrement using a 20-bit prescalar.

5.5.7 Information about WDT

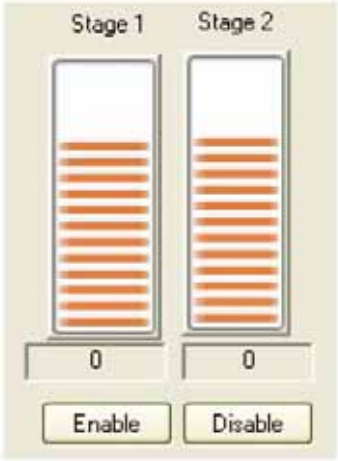
This area shows status of the WDT.

5.5.8 Setting the Reload Rate

The reload rate is set by using the button control that is in the lower center of the application. The rate can be adjusted from between 0 and 100 seconds.

5.5.9 Starting and Stopping the Refresh of the WDT

Clicking the Enable button starts the WDT counting down. Click the Disable button to stop the WDT from counting down.



5.5.10 Starting and Stopping the reload counter

Click the Start button to begin refreshing the WDT. Click the Stop button to stop refreshing the WDT. You can force an immediate refresh of the WDT by clicking the Force Reload Now button. To prevent Stage 1 or Stage 2 timeouts you must start “refresh” and have a refresh rate that ensures that the timer is refreshed before the first stage and or second stage time out.

This page intentionally left blank.

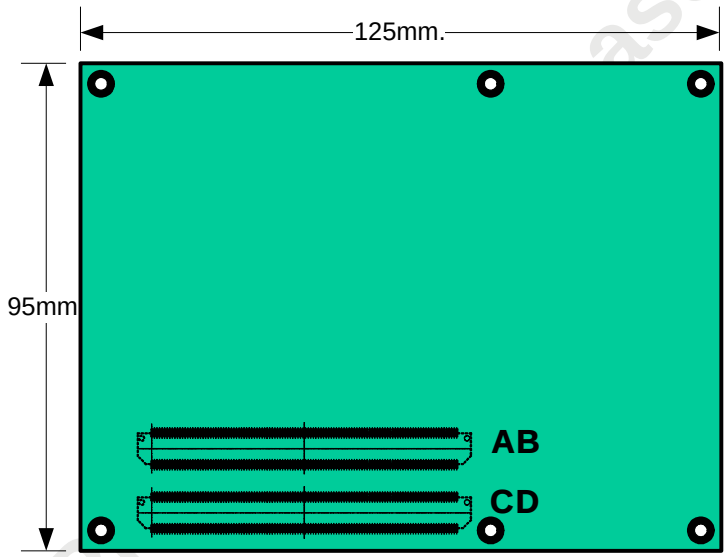
6 Connectors

6.1 COM Express® Type 2

All pin-outs on AB and CD connector of the Express-IW400 comply with pin-out and signal descriptions used in the original "PICMG® COM.0 R1.0: COM Express Module Base Specification". This document contains a description of pin-outs, signal descriptions, and mechanical characteristics of the COM Express® (Expresss®) formfactor.

An additional document, " Express® Design Guide" gives a general introduction to carrier board designs for COM Express® (Express®) modules.

AB Connector
1 Gigabit Ethernet port
LPC interface
4 Serial ATA channels
High Definition Audio
8 USB 2.0 ports
3 PCI Express Lanes x1
Dual 24-bit LVDS channels
Analog VGA
TV-out ports (SDTV/HDTV)
8 GPIO pins
+12V primary power input
+5V standby and 3V RTC

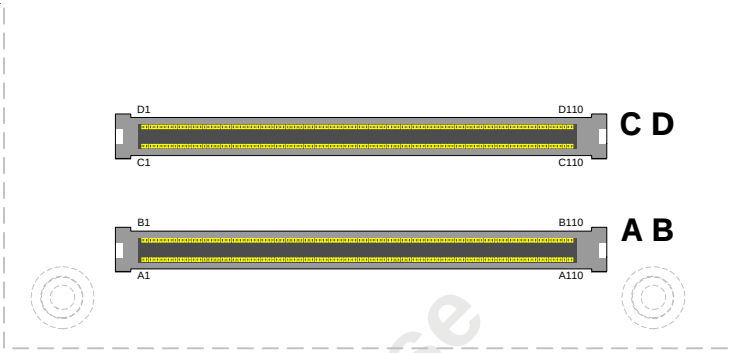


CD Connector
Parallel ATA, IDE port alternate definition assigns this to 2 additional Gigabit Ethernet ports
32-bit PCI v2.3 bus alternate definition assigns this to 10 additional PCI Express x1 lanes
PCI Express x16 for Graphics these pins can also be assigned to two SDVO extensions (multiplexed)
SMB and I²C bus
Power / Thermal control
+12V primary power input

6.2 COM Express® Board to Board Connectors

Signals and Pin-out for :

Basic formfactor, Type 2.



Row A			Row B	
Pin No.	Pin Name		Pin No.	Pin Name
A1	GND (FIXED)		B1	GND (FIXED)
A2	GBE0_MDI3-		B2	GBE0_ACT#
A3	GBE0_MDI3+		B3	LPC_FRAME#
A4	GBE0_LINK100#		B4	LPC_AD0
A5	GBE0_LINK1000#		B5	LPC_AD1
A6	GBE0_MDI2-		B6	LPC_AD2
A7	GBE0_MDI2+		B7	LPC_AD3
A8	NC		B8	LPC_DRQ1#
A9	GBE0_MDI1-		B9	LPC_DRQ1#
A10	GBE0_MDI1+		B10	LPC_CLK
A11	GND (FIXED)		B11	GND (FIXED)
A12	GBE0_MDI0-		B12	PWRBTN#
A13	GBE0_MDI0+		B13	SMB_CK
A14	GBE0_CTREF		B14	SMB_DAT
A15	SUS_S3#		B15	SMB_ALERT#
A16	SATA0_TX+		B16	SATA1_TX+
A17	SATA0_TX-		B17	SATA1_TX-
A18	SUS_S4#		B18	SUS_STAT#
A19	SATA0_RX+		B19	SATA1_RX+
A20	SATA0_RX-		B20	SATA1_RX-
A21	GND (FIXED)		B21	GND (FIXED)
A22	SATA2_TX+		B22	SATA3_TX+
A23	SATA2_TX-		B23	SATA3_TX-
A24	SUS_S5#		B24	PWR_OK
A25	SATA2_RX+		B25	SATA3_RX+
A26	SATA2_RX-		B26	SATA3_RX-
A27	NC		B27	WDT
A28	ATA_ACT#		B28	NC
A29	NC		B29	NC
A30	NC		B30	NC
A31	GND (FIXED)		B31	GND (FIXED)
A32	NC		B32	SPKR
A33	NC		B33	I2C_CK
A34	BIOS_DISABLE#		B34	I2C_DAT
A35	THRMTRIP#		B35	THRM#
A36	NC		B36	NC
A37	NC		B37	NC
A38	NC		B38	USB_4_5_OC#
A39	USB4- Client		B39	NC
A40	USB4+ Client		B40	NC
A41	GND (FIXED)		B41	GND (FIXED)
A42	USB2-		B42	USB3-
A43	USB2+		B43	USB3+
A44	USB_2_3_OC#		B44	USB_0_1_OC#
A45	USB0-		B45	USB1-
A46	USB0+		B46	USB1+

Row C			Row D	
Pin No.	Pin Name		Pin No.	Pin Name
C1	GND FIXED)		D1	GND FIXED)
C2	IDE_D7		D2	IDE_D5
C3	IDE_D6		D3	IDE_D10
C4	IDE_D3		D4	IDE_D11
C5	IDE_D15		D5	IDE_D12
C6	IDE_D8		D6	IDE_D4
C7	IDE_D9		D7	IDE_D0
C8	IDE_D2		D8	IDE_REQ
C9	IDE_D13		D9	IDE_IOW#
C10	IDE_D1		D10	IDE_ACK#
C11	GND (FIXED)		D11	GND (FIXED)
C12	IDE_D14		D12	IDE_IRQ
C13	IDE_IORDY		D13	IDE_A0
C14	IDE_IOR#		D14	IDE_A1
C15	PCI_PME#		D15	IDE_A2
C16	PCI_GNT2#		D16	IDE_CS1#
C17	PCI_REQ2#		D17	IDE_CS3#
C18	PCI_GNT1#		D18	IDE_RESET#
C19	PCI_REQ1#		D19	PCI_REQ3#
C20	PCI_GNT0#		D20	PCI_GNT3#
C21	GND (FIXED)		D21	GND (FIXED)
C22	PCI_REQ0#		D22	PCI_AD1
C23	PCI_RESET#		D23	PCI_AD3
C24	PCI_AD0		D24	PCI_AD5
C25	PCI_AD2		D25	PCI_AD7
C26	PCI_AD4		D26	PCI_C/BE0#
C27	PCI_AD6		D27	PCI_AD9
C28	PCI_AD8		D28	PCI_AD11
C29	PCI_AD10		D29	PCI_AD13
C30	PCI_AD12		D30	PCI_AD15
C31	GND (FIXED)		D31	GND (FIXED)
C32	PCI_AD14		D32	PCI_PAR
C33	PCI_C/BE1#		D33	PCI_SERR#
C34	PCI_PERR#		D34	PCI_STOP#
C35	PCI_LOCK#		D35	PCI_TRDY#
C36	PCI_DEVSEL#		D36	PCI_FRAME#
C37	PCI_IRDY#		D37	PCI_AD16
C38	PCI_C/BE2#		D38	PCI_AD18
C39	PCI_AD17		D39	PCI_AD20
C40	PCI_AD19		D40	PCI_AD22
C41	GND (FIXED)		D41	GND (FIXED)
C42	PCI_AD21		D42	PCI_AD24
C43	PCI_AD23		D43	PCI_AD26
C44	PCI_C/BE3#		D44	PCI_AD28
C45	PCI_AD25		D45	PCI_AD30
C46	PCI_AD27		D46	PCI_IRQC#

Row A (cont.)			Row B (cont.)	
Pin No.	Pin Name		Pin No.	Pin Name
A48	EXCD0_PERST#		B48	EXCD1_CPPE#
A49	EXCD0_CPPE#		B49	SYS_RESET#
A50	LPC_SERIRQ		B50	CB_RESET#
A51	GND (FIXED)		B51	GND (FIXED)
A52	NC		B52	NC
A53	NC		B53	NC
A54	GPI0		B54	GPO1
A55	NC		B55	NC
A56	NC		B56	NC
A57	GND		B57	GPO2
A58	PCIE_TX3+		B58	PCIE_RX3+
A59	PCIE_TX3-		B59	PCIE_RX3-
A60	GND (FIXED)		B60	GND (FIXED)
A61	PCIE_TX2+		B61	PCIE_RX2+
A62	PCIE_TX2-		B62	PCIE_RX2-
A63	GPI1		B63	GPO3
A64	PCIE_TX1+		B64	PCIE_RX1+
A65	PCIE_TX1-		B65	PCIE_RX1-
A66	GND		B66	WAKE0#
A67	GPI2		B67	WAKE1#
A68	PCIE_TX0+		B68	PCIE_RX0+
A69	PCIE_TX0-		B69	PCIE_RX0-
A70	GND (FIXED)		B70	GND (FIXED)
A71	NC		B71	NC
A72	NC		B72	NC
A73	NC		B73	NC
A74	NC		B74	NC
A75	NC		B75	NC
A76	NC		B76	NC
A77	NC		B77	NC
A78	NC		B78	NC
A79	NC		B79	NC
A80	GND (FIXED)		B80	GND (FIXED)
A81	NC		B81	NC
A82	NC		B82	NC
A83	NC		B83	NC
A84	NC		B84	VCC_5V_SBY
A85	GPI3		B85	VCC_5V_SBY
A86	KBD_RST#		B86	VCC_5V_SBY
A87	KBD_A20GATE		B87	VCC_5V_SBY
A88	PCIE0_CK_REF+		B88	RSVD
A89	PCIE0_CK_REF-		B89	NC
A90	GND (FIXED)		B90	GND (FIXED)
A91	RSVD		B91	NC
A92	RSVD		B92	NC
A93	GPO0		B93	NC
A94	RSVD		B94	NC
A95	RSVD		B95	NC
A96	GND		B96	NC
A97	VCC_12V		B97	NC
A98	VCC_12V		B98	NC
A99	VCC_12V		B99	NC
A100	GND (FIXED)		B100	GND (FIXED)
A101	VCC_12V		B101	VCC_12V
A102	VCC_12V		B102	VCC_12V
A103	VCC_12V		B103	VCC_12V
A104	VCC_12V		B104	VCC_12V
A105	VCC_12V		B105	VCC_12V
A106	VCC_12V		B106	VCC_12V
A107	VCC_12V		B107	VCC_12V
A108	VCC_12V		B108	VCC_12V

Row C (cont.)			Row D	
Pin No.	Pin Name		Pin No.	Pin Name
C48	PCI_AD31		D48	PCI_CLKRUN#
C49	PCI_IRQA#		D49	NC
C50	PCI_IRQB#		D50	PCI_CLK
C51	GND (FIXED)		D51	GND (FIXED)
C52	PCIE_RX16+		D52	PCIE_TX16+
C53	PCIE_RX16-		D53	PCIE_TX16-
C54	NC		D54	NC
C55	PCIE_RX17+		D55	PCIE_TX17+
C56	PCIE_RX17-		D56	PCIE_TX17-
C57	NC		D57	TYPE2#
C58	PCIE_RX18+		D58	PCIE_TX18+
C59	PCIE_RX18-		D59	PCIE_TX18-
C60	GND (FIXED)		D60	GND (FIXED)
C61	PCIE_RX19+		D61	PCIE_TX19+
C62	PCIE_RX19-		D62	PCIE_TX19-
C63	RSVD		D63	RSVD
C64	RSVD		D64	RSVD
C65	PCIE_RX20+		D65	PCIE_TX20+
C66	PCIE_RX20-		D66	PCIE_TX20-
C67	RSVD		D67	GND
C68	PCIE_RX21+		D68	PCIE_TX21+
C69	PCIE_RX21-		D69	PCIE_TX21-
C70	GND (FIXED)		D70	GND (FIXED)
C71	PCIE_RX22+		D71	PCIE_TX22+
C72	PCIE_RX22-		D72	PCIE_TX22-
C73	NC		D73	NC
C74	PCIE_RX23+		D74	PCIE_TX23+
C75	PCIE_RX23-		D75	PCIE_TX23-
C76	GND		D76	GND
C77	RSVD		D77	IDE_CBLID#
C78	NC		D78	NC
C79	NC		D79	NC
C80	GND (FIXED)		D80	GND (FIXED)
C81	NC		D81	NC
C82	NC		D82	NC
C83	RSVD		D83	RSVD
C84	GND		D84	GND
C85	NC		D85	NC
C86	NC		D86	NC
C87	GND		D87	GND
C88	NC		D88	NC
C89	NC		D89	NC
C90	GND (FIXED)		D90	GND (FIXED)
C91	NC		D91	NC
C92	NC		D92	NC
C93	GND		D93	GND
C94	NC		D94	NC
C95	NC		D95	NC
C96	GND		D96	GND
C97	RSVD		D97	NC
C98	NC		D98	NC
C99	NC		D99	NC
C100	GND (FIXED)		D100	GND (FIXED)
C101	NC		D101	NC
C102	NC		D102	NC
C103	GND		D103	GND
C104	VCC_12V		D104	VCC_12V
C105	VCC_12V		D105	VCC_12V
C106	VCC_12V		D106	VCC_12V
C107	VCC_12V		D107	VCC_12V
C108	VCC_12V		D108	VCC_12V

This page intentionally left blank.

7 System Resources

7.1 System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - TOM (1)	100000 - N.A	N.A.	Note (1)
960 K - 1024 K	F0000 - FFFFF	64 KB	System BIOS Area
928 K - 960 K	E0000 - EFFFF	64 KB	Extended System BIOS Area
800 K - 928 K	C8000 - E7FFF	160 KB	Expansion ROM. Note (2)
768 K - 800 K	C0000 - C7FFF	32 KB	Extended VGA BIOS. Note (2)
640 K - 768 K	A0000 - BFFFF	128 KB	Video Buffer & SMM space
0 - 640 K	00000 - 7FFFF	640K	Conventional memory

(1) TOM = Top of Memory, some memory ranges such as the ACPI reserved area are unavailable for use.

(2) When a PCI/PCIE VGA card is used, it may need a larger memory range than 32 KB. The VGA BIOS area may be changed to 48 KB or 64 KB. When onboard LAN PXE functionality is enabled, it will occupy memory from the expansion ROM range.

7.2 Direct Memory Access Channels

Channel Number	Data Width	System Resource	Available
0	8- or 16-bits		Note (1)
1	8- or 16-bits	Parallel Port	Note (1), (2)
2	8- or 16-bits	Floppy Controller	Note (1)
3	8- or 16-bits	Parallel Port	Note (1), (2)
4	8- or 16-bits	Reserved. Cascade channel	No
5	16-bits		Note (1)
6	16-bits		Note (1)
7	16-bits		Note (1)

(1) The DMA channels can only be used on LPC bus.

(2) The parallel port ECP mode will occupy channel 1 or 3. If it is enabled, it will occupy memory from the expansion ROM range.

7.3 Legacy I/O Map

Address (hex)	Size	Description	Available
0000 - 00FF	256 bytes	Motherboard resources	No
0278 - 027F	8 bytes	Parallel Port 2 (LPT2)	Note (1)
02E0 - 02E7	8 bytes	CIR Port	Note (1)
02E8 - 02EF	8 bytes	Serial Port 4 (COM4)	Note (2)
02F8 - 02FF	8 bytes	Serial Port 2 (COM2)	Note (2)
0378 - 037F	8 bytes	Parallel Port 1 (LPT1)	Note (1)
03B0 - 03BB	12 bytes	Video (monochrome)	No
03BC - 03BF	4 bytes	Parallel Port 3 (LPT3)	Note (2)
03C0 - 03DF	32 bytes	Video (VGA)	No
03E0 - 03E7	8 bytes	CIR Port	Note (1)
03E8 - 03EF	8 bytes	Serial Port 3 (COM3)	Note (2)
03F0 - 03F5	6 bytes	Diskette controller	Note (1)
03F8 - 03FF	8 bytes	Serial Port 1(COM1)	Note (2)
0400 - 047F	128 bytes	Motherboard resource	No
04D0 - 04D1	2 bytes	Motherboard resource	No
0500 - 055F	96 bytes	Motherboard resource	No
0A00 - 0A07	8 bytes	Motherboard resource	No
0CF9	1 byte	Motherboard resource	No
1000 - EFFF		PCI Bus	Note (3)

(1) The occupation of I/O ranges depends on BIOS setting, only one I/O range will be used and the others are forwarded to LPC bus.

(2) The occupation of I/O range depends on BIOS setting. If external Super I/O controller is present for two external serial ports on LPC bus, the I/O range must be set in BIOS in order to make sure they are really forwarded to LPC bus.

(3) Non PnP/PCI devices must not occupy I/O resource in these areas to avoid abnormal behavior.

7.4 Interrupt Request (IRQ) Lines

PIC Mode Only

IRQ#	Typical Interrupt Resource	Connected	Available
0	AT Timer	N.A.	No
1	Keyboard	N.A.	No
2	Cascade interrupt	N.A.	No
3	COM2/PCI device	IRQ3 via SERIRQ	Note (1)
4	COM1/PCI device	IRQ4 via SERIRQ	Note (1)
5	LPT/PCI device	IRQ5 via SERIRQ	Note (1)
6	Floppy Drive Controller	IRQ6 via SERIRQ	No
7	LPT/PCI device	IRQ7 via SERIRQ	Note (1)
8	System CMOS/Real-time clock	N.A.	No
9	Microsoft® ACPI-Compliant System	IRQ9 via SERIRQ	Note (1), (2)
10	PCI device	IRQ10 via SERIRQ	Yes
11	PCI device	IRQ11 via SERIRQ	Yes
12	PS/2 Mouse	IRQ12 via SERIRQ	No
13	Math Processor	N.A.	No
14	PCI device	IRQ14 via SERIRQ	Yes
15	PCI device	IRQ15 via SERIRQ	Yes

(1) Enable/disable onboard devices. When disabled, the IRQ is free for other PCI devices to use.

(2) In ACPI mode, IRQ9 is used for the SCI (System Control Interrupt) to issue an ACPI

7.5 PCI Configuration Space Map

Bus Number	Device Number	Function Number	Routing	Description
00h	00h	00h	Internal	Intel® Host Bridge
00h	00h	01h	Internal	Intel® DRAM Error Reporting Device
00h	01h	00h	Internal	Intel® EDMA Device
00h	02h	00h	Internal	Intel® PCI Express® Port A0
00h	03h	00h	Internal	Intel® PCI Express® Port A1
00h	1Ch	00h	Internal	Intel® PCI Express® Port B0
00h	1Ch	01h	Internal	Intel® PCI Express® Port B1
00h	1Ch	02h	Internal	Intel® PCI Express® Port B2
00h	1Ch	03h	Internal	Intel® PCI Express® Port B3
00h	1Dh	00h	Internal	Intel® USB 1.1 Controller
00h	1Dh	01h	Internal	Intel® USB 1.1 Controller
00h	1Dh	07h	Internal	Intel® USB 2.0 Host Controller
00h	1Eh	00h	Internal	Intel® PCI to PCI Bridge
00h	1Fh	00h	Internal	Intel® LPC Interface
00h	1Fh	02h	Internal	Intel® SATA Host Controller
00h	1Fh	03h	Internal	Intel® SMbus Controller
05h	00h	00h	INTA - INTD	Intel® Ethernet Controller (Note 1)
01h	04h	00h	INTA - INTD	External PCI Slot 1 (Note 1)
01h	05h	00h	INTA - INTD	External PCI Slot 2 (Note 1)

The bus number will change when a PCIe® VGA card is plugged into the system.

7.6 PCI Interrupt Routing Map

PIRQ	INT	Lan	SATA	UHCI1	UHCI2	EHCI	PCI slot1	PCI slot1	PCIe devices
A	INTA	INTA					INTA	INTD	INTA
B	INTB	INTB					INTB	INTA	INTB
C	INTC	INTC					INTC	INTB	INTC
D	INTD	INTD	INTB		INTB		INTD	INTC	INTD
E	INTE								
F	INTF								
G	INTG								
H	INTH			INTA		INTA			

7.7 System Management Bus and I²C Bus

Internally the SMB bus and I²C bus are one and the same, both coming from the same source, the GX2 companion chip CS5535 . The X4 connector has pin-outs for both I²C and SMB bus. The following onboard devices are connected to the SMB/I²C bus :

Address (hex)	Function	Device	Bus
01001100 (4C)	Thermal Sensor	NS LM63	
10100000 (A0)	DDR2	SO-RDIMM1	
10100010 (A2)	DDR2	SO-RDIMM2	
10101100 (AC)	EEPROM (optional)	AT24C02A	
10101110 (AE)	EEPROM (optional)	AT24C02A	
11100010 (D2)	Clock generator	ICS932S208	
11101100 (DC)	Clock buffer	ICS9DB108	

This page intentionally left blank.

8 AMIBIOS8™ Setup Utility

The following chapter describes the basic navigation of the AMIBIOS8™ BIOS setup utility.

8.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keybaord when you see the following text prompt:

   < Press DEL to run Setup >

3. After you press the < Delete > key, the main BIOS setup menu diplays. You can access the other setup screens from the main BIOS setup menu, such as the Chipset and Power menus.

NOTE:

This manual describes the standard look of the setup screen. The motherboard manufacturer has the ability to change any and all of the settings described in this manual. This means that some of the options described in this manual do not exist in your motherboard's AMIBIOS.

NOTE:

In most cases, the <Delete> key is used to invoke the setup screen. There are a few cases that other keys are used, such as <F1>, <F2>, and so on.

8.1.1 Setup Menu

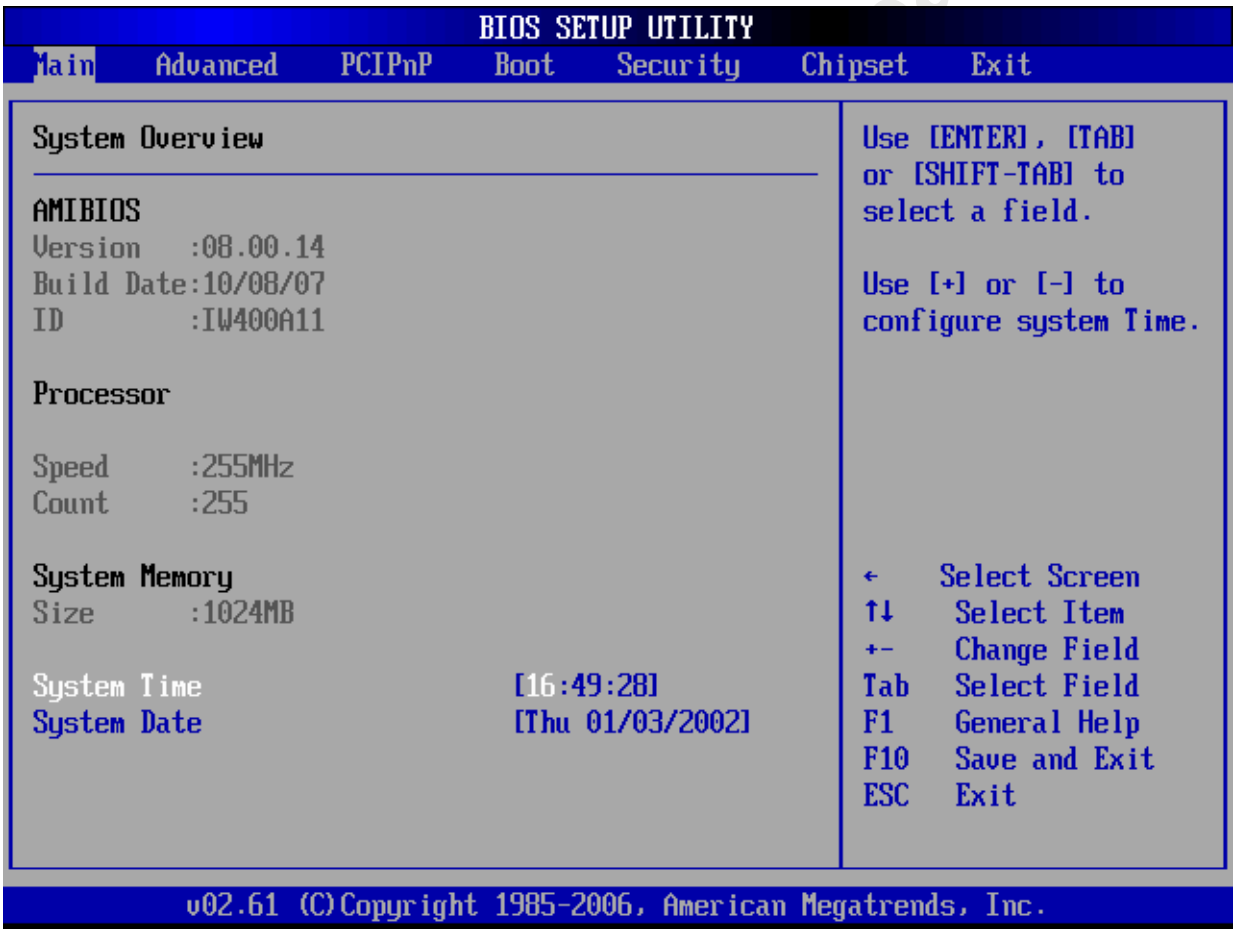
The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed-out" options cannot be configured. Options is blue can be.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

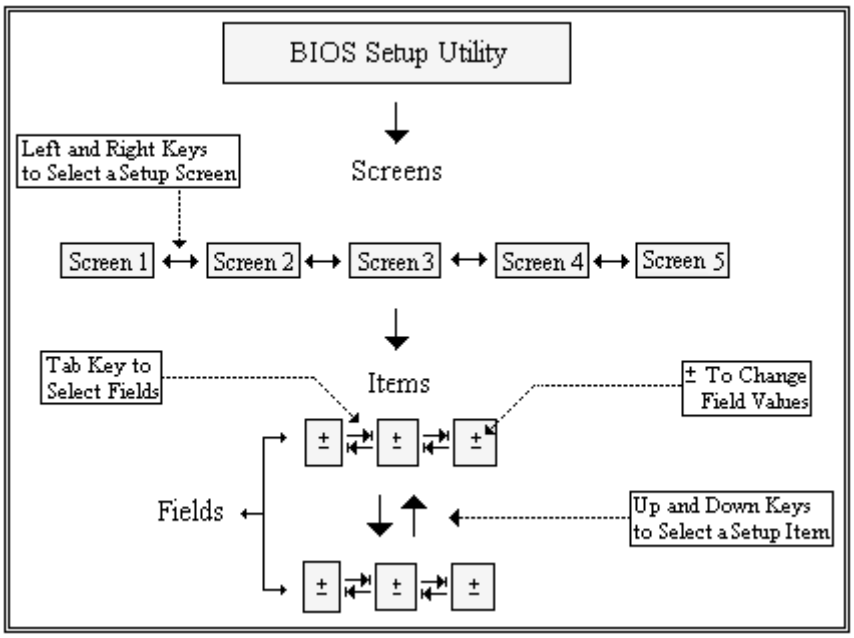
NOTE:

AMIBIOS8™ has default text messages built into it. The motherboard manufacture retains the option to include, leave out, or change any of these text messages. They can also add their own text messages. Because of this, many screen shots in this manual are different from your setup screen.



8.1.2 Navigation

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process. These keys include < F1 >, < F10 >, < Enter >, < ESC >, < Arrow > keys, and so on.



NOTE:

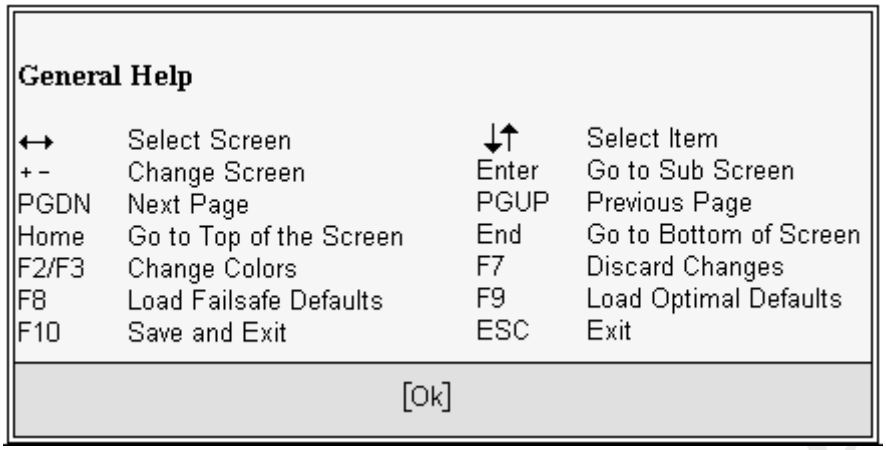
There is a hot key legend located in the right frame on most setup screens.

Hot Key	Description
→←	Left/Right The *Left and Right* < Arrow > keys allow you to select an setup screen. For example: Main screen, Advanced screen, Chipset screen, and so on.
↑↓	Up/Down The *Up and Down* < Arrow > keys allow you to select an setup item or sub-screen.
+ −	Plus/Minus The *Plus and Minus* < Arrow > keys allow you to change the field value of a particular setup item. For example: Date and Time.
Tab	The < Tab > key allows you to select setup fields.

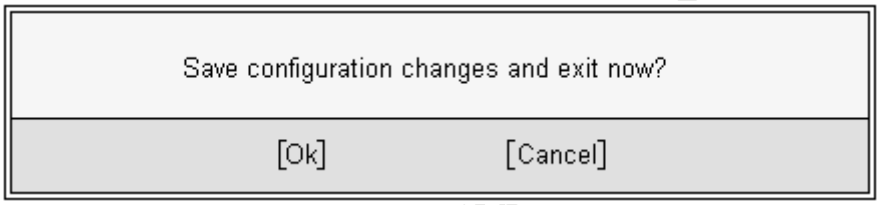
NOTE:

The < F8 > key on your keyboard is the Fail-Safe key. It is not displayed on the key legend by default. To set the Fail-Safe settings of the BIOS, press the < F8 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The Fail-Safe settings allow the motherboard to boot up with the least amount of options set. This can lessen the probability of conflicting settings.

Hot Key	Description
F1	The < F1 > key allows you to display the *General Help screen*. Press the < F1 > key to open the *General Help screen*.

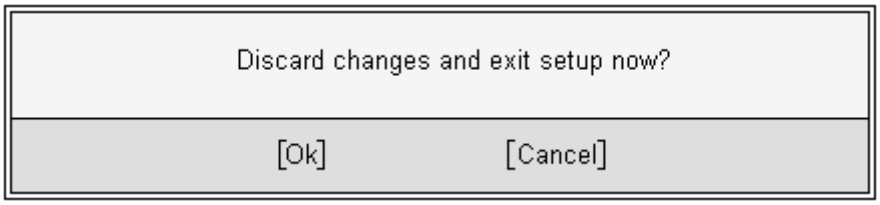


F10	The < F10 > key allows you to save any changes you have made and exit Setup. Press the < F10 > key to save your changes. The following screen will appear:



Press the < Enter > key to save the configuration and exit. You can also use the < Arrow > key to select *Cancel* and then press the < Enter > key to abort this function and return to the previous screen.

ESC	The < Esc > key allows you to discard any changes you have made and exit the Setup. Press the < Esc > key to exit the setup without saving your changes. The following screen will appear:

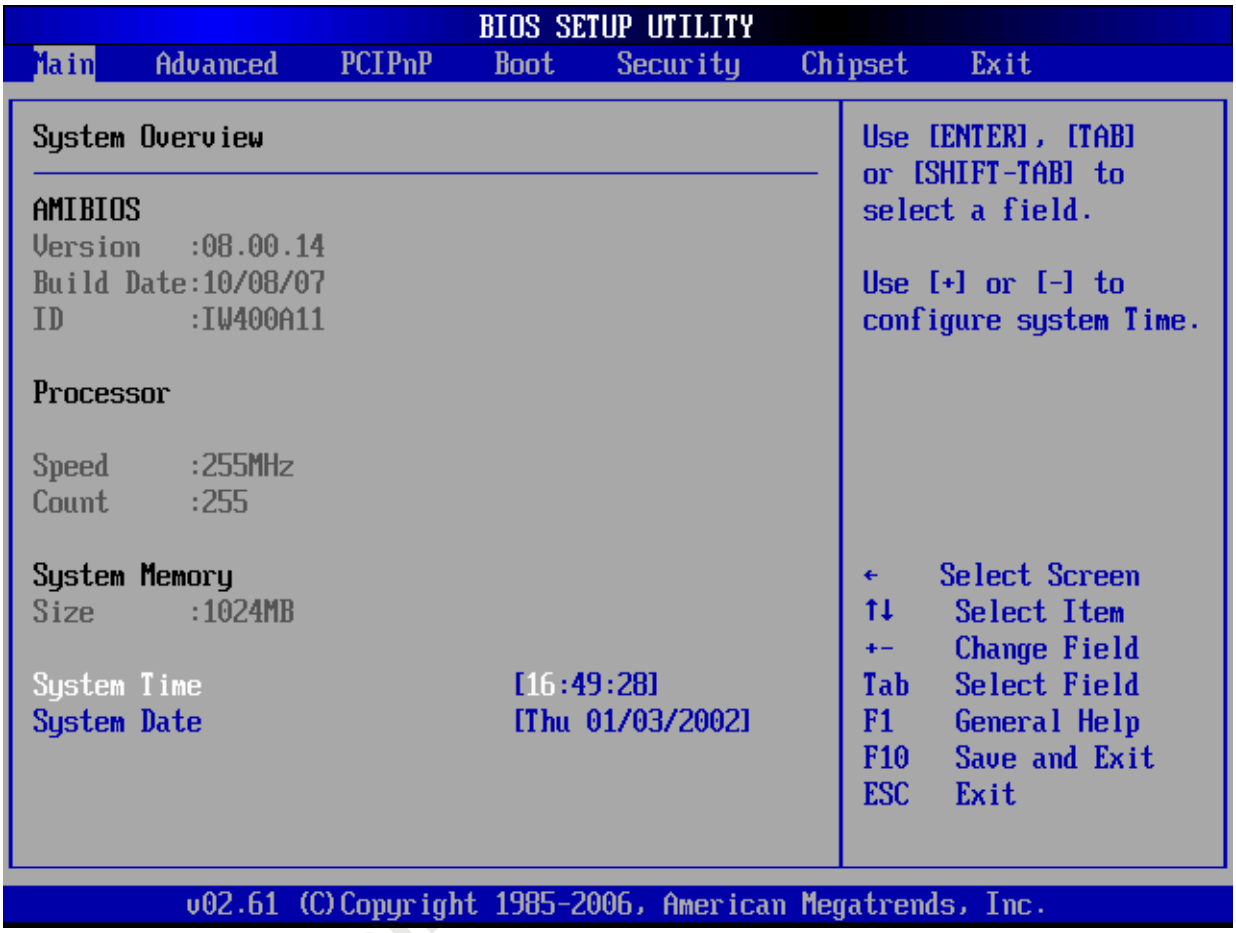


Press the < Enter > key to discard changes and exit. You can also use the < Arrow > key to select *Cancel* and then press the < Enter > key to abort this function and return to the previous screen.

Enter	The < Enter > key allows you to display or change the setup option listed for a particular setup item. The < Enter > key can also allow you to display the setup sub-screens.

8.2 Main Setup

When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the *Main* tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



8.2.1 System Time/System Date

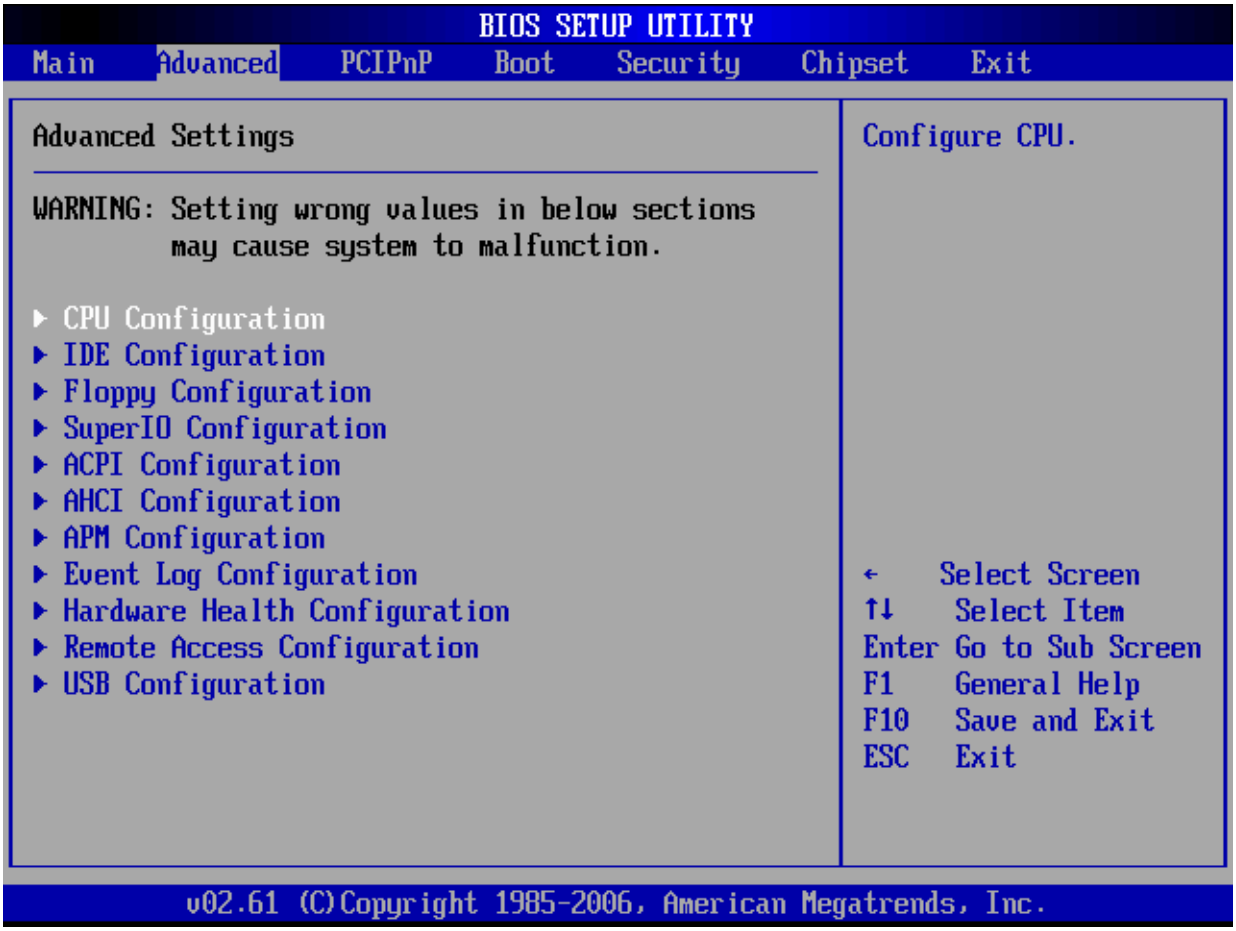
Use this option to change the system time and date. Highlight *System Time* or *System Date* using the < Arrow > keys. Enter new values through the keyboard. Press the < Tab > key or the < Arrow > keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

NOTE: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

8.3 Advanced BIOS Setup

Select the *Advanced* tab from the setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as SuperIO Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the < Arrow > keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screen is shown below.

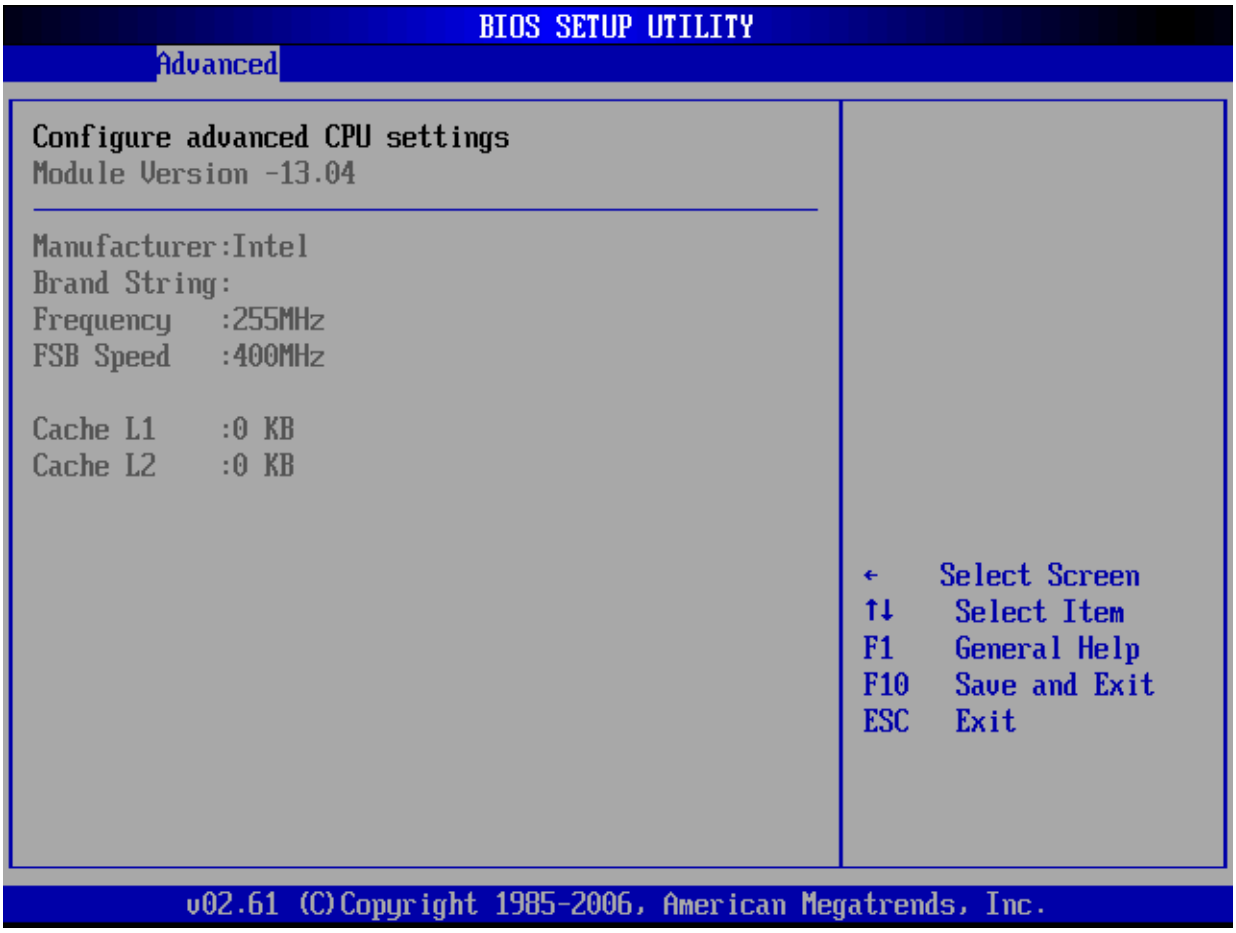
The sub menus are described on the following pages.



8.3.1 CPU Configuration

CPU Configuration Settings

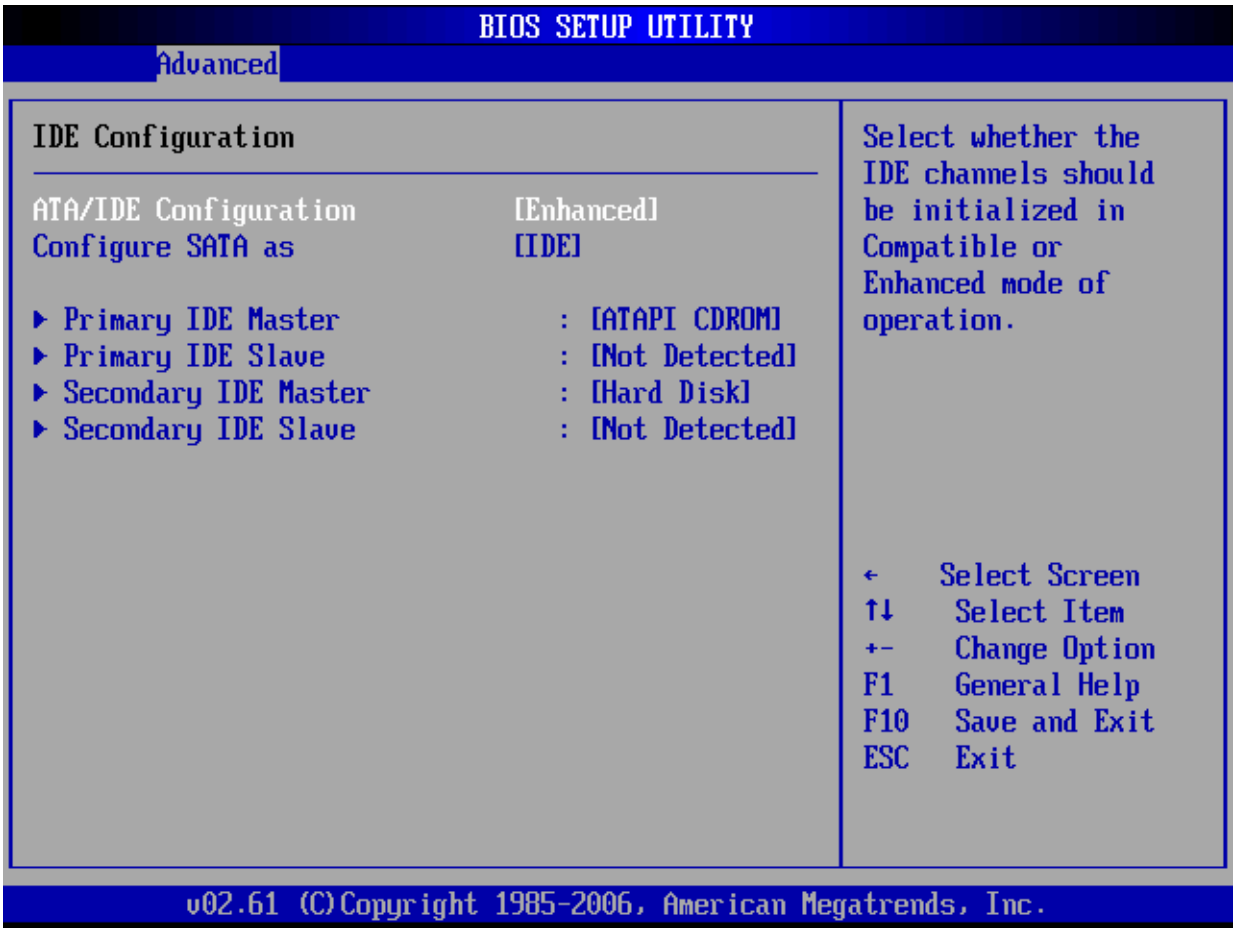
You can use this screen to select options for the CPU Configuration Settings. Use the up and down < `Arrow` > keys to select an item. Use the < `Plus` > and < `Minus` > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the *CPU Configuration* screen is shown below.



8.3.2 IDE Configuration

IDE Configuration Settings

You can use this screen to select options for the IDE Configuration Settings. Use the up and down < `Arrow` > keys to select an item. Use the < `Plus` > and < `Minus` > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the *IDE Configuration* screen is shown below.



Onboard PCI IDE Controller

This item specifies the IDE channels used by the onboard PCI IDE controller. The settings are *Disabled, Primary, Secondary,* or *Both.* The Optimal and Fail-Safe default setting is *Both.*

Option	Description
Disabled	Set this value to prevent the computer system from using the onboard IDE controller.
Primary	Set this value to allow the computer system to detect only the Primary IDE channel. This includes both the Primary Master and the Primary Slave.
Secondary	Set this value to allow the computer system to detect only the Secondary IDE channel. This includes both the Secondary Master and the Secondary Slave.
Both	Set this value to allow the computer system to detect the Primary and Secondary IDE channels. This includes both the Primary Master, Primary Slave, Secondary Master, and Secondary Slave. This is the default setting.

Primary IDE Master, Primary IDE Slave, Secondary IDE Master, Secondary IDE Slave

Select one of the hard disk drives to configure it. Press < `Enter` > to access its the sub menu. The options on the sub menu are described in the following sections.

Hard disk drive Write Protect

Set this option to protect the hard disk drive from being overwritten. The Optimal and Fail-Safe default setting is *Disabled*.

Option	Description
Disabled	Set this value to allow the hard disk drive to be used normally. Read, write, and erase functions can be performed to the hard disk drive. This is the default setting.
Enabled	Set this value to prevent the hard disk drive from being erased.

IDE Detect Time Out (Seconds)

Set this option to stop the AMIBIOS from searching for IDE devices within the specified number of seconds. Basically, this allows you to fine-tune the settings to allow for faster boot times. Adjust this setting until a suitable timing that can detect all IDE disk drives attached is found.

The Optimal and Fail-Safe default setting is *35*.

Option	Description
0	This value is the best setting to use if the onboard IDE controllers are set to a specific IDE disk drive in the AMIBIOS.
5	Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in five seconds. A large majority of ultra ATA hard disk drives can be detected well within five seconds.
10	Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 10 seconds.
15	Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 15 seconds.
20	Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 20 seconds.
25	Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 25 seconds.
30	Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 30 seconds.
35	*35* is the default value. It is the recommended setting when all IDE connectors are set to *AUTO* in the AMIBIOS setting.

Different IDE disk drives take longer for the BIOS to locate than others do.

ATA (PI) 80 pin Cable Detection

Set this option to select the method used to detect the ATA (PI) 80 pin cable. The Optimal and Fail-Safe setting is *Host & Device*.

Option	Description
Host & Device	Set this value to use both the motherboard onboard IDE controller and IDE disk drive to detect the type of IDE cable used. This is the default setting.
Host	Set this value to use motherboard onboard IDE controller to detect the type of IDE cable used.
Device	Set this value to use IDE disk drive to detect the type of IDE cable used.

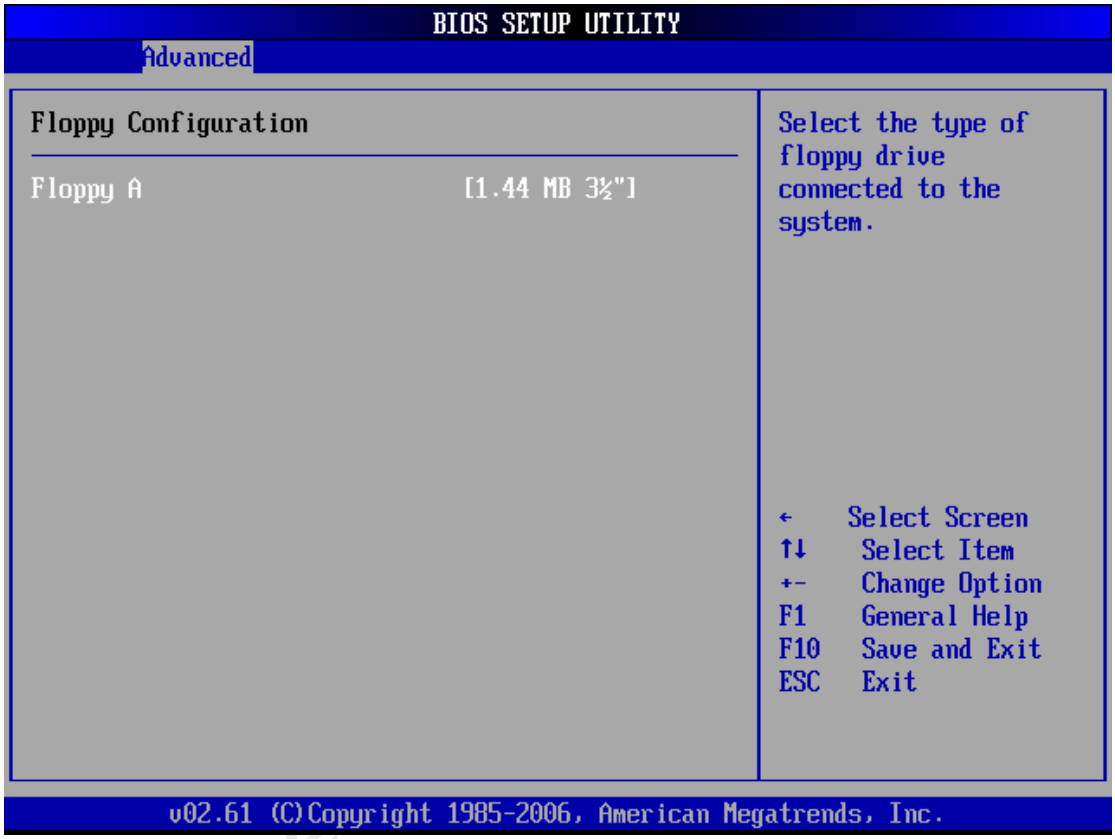
The use of an 80-conductor ATA cable is mandatory for running Ultra ATA/66, Ultra ATA/100 and Ultra ATA/133 IDE hard disk drives. The standard 40-conductor ATA cable cannot handle the higher speeds.

80-conductor ATA cable is plug compatible with the standard 40-conductor ATA cable. Because of this, the system must determine the presence of the correct cable. This detection is achieved by having a break in one of the lines on the 80-conductor ATA cable that is normally an unbroken connection in the standard 40-conductor ATA cable. It is this break that is used to make this determination. The AMIBIOS can instruct the drive to run at the correct speed for the cable type detected.

8.3.3 Floppy Configuration

Floppy Configuration Settings

You can use this screen to specify options for the Floppy Configuration Settings. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



Floppy Drive A:

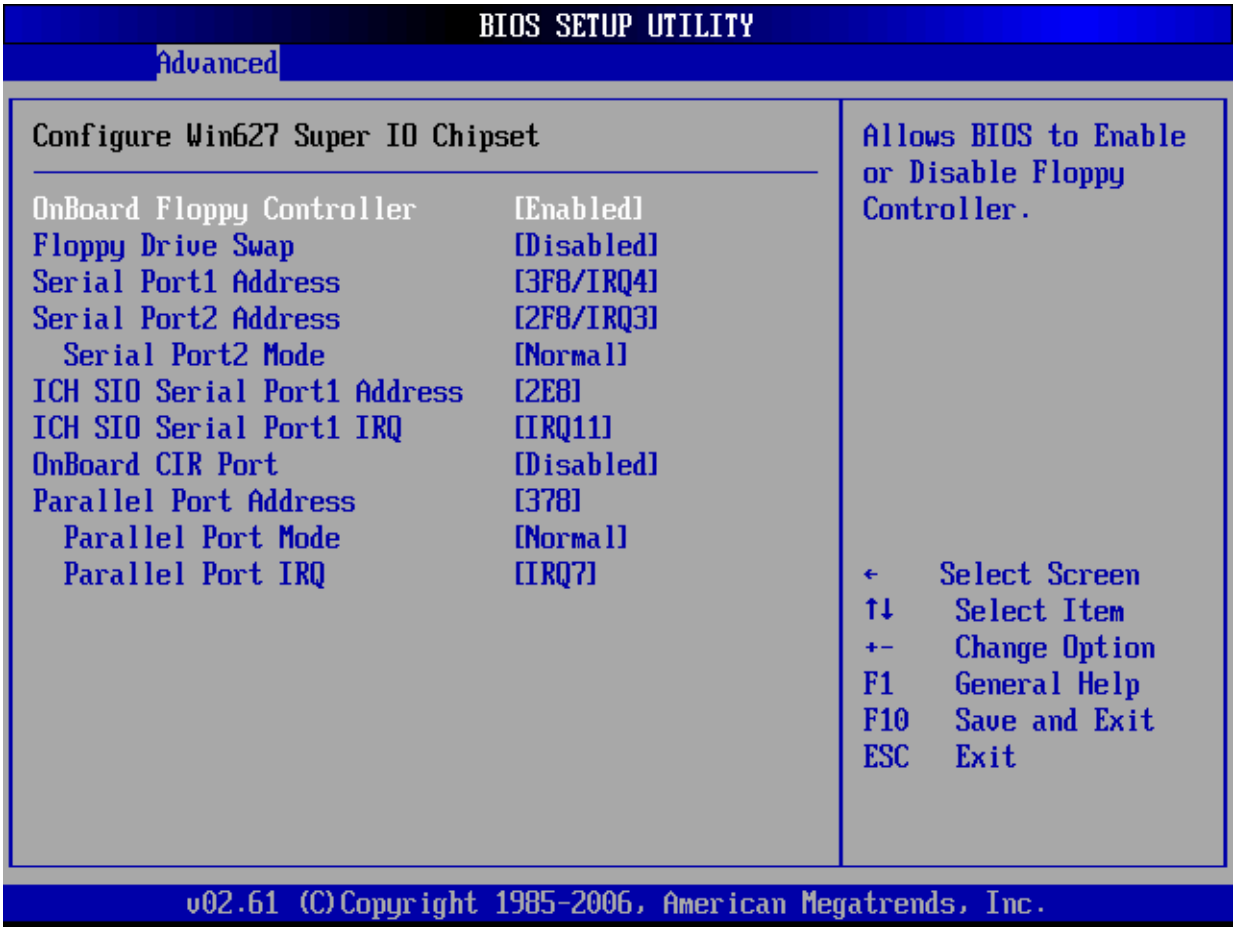
Move the cursor to these fields via up and down <arrow> keys. Select the floppy type. The Optimal setting for floppy drive A: is *1.44 MB 3½".* The Fail-Safe setting for floppy drive A: is *1.44 MB 3½".*

Option	Description
Disabled	Set this value to prevent the use of the selected floppy disk drive channel. This option should be set if no floppy disk drive is installed on the specified channel.
360 KB 5 ¼"	Set this value if the floppy disk drive attached to the corresponding channel is a 360 KB 5¼" floppy disk drive.
1.2 MB 5 ¼"	Set this value if the floppy disk drive attached to the corresponding channel is a 1.2 MB 5¼" floppy disk drive.
720 KB 3 ½"	Set this value if the floppy disk drive attached to the corresponding channel is a 720 KB 3½" floppy disk drive.
1.44 MB 3 ½"	Set this value if the floppy disk drive attached to the corresponding channel is a 1.44 MB 3½" floppy disk drive. This is the default setting for *Floppy Drive A*.

8.3.4 Super IO Configuration

SuperIO Configuration Screen

You can use this screen to select options for the Super I/O settings. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



OnBoard Floppy Controller

This option enables the floppy drive controller on the module. The settings are Enabled and Disabled. The default setting is Enabled.

Floppy Drive Swap

This option is used to logically swap the mapping of drives A: and B:. This option is dependent upon having two installed floppy drives. The settigns are Enabled and Disabled. The Fail-Safe default setting is *Disabled*.

Serial Port1 Address

This option specifies the base I/O port address and Interrupt Request address of serial port 1. The Optimal setting is *3F8/IRQ4*. The Fail-Safe default setting is *Disabled.*

Option	Description
Disabled	Set this value to prevent the serial port from accessing any system resources. When this option is set to *Disabled*, the serial port physically becomes unavailable.
3F8/IRQ4	Set this value to allow the serial port to use 3F8 as its I/O port address and IRQ 4 for the interrupt address. This is the default setting. The majority of serial port 1 or COM1 ports on computer systems use IRQ4 and I/O Port 3F8 as the standard setting. The most common serial device connected to this port is a mouse. If the system will not use a serial device, it is best to set this port to *Disabled*.
2F8/IRQ3	Set this value to allow the serial port to use 2F8 as its I/O port address and IRQ 3 for the interrupt address. If the system will not use a serial device, it is best to set this port to *Disabled*.
3E8/IRQ4	Set this value to allow the serial port to use 3E8 as its I/O port address and IRQ 4 for the interrupt address. If the system will not use a serial device, it is best to set this port to *Disabled*.
2E8/IRQ3	Set this value to allow the serial port to use 2E8 as its I/O port address and IRQ 3 for the interrupt address. If the system will not use a serial device, it is best to set this port to *Disabled*.

Serial Port2 Address

This option specifies the base I/O port address and Interrupt Request address of serial port 2. The Optimal setting is *2F8/IRQ3*. The Fail-Safe setting is *Disabled.*

Option	Description
Disabled	Set this value to prevent the serial port from accessing any system resources. When this option is set to *Disabled*, the serial port physically becomes unavailable.
3F8/IRQ4	Set this value to allow the serial port to use 3F8 as its I/O port address and IRQ 4 for the interrupt address. If the system will not use a serial device, it is best to set this port to Disabled.
2F8/IRQ3	Set this value to allow the serial port to use 2F8 as its I/O port address and IRQ 3 for the interrupt address. This is the default setting. The majority of serial port 2 or COM2 ports on computer systems use IRQ3 and I/O Port 2F8 as the standard setting. The most common serial device connected to this port is an external modem. If the system will not use an external modem, set this port to *Disabled*.

Most internal modems require the use of the second COM port and use 3F8 as its I/O port address and IRQ 4 for its interrupt address. This requires that the Serial Port2 Address be set to *Disabled* or another base I/O port address and Interrupt Request address.

3E8/IRQ4	Set this value to allow the serial port to use 3E8 as its I/O port address and IRQ 4 for the interrupt address. If the system will not use a serial device, it is best to set this port to Disabled.
2E8/IRQ3	Set this value to allow the serial port to use 2E8 as its I/O port address and IRQ 3 for the interrupt address. If the system will not use a serial device, it is best to set this port to *Disabled*.

Serial Port2 Mode

This option specifies allows installation of an Infra-red device by the Serial Port. The settings are Normal, IRDA and ASK IR. The Fail-Safe setting is *Normal.*

ICH SIO Serial Port1 Address

This option specifies the bas I/O port address and Interrupt Request address of serial port 3. The Optimal setting is 3E8/IRQ5. The Fail-Safe default setting is Disabled.

Option	Description
Disabled	Set this value to preven the serial port form accessing any system resxources. When this option is set to Disabled, the serial port physically becomes unavailable.
3F8/IRQ4	Set this value to allow the serial port to use 3F8 as its I/O port address and IRQ 4 for the interrupt address. This is the defaul setting. The majority of serial port 1 or COM 1 ports on computer systems use IRQ4 and I/O Port 3F8 as the standard setting. The most common serial device connected to this port is a mouse. If the system will not use a serial device, it is best to set this port to Disabled.
2F8/IRQ3	Set this value to allow the serial port to use 2F8 as its I/O port address and IRQ 3 for the interrupt address. If the system will not use a serial device, it is best to set this port to Disabled.
3E8/IRQ5	Set this value to allow the serial port to use 3E8 as its I/O port address and IRQ 5 for the interrupt address. If the system will not use a serial device, it is best to set this port to Disabled.
2E8/IRQ7	Set this value to allow the serial port to use 2E8 as its I/O port address and IRQ 7 for the interrupt address. If the system will not use a serial device, it is best to set this port to Disabled.

Onboard CIR Port

This option specifies the base I/O port address of the onboard CIR port. The Optimal setting is 3E0. The Fail-Safe setting is *Disabled*

Option	Description
Disabled	Set this value to prevent the Onboard CIR Port from accessing any system resources. When the value of this option is set to *Disabled*, the infrared port becomes unavailable.
3E0	Set this value to allow the Onboard CIR Port to use 3E0 as its I/O port address.
2E0	Set this value to allow the Onboard CIR Port to use 2E0 as its I/O port address.

Parallel Port Address

This option specifies the I/O address used by the parallel port. The Optimal setting is *378*. The Fail-Safe setting is *Disabled*.

Option	Description
Disabled	Set this value to prevent the parallel port from accessing any system resources. When the value of this option is set to *Disabled*, the printer port becomes unavailable.
378	Set this value to allow the parallel port to use 378 as its I/O port address. This is the default setting. The majority of parallel ports on computer systems use IRQ7 and I/O Port 378H as the standard setting.
278	Set this value to allow the parallel port to use 278 as its I/O port address.
3BC	Set this value to allow the parallel port to use 3BC as its I/O port address.

Parallel Port Mode

This option specifies the parallel port mode. The Optimal setting is *Normal*. The Fail-Safe setting is *Disabled*.

Option	Description
Normal	Set this value to allow the standard parallel port mode to be used. This is the default setting.
Bi-Directional	Set this value to allow data to be sent to and received from the parallel port.
EPP	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bi-directional data transfer driven by the host device.
ECP	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Megabits per second. ECP provides symmetric bi-directional communication.

Parallel Port IRQ

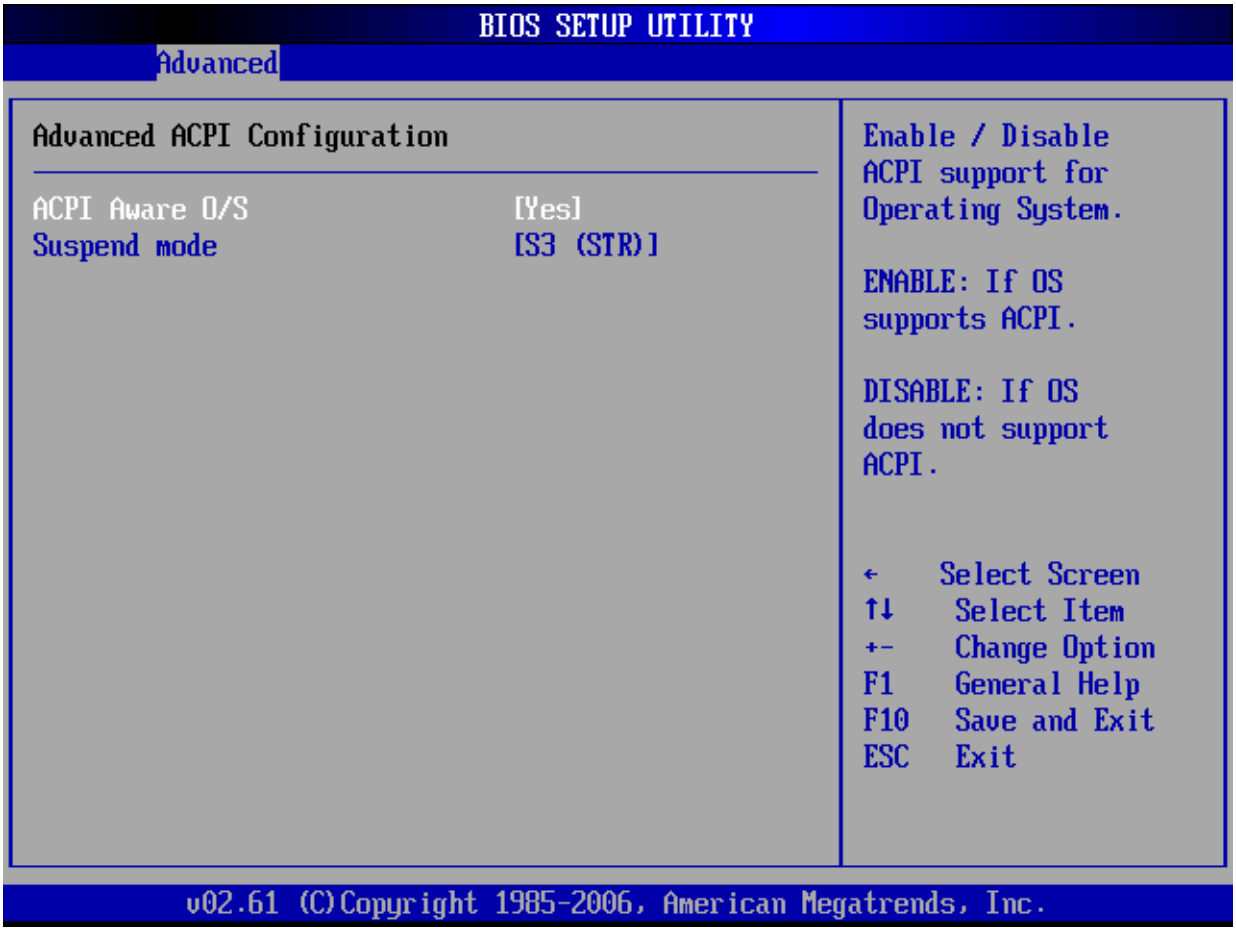
This option specifies the IRQ used by the parallel port. The Optimal and Fail-Safe default setting is 7.

Option	Description
5	Set this value to allow the serial port to use Interrupt 3.
7	Set this value to allow the serial port to use Interrupt 7. This is the default setting. The majority of parallel ports on computer systems use IRQ7 and I/O Port 378H as the standard setting.

8.3.5 Advanced ACPI Configuration

Advanced ACPI Configuration

You can use this screen to select options for the ACPI Advanced Configuration Settings. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on this page. The screen is shown below.



ACPI Aware O/S

Set this value to allow the system to utilize the Intel ACPI (Advanced Configuration and Power Interface) specification. The Optimal and Fail-Safe default setting is Yes.

Option	Description
No	This setting should be set if the operating system in use does not comply with the ACPI (Advanced Configuration and Power Interface) specification. DOS®, Windows 3.x®, and Windows NT® are examples of non-ACPI aware operating systems.
Yes	This setting should be set if the operating system complies with the ACPI (Advanced Configuration and Power Interface) specification. This is the default setting. Windows 95®, Windows 98® and Windows 2000® are examples of ACPI aware operating systems.

Suspend mode (S3 STR)

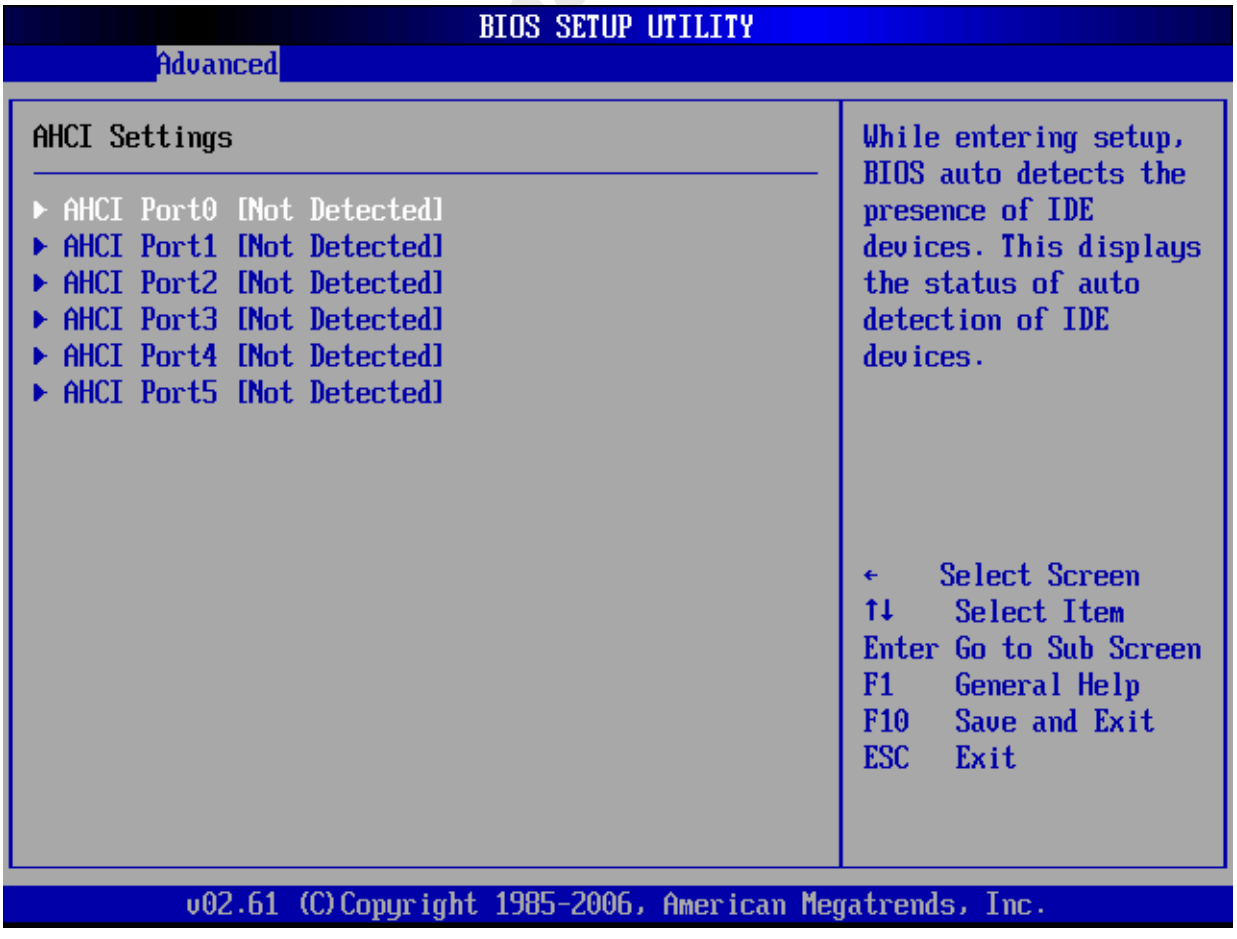
Set this value to allow Suspend to RAM (STR) support. The Optimal and Fail-Safe default setting is Disabled.

Option	Description
Disabled	This setting prevents the system to save information to main memory when in a low power state. This is the default setting.
Enabled	This setting causes the system to enter a low power state instead of being completely shut off. This allows the computer system to boot up in a few seconds. Suspend to RAM (STR) is a technology that is closely associated with the S3 state of the ACPI (Advanced Configuration and Power Interface) specification. STR allows a properly configured system to go into a low power state while saving information to main memory about the system's configuration, open applications, and active files. While in the low power (STR) state, memory remains powered to retain the system information while most other components turn off to conserve energy. Fans are turned off to provide silent operation and to minimize power consumption. Properly configured systems in STR typically can use less than 5 watts.

8.3.6 AHCI Settings

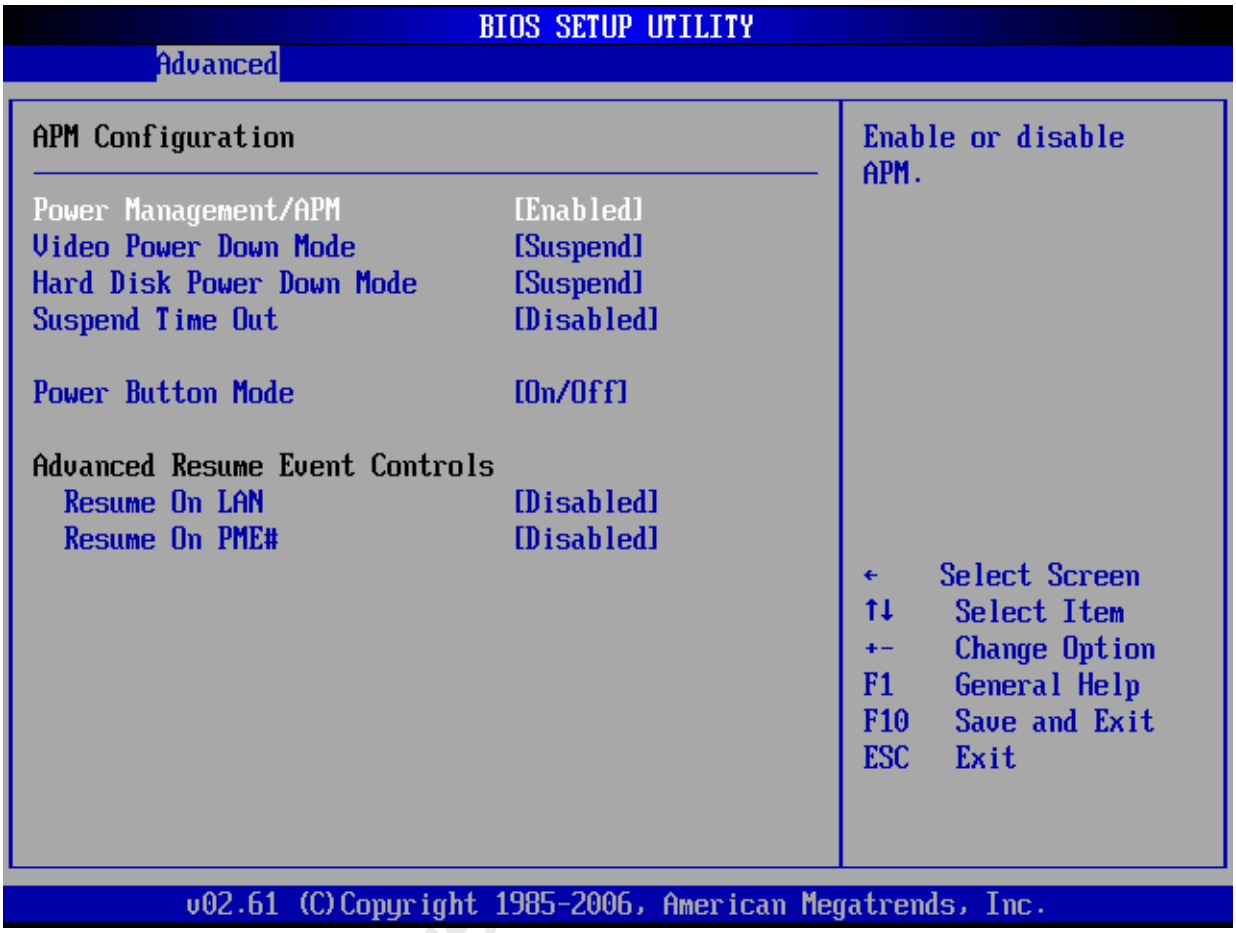
Set this value to allow the Advanced Host Controller Interface. It is an interface specification that allows the SATA controller driver to support advanced features like Native Command Queuing and Hot Plug.

Option	Description
Disabled	This setting prevents the system to use its AHCI features after boot.
Enabled	This setting causes the system to enable its AHCI features after boot to detect the presence of IDE devices.



8.3.7 APM Configuration

Select the Power tab from the setup screen to enter the Power Management BIOS Setup screen. You can display a Power Management BIOS Setup option by highlighting it using the <Arrow> keys. All Power Management BIOS Setup options are described in this section.



NOTE: The Power Management Setup screen is not displayed when Advanced Power Management (APM) is not supported. The Power Setup screen can vary for different motherboards.

Power Management/APM

Set this value to allow Power Management/APM support. The Optimal and Fail-Safe default setting is Enabled.

Option	Description
Disabled	Set this value to prevent the chipset power management and APM (Advanced Power Management) features.
Enabled	Set this value to allow the chipset power management and APM (Advanced Power Management) features. This is the default setting.

Video Power Down Mode

This option specifies the Power State that the video subsystem enters when the BIOS places it in a power saving state after the specified period of display inactivity has expired. The Optimal and Fail-Safe setting is Suspend.

Option	Description
Disabled	This setting prevents the BIOS from initiating any power saving modes concerned with the video display or monitor.
Standby	This option places the monitor into standby mode after the specified period of display inactivity has expired. This means the monitor is not off. The screen will appear blacked out. The standards do not cite specific power ratings because they vary from monitor to monitor.
Suspend	This option places the monitor into suspend mode after the specified period of display inactivity has expired. This means the monitor is not off. The screen will appear blacked out. The standards do not cite specific power ratings because they vary from monitor to monitor, but this setting use less power than Standby mode. This is the default setting.

Hard Disk Drive Power Down Mode

This option specifies the power conserving state that the hard disk drive enters after the specified period of hard drive inactivity has expired. The Optimal and Fail-Safe setting is Suspend.

Option	Description
Disabled	This setting prevents hard disk drive power down mode.
Standby	This option stops the hard disk drives from spinning during a system standby.
Suspend	This option cuts the power to the hard disk drives during a system suspend. This is the default setting.

Suspend Time Out (Minute)

This option specifies the length of time the system waits before it enters suspend mode. The Optimal and Fail-Safe default setting is Disabled.

Option	Description
Disabled	This setting prevents the system from entering suspend mode. This is the default setting.
1Min	Set this value to allow the computer system to enter suspend mode after being inactive for 1 minute.
5Min	Set this value to allow the computer system to enter suspend mode after being inactive for 5 minutes.
10Min	Set this value to allow the computer system to enter suspend mode after being inactive for 10 inutes.

Power Button Mode

This option specifies how the externally mounted power button on the front of the computer chassis is used. The Optimal and Fail-Safe default setting is On/Off.

Option	Description
On/Off	Pushing the power button turns the computer on or off. This is the default setting. This is the default setting.
Standby	Pushing the power button places the computer in Standby mode
Suspend	Pushing the power button places the computer in Suspend mode or Full On power mode.

8.3.8 Event Log Configuration

View Event Log

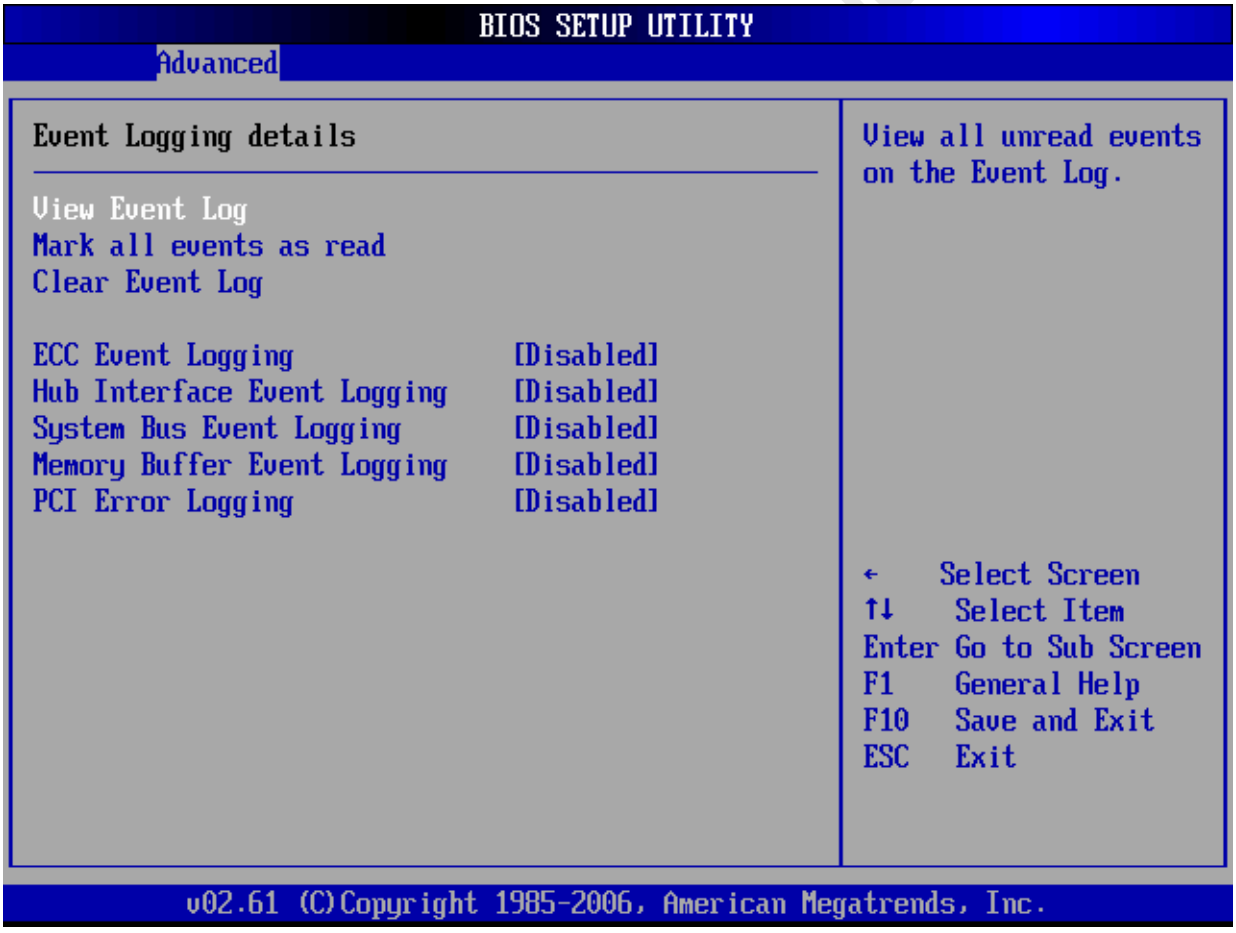
Displays a window with the view of all unread events on the event log. Errors and warnings during boot up of the BIOS will be logged in the event log.

Mark all events as read

Option	Description
Ok	Displays a window with the question “Mark all Events as read now?”.
Cancel	Cancels the action.

Clear Event Log

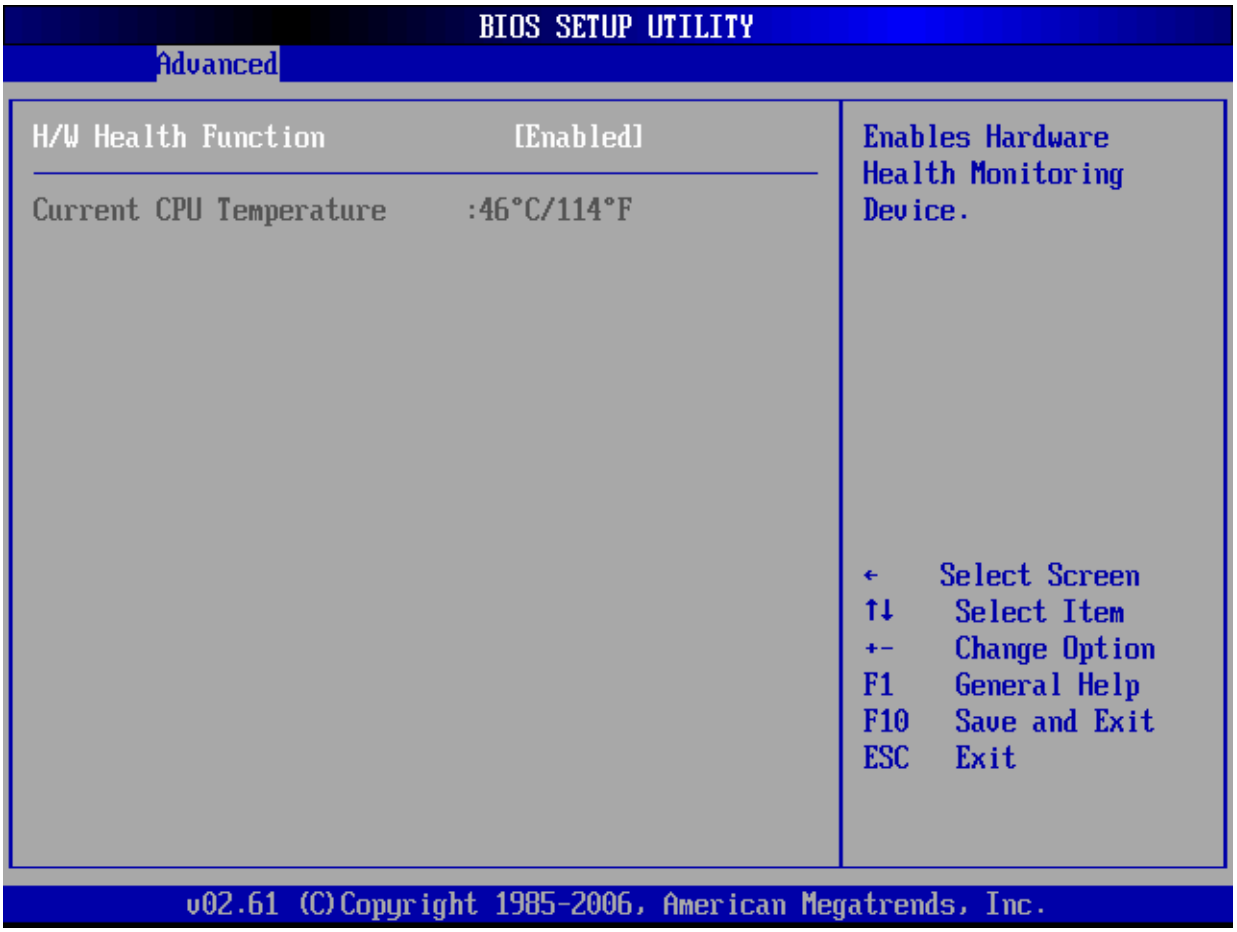
Option	Description
Ok	Displays a window with the question “Clear Event Log now?”.
Cancel	Cancels the action.



8.3.9 Hardware Health Configuration

This option displays the current status of all of the monitored hardware devices/components such as CPU voltages, temperatures and fan speeds.

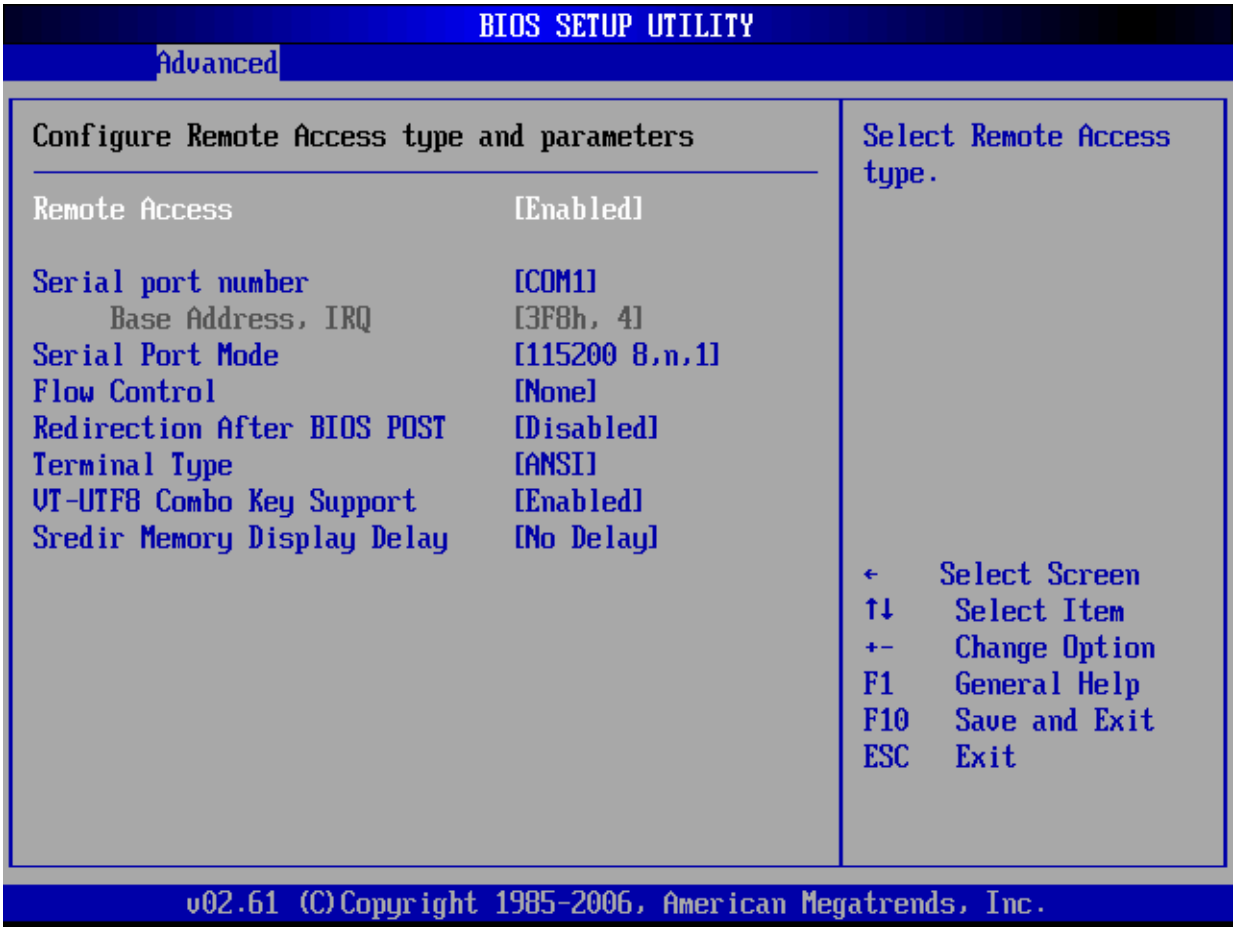
Option	Description
Enabled	Enables Hardware Health Monitoring Devices.
Disabled	Disables Hardware Health Monitoring Devices.



8.3.10 Remote Access Configuration

Remote Access Configuration

You can use this screen to select options for the Remote Access Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



Remote Access

You can disable or enable the BIOS remote access feature here.

Option	Description
Disabled	Set this value to prevent the BIOS from using Remote Access.
Serial	Set the value for this option to *Serial* to allow the system to use the remote access feature. Theremote access feature requires a dedicated serial port connection.

Serial Port Number

Select the serial port you want to use for console redirection. You can set the value for this option to either *COM1* or *COM2*.

Option	Description
COM1	Set this value to allow the system to use COM1 (Communication port1) for the remote access interface.
COM2	Set this value to allow the system to use COM2 (Communication port2) for the remote access interface.

Serial Port Mode

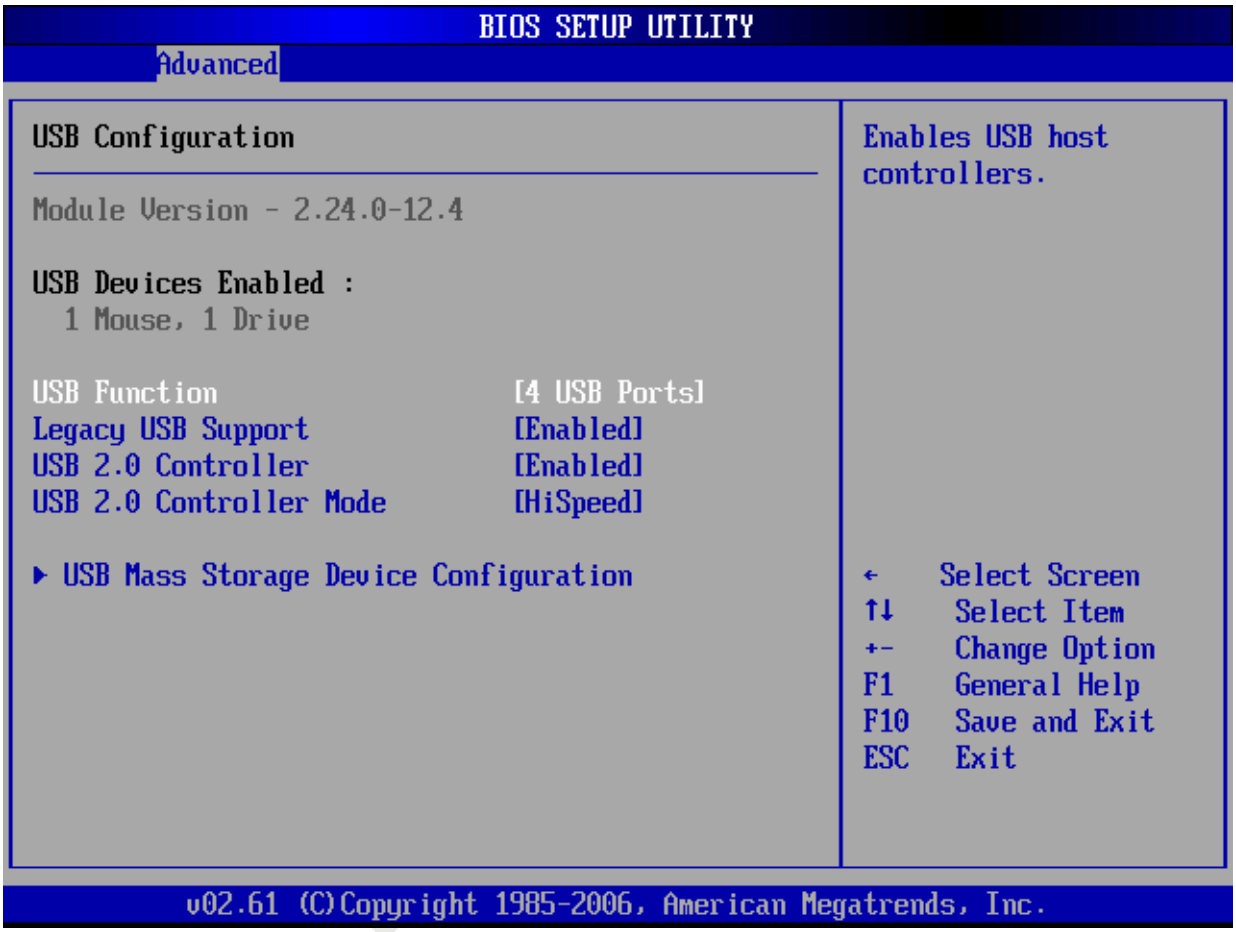
Select the baud rate you want the serial port to use for console redirection.

Option	Description
115200 8,n,1	Set this value to allow you to select 115200 as the baud rate (transmitted bits per second) of the serial port.
57600 8,n,1	Set this value to allow you to select 57600 as the baud rate (transmitted bits per second) of the serial port.
19200 8,n,1	Set this value to allow you to select 19200 as the baud rate (transmitted bits per second) of the serial port.

8.3.11 USB Configuration

USB Configuration

You can use this screen to select options for the USB Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



USB Function

Set this value to allow the system to enable or disable the onboard USB ports. The Optimal and Fail-Safe default setting is Enabled.

Option	Description
Disabled	This setting makes the onboard USB ports unavailable.
Enabled	This setting allows the use of the USB ports. This is the default setting.

Legacy USB Support

Legacy USB Support refers to the USB mouse and USB keyboard support. Normally if this option is not enabled, any attached USB mouse or USB keyboard will not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there is no USB drivers loaded on the system. Set this value to enable or disable the Legacy USB Support. The Optimal and Fail-Safe default setting is Disabled.

Option	Description
Disabled	Set this value to prevent the use of any USB device in DOS or during system boot. This is the default setting.
Enabled	Set this value to allow the use of USB devices during boot and while using DOS.
Auto	This option auto detects USB Keyboards or Mice and if found, allows them to be utilized during boot and while using DOS.

USB Zip Emulation

USB Zip Emulation refers the system being able to boot to a USB Zip drive. Normally if this option is not enabled, any attached USB Zip drive will not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB Zip drive can boot the system even when there is no USB drivers loaded on the system. Set this value to allow the system to select the Emulation type for a USB ZIP drive.

Option	Description
Auto	Set this value to allow the system to automatically detect a USB Zip drive emulation type.
Floppy	Set this value to allow the system to select floppy emulation type.
Hard disk	Set this value to allow the system to select hard disk drive emulation type.

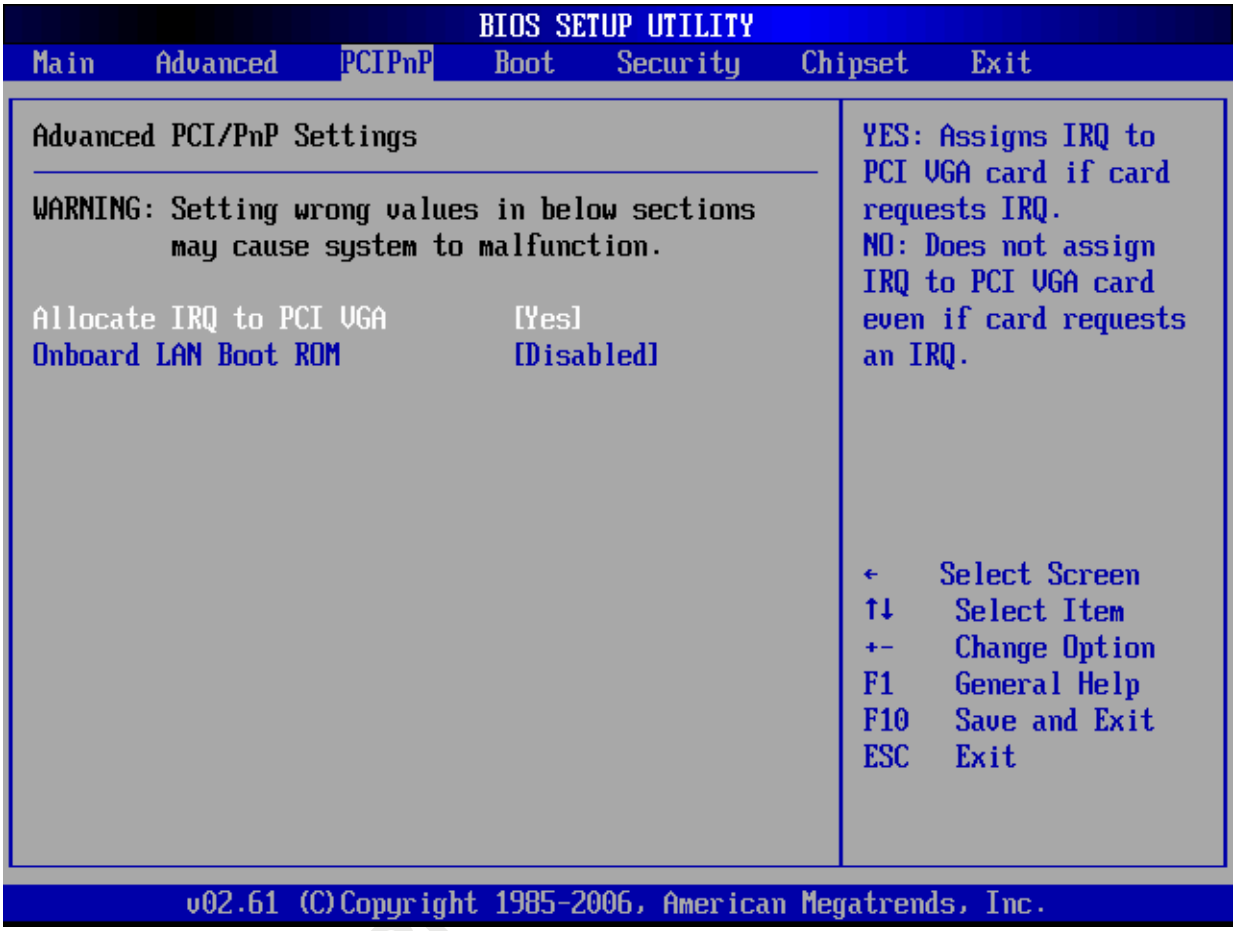
USB Beep Message

Set this value to allow the system to enable or disable generating a beep during USB devices enumeration.

Option	Description
Disabled	Set this value to allow the system to disable beep generation during USB devices emulation.
Enabled	Set this value to allow the system to enable beep generation during USB devices emulation.

8.4 PCI/PnP Setup

Select the PCI/PnP tab from the setup screen to enter the Plug and Play BIOS Setup screen. You can display a Plug and Play BIOS Setup option by highlighting it using the <Arrow> keys. All Plug and Play BIOS Setup options are described in this section. The Plug and Play BIOS Setup screen is shown below.



Allocate IRQ to VGA

Set this value to allow or restrict the system from giving the VGA adapter card an interrupt address. The Optimal and Fail-Safe default setting is Yes.

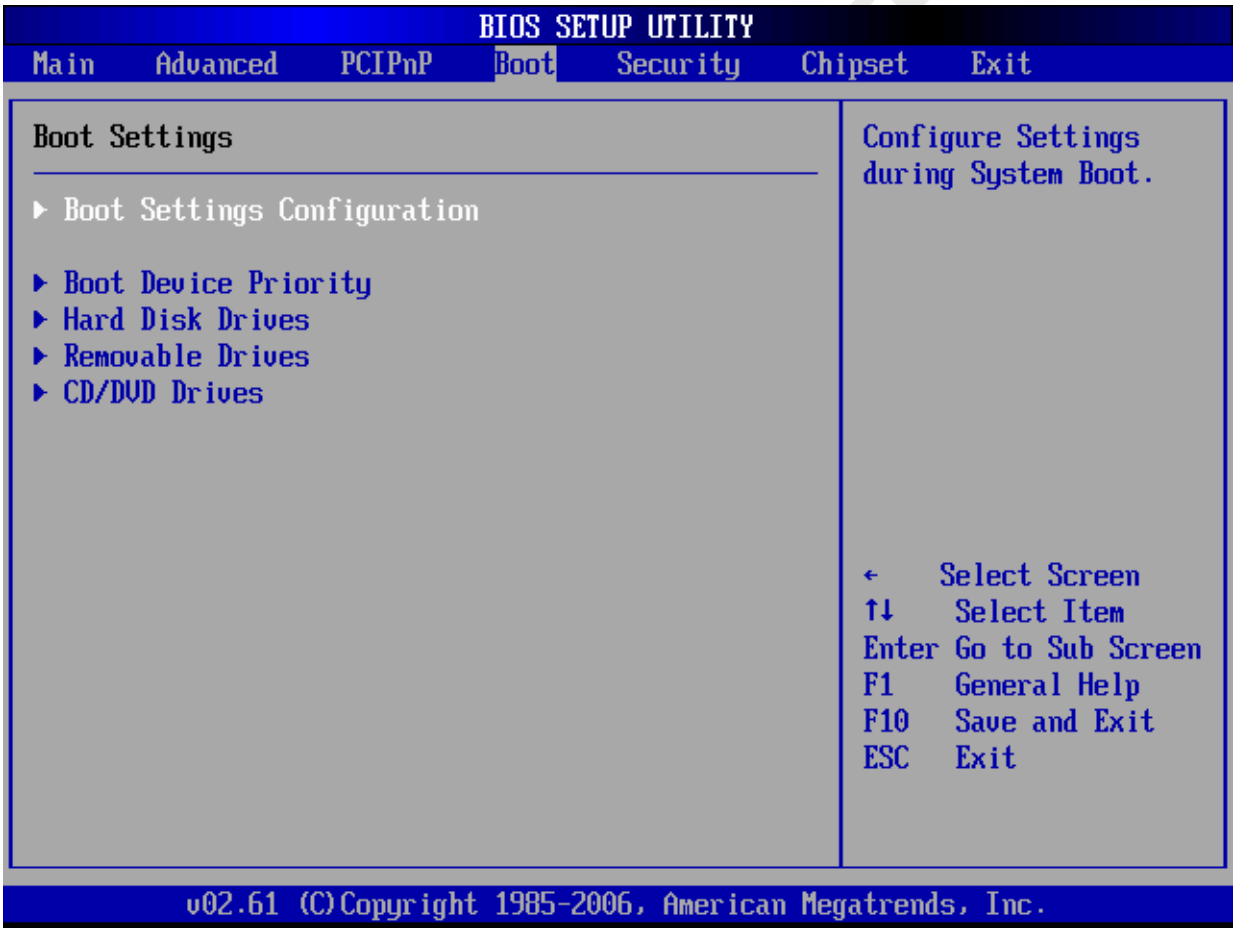
Option	Description
Yes	Set this value to allow the allocation of an IRQ to a VGA adapter card that uses the PCI local bus. This is the default setting.
No	Set this value to prevent the allocation of an IRQ to a VGA adapter card that uses the PCI local bus.

8.5 Boot Setup

Select the Boot tab from the setup screen to enter the Boot BIOS Setup screen. You can select any of the items in the left frame of the screen, such as Boot Device Priority, to go to the sub menu for that item. You can display an Boot BIOS Setup option by highlighting it using the <Arrow> keys. All Boot Setup options are described in this section. Select an item on the Boot Setup screen to access the sub menu for:

- Boot Device Priority
- Hard disk drives
- Removable Devices
- ATAPI CD-ROM Drives

The Boot Setup screen is shown below:



8.6 Security Setup

8.6.1 Password Support

Two Levels of Password Protection

provides both a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first.

The system can be configured so that all users must enter a password every time the system boots or when Setup is executed, using either or either the Supervisor password or User password.

The Supervisor and User passwords activate two different levels of password security. If you select password support, you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed. Make sure you write it down. If you forget it, you must drain NVRAM and reconfigure.

Remember the Password

Keep a record of the new password when the password is changed. If you forget the password, you must erase the system configuration information in NVRAM. See (Deleting a Password) for information about erasing system configuration information.

Select Security Setup from the Setup main BIOS setup menu. All Security Setup options, such as password protection and virus protection, are described in this section. To access the sub menu for the following items, select the item and press <Enter>:

• Change Supervisor Password

• Change User Password

• Clear User Password

The Security Setup screen is shown below. The sub menus are documented on the following pages.

Supervisor Password

Indicates whether a supervisor password has been set. If the password has been installed, Installed displays. If not, Not Installed displays.

User Password

Indicates whether a user password has been set. If the password has been installed, Installed displays. If not, Not Installed displays.

Change Supervisor Password

Select this option and press <Enter> to access the sub menu. You can use the sub menu to change the supervisor password.

Change User Password

Select this option and press <Enter> to access the sub menu. You can use the sub menu to change the user password.

Clear User Password

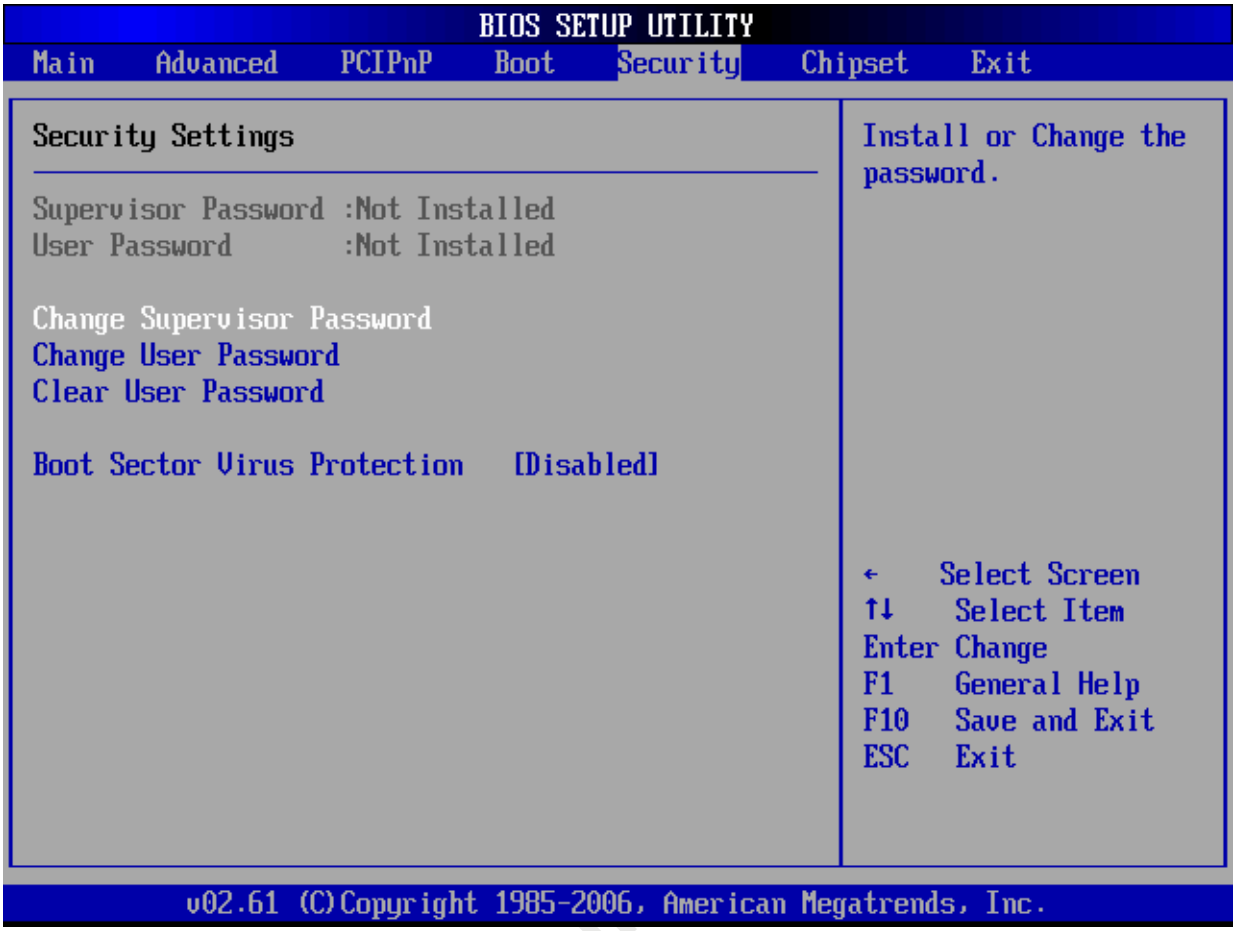
Select this option and press <Enter> to access the sub menu. You can use the sub menu to clear the user password.

Boot Sector Virus Protection

This option is near the bottom of the Security Setup screen. The Optimal and Fail-Safe default setting is Disabled

Option	Description
Disabled	Set this value to prevent the Boot Sector Virus Protection. This is the default setting.
Enabled	Select Enabled to enable boot sector protection. displays a warning when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive. If enabled, the following appears when a write is attempted to the boot sector. You may have to type N several times to prevent the boot sector write. Boot Sector Write! Possible VIRUS: Continue (Y/N)? _ The following appears after any attempt to format any cylinder, head, or sector of any hard disk drive via the BIOS INT 13 Hard disk drive Service: Format!!! Possible VIRUS: Continue (Y/N)? _

8.6.2 Change Supervisor Password



Select Change Supervisor Password from the Security Setup menu and press <Enter>.

Enter New Password:

appears. Type the password and press <Enter>. The screen does not display the characters entered. Retype the password as prompted and press <Enter>. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after completes.

Change User Password

Select Change User Password from the Security Setup menu and press <Enter>.

Enter New Password:

appears. Type the password and press <Enter>. The screen does not display the characters entered. Retype the password as prompted and press <Enter>. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after completes.

Clear User Password

Select Clear User Password from the Security Setup menu and press <Enter>.

Clear New Password

[Ok] [Cancel]

appears. Type the password and press <Enter>. The screen does not display the characters entered. Retype the password as prompted and press <Enter>. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after completes.

8.7 Chipset Setup

Select the Chipset tab from the setup screen to enter the Chipset BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. You can display a Chipset BIOS Setup option by highlighting it using the <Arrow> keys. All Chipset BIOS Setup options are described in this section. The Chipset BIOS Setup screen is shown below.

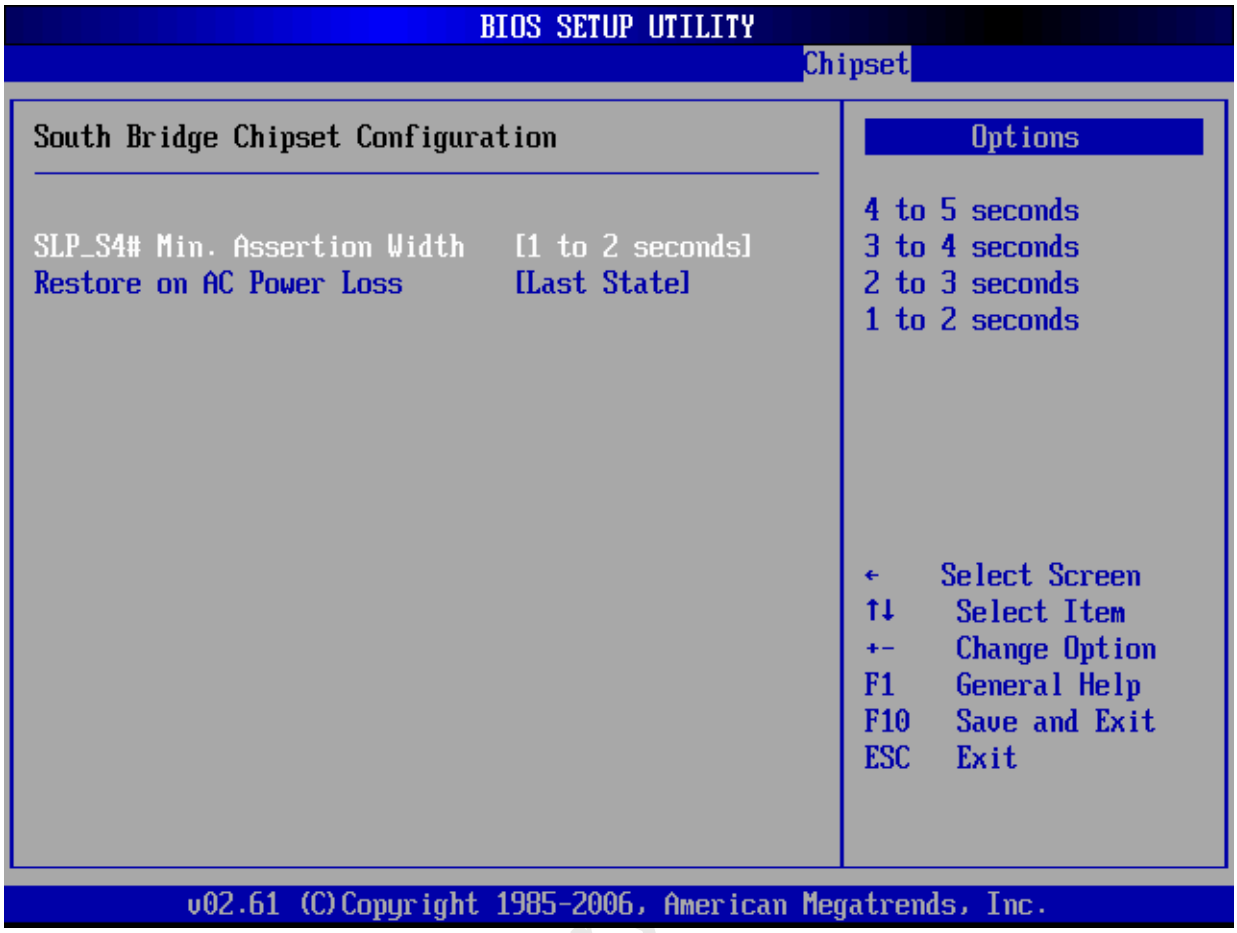
CPU Configuration

You can use this screen to select options for the CPU Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option.

NOTE: The CPU Configuration setup screen varies depending on the installed processor.

8.7.1 South Bridge Configuration

You can use this screen to select options for the South Bridge Configuration. South Bridge is a chipset on the motherboard that controls the basic I/O functions, USB ports, audio functions, modem functions, IDE channels, and PCI slots. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option.

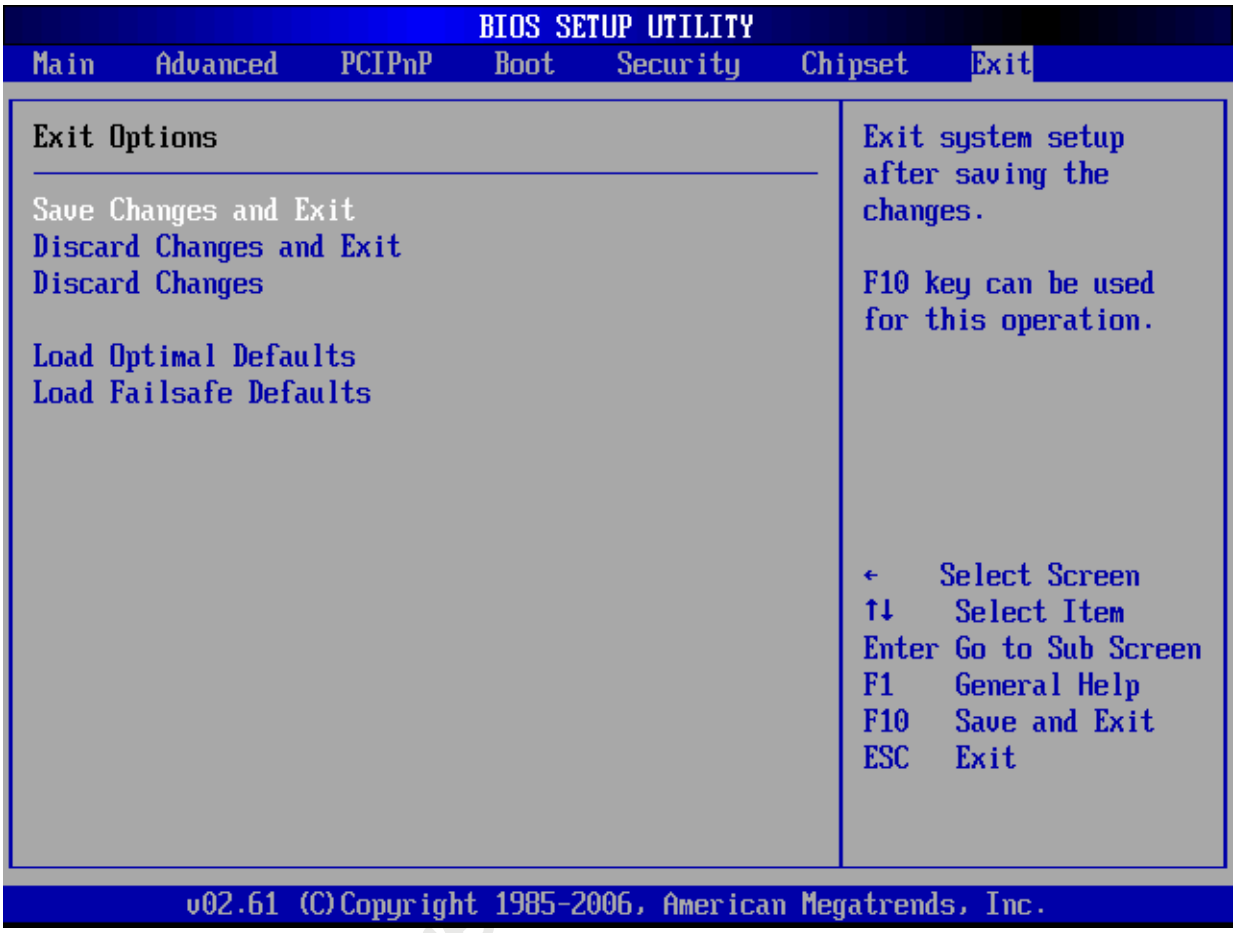


NOTE:

The South Bridge Configuration setup screen varies depending on the supported South Bridge chipset.

8.8 Exit Menu

Select the *Exit* tab from the setup screen to enter the Exit BIOS Setup screen. You can display an Exit BIOS Setup option by highlighting it using the <Arrow> keys. All Exit BIOS Setup options are described in this section. The Exit BIOS Setup screen is shown below.



Exit Saving Changes

When you have completed the system configuration changes, select this option to leave Setup and reboot the computer so the new system configuration parameters can take effect. Select Exit Saving Changes from the Exit menu and press <Enter>.

Save Configuration Changes and Exit Now?

[Ok] [Cancel]

appears in the window. Select Ok to save changes and exit.

Exit Discarding Changes

Select this option to quit Setup without making any permanent changes to the system configuration. Select Exit Discarding Changes from the Exit menu and press <Enter>.

Discard Changes and Exit Setup Now?

[Ok] [Cancel]

appears in the window. Select *Ok* to discard changes and exit.

Load Optimal Defaults

Automatically sets all Setup options to a complete set of default settings when you Select this option. The Optimal settings are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Optimal Setup options if your computer is experiencing system configuration problems.

Select Load Optimal Defaults from the Exit menu and press <Enter>.

Select *Ok* to load optimal defaults.

Load Fail-Safe Defaults

Automatically sets all Setup options to a complete set of default settings when you Select this option. The Fail-Safe settings are designed for maximum system stability, but not maximum performance. Select the Fail-Safe Setup options if your computer is experiencing system configuration problems.

Select Load Fail-Safe Defaults from the Exit menu and press <Enter>.

Load Fail-Safe Defaults?

[Ok] [Cancel]

appears in the window. Select Ok to load Fail-Safe defaults.

Discard Changes

Select Discard Changes from the Exit menu and press <Enter>.

Select *Ok* to discard changes.

8.9 AMIBIOS™ Checkpoints and Beep Codes

This section of this document lists checkpoints and beep codes generated by AMIBIOS. The checkpoints defined in this document are inherent to the AMIBIOS generic core, and do not include any chipset or board specific checkpoint definitions.

8.9.1 Checkpoints and Beep Codes Definition

A checkpoint is either a byte or word value output to I/O port 80h. The BIOS outputs checkpoints throughout bootblock and Power-On Self Test (POST) to indicate the task the system is currently executing. Checkpoints are very useful in aiding software developers or technicians in debugging problems that occur during the pre-boot process.

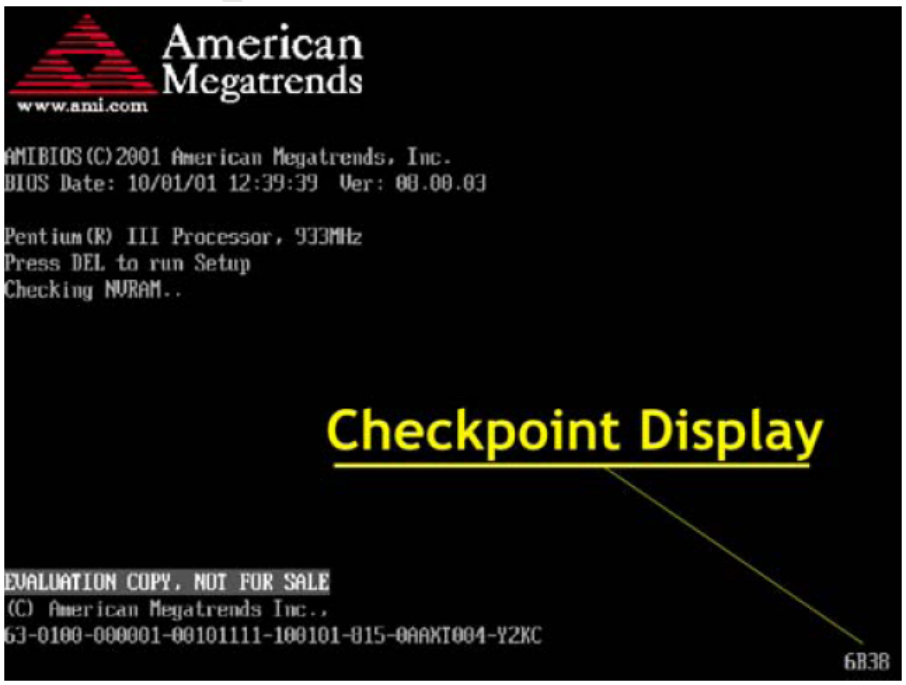
Beep codes are used by the BIOS to indicate a serious or fatal error to the end user. Beep codes are used when an error occurs before the system video has been initialized. Beep codes will be generated by the system board speaker, commonly referred to as the “PC speaker.”

8.9.2 Viewing BIOS Checkpoints

Viewing all checkpoints generated by the BIOS requires a checkpoint card, also referred to as a “POST Card” or “POST Diagnostic Card”. These are ISA or PCI add-in cards that show the value of I/O port 80h on a LED display. Checkpoint cards are available through a variety of computer mail-order outlets.

Some computers using AMIBIOS display checkpoints in the bottom right corner of the screen during POST. This display method is limited, since it only displays checkpoints that occur after the video card has been activated.

Keep in mind that not all computers using AMIBIOS enable this feature. In most cases, a checkpoint card is the best tool for viewing AMIBIOS checkpoints.



8.10 Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS:

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs from add-in PCI devices.

Checkpoint	Description
Before D0	If boot block debugger is enabled, CPU cache-as-RAM functionality is enabled at this point. Stack will be enabled from this point.
D0	Early Boot Strap Processor (BSP) initialization like microcode update, frequency and other CPU critical initialization. Early chipset initialization is done.
D1	Early super I/O initialization is done including RTC and keyboard controller. Serial port is enabled at this point if needed for debugging. NMI is disabled. Perform keyboard controller BAT test. Save power-on CPUID value in scratch CMOS. Go to flat mode with 4GB limit and GA20 enabled.
D2	Verify the boot block checksum. System will hang here if checksum is bad.
D3	Disable CACHE before memory detection. Execute full memory sizing module. If memory sizing module not executed, start memory refresh and do memory sizing in Boot block code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM. Copies compressed boot block code to memory in right segments. Copies BIOS from ROM to RAM for faster access. Performs main BIOS checksum and updates recovery status accordingly.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. If BIOS recovery is necessary, control flows to checkpoint E0. See *Bootblock Recovery Code Checkpoints* section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See *POST Code Checkpoints* section of document for more information.
DC	System is waking from ACPI S3 state
E1-E8 EC-EE	OEM memory detection/configuration error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.

8.11 Bootblock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS:

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs From add-in PCI devices.

Checkpoint	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.
FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

8.12 POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS preboot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs From add-in PCI devices.

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
07	Fixes CPU POST interface calling pointer.
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache - Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor
C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
20	Relocate System Management Interrupt vector for all CPU in the system.
24	Uncompress and initialize any platform specific BIOS modules. GPNV is
	initialized at this checkpoint.
2A	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.

Checkpoint	Description
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information. USB controllers are initialized at this point.
39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, ... etc.) successfully installed in the system and update the BDA, EBDA...etc.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory. Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed / requested. Check boot password if installed.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disable NMI as selected
90	Initialization of system management interrupt by invoking all handlers. *Please note this checkpoint comes right after checkpoint 20h*
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module. Display boot option popup menu.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector.
AB	Prepare BBS for Int 19 boot. Init MP tables.
AC	End of POST initialization of chipset registers. De-initializes the ADM module.
B1	Save system context for ACPI. Prepare CPU for OS boot including final MTRR values.
00	Passes control to OS Loader (typically INT19h).

8.13 OEM POST Error Checkpoints

Checkpoints from the range 61h to 70h are reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.

8.14 DIM Code Checkpoints

The Device Initialization Manager (DIM) gets control at various times during BIOS POST to initialize different system busses. The following table describes the main checkpoints where the DIM module is accessed:

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs from add-in PCI devices.

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI-PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.

While control is in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two fields. The details of the high byte of these checkpoints are as follows:

HIGH BYTE XY

The upper nibble 'X' indicates the function number that is being executed. 'X' can be from 0 to 7.

0 = func#0, disable all devices on the BUS concerned.
1 = func#1, static devices initialization on the BUS concerned.
2 = func#2, output device initialization on the BUS concerned.
3 = func#3, input device initialization on the BUS concerned.
4 = func#4, IPL device initialization on the BUS concerned.
5 = func#5, general device initialization on the BUS concerned.
6 = func#6, error reporting for the BUS concerned.
7 = func#7, add-on ROM initialization for all BUSes.
8 = func#8, BBS ROM initialization for all BUSes.

The lower nibble 'Y' indicates the BUS on which the different routines are being executed. 'Y' can be from 0 to 5.

0 = Generic DIM (Device Initialization Manager).
1 = On-board System devices.
2 = ISA devices.
3 = EISA devices.
4 = ISA PnP devices.
5 = PCI devices.

8.15 ACPI Runtime Checkpoints

ACPI checkpoints are displayed when an ACPI capable operating system either enters or leaves a sleep state. The following table describes the type of checkpoints that may occur during ACPI sleep or wake events:

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs from add-in PCI devices.

Checkpoint	Description
AC	First ASL check point. Indicates the system is running in ACPI mode.
AA	System is running in APIC mode.
01, 02, 03, 04, 05	Entering sleep state S1, S2, S3, S4, or S5.
10, 20, 30, 40, 50	Waking from sleep state S1, S2, S3, S4, or S5.

8.16 Boot Block Beep Codes

Number of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
3	Base Memory error
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

8.17 POST BIOS Beep Codes

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
3	Base memory read/write test error
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

8.17.1Troubleshooting POST BIOS Beep Codes

Number of Beeps	Troubleshooting Action
1, 2 or 3	Reseat the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. • If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. • If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning card.
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

This page intentionally left blank.

Appendix A: USB Client Port

A.1 Description

The Express-IW400 includes a USB client port that offers access to a RS-232 port comming off the Intel® 3100 chipset.

In headless applications without a Super I/O chip, this is the only way to get a “console port” to the Express-IW400.

The console port can be used to get BIOS setup access or to get a root terminal under Windows®.

The provided USB driver should be loaded under the host PC for console access, not on the Express-IW400.