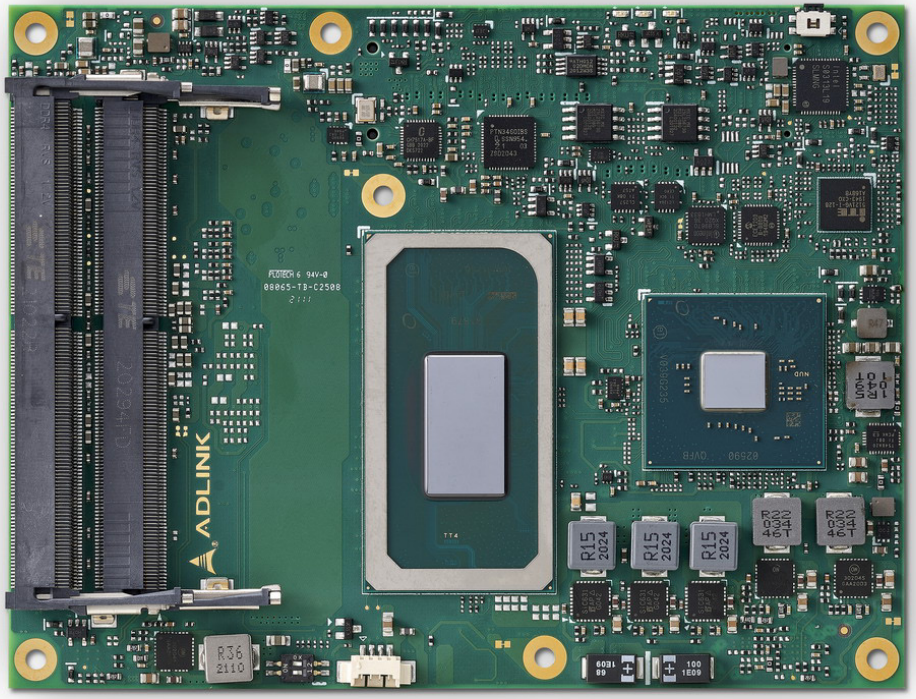
Express-TL

User's Guide



COM Express®

Revision:	Rev. 1.5
Date:	2025-05-29
Part Number:	50M-72138-1050

ADLINK
LEADING EDGE COMPUTING

Revision History

Revision	Description	Date	Author
1.0	Initial release	2021-12-16	JC
1.1	Pin definitions and I/O, LED specifications updated	2022-03-16	CC
1.2	Operating temperature specifications updated	2022-08-10	CC
1.3	BIOS tables added	2024-06-07	AL
1.4	Block diagram updated	2024-11-07	AL
1.5	Pinout and signal descriptions updated	2025-05-29	AL

Preface

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California Proposition 65 Warning: This product can expose you to chemicals including acrylamide, arsenic, benzene, cadmium, Tris(1,3-dichloro-2-propyl)phosphate (TDCPP), 1,4-Dioxane, formaldehyde, lead, DEHP, styrene, DINP, BBP, PVC, and vinyl materials, which are known to the State of California to cause cancer, and acrylamide, benzene, cadmium, lead, mercury, phthalates, toluene, DEHP, DIDP, DnHP, DBP, BBP, PVC, and vinyl materials, which are known to the State of California to cause birth defects or other reproductive harm. For more information go to www.P65Warnings.ca.gov.

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Safety Instructions

For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

Read these safety instructions carefully.

- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

Conventions

The following conventions may be used throughout this manual, denoting special levels of information

Note: This information adds clarity or specifics to text and illustrations.

Caution: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

Warning: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

Getting Service

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1. Introduction

The Express-TL is a COM Express® COM.0 R3.0 Basic Size Type 6 module based on the Intel® Xeon®, 11th Generation Intel® Core™, and Intel® Celeron® 6000 processors (formerly "Tiger Lake-H") with up to 8 cores (16 threads) at maximum 4.7GHz boost frequency, features a brand new Intel® Iris® Xe high performance graphics core, and supports AVX512-VNNI (Vector Neural Network Instructions) that almost triples AI inferencing performance. Typical industries in need of such high performance, low power characteristics are industrial automation and control, medical ultra sound, image processing and analysis, high speed video encoding and streaming, predictive traffic analysis, and multi camera-based AI.

The Express-TL has up to four SODIMM sockets supporting up to 128GB (4x 32GB) of DDR4 memory. Memory frequency is up to 3200 MT/s dependent on configuration. Modules equipped with the Intel® Xeon® processor and Intel® RM590E Chipset support both ECC and non-ECC SODIMMs.

The integrated Intel® Iris® Xe Graphics (Gen12) includes features such as OpenGL 4.5, DirectX 12, OpenCL 2.1/2.0/1.2, Intel® Clear Video HD Technology, and DirectX Video Acceleration (DXVA) support for full H.265/HEVC 10-bit, VP9 hardware codecs. In addition, High Dynamic Range is supported for enhanced picture color and quality, and digital content protection has been upgraded to HDCP 2.3. Graphics outputs include LVDS and three DDI ports supporting HDMI/DVI/DisplayPort and eDP/VGA as a build option, with a maximum of four 4K displays supported. In addition, USB4 that can transfer media and data through single tunnel is a build option supported by project basis in place of DDI 1/2. The Express-TL is specifically designed for customers with high-performance processing graphics requirements who want to outsource the custom core logic of their systems for reduced development time. In addition to the onboard integrated graphics, a multiplexed PCIe x16 Gen4 graphics bus is available for discrete graphics expansion.

Input/output features include up to eight PCIe Gen3 lanes that can be used for NVMe SSD, allowing application access to the highest speed storage solutions, as well as a single onboard 2.5Gigabit Ethernet port with optional Time Sensitive Network (TSN), four USB 3.2 Gen2 ports, four USB 2.0 ports, and two SATA 6 Gb/s ports. Optional onboard PCIe Gen3 NVMe SSD is offered by project basis. Support is provided for SMBus and I^2C. The module is equipped with SPI AMI EFI BIOS with CMOS backup, supporting embedded features such as remote console, hardware monitor, and watchdog timer.

2. Specifications

2.1. Core System

CPU

11th Gen Intel® Core™, Intel® Xeon®, and Intel® Celeron® Processor (formerly "Tiger Lake-H")

- Intel® Xeon® W-11865MRE, 2.6(4.7) GHz, 24MB, 45W(35W cTDP), 8C/16T
- Intel® Xeon® W-11865MLE, 1.5(4.5) GHz, 24MB, 25W, 8C/16T
- Intel® Core™ i7-11850HE, 2.6(4.7) GHz, 24MB, 45W(35W cTDP), 8C/16T
- Intel® Xeon® W-11555MRE, 2.6(4.5) GHz, 12MB, 45W(35W cTDP), 6C/12T
- Intel® Xeon® W-11555MLE, 1.9(4.4) GHz, 12MB, 25W, 6C/12T
- Intel® Core™ i5-11500HE, 2.6(4.5) GHz, 12MB, 45W(35W cTDP), 6C/12T
- Intel® Xeon® W-11155MRE, 2.4(4.4) GHz, 8MB, 45W(35W cTDP), 4C/8T
- Intel® Xeon® W-11155MLE, 1.8(3.1) GHz, 8MB, 25W, 4C/8T
- Intel® Core™ i3-11100HE, 2.4(4.4) GHz, 8MB, 45W(35W cTDP), 4C/8T
- Intel® Celeron® 6600HE, 2.6GHz, 8MB, 35W, 2C/2T

Supporting: Intel® VT, Intel® VT-d, Intel® TXT, Intel® SSE4.2, Intel® HT Technology, Intel® 64 Architecture, Execute Disable Bit, Intel® Turbo Boost Technology 2.0, Intel® AVX-512, Intel® AVX2, Intel® AES-NI, PCLMULQDQ Instruction, Intel® Device Protection Technology with Intel® Secure Key, Intel® TSX-NI (availability of features may vary between processor SKUs)

Memory

Up to 128GB DDR4 in four SODIMM sockets (two on top, two on bottom), maximum 32GB per socket, maximum 3200 MT/s.

Xeon® processors paired with RM590E Chipset can support both of ECC and non-ECC memory. Other processor/chipset combinations support non-ECC memory. Fourth SODIMM on bottom side is supported by build option.

Note: Top SODIMM sockets must be populated first. Make sure to check that the bottom-side specs are suitable for your application purposes.

Chipset

Intel® RM590E, QM580E and HM570E

Embedded BIOS

AMI Aptio V UEFI with CMOS backup in 32 (or 16, TBC) MB SPI BIOS, dual BIOS by build option

2.2. Video

GPU

Intel® UHD Graphics integrated, up to 32 execution units

Feature Support

- 4 independent and simultaneous combinations of DisplayPort/HDMI/LVDS graphics outputs (4x 4K @60Hz)
- (eDP optional in place of LVDS, VGA optional in place of DDI 3)
- Encode/transcode HD content
- Playback of high-definition content including Blu-ray Disc and Blu-ray Disc 3D content using HDMI (1.4a spec compliant with 3D)
- DirectX Video Acceleration (DXVA) support for accelerated video processing
- HEVC/H.265, H.264, M/JPEG, MPEG2, AV1, WMV9, VP9 HW decode
- HEVC/H.265, H.264, JPEG, VP9 HW encode
- Advanced Scheduler 2.0, 1.0, XPDM support
- DirectX up to 12
- OpenGL up to 4.5 and ES 2.0 support
- OpenCL up to 2.1 support

Note: Availability of features is dependent on the operating system (Windows 10 64-bit, Linux 64-bit).

2.2.1 Display Interface Support

LVDS: Single/dual channel 18/24-bit LVDS through eDP to LVDS IC, supports DE mode and Hsync/Vsync mode.
Max. resolution 1920x1200@60Hz in dual mode. Pixel clock frequency up to 112 MHz. VESA and JEIDA panel data formats supported.

eDP: eDP 1.4b up to 4 lane support, in place of LVDS (BOM option), up to 4096x2304@60Hz bpp with DSC

DDI x3: Digital Display Ports (DDI) support DisplayPort 1.4a, HDMI 2.0b or DVI

VGA: VGA BOM option support in place of DDI 3; max. resolution 1920x1200@60Hz

Note: USB4 is a build option (HW and BIOS) supported by project basis in place of DDI channels. Maximum 2x USB4 by using DDI 1 and DDI 2 channels. USB4 support also requires re-timer and PD on carrier.

2.3. Audio

Intel® HD Audio integrated

Located on carrier Express-BASE6 (ALC886 standard support)

2.4. Expansion Busses

1 PCI Express x16 Gen4: PEG0-15 (configurable to 1 x16, 2 x8 or 1 x8 + 2 x4). Gen4 support dependent on carrier design.

8 PCI Express x1 Gen3: Lanes 0-3 (configurable to 4 x1, 2 x2, 1 x4, 1 x2 + 2 x1) and Lanes 4-7 (configurable to 4 x1, 2 x2, 1 x4, 1 x2 + 2 x1)

Other: SMBus (system), I^2C (user), LPC bus (via eSPI to LPC bridge IC)

2.5. Ethernet

2.5GbE Intel® Ethernet Controller I225 Series (V, IT or LM version)

Supports up to 2.5GbE and 1000/100/10 Mbit/s connections

IT version supports TSN feature on Linux OS, GbE0_SDP available if TSN support enabled

Intel® Core™ and Celeron® processors pair with I225-V, Intel® Xeon® processor pairs with I225-IT by default, other combinations supported by project basis

2.6. Multi I/O and Storage

USB

4x USB 3.2 Gen2 (USB 0,1,2,3), 4x USB 2.0/1.1 (USB 4,5,6,7)

SuperSpeedPlus, SuperSpeed, High-Speed, Full-Speed and Low-Speed USB signaling

Note: Carrier board must be designed for Gen2 operation.
USB 0,1,2,3 are backward compatible with USB 2.0/1.1.

SATA

4x SATA 6Gb/s (SATA 0,1,2,3)

Note: For SATA 6Gb/s compatibility, it is strongly recommended to use a SATA redriver on the carrier board

GPIO ~~or SD~~

4 GPO and 4 GPI (GPI with interrupt)

On-board Storage

Soldered type PCIe NVMe SSD, available capacities: 60GB/120GB/240GB. Build option support by project basis

Note: For the NVMe SSD build option, DIMM support is limited to 3 slots. Please contact your local ADLINK representative for details.

UART

Two UART interfaces SER0 and SER1 RX/TX on module

Console Redirection via COM 1 or COM 2 selectable in BIOS

Up to 4 serial ports supported by standard BIOS, including Super I/O on carrier board

COM Port	Description	IRQ	Address	Console Redirection Support
COM 1	Supported by module (SER0, A98/A99), via embedded controller	4	0x3F8	Yes
COM 2	Supported by module (SER1, A101/A102), via embedded controller	3	0x2F8	Yes
COM 3	Supported by Super I/O (W83627DHG) on carrier board	5	0x240	Yes
COM 4	Supported by Super I/O (W83627DHG) on carrier board	7	0x248	Yes

Note: SER0, SER1 from SoC HSUART are BOM option support by project basis

2.7. Trusted Platform Module (TPM)

Chipset: Infineon solution

Type: TPM 2.0 (SPI bus based)

2.8. SEMA Board controller

Supports: Voltage/current monitoring, power sequence debug support, AT/ATX mode control, logistics and forensic information, flat panel control, general purpose I^2C, failsafe BIOS (dual BIOS, opt. support), watchdog timer and fan control

2.9. Debug

30-pin flat cable connector for use with DB-30 x86 debug module

Supports embedded controller access, SPI BIOS flashing, internal power rail test points, debug LEDs

2.10. Power

Power Modes: AT and ATX mode (AT mode startup controlled by SEMA Board Controller)

Standard Voltage Input:	ATX: 12V±5% / 5Vsb ±5%	or	AT: 12V±5%
Wide Voltage Input:	ATX: 8.5-20V, 5Vsb ±5%	or	AT: 8.5-20V

Power Management: ACPI 5.0 compliant, Smart Battery support
Power States: C1-C6, S0, S1, S3, S4, S5, S5 ECO mode (Wake-on-USB S3/S4, WoL S3/S4/S5)
ECO Mode support for deep S5 for 5Vsb power saving

Power Consumption
Please contact your ADLINK representative for the document "COM Express Module Power Consumption".

2.11. Mechanical and Environmental

Form Factor and specification

PICMG COM Express Rev 3.0 (COM.0 R3.0), Type 6, Basic size 125 x 95 mm

Operating Temperature

Standard	0°C to 60°C (wide voltage input)	Storage: -20°C to 80°C
Extreme Rugged	-40°C to 85°C (selected SKUs, up to 2933MT/s memory frequency)	Storage: -40°C to 85°C (selected SKUs)

Humidity

5-90% RH operating, non-condensing, 5-95% RH storage (and operating with conformal coating)

Shock and Vibration

IEC 60068-2-64 and IEC-60068-2-27
MIL-STD-202F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D

HALT tested

Thermal Stress, Vibration Stress, Thermal Shock and Combined Test

3. Block Diagram

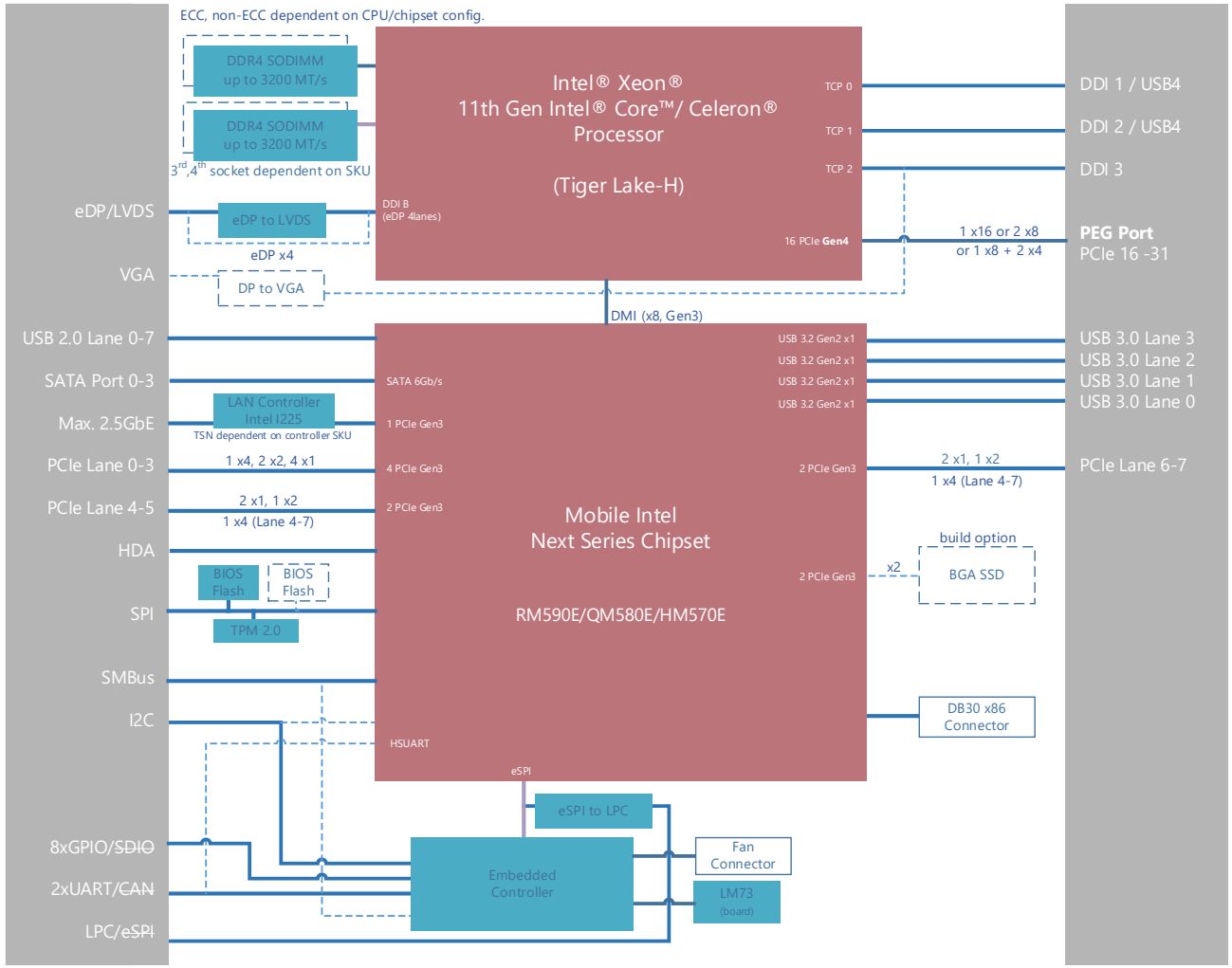


Figure 1 – Module function diagram

4. Pinout and Signal Descriptions

4.1. Pin Summary

The table below is a comprehensible list of all signal pins supported on the dual 220-pin COM Express connectors as defined for Type 6 in the PICMG COM.0 R3.0 specification. Signals described in the specification but not supported on the Express-TL are marked with ~~strike-through.~~

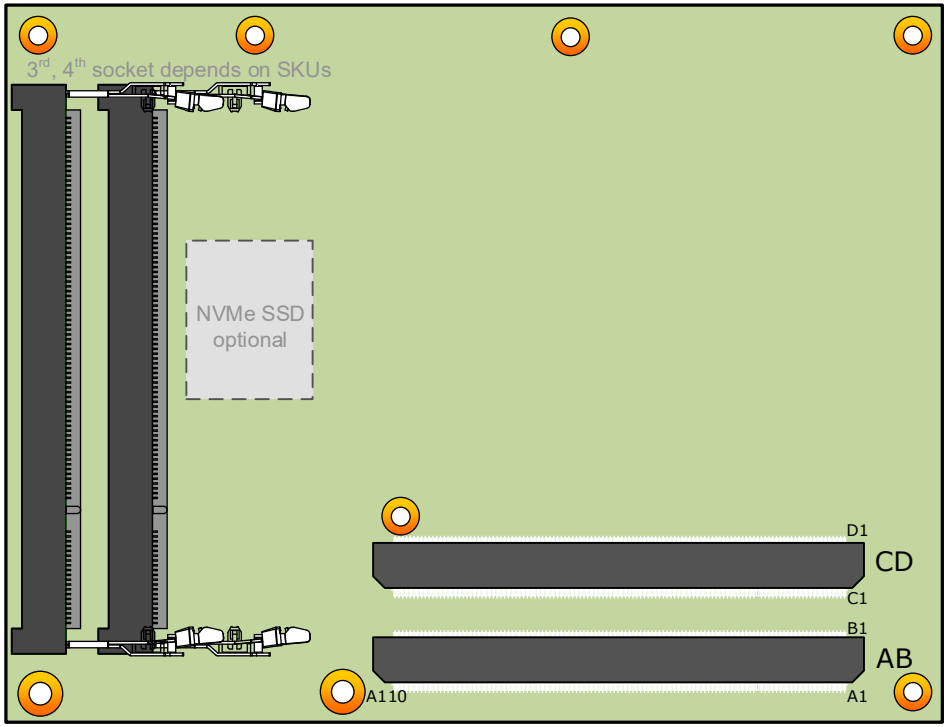


Figure 2 - Module rear side row and pin numbering

Row A			Row B			Row C			Row D	
A1	GND (FIXED)		B1	GND (FIXED)		C1	GND FIXED)		D1	GND FIXED)
A2	GBE0_MDI3-		B2	GBE0_ACT#		C2	GND		D2	GND
A3	GBE0_MDI3+		B3	LPC_FRAME#/~~ESPI_CS0#~~		C3	USB_SSRX0-		D3	USB_SSTX0-
A4	GBE0_LINK100# *		B4	LPC_AD0/~~ESPI_IO_0~~		C4	USB_SSRX0+		D4	USB_SSTX0+
A5	GBE0_LINK1000# *		B5	LPC_AD1/~~ESPI_IO_1~~		C5	GND		D5	GND
A6	GBE0_MDI2-		B6	LPC_AD2/~~ESPI_IO_2~~		C6	USB_SSRX1-		D6	USB_SSTX1-
A7	GBE0_MDI2+		B7	LPC_AD3/~~ESPI_IO_3~~		C7	USB_SSRX1+		D7	USB_SSTX1+
A8	GBE0_LINK#		B8	~~LPC_DRQ0#/ESPI_ALERT0#~~		C8	GND		D8	GND
A9	GBE0_MDI1-		B9	~~LPC_DRQ1#/ESPI_ALERT1#~~		C9	USB_SSRX2-		D9	USB_SSTX2-
A10	GBE0_MDI1+		B10	LPC_CLK/~~ESPI_CK~~		C10	USB_SSRX2+		D10	USB_SSTX2+
A11	GND (FIXED)		B11	GND (FIXED)		C11	GND (FIXED)		D11	GND (FIXED)
A12	GBE0_MDI0-		B12	PWRBTN#		C12	USB_SSRX3-		D12	USB_SSTX3-
A13	GBE0_MDI0+		B13	SMB_CK		C13	USB_SSRX3+		D13	USB_SSTX3+
A14	GBE0_CTREF		B14	SMB_DAT		C14	GND		D14	GND
A15	SUS_S3#		B15	SMB_ALERT#		C15	~~DDI1_PAIR6+~~		D15	DDI1_CTRLCLK_AUX+
A16	SATA0_TX+		B16	SATA1_TX+		C16	~~DDI1_PAIR6-~~		D16	DDI1_CTRLDATA_AUX-
A17	SATA0_TX-		B17	SATA1_TX-		C17	RSVD		D17	RSVD
A18	SUS_S4#		B18	SUS_STAT#/~~ESPI_RESET#~~		C18	RSVD		D18	RSVD
A19	SATA0_RX+		B19	SATA1_RX+		C19	PCIE_RX6+		D19	PCIE_TX6+
A20	SATA0_RX-		B20	SATA1_RX-		C20	PCIE_RX6-		D20	PCIE_TX6-
A21	GND (FIXED)		B21	GND (FIXED)		C21	GND (FIXED)		D21	GND (FIXED)
A22	SATA2_TX+		B22	SATA3_TX+		C22	PCIE_RX7+		D22	PCIE_TX7+
A23	SATA2_TX-		B23	SATA3_TX-		C23	PCIE_RX7-		D23	PCIE_TX7-
A24	SUS_S5#		B24	PWR_OK		C24	DDI1_HPD		D24	RSVD
A25	SATA2_RX+		B25	SATA3_RX+		C25	~~DDI1_PAIR4+~~		D25	GND
A26	SATA2_RX-		B26	SATA3_RX-		C26	~~DDI1_PAIR4-~~		D26	DDI1_PAIR0+
A27	BATLOW#		B27	WDT		C27	RSVD		D27	DDI1_PAIR0-
A28	(S)ATA_ACT#		B28	AC/HDA_SDIN2		C28	RSVD		D28	GND
A29	AC/HDA_SYNC		B29	AC/HDA_SDIN1		C29	~~DDI1_PAIR5+~~		D29	DDI1_PAIR1+
A30	AC/HDA_RST#		B30	AC/HDA_SDIN0		C30	~~DDI1_PAIR5-~~		D30	DDI1_PAIR1-
A31	GND (FIXED)		B31	GND (FIXED)		C31	GND (FIXED)		D31	GND (FIXED)
A32	AC/HDA_BITCLK		B32	SPKR		C32	DDI2_CTRLCLK_AUX+		D32	DDI1_PAIR2+
A33	AC/HDA_SDOUT		B33	I2C_CK		C33	DDI2_CTRLDATA_AUX-		D33	DDI1_PAIR2-
A34	BIOS_DIS0#/~~ESPI_SAFS~~		B34	I2C_DAT		C34	DDI2_DDC_AUX_SEL		D34	DDI1_DDC_AUX_SEL
A35	THRMTRIP#		B35	THRM#		C35	RSVD		D35	RSVD

Row A			Row B			Row C			Row D	
A36	USB6-		B36	USB7-		C36	DDI3_CTRLCLK_AUX+		D36	DDI1_PAIR3+
A37	USB6+		B37	USB7+		C37	DDI3_CTRLDATA_AUX-		D37	DDI1_PAIR3-
A38	USB_6_7_OC#		B38	USB_4_5_OC#		C38	DDI3_DDC_AUX_SEL		D38	GND
A39	USB4-		B39	USB5-		C39	DDI3_PAIR0+		D39	DDI2_PAIR0+
A40	USB4+		B40	USB5+		C40	DDI3_PAIR0-		D40	DDI2_PAIR0-
A41	GND (FIXED)		B41	GND (FIXED)		C41	GND (FIXED)		D41	GND (FIXED)
A42	USB2-		B42	USB3-		C42	DDI3_PAIR1+		D42	DDI2_PAIR1+
A43	USB2+		B43	USB3+		C43	DDI3_PAIR1-		D43	DDI2_PAIR1-
A44	USB_2_3_OC#		B44	USB_0_1_OC#		C44	DDI3_HPD		D44	DDI2_HPD
A45	USB0-		B45	USB1-		C45	RSVD		D45	GND
A46	USB0+		B46	USB1+		C46	DDI3_PAIR2+		D46	DDI2_PAIR2+
A47	VCC_RTC		B47	~~ESPI_EN#~~		C47	DDI3_PAIR2-		D47	DDI2_PAIR2-
A48	RSVD		B48	~~USB0_HOST_PRSNT~~		C48	RSVD		D48	GND
A49	GBE0_SDP		B49	SYS_RESET#		C49	DDI3_PAIR3+		D49	DDI2_PAIR3+
A50	LPC_SERIRQ~~/ESPI_CS1#~~		B50	CB_RESET#		C50	DDI3_PAIR3-		D50	DDI2_PAIR3-
A51	GND (FIXED)		B51	GND (FIXED)		C51	GND (FIXED)		D51	GND (FIXED)
A52	PCIE_TX5+		B52	PCIE_RX5+		C52	PEG_RX0+		D52	PEG_TX0+
A53	PCIE_TX5-		B53	PCIE_RX5-		C53	PEG_RX0-		D53	PEG_TX0-
A54	GPI0		B54	GPO1		C54	TYPE0#		D54	PEG_LANE_RV#
A55	PCIE_TX4+		B55	PCIE_RX4+		C55	PEG_RX1+		D55	PEG_TX1+
A56	PCIE_TX4-		B56	PCIE_RX4-		C56	PEG_RX1-		D56	PEG_TX1-
A57	GND		B57	GPO2		C57	TYPE1#		D57	TYPE2#
A58	PCIE_TX3+		B58	PCIE_RX3+		C58	PEG_RX2+		D58	PEG_TX2+
A59	PCIE_TX3-		B59	PCIE_RX3-		C59	PEG_RX2-		D59	PEG_TX2-
A60	GND (FIXED)		B60	GND (FIXED)		C60	GND (FIXED)		D60	GND (FIXED)
A61	PCIE_TX2+		B61	PCIE_RX2+		C61	PEG_RX3+		D61	PEG_TX3+
A62	PCIE_TX2-		B62	PCIE_RX2-		C62	PEG_RX3-		D62	PEG_TX3-
A63	GPI1		B63	GPO3		C63	RSVD		D63	RSVD
A64	PCIE_TX1+		B64	PCIE_RX1+		C64	RSVD		D64	RSVD
A65	PCIE_TX1-		B65	PCIE_RX1-		C65	PEG_RX4+		D65	PEG_TX4+
A66	GND		B66	WAKE0#		C66	PEG_RX4-		D66	PEG_TX4-
A67	GPI2		B67	WAKE1#		C67	~~RAPID_SHUTDOWN~~		D67	GND
A68	PCIE_TX0+		B68	PCIE_RX0+		C68	PEG_RX5+		D68	PEG_TX5+
A69	PCIE_TX0-		B69	PCIE_RX0-		C69	PEG_RX5-		D69	PEG_TX5-
A70	GND (FIXED)		B70	GND (FIXED)		C70	GND (FIXED)		D70	GND (FIXED)

Row A			Row B			Row C			Row D	
A71	LVDS_A0+ / eDP_TX2+		B71	LVDS_B0+		C71	PEG_RX6+		D71	PEG_TX6+
A72	LVDS_A0- / eDP_TX2-		B72	LVDS_B0-		C72	PEG_RX6-		D72	PEG_TX6-
A73	LVDS_A1+ / eDP_TX1+		B73	LVDS_B1+		C73	GND		D73	GND
A74	LVDS_A1- / eDP_TX1-		B74	LVDS_B1-		C74	PEG_RX7+		D74	PEG_TX7+
A75	LVDS_A2+ / eDP_TX0+		B75	LVDS_B2+		C75	PEG_RX7-		D75	PEG_TX7-
A76	LVDS_A2- / eDP_TX0-		B76	LVDS_B2-		C76	GND		D76	GND
A77	LVDS_VDD_EN / eDP_VDD_EN		B77	LVDS_B3+		C77	RSVD		D77	RSVD
A78	LVDS_A3+		B78	LVDS_B3-		C78	PEG_RX8+		D78	PEG_TX8+
A79	LVDS_A3-		B79	LVDS_BKLT_EN		C79	PEG_RX8-		D79	PEG_TX8-
A80	GND (FIXED)		B80	GND (FIXED)		C80	GND (FIXED)		D80	GND (FIXED)
A81	LVDS_A_CK+ / eDP_TX3+		B81	LVDS_B_CK+		C81	PEG_RX9+		D81	PEG_TX9+
A82	LVDS_A_CK- / eDP_TX3-		B82	LVDS_B_CK-		C82	PEG_RX9-		D82	PEG_TX9-
A83	LVDS_I2C_CK / eDP_AUX+		B83	LVDS_BKLT_CTRL / eDP_BKLT_CTRL		C83	RSVD		D83	RSVD
A84	LVDS_I2C_DAT / eDP_AUX-		B84	VCC_5V_SBY		C84	GND		D84	GND
A85	GPI3		B85	VCC_5V_SBY		C85	PEG_RX10+		D85	PEG_TX10+
A86	RSVD		B86	VCC_5V_SBY		C86	PEG_RX10-		D86	PEG_TX10-
A87	eDP_HPD		B87	VCC_5V_SBY		C87	GND		D87	GND
A88	PCIE0_CK_REF+		B88	BIOS_DIS1#		C88	PEG_RX11+		D88	PEG_TX11+
A89	PCIE0_CK_REF-		B89	VGA_RED *		C89	PEG_RX11-		D89	PEG_TX11-
A90	GND (FIXED)		B90	GND (FIXED)		C90	GND (FIXED)		D90	GND (FIXED)
A91	SPI_POWER		B91	VGA_GRN *		C91	PEG_RX12+		D91	PEG_TX12+
A92	SPI_MISO		B92	VGA_BLU *		C92	PEG_RX12-		D92	PEG_TX12-
A93	GPO0		B93	VGA_HSYNC *		C93	GND		D93	GND
A94	SPI_CLK		B94	VGA_VSYNC *		C94	PEG_RX13+		D94	PEG_TX13+
A95	SPI_MOSI		B95	VGA_I2C_CK *		C95	PEG_RX13-		D95	PEG_TX13-
A96	TPM_PP		B96	VGA_I2C_DAT *		C96	GND		D96	GND
A97	TYPE10#		B97	SPI_CS#		C97	RSVD		D97	RSVD
A98	SER0_TX		B98	RSVD		C98	PEG_RX14+		D98	PEG_TX14+
A99	SER0_RX		B99	RSVD		C99	PEG_RX14-		D99	PEG_TX14-
A100	GND (FIXED)		B100	GND (FIXED)		C100	GND (FIXED)		D100	GND (FIXED)
A101	SER1_TX~~/CAN_TX~~		B101	FAN_PWMOUT		C101	PEG_RX15+		D101	PEG_TX15+
A102	SER1_RX~~/CAN_RX~~		B102	FAN_TACHIN		C102	PEG_RX15-		D102	PEG_TX15-
A103	LID#		B103	SLEEP#		C103	GND		D103	GND
A104	VCC_12V		B104	VCC_12V		C104	VCC_12V		D104	VCC_12V
A105	VCC_12V		B105	VCC_12V		C105	VCC_12V		D105	VCC_12V

Row A			Row B			Row C			Row D	
A106	VCC_12V		B106	VCC_12V		C106	VCC_12V		D106	VCC_12V
A107	VCC_12V		B107	VCC_12V		C107	VCC_12V		D107	VCC_12V
A108	VCC_12V		B108	VCC_12V		C108	VCC_12V		D108	VCC_12V
A109	VCC_12V		B109	VCC_12V		C109	VCC_12V		D109	VCC_12V
A110	GND (FIXED)		B110	GND (FIXED)		C110	GND (FIXED)		D110	GND (FIXED)

Note: ~~Strike-through~~ entries are not supported functions on this product.
eDP (in place of LVDS) and VGA (in place of DDI 3) are BOM option support by project basis.
Ethernet support up to 2.5GbE. LAN LED behavior (GBE0_LINK 100#, GBE0_LINK1000#) is optimized based on maximum 2.5GbE speed (see 4.3.4 Gigabit Ethernet on page 31).
Maximum 2x USB4 is a build option in place of DDI 1, DDI 2 channels by project basis. Please contact your local representative for details.

4.2. Signal Terminology Descriptions

Meaning of the terms used for signal description tables

Term	Description
I	Input to the module
O	Output from the module
I/O	Bi-directional Input / Output
OD	Open drain output from the module
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I/O $3.3V_{SB}$	Input or output 3.3V tolerant active in standby state
DDC	Display Data Channel
PCIE	PCI Express compatible differential signal
PEG	PCI Express Graphics
SATA	Serial ATA specification Revision 2.6 and 3
LVDS	Low Voltage Differential Signal - 330 mV nominal; 450 mV maximum differential signal
P	Power Input / Output
REF	Reference voltage output. May be sourced from a Module power plane.
PDS	Pull-down strap. A Module output pin that is either tied to GND or is not connected. Used to signal Module capabilities to the Carrier Board.
PU	PU (pull-up) resistor on module
PD	PD (pull-down) resistor on module

4.3. AB Connector Signal Descriptions

4.3.1 Audio

Name	Pin #	Description	I/O	PU / PD	Comment
AC_RST# / HDA_RST#	A30	Reset output to CODEC, active low.	O 3.3VSB		
AC_SYNC / HDA_SYNC	A29	Sample-synchronization signal to the CODEC(s).	O 3.3VSB		PCH internal PD 20Kohm
AC_BITCLK / HDA_BITCLK	A32	Serial data clock generated by the external CODEC(s).	I/O 3.3VSB		
AC_SDOUT / HDA_SDOUT	A33	Serial TDM data output to the CODEC.	O 3.3VSB		PCH internal PD 20Kohm
AC_SDIN[2:0] / HDA_SDIN[2:0]	~~B28~~ B29 B30	Serial TDM data inputs from up to 3 CODECs.	I/O 3.3VSB		PCH internal PD 20Kohm AC_SDNI2/HDA_SDIN2 not supported

4.3.2 Analog VGA

Name	Pin #	Description	I/O	PU / PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	
VGA_GRN	B91	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3V		
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3V		
VGA_I2C_CK	B95	DDC clock line (I^2C port dedicated to identifying VGA monitor capabilities)	I/O OD 3.3V	PU 2k2 3.3V	
VGA_I2C_DAT	B96	DDC data line.	I/O OD 3.3V	PU 2k2 3.3V	

Note: VGA is BOM option support (in place of DDI 3) by project basis

4.3.3 LVDS or eDP

The module default supports a single or dual channel LVDS display panel with up to 24-bit colors. A BOM option that removes the eDP to LVDS bridge IC and outputs the eDP signals directly is available. eDP vs LVDS pin mapping is described below.

Pin #	LVDS mode	eDP mode
A71	LVDS_A0+	eDP_TX2+
A72	LVDS_A0-	eDP_TX2-
A73	LVDS_A1+	eDP_TX1+
A74	LVDS_A1-	eDP_TX1-
A75	LVDS_A2+	eDP_TX0+
A76	LVDS_A2-	eDP_TX0-
A78	LVDS_A3+	-
A79	LVDS_A3-	-
A81	LVDS_A_CK+	eDP_TX3+
A82	LVDS_A_CK-	eDP_TX3-
B71	LVDS_B0+	-
B72	LVDS_B0-	-
B73	LVDS_B1+	-
B74	LVDS_B1-	-
B75	LVDS_B2+	-
B76	LVDS_B2-	-
B77	LVDS_B3+	-
B78	LVDS_B3-	-
B81	LVDS_B_CK+	-
B82	LVDS_B_CK-	-
A77	LVDS_VDD_EN	eDP_VDD_EN
B79	LVDS_BKLT_EN	eDP_BKLT_EN
B83	LVDS_BKLT_CTRL	eDP_BKLT_CTRL
A83	LVDS_I2C_CK	eDP_AUX+
A84	LVDS_I2C_DAT	eDP_AUX-
A87	-	eDP_HPD

Note: LVDS is the default mode and eDP is a BOM option

4.3.3.1. Single/Dual Channel LVDS (default)

Name	Pin #	Description	I/O	PU / PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 100K	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V	PD 100K	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V	PD 100K	
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.	O 3.3V	PU 2k2 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	

4.3.3.2. 4-lane eDP

Name	Pin #	Description	I/O	PU / PD	Comment
eDP_TX3+ eDP_TX3- eDP_TX2+ eDP_TX2- eDP_TX1+ eDP_TX1- eDP_TX0+ eDP_TX0-	A81 A82 A71 A72 A73 A74 A75 A76	eDP differential pairs	O PCIE		AC coupled off module
eDP_VDD_EN	A77	eDP power enable	O 3.3V	PD 100K	
eDP_BKLT_EN	B79	eDP backlight enable	O 3.3V	PD 100K	
eDP_BKLT_CTRL	B83	eDP backlight brightness control	O 3.3V	PD 100K	
eDP_AUX+	A83	eDP AUX+	I/O PCIE		AC coupled off module
eDP_AUX-	A84	eDP AUX-	I/O PCIE		AC coupled off module
eDP_HPD	A87	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	PD 100K on this pin when eDP is supported

4.3.4 Gigabit Ethernet

Name	Pin #	Description	I/O	PU / PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: **1000 / 100 / 10** MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	I/O Analog		Twisted pair signals for external transformer.
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	OD 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	OD 3.3VSB		
GBE0_LINK100# *	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	OD 3.3VSB		
GBE0_LINK1000# *	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	OD 3.3VSB		
~~GBE0_CTREF~~	~~A14~~	~~Reference voltage for Carrier Board Ethernet channel 1 and 2 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be 250 mA or less.~~	~~REF~~ ~~GND min~~ ~~3.3V max~~		Not supported
GBE0_SDP	A49	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as 1pps signal.	IO 3.3VSB	GBE0_SDP	Depends on the selection of LAN controller. i225-IT support this pin

Note: This product supports up to 2.5GbE. The LAN LED behavior is optimized for maximum 2.5GbE speed.
GBE0_LINK1000# will be active for 2.5GbE speed indication.
GBE0_LINK100# will be active for 1GbE speed indication or lower.
GBE0_ACT# and GBE0_LINK# share the same source from the LAN controller.
For 100Mbit/sec and 10Mbit/sec speed, the LAN LED will be OFF.

4.3.5 SATA

Name	Pin #	Description	I/O	PU / PD	Comment
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		AC coupled on Module
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		AC coupled on Module
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2, Receive Input differential pair.	I SATA		AC coupled on Module
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3, Receive Input differential pair.	I SATA		AC coupled on Module
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	O 3.3V	PU 10K 3.3V	AC coupled on Module

4.3.5.1. PCH HSIO Lane Assignments

Name	HSIO name on SOC	Comment
SATA0	HSIO 26	
SATA1	HSIO 27	
SATA2	HSIO 28	
SATA3	HSIO 29	

4.3.6 PCI Express

Name	Pin #	Description	I/O	PU / PD	Comment
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		

4.3.6.1. PCH HSIO Lane Assignments

Name	HSIO name on SOC	Comment
PCIE0	HSIO 22	
PCIE1	HSIO 23	
PCIE2	HSIO 24	
PCIE3	HSIO 25	
PCIE4	HSIO 30	
PCIE5	HSIO 31	
PCIE6	HSIO 32	
PCIE7	HSIO 33	

4.3.7 LPC Bus

Name	Pin #	Description	I/O	PU / PD	Comment
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	B4 B5 B6 B7	LPC multiplexed address, command and data bus	I/O 3.3VSB		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3VSB		
LPC_DRQ0# LPC_DRQ1#	B8 B9	LPC serial DMA request	I 3.3V		Not connected
LPC_SERIRQ	A50	LPC serial interrupt	I/O 3.3VSB	PU 8.2K 3.3VSB	
LPC_CLK	B10	LPC clock output –33MHz nominal	O 3.3VSB		The LPC_CLK frequency is 24MHz on this platform

Note: LPC Bus is supported by an eSPI to LPC bridge IC

4.3.8 USB

Name	Pin #	Description	I/O	PU / PD	Comment
USB0+ USB0-	A46 A45	USB differential data pairs for Port 0	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB1+ USB1-	B46 B45	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB2+ USB2-	A43 A42	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB3+ USB3-	B43 B42	USB differential data pairs for Port 2	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB4+ USB4-	A40 A39	USB differential data pairs for Port 3	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB5+ USB5-	B40 B39	USB differential data pairs for Port 4	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB6+ USB6-	A37 A36	USB differential data pairs for Port 5	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB7+ USB7-	B37 B37	USB differential data pairs for Port 6	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on carrier
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on carrier
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on carrier
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on carrier
USB0_HOST_PRSNT	B48	Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present.	I 3.3VSB		Not supported

***Note**: A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.

4.3.9 SPI Bus (BIOS only)

Name	Pin #	Description	I/O	PU / PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB	PU 10K 3.3VSB	
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier	O P 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I	PU 10K 3.3VSB	Carrier shall pull to GND or leave not- connected.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I	PU 10K 3.3VSB	Carrier shall pull to GND or leave not- connected

4.3.10 Miscellaneous

Name	Pin #	Description	I/O	PU / PD	Comment
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3V		
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V	PU 10K 3.3V	
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3VSB		
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3VSB	PU 100K 3.3VSB	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3V		There shall be PD on carrier board
FAN_TACHIN	B102	Fan tachometer input for a fan with a two-pulse output.	I OD 3.3V	PU 47K 3.3V	
TPM_PP	A96	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V	PD 100K	PD only when TPM on module. Modules implementing a TPM shall pull down

4.3.11 SMBus

Name	Pin #	Description	I/O	PU / PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line. Power sourced through 3.3V standby rail and main power rails.	I/O OD 3.3VSB	PU 2.2K 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line. Power sourced through 3.3V standby rail and main power rails.	I/O OD 3.3VSB	PU 2.2K 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 3.3V standby rail and main power rails.	I 3.3VSB	PU 4.7K 3.3VSB	

4.3.12 I^2C Bus

Name	Pin #	Description	I/O	PU / PD	Comment
I2C_CK	B33	General purpose I^2C port clock output/input	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Source SEMA BMC as default (chipset by BOM option)
I2C_DAT	B34	General purpose I^2C port data I/O line	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Source SEMA BMC as default (chipset by BOM option)

4.3.13 General Purpose I/O (GPIO)

Name	Pin #	Description	I/O	PU / PD	Comment
GPO[0]	A93	General purpose output pins.	O 3.3V	PD 10K	After hardware RESET output low
GPO[1]	B54	General purpose output pins.	O 3.3V	PD 10K	After hardware RESET output low
GPO[2]	B57	General purpose output pins.	O 3.3V	PD 10K	After hardware RESET output low
GPO[3]	B63	General purpose output pins.	O 3.3V	PD 10K	After hardware RESET output low
GPI[0]	A54	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[1]	A63	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[2]	A67	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[3]	A85	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	

4.3.14 Serial Interface Signals

Name	Pin #	Description	I/O	PU / PD	Comment
SER0_TX	A98	General purpose serial port transmitter	O CMOS 3.3V		Power rail tolerance 5V, 12V There shall be PD on carrier board
SER0_RX	A99	General purpose serial port receiver	I CMOS 3.3V	PU 10K 3.3V	Power rail tolerance 5V, 12V
SER1_TX	A101	General purpose serial port transmitter	O CMOS 3.3V		Power rail tolerance 5V, 12V There shall be PD on carrier board
SER1_RX	A102	General purpose serial port receiver	I CMOS 3.3V	PU 10K 3.3V	Power rail tolerance 5V, 12V

4.3.15 Power and System Management

Name	Pin #	Description	I/O	PU / PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge.	I 3.3VSB	PU 10K 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low request for module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.	I 3.3VSB	PU 10K 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow carrier-based FPGAs or other configurable devices time to be programmed.	I 3.3VSB	PU 10K 3.3VSB	Should have weak pull up.
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON") may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB	PD 100K	
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB	PD 100K	
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB	PD 100K	
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10K 3.3VSB	
WAKE1#	B67	General purpose wake-up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 10K 3.3VSB	Connect to WAKE 0#
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low or may be used to signal some other external power-management event.	I 3.3VSB	PU 10K 3.3VSB	
LID#	A103	LID button. Low active signal used by the ACPI operating system for a LID switch.	I OD 3.3VSB	PU 47K 3.3VSB	Emulated on GPIO (BIOS)
SLEEP#	B103	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I OD 3.3VSB	PU 47K 3.3VSB	Emulated on GPIO (BIOS)
RAPID_ SHUTDOWN	C67	~~Trigger for Rapid Shutdown. Must be driven to 5V though a <=50-ohm source impedance for ≥ 20 µs.~~	I CMOS 5VSB		Not supported

4.3.16 Power and Ground

Name	Pin #	Description	I/O	PU / PD	Comment
VCC_12V	A104, A105, A106, A107, A108, A109, B104, B105, B106, B107, B109	Primary power input supports a wide range of 5 to 20V input. All available VCC_12V pins on the connector(s) shall be used.	P		8.5-20 V
VCC_5V_SBY	B84, B85, B86, B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		5Vsb ±5%
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path.	P		

4.4. CD Connector Signal Descriptions

4.4.1 USB 3.0 Extensions

Name	Pin #	Description	I/O	PU / PD	Comment
USB_SSRX0- USB_SSRX0+	C3 C4	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB0	I PCIE		AC coupled off module
USB_SSTX0- USB_SSTX0+	D3 D4	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB0	O PCIE		AC coupled on module
USB_SSRX1- USB_SSRX1+	C6 C7	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB1	I PCIE		AC coupled off module
USB_SSTX1- USB_SSTX1+	D6 D7	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB1	O PCIE		AC coupled on module
USB_SSRX2- USB_SSRX2+	C9 C10	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB2	I PCIE		AC coupled off module
USB_SSTX2- USB_SSTX2+	D9 D10	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB2	O PCIE		AC coupled on module
USB_SSRX3- USB_SSRX3+	C12 C13	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB3	I PCIE		AC coupled off module
USB_SSTX3- USB_SSTX3+	D12 D13	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB3	O PCIE		AC coupled on module

4.4.1.1. USB Root Segmentation

All USB interfaces are derived from the xHCI controller.

4.4.2 PCI Express

Name	Pin #	Description	I/O	PU / PD	Comment
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair.	I PCIE		AC coupled off Module

4.4.2.1. PCH HSIO Lane Assignments

Refer to Section 4.3.6.1 PCH HSIO Lane Assignments on page 34.

4.4.3 DDI1 Port

Name	Pin #	DisplayPort (DP)	HDMI
DDI1_PAIR0+ DDI1_PAIR0-	D26 D27	DP1_LANE0+ DP1_LANE0-	TMDS1_DATA2+ TMDS1_DATA2-
DDI1_PAIR1+ DDI1_PAIR1-	D29 D30	DP1_LANE1+ DP1_LANE1-	TMDS1_DATA1+ TMDS1_DATA1-
DDI1_PAIR2+ DDI1_PAIR2-	D32 D33	DP1_LANE2+ DP1_LANE2-	TMDS1_DATA0+ TMDS1_DATA0-
DDI1_PAIR3+ DDI1_PAIR3-	D36 D37	DP1_LANE3+ DP1_LANE3-	TMDS1_CLK+ TMDS1_CLK-
DDI1_PAIR4+ DDI1_PAIR4-	C25 C26	-	-
DDI1_PAIR5+ DDI1_PAIR5-	C29 C30	-	-
DDI1_PAIR6+ DDI1_PAIR6-	C15 C16	-	-
DDI1_HPD	C24	DP1_HPD	HDMI1_HPD
DDI1_CTRLCLK_AUX+	D15	DP1_AUX+	HMDI1_CTRLCLK
DDI1_CTRLCLK_AUX-	D16	DP1_AUX-	HMDI1_CTRLDATA
DDI1_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	DDI1_DDC_AUX_SEL

Note: Dual Mode (HDMI and DisplayPort on the same pins) implementations may be realized. This is desirable for SOCs that natively implement this capability. With such SOCs, the primary Dual Mode implementation challenge is that the HDMI_CTRL_DAT and HDMI_CTRL_CK lines are DC coupled, but the DP_AUX+ /- pair must be AC coupled. A set of FET switches is usually used to sort this out. The FET gates can be controlled by the AUX_SEL pin function.

4.4.3.1. DisplayPort (DP) Mode

Name	Pin #	Description	I/O	PU / PD	Comment
DP1_LANE0+ DP1_LANE0- DP1_LANE1+ DP1_LANE1- DP1_LANE2+ DP1_LANE2- DP1_LANE3+ DP1_LANE3-	D26 D27 D29 D30 D32 D33 D36 D37	DP Port 1, differential pair data lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
DP1_HPD	C24	DP Port 1, detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	Module must tolerate high level in stand-by mode. The carrier board shall include a blocking FET on DP1_HPD to prevent back-drive current from damaging the Module.
DP1_AUX+	D15	DP Port 1, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PD 100K	AC coupled on Module
DP1_AUX-	D16	DP Port 1, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PU 100K	AC coupled on Module
DDI1_DDC_AUX_SEL	D34	Strapping Signal to select HDMI or DP output 1M pull-down on the module and a floating pin on the carrier enable DisplayPort mode	I 3.3V	PD 1M	DP mode enabled

4.4.3.2. HDMI Mode

Name	Pin #	Description	I/O	PU / PD	Comment
TMDS1_DATA2+ TMDS1_DATA2- TMDS1_DATA1+ TMDS1_DATA1- TMDS1_DATA0+ TMDS1_DATA0-	D26 D27 D29 D30 D32 D33	HDMI / DVI Port, Differential Pair Data Lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
TMDS1_CLK+ TMDS1_CLK-	D36 D37	HDMI Port, Differential Pair Clock Lines			
HDMI_HPD	C24	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	
HDMI1_CTRLCLK	D15	I2C_CLK Line for HDMI	I/O PCIE	PU 2.2K	AC couple on Module
HDMI1_CTRLDATA	D16	I2C_DAT Line for HDMI	I/O PCIE	PU 2.2K	AC couple on Module
DDI1_DDC_AUX_SEL	D34	Strapping Signal to select HDMI or DP output 1M pull-down on the module and a pull high on the carrier enable HDMI mode	I 3.3V	PD 1M	HDMI mode enabled

4.4.4 DDI2 Port

Name	Pin #	DisplayPort (DP)	HDMI
DDI2_PAIR0+ DDI2_PAIR0-	D39 D40	DP2_LANE0+ DP2_LANE0-	TMDS2_DATA2+ TMDS2_DATA2-
DDI2_PAIR1+ DDI2_PAIR1-	D42 D43	DP2_LANE1+ DP2_LANE1-	TMDS2_DATA1+ TMDS2_DATA1-
DDI2_PAIR2+ DDI2_PAIR2-	D46 D47	DP2_LANE2+ DP2_LANE2-	TMDS2_DATA0+ TMDS2_DATA0-
DDI2_PAIR3+ DDI2_PAIR3-	D49 D50	DP2_LANE3+ DP2_LANE3-	TMDS2_CLK+ TMDS2_CLK-
DDI2_HPD	D44	DP2_HPD	HDMI2_HPD
DDI2_CTRLCLK_AUX+	C32	DP2_AUX+	HMDI2_CTRLCLK
DDI2_CTRLCLK_AUX-	C33	DP2_AUX-	HMDI2_CTRLDATA
DDI2_DDC_AUX_SEL	C34	DDI2_DDC_AUX_SEL	DDI2_DDC_AUX_SEL

Note:
Dual Mode (HDMI and DisplayPort on the same pins) implementations may be realized. This is desirable for SOCs that natively implement this capability. With such SOCs, the primary Dual Mode implementation challenge is that the HDMI_CTRL_DAT and HDMI_CTRL_CK lines are DC coupled, but the DP_AUX+ /- pair must be AC coupled. A set of FET switches is usually used to sort this out. The FET gates can be controlled by the AUX_SEL pin function.

4.4.4.1. DisplayPort (DP) Mode

Name	Pin #	Description	I/O	PU / PD	Comment
DP2_LANE0+ DP2_LANE0- DP2_LANE1+ DP2_LANE1- DP2_LANE2+ DP2_LANE2- DP2_LANE3+ DP2_LANE3-	D39 D40 D42 D43 D46 D47 D49 D50	DP Port 2, differential pair data lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
DP2_HPD	D44	DP Port 2, detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	Module must tolerate high level in stand-by mode. The carrier board shall include a blocking FET on DP1_HPD to prevent back-drive current from damaging the Module.
DP2_AUX+	C32	DP Port 2, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PD 100K	AC coupled on Module
DP2_AUX-	C33	DP Port 2, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PU 100K	AC coupled on Module
DDI2_DDC_AUX_SEL	C34	Strapping Signal to select HDMI or DP output 1M pull-down on the module and a floating pin on the carrier enable DisplayPort mode	I 3.3V	PD 1M	DP mode enabled

4.4.4.2. HDMI Mode

Name	Pin #	Description	I/O	PU / PD	Comment
TMDS2_DATA2+ TMDS2_DATA2- TMDS2_DATA1+ TMDS2_DATA1- TMDS2_DATA0+ TMDS2DATA0-	D39 D40 D42 D43 D46 D47	HDMI / DVI Port, Differential Pair Data Lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
TMDS2_CLK+ TMDS2_CLK-	D49 D50	HDMI Port, Differential Pair Clock Lines			
HDM2_HPD	D44	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	
HDMI2_CTRLCLK	C32	I2C_CLK Line for HDMI	I/O PCIE	PU 2.2K	AC couple on Module
HDMI2_CTRLDATA	C33	I2C_DAT Line for HDMI	I/O PCIE	PU 2.2K	AC couple on Module
DDI2_DDC_AUX_SEL	C34	Strapping Signal to select HDMI or DP output 1M pull-down on the module and a pull high on the carrier enable HDMI mode	I 3.3V	PD 1M	HDMI mode enabled

4.4.5 DDI3 Port

Name	Pin #	DisplayPort (DP)	HDMI
DDI3_PAIR0+ DDI3_PAIR0-	C39 C40	DP3_LANE0+ DP3_LANE0-	TMDS3_DATA2+ TMDS3_DATA2-
DDI3_PAIR1+ DDI3_PAIR1-	C42 C43	DP3_LANE1+ DP3_LANE1-	TMDS3_DATA1+ TMDS3_DATA1-
DDI3_PAIR2+ DDI3_PAIR2-	C46 C47	DP3_LANE2+ DP3_LANE2-	TMDS3_DATA0+ TMDS3_DATA0-
DDI3_PAIR3+ DDI3_PAIR3-	C49 C50	DP3_LANE3+ DP3_LANE3-	TMDS3_CLK+ TMDS3_CLK-
DDI3_HPD	C44	DP3_HPD	HDMI3_HPD
DDI3_CTRLCLK_AUX+	C36	DP3_AUX+	HMDI3_CTRLCLK
DDI3_CTRLCLK_AUX-	C37	DP3_AUX-	HMDI3_CTRLDATA
DDI3_DDC_AUX_SEL	C38	DDI3_DDC_AUX_SEL	DDI3_DDC_AUX_SEL

Note:
Dual Mode (HDMI and DisplayPort on the same pins) implementations may be realized. This is desirable for SOCs that natively implement this capability. With such SOCs, the primary Dual Mode implementation challenge is that the HDMI_CTRL_DAT and HDMI_CTRL_CK lines are DC coupled, but the DP_AUX+ /- pair must be AC coupled. A set of FET switches is usually used to sort this out. The FET gates can be controlled by the AUX_SEL pin function.

4.4.5.1. DisplayPort (DP) Mode

Name	Pin #	Description	I/O	PU / PD	Comment
DP3_LANE0+ DP3_LANE0- DP3_LANE1+ DP3_LANE1- DP3_LANE2+ DP3_LANE2- DP3_LANE3+ DP3_LANE3-	C39 C40 C42 C43 C46 C47 C49 C50	DP Port 3, differential pair data lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
DP3_HPD	C44	DP Port 3, detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	Module must tolerate high level in stand-by mode. The carrier board shall include a blocking FET on DP1_HPD to prevent back-drive current from damaging the Module.
DP3_AUX+	C36	DP Port 3, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PD 100K	AC coupled on Module
DP3_AUX-	C37	DP Port 3, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PU 100K	AC coupled on Module
DDI3_DDC_AUX_SEL	C38	Strapping Signal to select HDMI or DP output 1M pull-down on the module and a floating pin on the carrier enable DisplayPort mode	I 3.3V	PD 1M	DP mode enabled

4.4.5.2. HDMI Mode

Name	Pin #	Description	I/O	PU / PD	Comment
TMDS3_DATA2+ TMDS3_DATA2- TMDS3_DATA1+ TMDS3_DATA1- TMDS3_DATA0+ TMDS3_DATA0-	C39 C40 C42 C43 C46 C47	HDMI / DVI Port, Differential Pair Data Lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
TMDS3_CLK+ TMDS3_CLK-	C49 C50	HDMI Port, Differential Pair Clock Lines			
HDM3_HPD	C44	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	
HDMI3_CTRLCLK	C36	I2C_CLK Line for HDMI	I/O PCIE	PU 2.2K	AC couple on Module
HDMI3_CTRLDATA	C37	I2C_DAT Line for HDMI	I/O PCIE	PU 2.2K	AC couple on Module
DDI3_DDC_AUX_SEL	C38	Strapping Signal to select HDMI or DP output 1M pull-down on the module and a pull high on the carrier enable HDMI mode	I 3.3V	PD 1M	HDMI mode enabled

4.4.6 PCIe Graphics Port (PEG)

Name	Pin #	Description	I/O	PU / PD	Comment
PEG_TX0+ PEG_TX0-	D52 D53	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX0+ PEG_RX0-	C52 C53	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX1+ PEG_TX1-	D55 D56	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX1+ PEG_RX1-	C55 C56	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX2+ PEG_TX2-	D58 D59	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX2+ PEG_RX2-	C58 C59	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX3+ PEG_TX3-	D61 D62	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX3+ PEG_RX3-	C61 C62	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX4+ PEG_TX4-	D65 D66	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX4+ PEG_RX4-	C65 C66	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX5+ PEG_TX5-	D68 D69	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module

Name	Pin #	Description	I/O	PU / PD	Comment
PEG_RX5+ PEG_RX5-	C68 C69	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX6+ PEG_TX6-	D71 D72	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX6+ PEG_RX6-	C71 C72	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX7+ PEG_TX7-	D74 D75	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX7+ PEG_RX7-	C74 C75	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX8+ PEG_TX8-	D78 D79	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX8+ PEG_RX8-	C78 C79	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX9+ PEG_TX9-	D81 D82	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX9+ PEG_RX9-	C81 C82	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX10+ PEG_TX10-	D85 D86	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX10+ PEG_RX10-	C85 C86	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module

Name	Pin #	Description	I/O	PU / PD	Comment
PEG_TX11+ PEG_TX11-	D88 D89	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX11+ PEG_RX11-	C88 C89	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX12+ PEG_TX12-	D91 D92	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX12+ PEG_RX12-	C91 C92	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX13+ PEG_TX13-	D94 D95	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX13+ PEG_RX13-	C94 C95	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX14+ PEG_TX14-	D98 D99	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX14+ PEG_RX14-	C98 C99	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX15+ PEG_TX15-	D101 D102	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX15+ PEG_RX15-	C101 C102	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the Carrier Board to reverse lane order.	I 3.3V		

4.4.7 Module Type Definition

Name	Pin #	Description	I/O	PU / PD	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). For Pin-out Type 1 and Type 10 that lack a CD connector, these pins are not present (X) **TYPE2# TYPE1# TYPE0#** X X X Pinout Type 1 X X X Pinout Type 10 NC NC NC Pinout Type 2 NC NC GND Pinout Type 3 NC GND NC Pinout Type 4 NC GND GND Pinout Type 5 GND NC NC Pinout Type 6 GND NC GND Pinout Type 7 The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g. deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.			Type 6
TYPE10#	A97	In case of a type 10 module this pin signal is tied to GND through a 47K resistor on the module.			No PD

4.4.8 Power and Ground

Name	Pin #	Description	I/O	PU / PD	Comment
VCC_12V	C104, C105, C106, C107, C108, C109, D104, D105, D106, D107, D108, D109	Primary power input supports a wide range of 5 to 20V input. All available VCC_12V pins on the connector(s) shall be used.	P		8.5-20 V
GND	C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70, C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path.	P		

5. Additional Features

This chapter describes connectors, LEDs, switches and additional items located on the module and not necessarily included in the PICMG standard specification. The locations of these items are as below:

5.1. Module Feature Locations

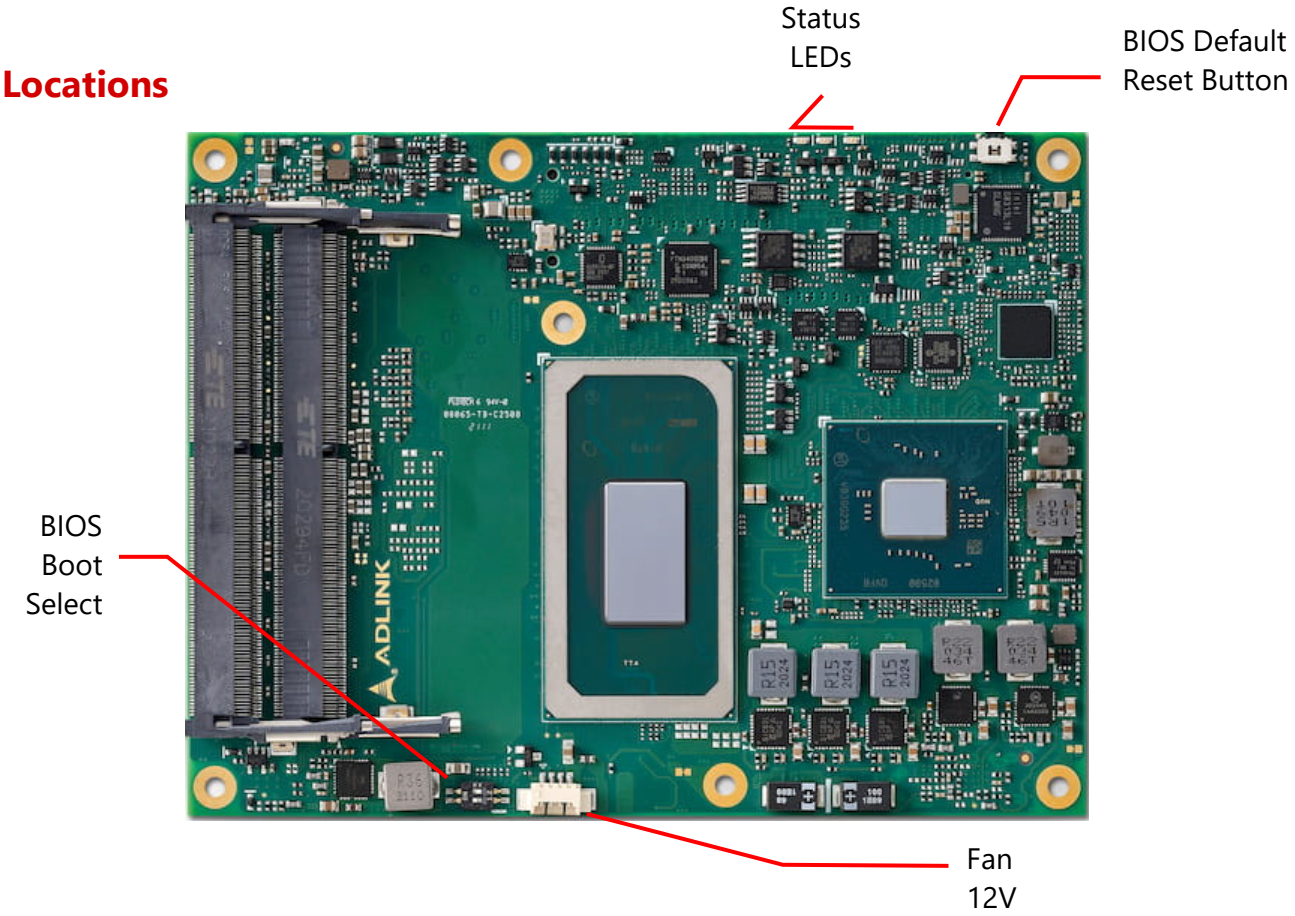


Figure 3 – Module feature locations (top side)

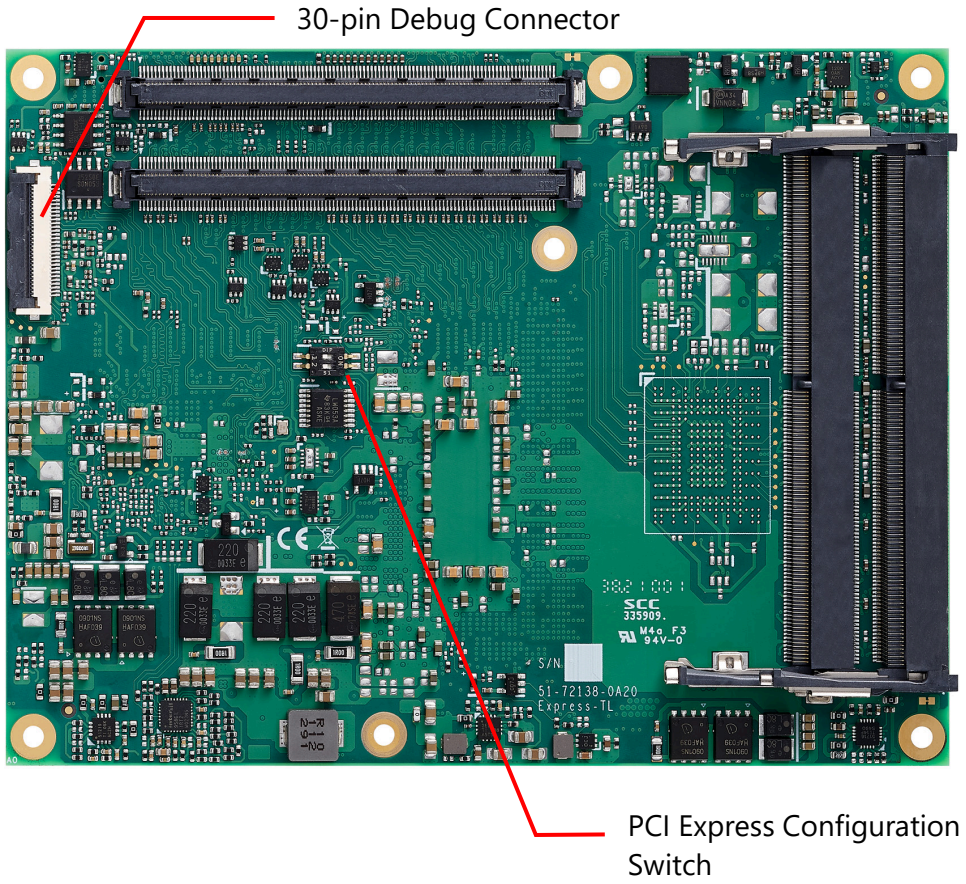


Figure 4 – Module feature locations (bottom side)

5.2. Debug Connector

This connector is particular useful during carrier design and bring up phase. It offers access to the following critical parts of the module:

- Test points measurement of internal power rails
- SPI BIOS programming interface
- Embedded Controller programming interface

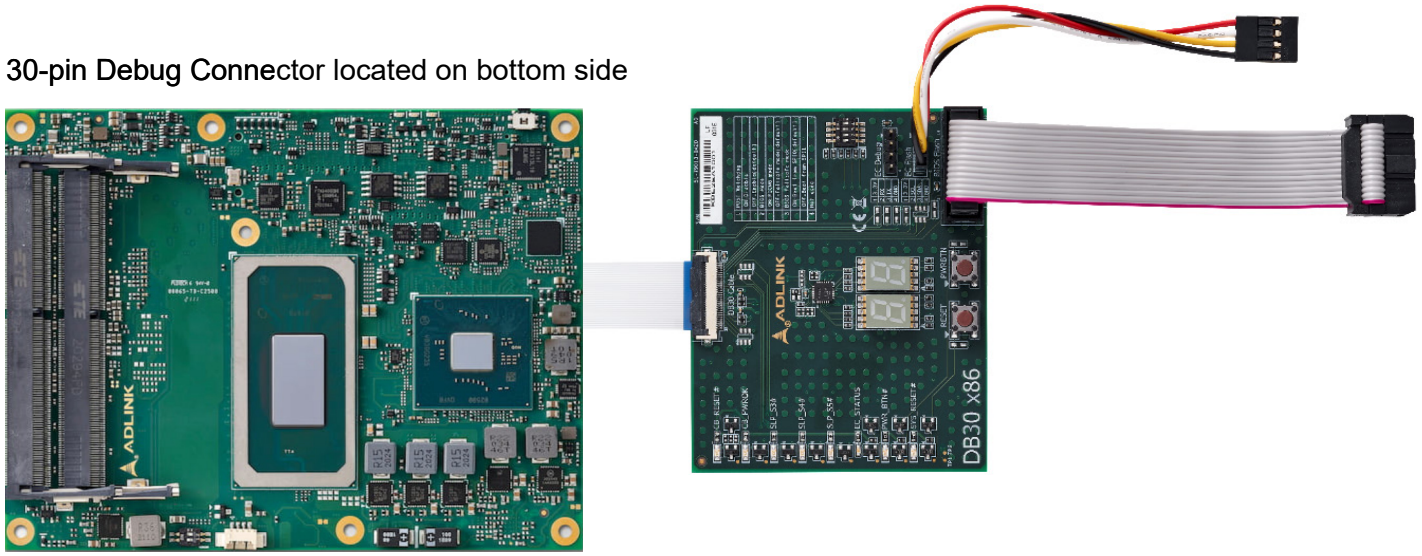


Figure 5 – Express-TL and Debug Module

5.3. Status LEDs

Status LEDs are mounted on the module to facilitate easier maintenance.

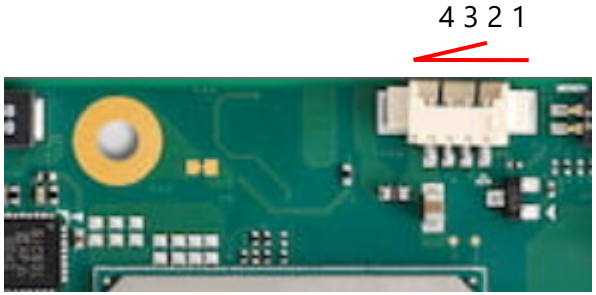
Name	Color	Connection	Function
LED1	Blue	BMC output	Power Sequence Status Code (BMC) Power Changes, RESET (see Exception Codes below)
LED2	Green	Power Source 3Vcc	S0 LED ON S3/S4/S5 LED OFF ECO mode LED OFF
LED3	Red	BMC output and same signal as WDT (B27) on BtB connector	Module power up WD LED = LED OFF Watchdog counting WD LED = Keep Last State Watchdog timed out WD LED = LED ON Watchdog RESET WD LED = LED ON Rebooted after WD RESET WD LED = LED ON Rebooted after PWRBTN WD LED = LED OFF Rebooted after RESET BTN WD LED = LED OFF Note: only a RESET not initiated by the BMC can clear the WD LED (user action)

5.4. Exception Codes

Exception Code	Error Message
0	NOERROR
3	NO_SLP_S5
4	NO_SLP_S4
5	NO_SLP_S3
6	BIOS_FAIL
7	RESET_FAIL
9	NO_CB_PWROK
10	CRITICAL_TEMP
11	POWER_FAIL
12	VOLTAGE_FAIL
13	RSMRST_FAIL
14	NO_VDDQ_PG
16	NO_VCORE_PG
17	NO_SYS_GD
19	NO_V3P3A
21	NO_PWRSRC_GD

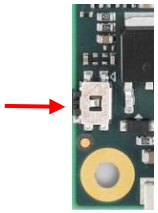
5.5. Fan Connector

Connector type: JVE 24W1125A-04M00



Name	Description
1	FAN_PWMOUT
2	FAN_TACHIN
3	GND
4	12V

5.6. BIOS Default Reset Button



To perform a hardware reset of BIOS default settings, perform the following steps:

1. Shut down the system.
2. Keep the BIOS Setup Defaults Reset Button pressed and boot up the system. You can release the button when the BIOS prompt screen appears
3. The BIOS prompt screen will display a confirmation that BIOS defaults have been reset and request that you reboot the system.

5.7. PCI Express Configuration Switch

The PCI Express Configuration Switch allows you to configure the PCI Express x16 lanes from the CPU as 1 PCIe x16, 2 PCIe x8, or 1 PCIe x8 + 2 PCIe x4.

Mode	Pin 1	Pin 2
1 PCIe x16 (default)	Off	Off
2 PCIe x8	Off	On
1 PCIe x8 + 2 PCIe x4	On	On
Reserved	On	Off

5.8. BIOS Boot Select

The module has two BIOS chips (BOM option) and BIOS operation can be configured to "PICMG" and dual-BIOS "Failsafe" modes using BIOS Select and Mode Configuration Switch, Pin 2.

Setting the module to PICMG mode will configure the BIOS chips on the module as SPI0 and SPI1. In PICMG mode, a BIOS chip cannot be placed in the SPI0 slot on the carrier.

In dual-BIOS Failsafe mode, both BIOS chips on the module are configured as SPI1. Only one of the two is connected to the SPI bus at any given time. In case of failure of the primary SPI1 BIOS, the system will reboot and switch to the secondary SPI1 BIOS on the module. In Failsafe mode, the SPI0 BIOS socket on the carrier can be populated.

In either mode, BIOS Select and Mode Configuration Switch Pin 1 is used to select whether to boot from SPI0 or SPI1.

Mode	Pin 1	Pin 2
Boot from SPI0 (default)	On	-
Boot from SPI1	Off	-
Set BIOS to PICMG mode (default)	-	On
Set BIOS to Failsafe BIOS mode	-	Off

6. BIOS Setup

6.1. Menu Structure

This section presents the six primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. The subsections in this section describe the submenus and setting options for each menu item. The default setting options are presented in **bold**, and the function of each setting is described in the right-hand column of the respective table.

Main	Advanced	Chipset	Security	Boot	Save & Exit
BIOS Information System Information Board Information System Date and Time Access Level	CPU Configuration Power & Performance TCSS Platform Settings Intel(R) Time Coordinated Computing Graphics Configuration Power Management System Management Thermal Management Watchdog Timer Super IO Configuration Miscellaneous AMT Configuration USB Configuration AMI Graphic Output Protocol Policy Serial Port Console Redirection Network Stack Configuration NVMe Configuration Trusted Computing	System Agent (SA) Configuration PCH-IO Configuration	Setup Administrator Password User Password Secure Boot	Boot Configuration FIXED BOOT ORDER Priorities UEFI USB Key Drive BBS Priorities	Save Change and Exit Discard Changes and Exit Save Changes and Reset Discard Changes and Reset Save Options Boot Override

6.2. Main

6.2.1 Main > BIOS Information

Feature	Options	Description
BIOS Vendor	Info only	American Megatrends
BIOS Version	Info only	ADLINK BIOS Version
Build Date	Info only	ADLINK BIOS Build Date
MRC Version	Info only	Display MRC Version
GOP Version	Info only	Display GOP Version
ME FW Version	Info only	Display ME FW Version
BIOS Boot Source	Info only	Display BIOS Boot Source

6.2.2 Main > System Information

Feature	Options	Description
Project Name	Info only	Display Project Name
CPU Board version	Info only	Display CPU Board Version
CPU Board String	Info only	Display CPU Board String
CPU Frequency	Info only	Display CPU Frequency
Total Memory	Info only	Display Installed Memory Size
Memory Frequency	Info only	Display Memory Frequency
PCH SKU	Info only	Display PCH SKU Version

6.2.3 Main > Board Information

Feature	Options	Description
Board Information	Info only	
Serial Number	Info only	Display SEMA Serial Number.
Manufacturing Date	Info only	Display SEMA Manufacturing Date.
Last Repair Date	Info only	Display SEMA Last Repair Date.
MAC ID	Info only	Display SEMA MAC ID.
Runtime Statistics	Info only	
Total Runtime	Info only	The returned value specifies the total time in minutes the system is running in S0 state.
Current Runtime	Info only	The returned value specifies the time in seconds the system is running in S0 state. This counter is cleared when the system is removed from the external power supply.
Power Cycles	Info only	The returned value specifies the number of times the external power supply has been shut down
Boot Cycles	Info only	The Boot counter is increased after a HW- or SW-Reset or after a successful power-up.
Boot Reason	Info only	The boot reason is the event which causes the reboot of the system.

6.2.4 Main > System Date/Time

Feature	Options	Description
System Date	Info only	
System Time	Info only	

6.2.5 Main > Access Level

Feature	Options	Description
Access Level	Info only	

6.3. Advanced

This menu contains the settings for most of the user interfaces in the system.

6.3.1 Advanced > CPU Configuration

Feature	Options	Description
CPU Configuration	Info only	
Type	Info only	Socket Specific CPU Information.
Speed	Info only	Display Max CPU speed.
ID	Info only	Display Microcode Patch.
Stepping	Info only	Display Min CPU stepping.
Number of Processors	Info only	Display CPU number of cores
GT Info	Info only	Display GT information
eDRAM Size	Infor only	Display eDRAM size if support
L1 Data Cache	Info only	Display cache info.
L1 Instruction Cache	Info only	Display cache info.
L2 Cache	Info only	Display cache info.
L3 Cache	Info only	Display cache info.
L4 Cache	Info only	Display cache info.
VMX	Info only	Display VMX support info.
SMX/TXT	Info only	Display SMX/TXT support info.
Intel Virtualization Technology	Disabled **Enabled**	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.
Active Processor Cores	**ALL**	Number of cores to enable in each processor package.

Feature	Options	Description
	1 2 3	
Hyper-Threading	Disabled **Enabled**	Enable or Disable Hyper-Threading Technology.

6.3.2 Advanced > Power & Performance

Feature	Options	Description
CPU – Power Management Control	Submenu	CPU- Power Management Control Options
GT – Power Management Control	Submenu	GT- Power Management Control

6.3.2.1. Advanced > Power & Performance > CPU – Power Management

Feature	Options	Description
CPU – Power Management Control	Info only	
Boot performance mode	Max Battery Max Non-Turbo Performance **Turbo Performance**	Select the performance state that the BIOS will set starting from reset vector.
Intel(R) SpeedStep(tm)	Disabled **Enabled**	Allows more than two frequency ranges to be supported.
Race To Halt (RTH)	Disabled **Enabled**	Enable/Disable Race to Halt features. RTH will dynamically increase CPU frequency in order to enter pkg C-State faster to reduce overall power. (RTH is controlled through MSR 1FC bit 20)
Intel(R) Speed Shift Technology	Disabled **Enabled**	Enable/Disable Intel(R) Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware-controlled P-states.

Feature	Options	Description
Per Core P State OS control mode	Disabled **Enabled**	Enable/Disable Per Core P state OS control mode. Disabling will set Bit 31 = 1 command 0x06. When set, the highest core request is used for all other core requests.
HwP Autonomous Per Core P State	Disabled **Enabled**	Disable Autonomous PCPS (Bit 30 = 1, command 0x11) Autonomous will request the same value for all cores all the time. Enable PCPS (default Bit 30 = 0, command 0x11)
HwP Autonomous EPP Grouping	Disabled **Enabled**	Enable EPP grouping (default Bit 29 =0, command 0x11) Autonomous will request the same values for all cores with same EPP. Disable EPP grouping (Bit 29 =1 , command 0x11) autonomous will not necessarily request same values for all cores with same EPP.
EPB override over PECI	**Disabled** Enabled	Enable/Disable EPB override over PECI. Enable by sending pcode command 0x2b , subcommand 0x3 to 1. This will allow OOB EPB PECI override control
HwP Fast MSR Support	Disabled **Enabled**	Enable/Disable HwP Fast MSR Support for IA32_HWP_REQUEST MSR.
HDC Control	Disabled **Enabled**	This option allows HDC configuration.\n Disabled: Disable HDC\n Enabled: Can be enabled by OS if OS native support is available.
View/Configure Turbo Options	Submenu	View/Configure Turbo Options
Config TDP Configurations	Submenu	Config TDP Configurations
CPU VR Settings	Submenu	CPU VR Settings
Platform PL1 Enable	**Disabled** Enabled	Enable/Disable Platform Power Limit 1 programming. If this option is enabled, it activates the PL1 value to be used by the processor to limit the average power of given time window.
Platform PL2 Enable	**Disabled** Enabled	
Power Limit 4 override	**Disabled** Enabled	Enable/Disable Power Limit 4 override. If this option is disabled, BIOS will leave the default values for Power Limit 4.
C states	**Disabled** Enabled	Enable/Disable CPU Power Management. It allows CPU to go to C states when it's not 100% utilized.
Thermal Monitor	Disabled **Enabled**	Enable/Disable Thermal Monitor

Feature	Options	Description
Interrupt Redirection Mode Selection		Interrupt Redirection Mode Select for Logical Interrupts
Timed MWAIT	**Disabled** Enabled	Enable/Disable Timed MWAIT Support
Custom P-State Table	Submenu	Add Custom P-state Table
EC Turbo Control Mode		Enable/Disable EC Turbo Control Mode
Energy Performance Gain		Enable/Disable Energy Performance Gain.
EPG DIMM Idd3N	Info only	
EPG DIMM Idd3P	Info only	
Power Limit 3 Settings	Submenu	Power Limit 3 Settings
CPU Lock Configuration	Submenu	CPU Lock Configuration

6.3.2.2. Advanced > Power & Performance > CPU – Power Management Control > View/Configure Turbo Options

Feature	Options	Description
Current Turbo Settings	Info only	
Max Turbo Power Limit	Info only	
Min Turbo Power Limit	Info only	
Package TDP Limit	Info only	
Power Limit 1	Info only	
Power Limit 2	Info only	
1-core Turbo Ratio Limit Ratio	Info only	
2-core Turbo Ratio Limit Ratio	Info only	
3-core Turbo Ratio Limit Ratio	Info only	

Feature	Options	Description
4-core Turbo Ratio Limit Ratio	Info only	
Energy Efficient P-state	Disabled **Enabled**	Enable/Disable Energy Efficient P-state feature. When set to 0, will disable access to ENERGY_PERFORMANCE_BIAS MSR and CPUID Function 6 ECX[3] will read 0 indicating no support for Energy Efficient policy setting. When set to 1, it will enable access to ENERGY_PERFORMANCE_BIAS MSR.
Package Power Limit MSR Lock	**Disabled** Enabled	Enable/Disable locking of Package Power Limit settings. When enabled, PACKAGE_POWER_LIMIT MSR will be locked and a reset will be required to unlock the register.
1-Core Ratio Limit Override	44	1-Core Ratio Limit ranges from 0 to 83. The Minimum range may vary between Processors. This 1-Core Ratio Limit Must be greater than or equal to 2-Core Ratio Limit, 3-Core Ratio Limit, 4-Core Ratio Limit.
2-Core Ratio Limit Override	42	2-Core Ratio Limit ranges from 0 to 83. The Minimum range may vary between Processors. This 2-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit.
3-Core Ratio Limit Override	41	3-Core Ratio Limit ranges from 0 to 83. The Minimum range may vary between Processors. This 3-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit.
4-Core Ratio Limit Override	40	4-Core Ratio Limit ranges from 0 to 83. The Minimum range may vary between Processors. This 4-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit.
Energy Efficient Turbo	**Disabled** Enabled	Enable/Disable Energy Efficient Turbo Feature. This feature will opportunistically lower the turbo frequency to increase efficiency. Recommended only to disable in overclocking situations where turbo frequency must remain constant. Otherwise, leave enabled.

6.3.2.2.1. Advanced > Power & Performance > CPU – Power Management Control > Config TDP Configurations

Feature	Options	Description
Config TDP Configurations	Info only	
Enable Configurable TDP	**Applies to non-cTDP** Applies to cTDP	Applies TDP initialization settings based on non-cTDP or cTDP. Default is 1: Applies to cTDP; if 0 then applies non-cTDP and BIOS will bypass cTDP initialization flow.
Configurable TDP Boot Mode	**Normal** Down Deactivate	Configurable TDP Mode as Nominal/Up/Down/Deactivate TDP selection. Deactivate option will set MSR to Nominal and MMIO to Zero.
Configurable TDP Lock	Enabled	Configurable TDP Mode Lock sets the Lock bits on TURBO_ACTIVATION_RATIO and CONFIG_TDP_CONTROL.

Feature	Options	Description
	Disabled	Note: When CTDP Lock is enabled Custom ConfigTDP Count will be forced to 1 and Custom ConfigTDP Boot Index will be forced to 0.
CTDP BIOS control	Enabled **Disabled**	Enables CTDP control via runtime ACPI BIOS methods. This "BIOS only" feature does not require EC or driver support.
ConfigTDP Levels	Info only	
ConfigTDP Turbo Activation Ratio	Info only	
Power Limit1	Info only	
Power Limit2	Info only	
Custom Settings Nominal ConfigTDP Nominal	Info only	
Power Limit1	0	Power Limit 1 in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Overclocking SKU: The value must be between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). Other SKUs: This value must be between Min Power Limit and TDP Limit. If value is 0, BIOS will program TDP value.
Power Limit2	0	Power Limit 2 value in Milli Watts. BIOS will round to the nearest 1/8W when programming. If the value is 0, BIOS will program this value as 1.25*TDP. For 12.50W, enter 12500. Processor applies control policies such that the package power does not exceed this limit.
Power Limit 1 Time Window	0	Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0 = default value (28 sec for Mobile and 8 sec for Desktop). Defines time window which TDP value should be maintained.
ConfigTDP Turbo Activation Ratio	0	Custom value for Turbo Activation Ratio. Needs to be configured with valid values from LFM to Max Turbo. 0 means don't use custom value.
Custom Settings Down ConfigTDP Level1	Info only	
Power Limit1	0	Power Limit 1 in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Overclocking SKU: The value must be between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). Other SKUs: This value must be between Min Power Limit and TDP Limit. If value is 0, BIOS will program TDP value.
Power Limit2	0	Power Limit 2 value in Milli Watts. BIOS will round to the nearest 1/8W when programming. If the value is 0, BIOS

Feature	Options	Description
		will program this value as 1.25*TDP. For 12.50W, enter 12500. Processor applies control policies such that the package power does not exceed this limit.
Power Limit 1 Time Window	0	Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0 = default value (28 sec for Mobile and 8 sec for Desktop). Defines time window which TDP value should be maintained.
ConfigTDP Turbo Activation Ratio	0	Custom value for Turbo Activation Ratio. Needs to be configured with valid values from LFM to Max Turbo. 0 means don't use custom value.

6.3.2.2.2. Advanced > Power & Performance > CPU – Power Management Control > CPU VR Settings

Feature	Options	Description
CPU VR Settings	Info only	
PSYS Slope	0	PSYS Slope defined in 1/100 increments. The range is from 0-200. For a 1.25 slope, enter 125. 0 = AUTO. Uses BIOS VR mailbox command 0x9."
PSYS Offset	0	PSYS Offset defined in 1/1000 increments. The range is from 0-63999. For an offset of 25.348, enter 25348. PSYS Uses BIOS VR mailbox command 0x4.
PSYS Prefix	**+** -	Sets the offset value as positive or negative.
PSYS PMax Power	**0**	PSYS PMax power, defined in 1/8 watt increments. The range is from 0-8192. For a PMax of 125W, enter 1000. 0 = AUTO. Uses BIOS VR mailbox command 0xB.
Acoustic Noise Settings	Submenu	Configure Acoustic Noise Settings for IA, GT and SA domains
VccIn VR Settings	Submenu	VccIn VR Settings
RFI Settings	Submenu	RFI Settings

6.3.2.2.3. Advanced > Power & Performance > CPU – Power Management Control > Custom P-state Table

Feature	Options	Description
Custom P-state Table	Info only	
Number of P states	0	Sets the number of custom P-states. At least 2 states must be present.

6.3.2.2.4. Advanced > Power & Performance > CPU – Power Management Control >Power Limit 3 Setting

Feature	Options	Description
CFG Lock	Disabled **Enabled**	Configure MSR 0xE2[15], CFG Lock bit
Overclocking Lock	**Disabled** Enabled	Enable/Disable Overclocking Lock (BIT 20) in FLEX_RATIO(194) MSR

6.3.2.2.5. Advanced > Power & Performance > CPU – Power Management Control >CPU Lock Configuration

Feature	Options	Description
CFG Lock	Disabled **Enabled**	Configure MSR 0xE2[15], CFG Lock bit
Overclocking Lock	**Disabled** Enabled	Enable/Disable Overclocking Lock (BIT 20) in FLEX_RATIO(194) MSR

6.3.2.3. Advanced > Power & Performance > GT – Power Management Control

Feature	Options	Description
GT – Power Management Control	Info only	
RC6(Render Standby)	Disabled **Enabled**	
Maximum GT frequency	**Default Max Frequency** 100Mhz 150Mhz 200Mhz 250Mhz 300Mhz 350Mhz 400Mhz 450Mhz 500Mhz 550Mhz 600Mhz 650Mhz 700Mhz 750Mhz 800Mhz 850Mhz 900Mhz 950Mhz 1000Mhz 1050Mhz 1100Mhz 1150Mhz 1200Mhz	Maximum GT frequency limited by the user. Choose between 400MHz (RPN) and 400MHz (RP0). Value beyond the range will be clipped to min/max supported by SKU
Disable Turbo GT frequency	Enabled **Disabled**	Enabled: Disables Turbo GT frequency. Disabled: GT frequency is not limited

6.3.3 Advanced > TCC Platform Setting

Feature	Options	Description
TCC Platform Setting	Info only	
Control IOMMU Pre-Boot Behavior	Disable IOMMU Enable IOMMU during boot	Enable IOMMU in Pre-boot environment (If DMAR table is installed in DXE and If VTD_INFO_PPI is installed in PEI.)

6.3.4 Advanced > Intel(R) Time Coordinated Computing

Feature	Options	Description
Intel(R) Time Coordinated Computing (Intel(R) TCC)	Info only	
#AC Split Lock	Enabled **Disabled**	Enable or Disable Alignment Check Exception (#AC). When enabled, this will assert an #AC when any atomic operation has an operand that crosses two cache lines.
Intel(R) TCC Mode	Enabled **Disabled**	Enable or Disable Intel(R) TCC Mode. When enabled, this will modify system settings to improve real-time performance. The full list of settings and their current state are displayed below when Intel(R) TCC mode is enabled.
Intel(R) TCC Mode Affected Settings	Info only	
IO Fabric Low Latency	Enabled **Disabled**	Enable or Disable IO Fabric Low Latency. This will turn off some power management in the PCH IO fabrics. This option provides the most aggressive IO Fabric performance setting. S3 state is NOT supported.
GT CLOS	Enabled **Disabled**	Enable or Disable Graphics Technology (GT) Class of Service. Enable will reduce Gfx LLC allocation to minimize impact of Gfx workload on LLC.
OPIO Recentering	**Enabled** Disabled	Enable or Disable Opio Recentering to improve Pcie latency.
C states	Enabled **Disabled**	Enable/Disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.
Intel(R) Speed Shift Technology	**Enabled**	Enable/Disable Intel(R) Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for

Feature	Options	Description
	Disabled	hardware-controlled P-states.
Intel(R) SpeedStep(tm)	**Enabled** Disabled	Allows more than two frequency ranges to be supported.
Hyper-Threading	**Enabled** Disabled	Enable or Disable Hyper-Threading Technology.
ACPI D3Cold Support	**Enabled** Disabled	Enable/Disable ACPI D3Cold support to be executed on D3 entry and exit
Low Power S0 Idle Capability	Enabled **Disabled**	This variable determines if we enable ACPI Lower Power S0 Idle Capability (Mutually exclusive with Smart connect). While this is enabled, it also disables 8254 timer for SLP_S0 support.
SA GV	**Enabled** Disabled	System Agent Geyserville. Can disable, fix to a specific point, or enable frequency switching.
WRC Feature	Enabled **Disabled**	Enable/Disable SA WRC (Write Cache) Feature of IOP. When enabled, supports IO devices allocating onto the ring and into LLC.
Page Close Idle Timeout	**Enabled** Disabled	Page Close Idle Timeout Control
Power Down Mode	Auto No Power Down APD PPD-DLLoff	CKE Power Down Mode Control
RC6(Render Standby)	**Enabled** Disabled	Check to enable render standby support.
DMI Link ASPM Control	Enabled **Disabled**	The control of Active State Power Management of the DMI Link.
PCI Express Clock Gating	**Enabled** Disabled	PCI Express Clock Gating Enable/Disable for each root port.
Legacy IO Low Latency	**Enabled** Disabled	Set to enable low latency of legacy IO. Some systems require lower IO latency irrespective of power. This is a tradeoff between power and IO latency.

6.3.5 Advanced > Graphics Configuration

Feature	Options	Description
NXP Configuration	Info Only	
Data format and Color Depth	VESA 24 bpp JEIDA 24 bpp **JEIDA/vesa 18 bpp**	Data format and Color Depth select
LVDS Output Mode	Dual LVDS bus **Single LVDS bus**	Single/Dual mode select
DE Polarity	**Active High** Active Low	DE Polarity select
Vsync Polarity	**Active High** Active Low	Vsync Polarity select
Hsync Polarity	**Active High** Active Low	Hsync Polarity select
Spreading Depth	**No Spreading** 0.5% 1.0% 1.5% 2.0% 2.5%	Clock frequency center spreading depth.
Integrated Display Configuration	Info only	
eDP/LVDS	**Disabled** Enabled	Enable/Disable eDP/LVDS
DDI Port 1	No Device Display Port HDMI **DisplayPort with HDMI/DVI Compatibility**	DDI port 1 function choose to Display Port or HDMI

Feature	Options	Description
DDI Port 2	No Device Display Port HDMI **DisplayPort with HDMI/DVI Compatibility**	DDI port 2 function choose to Display Port or HDMI
DDI Port 3	No Device Display Port HDMI **DisplayPort With HDMI/DVI Compatibility**	DDI port 3 function choose to Display Port or HDMI

6.3.6 Advanced > Power Management

Feature	Options	Description
Power Management	Info Only	
Enable ACPI Auto Configuration	**Disabled** Enabled	Enables or Disables BIOS ACPI Auto Configuration
Enable Hibernation	Disabled **Enabled**	
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	
LID Function	**Disabled** Enabled	
Sleep Function	Disabled **Enabled**	
ECO Mode	**Disabled** Enabled	

Feature	Options	Description
Power-Up Mode	**Turn On** Remain Off Last State	
ATTENTION: The Power-Up Mode only has effect, if the module is in ATX-Mode	Info Only	
Power Consumption	Submenu	

6.3.6.1. Advanced > Power Management > Power Consumption

Feature	Options	Description
Power Consumption	Info only	
Main Current	Info only	Display Main Current information
Current Input Power	Info only	Display Current Input Power information
RTC	Info only	Display RTC information
5VSB	Info only	Display 5VSB information
VIN	Info only	Display VIN information
3.3V	Info only	Display 3.3V information
VMEM	Info only	Display VMEM information
3.3VSB	Info only	Display 3.3VSB information
VCORE	Info only	Display VCORE information

6.3.7 Advanced > System Management

Feature	Options	Description
System Management	Info Only	
Version	Info Only	Display SEMA Module Version
SEMA Firmware	Info Only	Display SEMA Firmware Version
SEMA Flags	Submenu	Display SEMA Flags
SEMA Features	Info	Display SEMA Supported Features

6.3.7.1. Advanced > System Management > SEMA Flags

Feature	Options	Description
SEMA Flags	Info Only	
SEMA Flags	Info Only	Display SEMA Flags
BIOS Select	Info Only	Display BIOS Select type
ATX/AT-Mode	Info Only	Display ATX or AT mode

6.3.8 Advanced > Thermal Management

Feature	Options	Description
Thermal Management	Info Only	
Critical Trip Point	**Disabled** 80 C 90 C 95 C	The value is the temperature threshold of the Critical Trip Point.
Passive Cooling Trip Point	**Disabled** 70 C	The value is the temperature threshold of the Passive Cooling Trip Point.

Feature	Options	Description
	80 C 90 C	
Active Cooling Trip Point	40 C 50 C 60 C 70 C **Refer to BMC**	This value is the temperature threshold of the active cooling trip point.
Watchdog ACPI Event Shutdown	**Disabled** Enabled	Watchdog ACPI Event Shutdown Enabled/Disabled
Temperature and Fan Speed	Submenu	

6.3.8.1. Advanced > Thermal Management > Thermal and Fan Speed

Feature	Options	Description
Temperatures and Fan Speed	Info Only	
CPU Temperature	Info Only	
Current	Info Only	Display Current CPU Temperature
Startup	Info Only	Display Startup Board Temperature
Min	Info Only	Display Min Board Temperature
Max	Info Only	Display Max Board Temperature
Board Temperatures	Info Only	
Current	Info Only	Display Current CPU Temperature
Startup	Info Only	Display Startup Board Temperature
Min	Info Only	Display Min Board Temperature
Max	Info Only	Display Max Board Temperature

Feature	Options	Description
CPU Fan Speed	Info Only	Display CPU Fan Speed
Smart Fan	Submenu	

6.3.8.1.1. Advanced > Thermal Management > Thermal and Fan Speed > Smart Fan

Feature	Options	Description
Smart Fan	Info Only	
CPU Smart FanTemperature Source	**CPU Sensor** Board Sensor	CPU Smart FanTemperature Source
CPU Fan Mode	**Auto** Off On Soft	CPU Fan Mode
Trigger Point1	Info Only	
Trigger Temperature	**45**	Trigger Temperature
PWM Level	**25**	PWM Level
Trigger Point2	Info Only	
Trigger Temperature	**60**	Trigger Temperature
PWM Level	**50**	PWM Level
Trigger Point3	Info Only	
Trigger Temperature	**75**	Trigger Temperature
PWM Level	**75**	PWM Level
Trigger Point4	Info Only	
Trigger Temperature	**90**	Trigger Temperature

Feature	Options	Description
PWM Level	**100**	PWM Level

6.3.9 Advanced > Watchdog Timer

Feature	Options	Description
Watchdog Timer	Info only	
Power-Up Watchdog	**Disabled** Enabled	The Power Up Watchdog resets the system after a certain amount of time after power up. Pressing F12 during start-up disables the Power Up Watchdog.
Timeout	**65535**	Here you can enter the time the Power Up Watchdog should wait until it resets the system. The value range starts by 24 and ends by 65535
RunTime Watchdog	**Disabled** Enabled	The RunTime Watchdog resets the system after a certain period following a power up.
Timeout	**24**	Here you can enter the time the Runtime Watchdog should wait until it resets the system. The value range starts from 30 and ends at 65535.

6.3.10 Advanced > Super IO Configuration

Feature	Options	Description
Super IO Configuration	Info only	
IT5121E Super IO Configuration	Submenu	System Super IO Chip Parameters.
W83627DHGSEC Super IO Configuration	Submenu	System Super IO Chip Parameters.

6.3.10.1.Advanced > Super IO Configuration > IT5121E Super IO Configuration

Feature	Options	Description
IT5121E Super IO Configuration	Info only	
Serial Port 1/2 Configuration	Submenu	Set Parameters of Serial Port 1/2
Serial Port 1/2 Configuration	Info only	
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	Info Only	Display IO / IRQ information of COM Port.
Change Settings	**Auto** IO=3F8h/2F8h; IRQ=4; IO=3F8h; IRQ=3,4,5,6,7,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for Super IO Device.
Change Settings	**Normal** High Speed	Select an optimal setting for Super IO Device

6.3.10.2.Advanced > Super IO Configuration > W83627DHGSEC Super IO Configuration

Feature	Options	Description
Serial Port 1/2 Configuration	Submenu	Set Parameters of Serial Port 2 (COMB).
Serial Port 1/2 Configuration	Info only	
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	Info Only	Display IO / IRQ information of COM Port.
Change Settings	**Auto** IO=248h; IRQ=11; IO=240h; IRQ=3,4,5,6,7,10,11,12 IO=248h; IRQ=3,4,5,6,7,10,11,12 IO=250h; IRQ=3,4,5,6,7,10,11,12 IO=258h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for Super IO Device.

6.3.11 Advanced > Miscellaneous

Feature	Options	Description
Miscellaneous	Info Only	
Power Supply Unit	Emulate AT Mode **ATX Mode**	Select Emulation AT or ATX function. If this option set to [Emulation AT], BIOS will report no suspend functions (S3 & S4) to ACPI OS. In windows XP, it will make OS show shutdown message during system shutdown. ATX: OS will turn off system power when shutdown.
I2C Speed Control	**100 kbps** 400 kbps	I2C Speed Control
WOL From S5	OFF **ON**	This Config to control power on/off LAN in S5 State by SEMA(EC)

Feature	Options	Description
Smart Battery Function	**Disabled** Enabled Auto	Enable/Disable Smart Battery function. Auto: disable Smart Battery function if charger IC not be detected.
SMBUS Select	**From PCH** From EC	Select SMBUS Routine

6.3.12 Advanced > AMT Configuration

Feature	Options	Description
MEBx hotkey Pressed	**Disabled** Enabled	

6.3.13 Advanced > USB Configuration

Feature	Options	Description
USB Configuration	Info Only	
USB Module Version	Info Only	Display USB Module Version
USB Controllers:	Info Only	Display USB Controllers is XHCI or EHCI.
USB Devices:	Info Only	Display attachment USB devices.
Legacy USB Support	**Enabled** Disabled Auto	Enables Legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications.
XHCI Hand-off	**Enabled** Disabled	This is a workaround for OSs without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	Disabled	Enable / Disable USB Mass Storge Driver Support.

Feature	Options	Description
	Enabled	
USB hardware delays and time-outs:	Info Only	
USB transfer rime-out	1 sec 5sec 10sec **20 sec**	The time-out value for Control, Bulk, and Interrupt transfers.
Device reset time-out	10 sec **20 sec** 30 sec 40 sec	USB mass storage device Start Unit command time-out.
Device power-up delay	**Auto** Manual	Maximum time the device will take before it properly reports itself to the Hot Controller. 'Auto' uses default value: for a Root po\rt it is 100ms, for a Hub port the delay is taken form Hub descriptor.

6.3.14 Advanced > AMI Graphic Output Protocol Policy

Feature	Options	Description
Intel (R) Graphics Controller	Info Only	
Intel (R) GOP Driver	Info Only	
Output Select	[ACTIVE Current]	Output Interface

6.3.15 Advanced > Serial Port Console Redirection

Feature	Options	Description
COM 0/1/2/3	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.

Feature	Options	Description
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.

6.3.15.1.Advanced > Serial Console Redirection > Console Redirection Settings (if COM 0/1/2/3 enabled)

Feature	Options	Description
COM1	Info only	
Console Redirection Settings	Info only	
Teriminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: The parity bit is 0 if the num of 1's in the data bits is even. Odd: The parity bit is 0 if num of 1's in the data bits is odd. Mark: The parity bit is always 1. Space: The parity bit is always 0. Mark and Space parity bits do not allow for error detection. They can be used as an additional data bit.
Stop Bits	**1**	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.

Feature	Options	Description
	2	
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
VT-UTF8 Combo Key Support	**Enabled** Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With this mode enabled only text will be sent. This is to capture Terminal data.
Resolution 100x31	Enabled **Disabled**	On Legacy OS, the Number of Rows and Columns supported redirection
Legacy OS Redirection Resolution	**80x24** 80x25	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** Intel Linux XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.

6.3.16 Advanced > Network Stack Configuration

Feature	Options	Description
Network Stack	**Disable** Enable	Enables/Disables UEFI Network Stack.
IPv4 PXE Support	**Disable** Enable	Enables/Disables IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.
IPv4 HTTP Support	**Disable** Enable	Enables/Disables IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.

Feature	Options	Description
IPv6 PXE Support	**Disable** Enable	Enables/Disables IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.
IPv6 HTTP Support	**Disable** Enable	Enables/Disables IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.
PXE boot wait time	**0**	Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.
Media detect count	**1**	Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

6.3.17 Advanced > NVMe Configuration

Feature	Options	Description
NVMe Controller and Drive information	Info Only	
Display NVMe device information	Info Only	

6.3.18 Advanced > Trusted Computing

Feature	Options	Description
TPM20 Device Found	Info Only	
Security Device Support	**Disable** Enable	Enables or Disables BIOS support for security device. OS will not show Security Device. TCG EFI protocol and available.

6.4. Chipset

6.4.1 Chipset > System Agent (SA) Configuration

Feature	Options	Description
Memory Configuration	Submenu	Memory Configuration Parameters
Graphics Configuration	Submenu	Graphics Configuration
PEG Port Feature Configuration	Submenu	
VMD setup menu	Submenu	
PCI Express Configuration	Submenu	
Stop Grant Configuration	Auto Manual	Automatic/Manual stop grant configuration
VT-d	Disabled **Enabled**	VT-d capability
X2APIC Opt Out	**Disabled** Enabled	Enable/Disable X2APIC_OPT_OUT
DMA Control Guarantee	Disabled **Enabled**	Enable/Disable DMA_CONTROL_GRARANTEE bit
Above 4GB MMIO BIOS assignment	Disabled **Enabled**	Enable/Disable above 4GB MemoryMappedIO BIOS assignment\n\nThis is enabled automatically when Aperture Size is set to 2048MB.

6.4.1.1. Chipset > System Agent (SA) Configuration > Memory Configuration

Feature	Options	Description
Memory Configuration	Info Only	
Memory RC Version	Info Only	
Memory Speed	Info Only	
Memory Timings (tCL-tRCD-tRP-tRAS)	Info Only	
Controller 0 Channel 0 Slot 0	Info Only	
Controller 0 Channel 0 Slot 1	Info Only	
Controller 1 Channel 0 Slot 0	Info Only	
Controller 0 Channel 0 Slot 1	Info Only	
Memory Test on Warm Boot	Disabled **Enabled**	
Maximum Memory Frequency	Auto 1067 1200 1333 1467 1733 1867 2133 2267 2533 2667 **2933** 3067 1600 2000 2400	

Feature	Options	Description
	2800 3200	
Max TOLUD	**Dynamic** 1 GB 1.25 GB 1.5 GB 1.75 GB 2 GB 2.25 GB 2.5 GB 2.75 GB 3 GB 3.25 GB 3.5 GB	Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller
Controller 0,Channel 0 DIMM Control	**Enable both DIMMs** Disable DIMM0 Disable DIMM1 Disable both DIMMs	Controller 0, Channel 0 DIMM Control Support - Enable or Disable Dimms on Controller 0, Channel 0.
Controller 1,Channel 0 DIMM Control	**Enable both DIMMs** Disable DIMM0 Disable DIMM1 Disable both DIMMs	Controller 1, Channel 0 DIMM Control Support - Enable or Disable Dimms on Controller 1, Channel 0.
In-Band ECC Support	**Disabled** Enabled	Enable/Disable In-Band ECC. Either the IBECC or the TME can be enabled.

6.4.1.2. Chipset > System Agent (SA) Configuration > Graphics Configuration

Feature	Options	Description
Graphics Configuration	Info Only	
Primary Display	**Auto** IGFX PEG PCIe	Select which of IGFX/PEG/PCIe Graphics device should be Primary Display Or select HG for Hybrid Gfx.
Select PCIE Card	**Auto** Elk Creek 4 PEG Eval	Select the card used on the platform Auto : Skip GPIO based Power Enable to dGPU Elk Creek 4: DGPU Power Enable = ActiveLow PEG Eval : DGPU Power Enable = ActiveHigh
Internal Graphics	**Auto** Disabled Enabled	Keep IGFX enabled based on the setup options.
GTT Size	2MB 4MB **8MB**	Select the GTT Size
Aperture Size	128MB **256MB** 512MB 1024MB 2048MB	Select the Aperture Size
DVMT Pre-Allocated	0M 32M 46M 96M 128M **60M**	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
DVMT Total Gfx Mem	128	Select DVMT5.0 Total Graphic Memory size used by

Feature	Options	Description
	256 MAX	the Internal Graphics Device.
Intel Graphics Pei Display Peim	Enabled **Disabled**	Enable/Disable Pei (Early) Display

6.4.1.3. Chipset > System Agent (SA) Configuration > PEG Port Feature Configuration

Feature	Options	Description
PEG Port Feature Configuration	Info Only	
Detect Non-Compliance Device	**Disabled** Enabled	Detect Non-Compliance PCI Express Device in PEG

6.4.1.4. Chipset > System Agent (SA) Configuration > VMD Configuration

Feature	Options	Description
VMD Configuration	Info Only	
Enable VMD controller	**Disabled** Enabled	Enable/Disable to VMD controller

6.4.1.5. Chipset > System Agent (SA) Configuration > PCI Express Configuration

Feature	Options	Description
PCI Express Configuration	Info Only	
PCI Express Clock Gating	Disabled **Enabled**	PCI Express Clock Gating Enable/Disable for each root port.
PCI Express Power Gating	Disabled	PCI Express Power Gating Enable/Disable for each

Feature	Options	Description
	Enabled	root port.
PCIe function swap	Disabled **Enabled**	When Disabled, prevents PCIE rootport function swap. If any function other than 0th is enabled, 0th will become visible.
PCI Express Root Port 1/2/3/4	Submenu	

6.4.2 Chipset > PCH-IO Configuration

Feature	Options	Description
PCH-IO Configuration	Info Only	Memory Configuration Parameters
PCI Express Configuration	Submenu	PCI Express Configuration setting
SATA and RST Configuration	Submenu	SATA Device Options Settings
USB Configuration	Submenu	USB Configuration settings
Security Configuration	Submenu	Security Configuration setting
HD Audio Configuration	Submenu	HD Audio Subsystem Configuration Settings
Serial I/O Configuration	Submenu	Serial I/O Configuration Settings
PCH LAN Controller	Info Only	
Enable TCO Timer	Disabled Enabled	Enable/Disable TCO timer. When disabled, it disables PCH ACPI timer, stops TCO timer, and ACPI WDAT table will not be published.
Pcie Ref Pll SSC	Auto	Pcie Ref Pll SSC Percentage. AUTO - Keep hw default, no BIOS override. The range is from 0.0%-0.5%
SPD Write Disable	TRUE FALSE	Enable/Disable setting SPD Write Disable. For security recommendations, SPD write disable bit must be set.

6.4.2.1. Chipset > PCH-IO Configuration > PCIE Express Configuration

Feature	Options	Description
PCI Express Configuration	Info Only	
DMI Link ASPM Control	**Disabled** L0s L1 L0sL1 Auto	The control of Active State Power Management of the DMI Link.
Port8xh Decode	**Disabled** Enabled	PCI Express Port8xh Decode Enable/Disable
Peer Memory Write Enable	**Disabled** Enabled	Peer Memory Write Enable/Disable
Compliance Test Mode	**Disabled** Enabled	Enable when using Compliance Load Board
PCIe function swap	Disabled **Enabled**	When disabled, prevents PCIE rootport function swap. If any function other than 0th is enabled, 0th will become visible.
PCIE Ports 1-4 Configuration	**4x1 Port** 1x2 2x1 Port 2x2 Port 1x4 Port	Note: Please make sure the system boots completed after changing the configuration. Do not Attempt to Shut Down Your Computer, doing that may lead to system malfunction.
PCIE Ports 5-8 Configuration	**4x1 Port** 1x2 2x1 Port 2x2 Port 1x4 Port	Note: Please make sure the system boots completed after changing the configuration. Do not Attempt to Shut Down Your Computer, doing that may lead to system malfunction.
PCIe EQ settings	Submenu	This form contains options for controlling PCIe EQ process.

Feature	Options	Description
PCI Express Root Port 9/10/11/12/16/17/18/19	Submenu	
PCIE clocks	Submenu	

6.4.2.1.1. Chipset > PCH-IO Configuration > PCI Express Configuration > PCIe EQ settings

Feature	Options	Description
PCIe EQ override	**Disabled** Enabled	Choose your own PCIe EQ settings, only for users who have a thorough understanding of equalization process

6.4.2.1.2. Chipset > PCH-IO Configuration > PCI Express Configuration > PCIe Express Root Port 9/10/11/12/17/18/19/20

Feature	Options	Description
PCI Express Root Port 9/10/11/12/17/18/19/20	Disabled **Enabled**	Control the PCI Express Root Port.
Connection Type	Build-in **Slot**	Built-In: a built-in device is connected to this root port. Slot Implemented bit will be clear. Slot: this root port connects to user-accessible slot. Slot Implemented bit will be set.
ASPM	**Disabled** L0s L1 L0sL1 Auto	Set the ASPM Level: Force L0s – Force all links to L0s State Auto – BIOS auto configure DISABLE – Disables ASPM
L1 Substates	Disabled L1.1 L1.1 & L1.2	PCI Express L1 Substates settings.
ACS	Disabled **Enabled**	Enable/Disable Access Control Services Extended Capability

Feature	Options	Description
PTM	**Disabled** Enabled	Enable/Disable Precision Time Measurement
DPC	Disabled **Enabled**	Enable/Disable Downstream Port Containment
EDPC	Disabled **Enabled**	Enable/Disable Rootport extensions for Downstream Port Containment
URR	**Disabled** Enabled	PCI Express Unsupported Request Reporting Enable/Disable.
FER	**Disabled** Enabled	PCI Express Device Fatal Error Reporting Enable/Disable.
NFER	**Disabled** Enabled	PCI Express Device Non-Fatal Error Reporting Enable/Disable.
CER	**Disabled** Enabled	PCI Express Device Correctable Error Reporting Enable/Disable.
SEFE	**Disabled** Enabled	Root PCI Express System Error on Fatal Error Enable/Disable.
SENFE	**Disabled** Enabled	Root PCI Express System Error on Non-Fatal Error Enable/Disable.
SECE	**Disabled** Enabled	Root PCI Express System Error on Correctable Error Enable/Disable.
PME SCI	Disabled **Enabled**	PCI Express PME SCI Enable/Disable.
Hot Plug	**Disabled** Enabled	PCI Express Hot Plug Enable/Disable.
Advanced Error Reporting	Disabled **Enabled**	Advanced Error Reporting Enable/Disable.

Feature	Options	Description
PCIe Speed	**Auto** Gen1 Gen2 Gen3	Configure PCIe Speed
Transmitter Halt Swing	**Disabled** Enabled	Transmitter Half Swing Enable/Disable.
Detect Timeout	0	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.
Extra Bus Reserved	0	Extra Bus Reserved (0-7) for bridges behind this Root Bridge.
Reserved Memory	10	Reserved Memory for this Root Bridge (1-20) MB
Reserved I/O	4	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.
PCH PCIe LTR Configuration	Info Only	
LTR	Disabled **Enabled**	PCH PCIE Latency Reporting Enable/Disable
Snoop Latency Override	Disabled Manual **Auto**	Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Non-Snoop Latency Override	Disabled Manual **Auto**	Non-Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manual enter override values. Auto (default): Maintain default bios flow.
Force LTR Override	**Disabled** Enabled	Force LTR Override for PCH PCIE.
LTR Lock	**Disabled** Enabled	PCIE LTR Configuration Lock

6.4.2.1.3. Chipset > PCH-IO Configuration > PCI Express Configuration > PCIE clocks

Feature	Options	Description
Clock0-15 assignment	Platform-POR **Enabled** Disabled	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock0-15	**Platform-POR** Disabled	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.

6.4.2.2. Chipset > PCH-IO Configuration > SATA And RST Configuration

Feature	Options	Description
SATA and RST Configuration	Info Only	
SATA Controller	**Enabled** Disabled	Enable/Disable SATA Device.
SATA Mode Selection	**AHCI** Intel RST Premium with Intel Optane System Acceleration	Determines how SATA controller(s) operate.
SATA Test Mode	Enabled **Disabled**	Test Mode Enable/Disable (Loop Back).
Software Feature Mask Configuration	Submenu	RST Legacy OROM/RST UEFI driver will refer to the SWFM configuration to enable/disable the storage features.
Aggressive LPM Support	Disabled **Enabled**	Enable PCH to aggressively enter link power state.
SATA Controller Speed	Default Gen1 **Gen2** Gen3	

Feature	Options	Description
Serial ATA Port x	Info Only	
Software Preserve	Info Only	
Port x	Disabled **Enabled**	Enable or Disable SATA Port
Hot Plug	**Disabled** Enabled	Designates this port as Hot Pluggable.
Configured as eSATA	Info Only	
External	**Disabled** Enabled	Marks this port as external.
Spin Up Device	**Disabled** Enabled	If enabled for any of ports Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise, all drives spin up at boot.
SATA Device Type	**Hard Disk Drive** Solid State Drive	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive
Topology	**Unknown** ISATA Direct Connect Flex M2	Identify the SATA Topology if it is Default or ISATA or Flex or Direct Connect or M2
SATA Portx DevSlp	**Disabled** Enabled	Enable/Disable SATA Port 0 DevSlp. For DevSlp to work, both hard drive and SATA port need to support DevSlp function, otherwise an unexpected behavior might happen. Please check board design before enabling it.
DITO Configuration	**Disabled** Enabled	Enable/Disable DITO Configuration
DITO value	Info Only	
DM Value	Info Only	

6.4.2.2.1. Chipset > PCH-IO Configuration > SATA Configuration > Software Feature Mask Configuration

Feature	Options	Description
Software Feature Mask Configuration	Info Only	
HDD Unlock	Disabled **Enabled**	If enabled, indicates that the HDD password unlock in the OS is enabled.
LED Locate	Disabled **Enabled**	If enabled, indicates that the LED/SGPIO hardware is attached and ping to locate feature is enabled on the OS.

6.4.2.3. Chipset > PCH-IO Configuration > USB Configuration

Feature	Options	Description
USB2 PHY Sus Well Power Gating	GEN1 **GEN2**	Select 'Enabled' to enable SUS Well PG for USB2 PHY. This option has no effect on PCH-H
USB3 Link Speed Selection	Disabled **Enabled**	This option is to select USB3 Link Speed GEN1 or GEN2
USB PD0 Programming	Disabled **Enabled**	Select 'Enabled' if Port Disable Override functionality is used.
XHCI LTR Mode	Disabled **Enabled**	Enable/Disable XHCI LTR Mode
USB Overcurrent	Disabled **Enabled**	Select 'Disabled' for pin-based debug. If pin-based debug is enabled but USB overcurrent is not disabled, USB DbC does not work.
USB Overcurrent Lock	Disabled **Enabled**	Select 'Enabled' if Overcurrent functionality is used. Enabling this will make xHCI controller consume the Overcurrent mapping data
USB Port Disable Override	**Disabled** Select Per-Pin	Selectively Enable/Disable the corresponding USB port from reporting a Device Connection to the controller.

6.4.2.4. Chipset > PCH-IO Configuration > Security Configuration

Feature	Options	Description
Security Configuration	Info Only	
RTC Memory Lock	Disabled **Enabled**	Enable will lock bytes 38h-3Fh in the lower/upper 128-byte bank of RTC RAM
BIOS Lock	**Disabled** Enabled	Enable/Disable the PCH BIOS Lock Enable feature. Required to be enabled to ensure SMM protection of flash.
Force unlock on all GPIO pads	**Disabled** Enabled	If Enabled BIOS will force all GPIO pads to be in unlocked state

6.4.2.5. Chipset > PCH-IO Configuration > HD Audio Configuration

Feature	Options	Description
HD Audio Subsystem Configuration Settings	Info Only	
HD Audio	Disabled **Enabled**	Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HDA will be unconditionally enabled.

6.4.2.6. Chipset > PCH-IO Configuration > Serial I/O Configuration

Feature	Options	Description
Serial I/O Configuration	Info Only	
I2C0 Controller	Disabled **Enabled**	Enables/Disables Serial I/O Controller
I2C1 Controller	**Disabled** Enabled	Enables/Disables Serial I/O Controller

Feature	Options	Description
I2C2 Controller	**Disabled** Enabled	Enables/Disables Serial I/O Controller
I2C3 Controller	**Disabled** Enabled	Enables/Disables Serial I/O Controller
I2C4 Controller	**Disabled** Enabled	Enables/Disables Serial I/O Controller
I2C5 Controller	**Disabled** Enabled	Enables/Disables Serial I/O Controller
I2C6 Controller	**Disabled** Enabled	Enables/Disables Serial I/O Controller
I2C7 Controller	**Disabled** Enabled	Enables/Disables Serial I/O Controller
SPI0 Controller	**Disabled** Enabled	Enables/Disables Serial I/O Controller
SPI1 Controller	Disabled Enabled	Enables/Disables Serial I/O Controller
SPI2 Controller	**Disabled** Enabled	Enables/Disables Serial I/O Controller
SPI3 Controller	**Disabled** Enabled	Enables/Disables Serial I/O Controller
UART0 Controller	**Disabled** Enabled Communication port (COM)	Enables/Disables Serial I/O Controller
UART1 Controller	**Disabled** Enabled Communication port	Enables/Disables Serial I/O Controller

Feature	Options	Description
	(COM)	
UART2 Controller	**Disabled** Enabled Communication port (COM)	Enables/Disables Serial I/O Controller
UART3 Controller	**Disabled** Enabled Communication port (COM)	Enables/Disables Serial I/O Controller
UART4 Controller	**Disabled** Enabled Communication port (COM)	Enables/Disables Serial I/O Controller
UART5 Controller	**Disabled** Enabled Communication port (COM)	Enables/Disables Serial I/O Controller
UART6 Controller	**Disabled** Enabled Communication port (COM)	Enables/Disables Serial I/O Controller
Serial I/O D3 State	Disabled **Enabled**	Enable/Disable Serial I/O D3 State
GPIO IRQ Route	**IRQ14** IRQ15	Route all GPIOs to one of the IRQ.
Serial I/O I2C0 Settings	Submenu	Configure Serial I/O Controller
Serial I/O I2C2 Settings	Submenu	Configure Serial I/O Controller
Serial I/O I2C3 Settings	Submenu	Configure Serial I/O Controller

Feature	Options	Description
Serial I/O I2C4 Settings	Submenu	Configure Serial I/O Controller
Serial I/O I2C5 Settings	Submenu	Configure Serial I/O Controller
WITT/MITT I2C Test Device	**Disabled** Enabled	Enable SIO I2C WITT Device and select which are all controller used it
UART Test Device	**Disabled** Enabled	Enable SIO UART Test Device and select which are all controller used it
Additional Serial I/O devices	**Disabled** Enabled	When enabled, ACPI will report additional devices connected to Serial I/O.
Serial I/O timing parameters	Disabled **Enabled**	Enables additional timing parameters for all Serial I/O controllers.

6.4.2.6.1. Chipset > PCH-IO Configuration > Serial I/O Configuration > Serial I/O I2C0/I2C2/I2C3/I2C4/I2C5 Settings

Feature	Options	Description
Serial io I2C0/I2C2/I2C3/I2C4/I2C5 Settings	Info Only	
Serial IO Touch Pad Settings	Submenu	
Timing parameters	Info Only	

6.4.2.6.1.1. Chipset > PCH-IO Configuration > Serial I/O Configuration > Serial I/O I2C0/I2C2/I2C3/I2C4/I2C5 Settings > Serial I/O Touch Pad Settings

Feature	Options	Description
Touch Pad	**Disabled** Synaptics Precision Touchpad Synaptics Forcepad ALPS Precision Touchpad ClickPad Custom Device	Indicates what type of I2C Touch Pad is connected to this Serial I/O controller

6.5. Security Menu

6.5.1 Security > Password Description

Feature	Options	Description
Password Description	Info only	
Setup Administrator Password	Enter Password	Set Setup Administrator Password
User Password	Enter Password	Set User Password
Secure Boot	Submenu	Customizable Secure Boot settings.
System Mode	Info only	
Secure Boot	Info only	
Secure Boot Control	**Disabled** Enabled	Secure Boot activated when Platform Key (PK) is enrolled, System mode is User / Deployed, and CSM function is disabled

6.6. Boot Menu

6.6.1 Boot > Boot Configuration

Feature	Options	Description
Boot Configuration	Info only	
Setup Prompt Timeout	**1**	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
Bootup NumLock State	**On** Off	Select the keyboard Number state.
Quiet Boot	Disabled **Enabled**	Select the keyboard NumLock state.
Fast Boot	Disabled **Enabled**	Enable or Disable FastBoot features. Most probes are skipped to reduce time cost during boot.
SATA Support	**Last Boot SATA Devices Only** All SATA Devices	If Last Boot SATA Devices Only, only last boot SATA device will be available in Post. If All SATA Devices, all SATA devices will be available in OS and Post.
VGA Support	Auto **EFI Driver**	If Auto, only install Legacy OpRom with Legacy OS and logo would NOT be shown during post. Efi driver will still be installed with EFI OS.
PS2 Devices Support	Disabled **Enabled**	If disabled, PS2 devices will be skipped.
Network Stack Driver Support	**Disabled** Enabled	If disabled, the Network Stack Driver will be skipped.
Redirection Support	Disabled **Enabled**	If disabled, the Redirection function will be disabled.

6.6.2 Boot > FIXED BOOT ORDER Priorities

Feature	Options	Description
Boot Option #1	Hardware	Set the system boot order.
Boot Option #2	CD/DVD	Set the system boot order.
Boot Option #3	USB Hard Disk	Set the system boot order.
Boot Option #4	USB CD/DVD	Set the system boot order.
Boot Option #5	USB Key	Set the system boot order.
Boot Option #6	USB Floppy	Set the system boot order.
Boot Option #7	USB Lan	Set the system boot order.
Boot Option #8	Network	Set the system boot order.

6.7. Save & Exit Menu

6.7.1 Save and Exit

Feature	Options	Description
Save Changes and Exit		Exit system setup after saving the changes.
Discard Changes and Exit		Exit system setup without saving any changes.
Save Change and Reset		Reset the system after saving the changes.
Discard Changes and Reset		Reset system setup without saving any changes.
Save Options	Info only	
Save Changes		Save Changes done so far to any of the setup options.
Save as User Defaults		Save the changes done so far as User Defaults.
Restore User Defaults		Restore the User Defaults to all the setup options.
Boot Override	Info only	

7. BIOS Checkpoints, Beep Codes

A status code is a data value used to provide diagnostic information about the boot process. Progress codes are status codes that signify successful progression to a following initialization step. Error codes signify error conditions encountered in the process of system initialization. The Aptio 5.x core can be configured to send status codes to a variety of sources. The two most commonly used types of status codes are checkpoint codes and beep codes. Checkpoint codes are byte length data values. Checkpoints are typically output to I/O port 80h, but the Aptio 5.x core can be configured to send checkpoints to a variety of sources. The Aptio 5.x core outputs checkpoints throughout the boot process to indicate the task the system is currently executing. Checkpoints are very useful in aiding software developers or technicians in debugging problems that occur during the pre-boot process on production hardware. A beep code is a series of short sound signals. Beep codes are typically error codes that do not occur during normal boot process.

Note: Beep codes are not the only sounds generated during the boot process. Some firmware components may use sounds to notify the user about other events such as detection of a hot-pluggable device. These sounds are typically generated using a frequency that is different from the frequency of the beep codes

Viewing Checkpoints

Checkpoints generated by the Aptio firmware can be viewed using a PCI checkpoint card, also referred to as a "POST Card" or "POST Diagnostic Card". These PCI add-on cards show the value of I/O port 80h on an LED display.

Aptio V Checkpoint and Beep Codes

Download the Aptio V Checkpoint and Beep Codes from the AMI website at: www.ami.com/download/aptio-v-checkpoint-and-beep-codes

8. Software Support

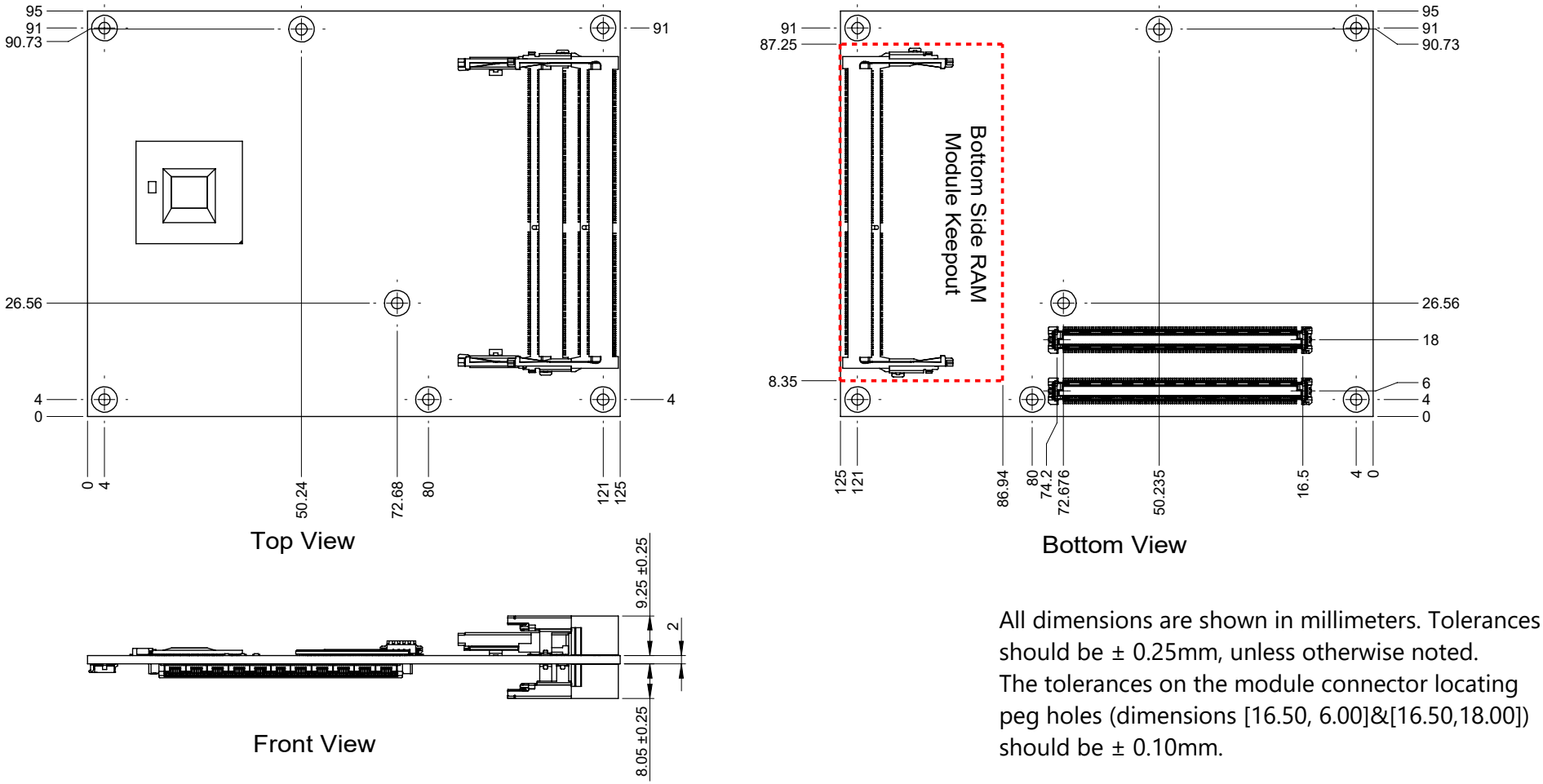
8.1. Windows 10 IoT Enterprise 64-bit

8.2. Yocto Linux 64-bit

https://github.com/ADLINK/meta-adlink-x86-64bit (TBC)

9. Mechanical and Thermal

9.1. Module Dimensions



All dimensions are shown in millimeters. Tolerances should be ± 0.25mm, unless otherwise noted.
The tolerances on the module connector locating peg holes (dimensions [16.50, 6.00]&[16.50,18.00]) should be ± 0.10mm.

Dimensions: mm

Figure 6 – Module mechanical dimensions

9.2. Thermal Solutions

9.2.1 Heatspreader: HTS

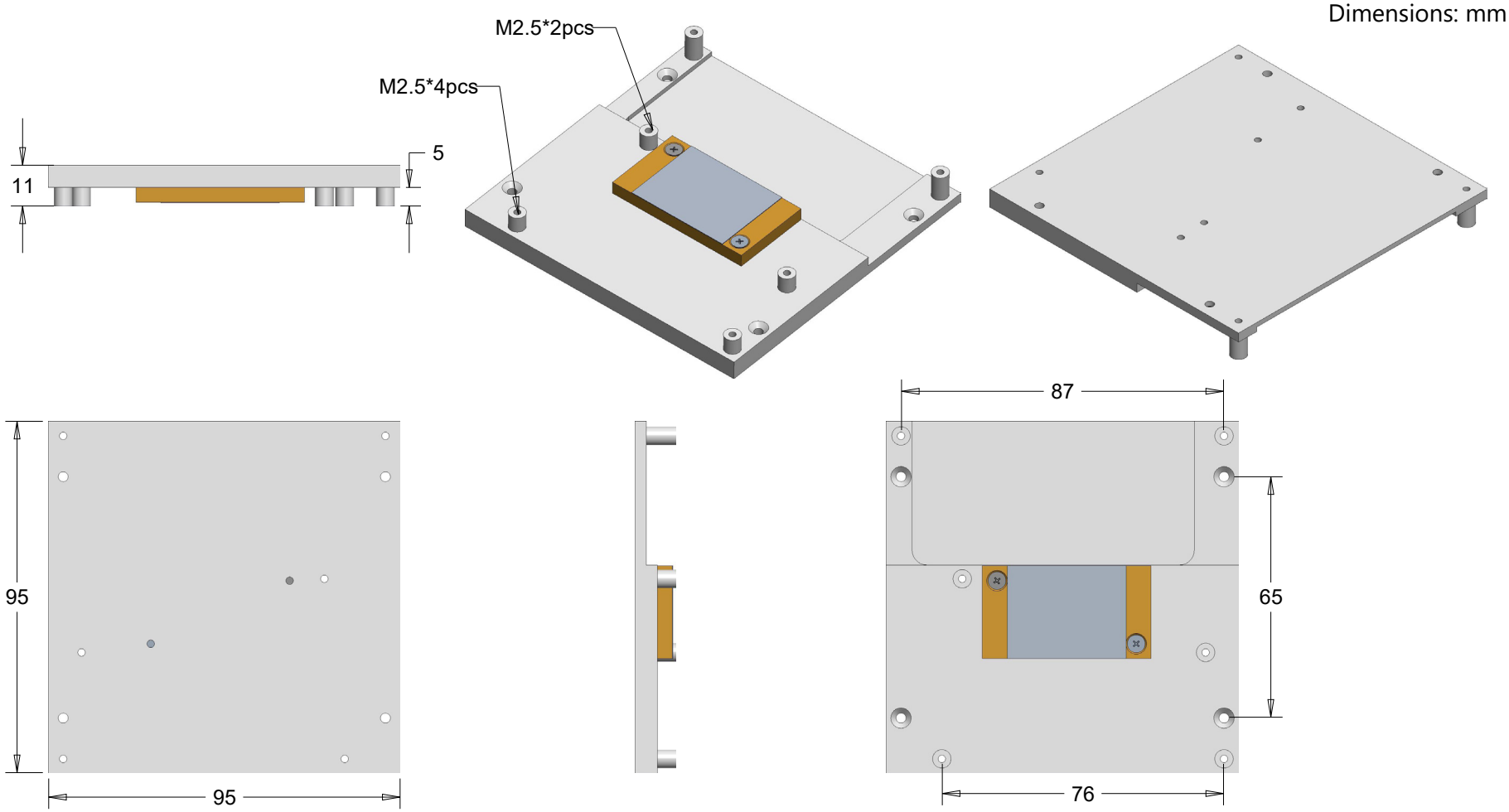


Figure 7 – Heatspreader: HTS

9.2.2 Heatsink: THS

Dimensions: mm

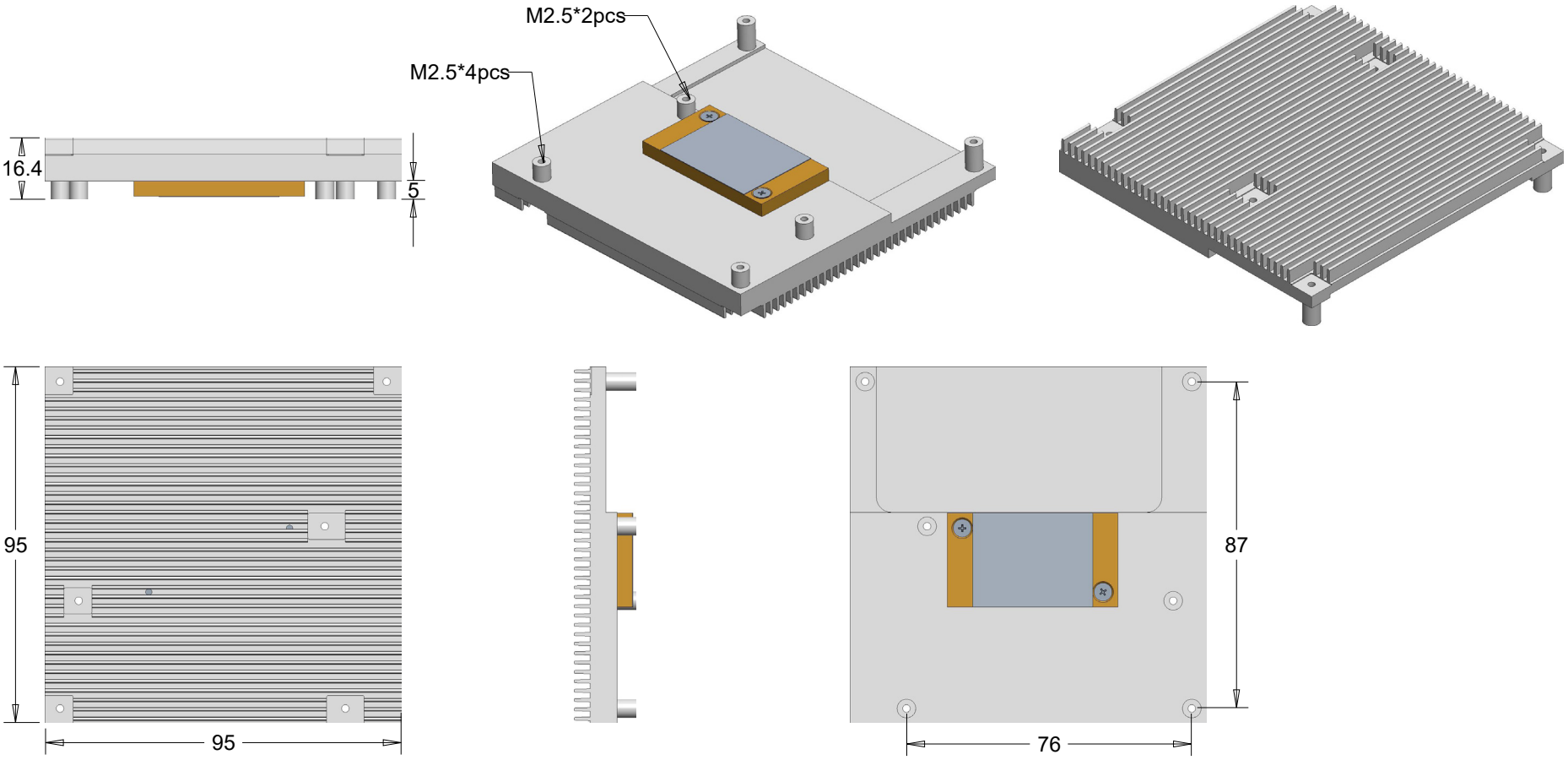


Figure 8 – Heatsink: THS

9.2.3 Heatsink High Profile: THSH

Dimensions: mm

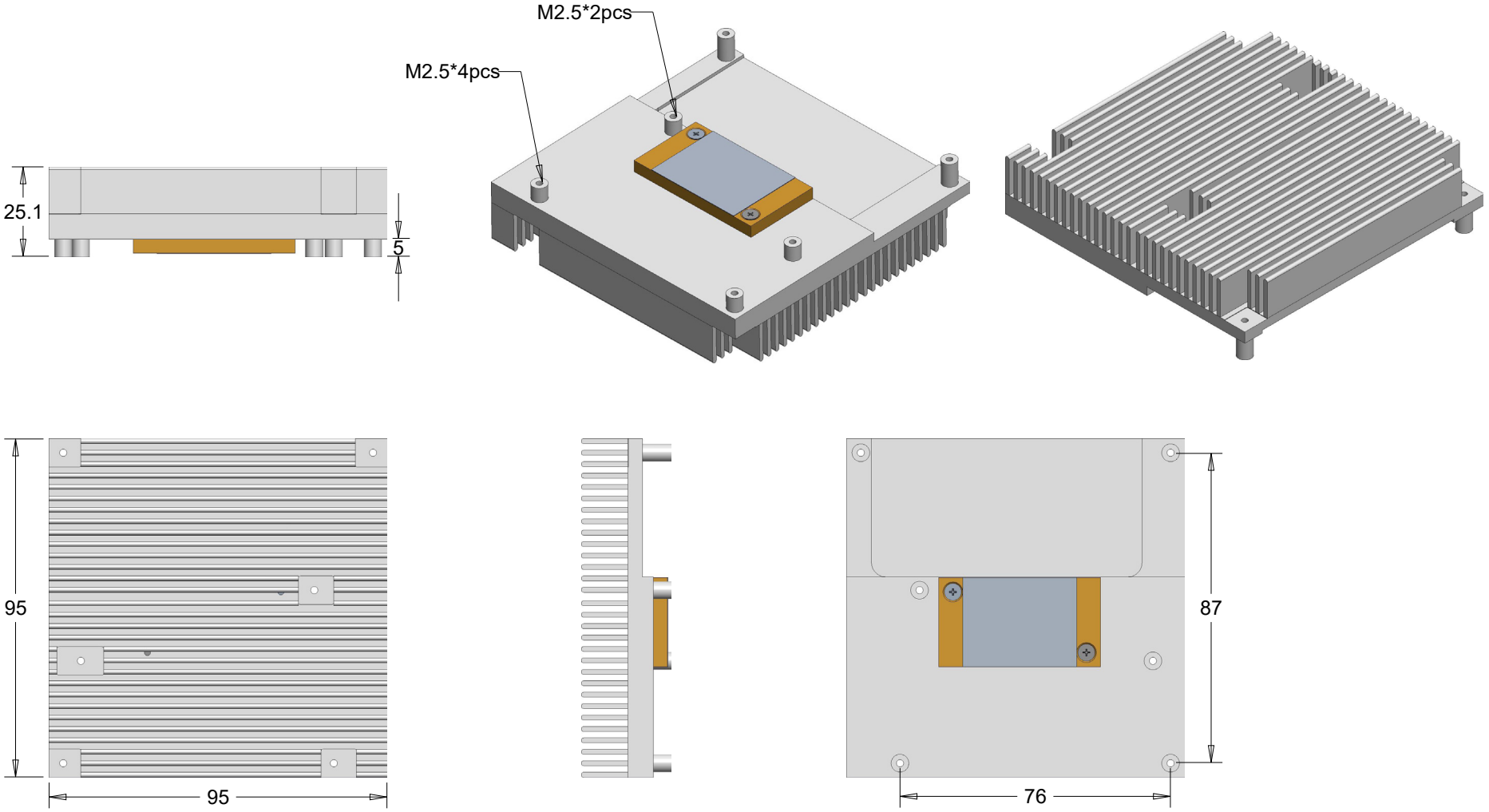


Figure 9 – Heatsink High Profile: THSH

9.2.4 Heatsink with Fan: THSF

Dimensions: mm

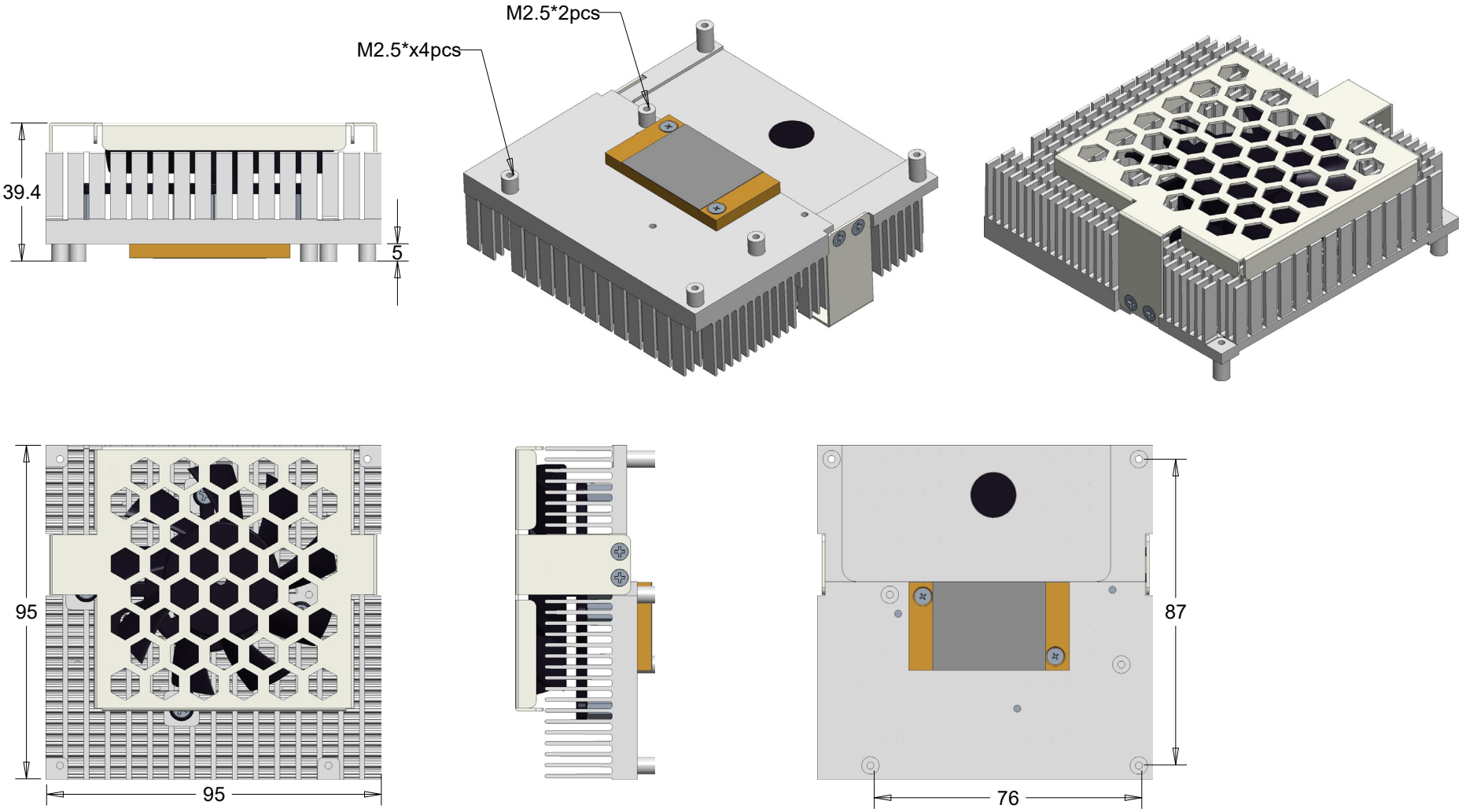


Figure 10 – Heatsink with Fan: THSF