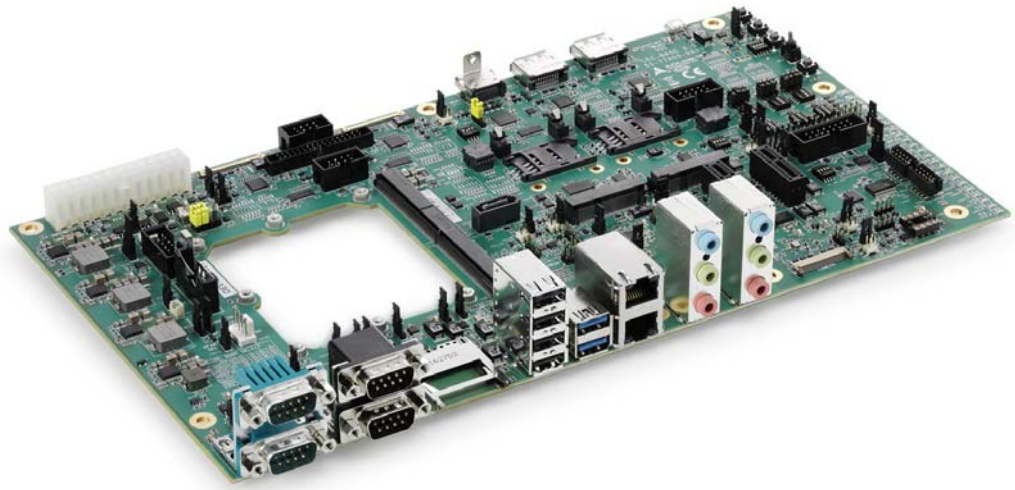
LEC-BASE 2.0

Technical Reference

Low Energy Computer-On-Module Carrier



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Leading **EDGE COMPUTING**

Preface

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Revision History

Revision	Date	Description of Change(s)
1.1	4/19/2018	Initial Release

Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

Environmental Responsibility

ADLINK is committed to fulfill its social responsibility to global environmental preservation through compliance with the European Union's Restriction of Hazardous Substances (RoHS) directive and Waste Electrical and Electronic Equipment (WEEE) directive. Environmental protection is a top priority for ADLINK. We have enforced measures to ensure that our products, manufacturing processes, components, and raw materials have as little impact on the environment as possible. When products are at their end of life, our customers are encouraged to dispose of them in accordance with the product disposal and/or recovery programs prescribed by their nation or company.

Important Safety Instructions

For user safety, please read and follow all **Instructions**, **WARNINGs**, **CAUTIONs,** and **NOTEs** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

Conventions

The following conventions may be used throughout this manual, denoting special levels of information.

This information adds clarity or specifics to text and illustrations.

This information indicates the possibility of ***minor*** physical injury, component damage, data loss, and/or program corruption.

This information warns of possible ***serious*** physical injury, component damage, data loss, and/or program corruption.

Table of Contents

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1 Product Overview

This chapter presents a general overview of the LEC-BASE 2.0 carrier. After reviewing this chapter you should understand the following aspects of the LEC-BASE 2.0 carrier board.

- Carrier Description
- I/O Feature List
- Functional Block Diagram
- Carrier Specifications

1.1 Carrier Description

The ADLINK LEC-BASE 2.0 is a host carrier board for ADLINK's SMARC modules and serves as reference design for SMARC modules conforming to the SMARC 2.0 specification. The SMARC module plugs directly into the LEC-BASE 2.0 where the carrier board becomes a design platform for testing and developing your applications. Figure 1-1 provides an overview of the LEC-BASE 2.0 with call outs of its interface hardware. The proceeding sections and chapters in this manual present these features in more detail.

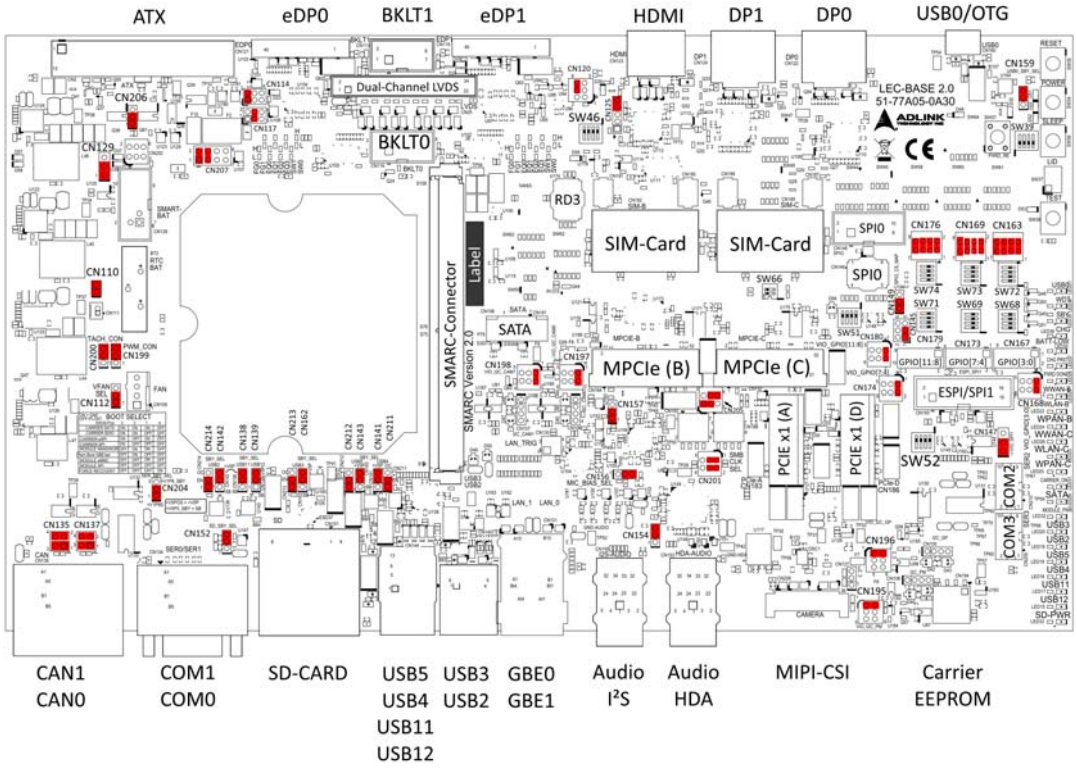


Figure 1-1: LEC-BASE 2.0 IO Overview

The ADLINK LEC-BASE 2.0 supports the features of SMARC Hardware Specification version 2.0 The following section presents the list of features for the LEC-BASE 2.0.

1.2 Features

- SMARC interface MXM3 connector
- PCI Express Bus
  - 2x PCIe x1 slots
  - 2x PCIe Mini slots
- Serial Port UART interfaces (4x UART)
  - Null Modem RS-232 on serial ports COM0 - COM3
  - 2-wire and 4-wire connectors
  - COM0 - COM3 interfaces on two 9-pin, DB9 connectors and two 10-pin headers
- USB interfaces
  - One USB 4-connector stack for ports 4-5 and 11-12 (USB 2.0)
  - One USB 2-connector stack for ports 2-3 (USB 3.0/2.0)
  - One micro-USB connector for port 0 OTG or client (USB 2.0)
  - Two USB 2.0 ports (13-14) on the two Mini PCIe slots
- Gigabit Ethernet interface
  - Two standard RJ-45 connectors (two-port stack)
  - Activity/Link and Speed LEDs on Ethernet connectors
- SDIO interface
  - One SDIO slot, 4-bit (for SD card)
- Audio interfaces
  - Supports HD Audio and AC'97
  - One 3-in-1 stack audio jack for I2S audio with Line In / Line Out / MIC In
  - One 3-in-1 stack audio jack for HD audio with Line In / Line Out / MIC In
- Video interfaces
  - One standard HDMI connector for HDMI interface
  - Two standard DisplayPort connectors (DP)
  - Two standard embedded DisplayPort connectors (eDP)
  - One dual-channel LVDS header (18/24-bit)
  - Two LVDS backlight headers
- Power interface
  - One ATX-2.2 Power In connector (+12V and +5V)
  - Interface voltages are generated on the carrier (+3.3V, +1.8V, and +1.5V)
  - Optional: BattMan power supply
- Camera interface
  - One MIPI-CSI, 36-pin Flat Foil connector
  - Two MIPI-CSI interfaces on the connector
  - Two I^2C camera interfaces
- Fan interfaces
  - One fan power selection (12V or 5V) jumper header
  - One fan interface header
- SATA interfaces
  - One standard SATA3 connector (SATA0)
  - One SATA Activity LED

- I^2C interfaces
  - One General Purpose I^2C interface
  - Two I^2C camera interfaces
  - One I^2C Power Management interface
- CAN interface
  - Two CAN DB9 connectors (stack)
- SPI interfaces
  - One SPI interface header
  - One eSPI/SPI header
- Miscellaneous
  - Twelve GPIOs (interrupt capable)
  - Watchdog LED
  - Smart Battery Connector
  - RTC Battery Socket
  - Power Button
  - Reset Button
  - Sleep Button
  - Test Button
  - LID Switch
  - Boot Select Switch

1.3 Ordering Information

Table 1-1: LEC-BASE 2.0 Models

Model Number	Description
LEC-BASE 2.0 (91-77A05-000E or higher)	SMARC evaluation carrier board for SMARC 2.0 compliant modules

1.4 Block Diagram

Figure 1-2 presents a functional representation of the carrier.

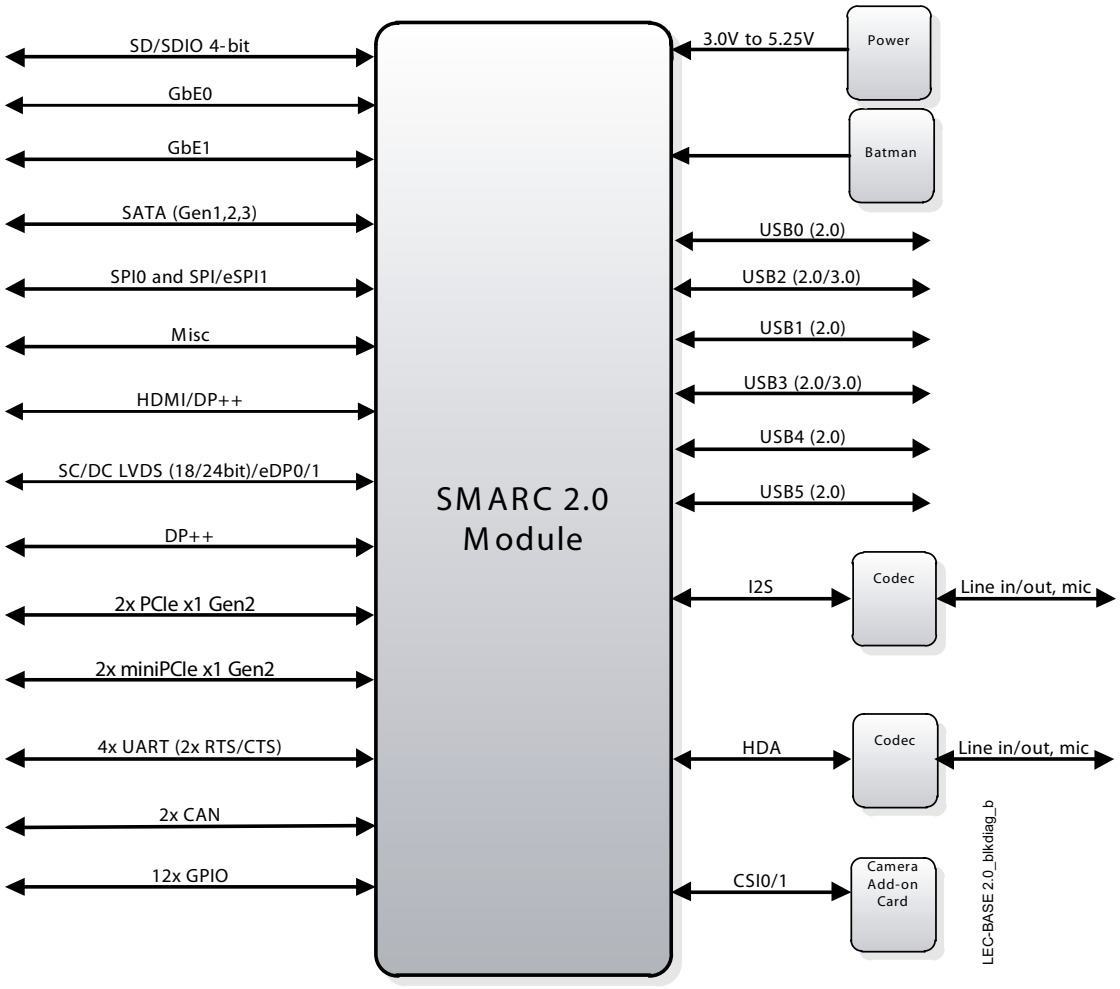


Figure 1-2: Functional Block Diagram

1.5 Specifications

1.5.1 Physical

Table 1-2 lists the physical dimensions of the carrier.

Table 1-2: Weight and Footprint Dimensions

Item	Dimension	
Weight	0.42 kg (0.93 lb)	Overall height is measured from the upper board surface to the top of the highest permanent component on the upper board surface. This measurement does not include the cooling solution, which can vary. The cooling solution will probably increase this dimension.
Height (overall)	37.70 mm (1.48 inches)	
Board thickness	2.00 mm (0.08 inches)	
Width	170.00 mm (6.69 inches)	
Length	304.80 mm (12.00 inches)	

1.5.2 Electrical

Table 1-3 specifies the voltage inputs of the carrier.

Table 1-3: Carrier Voltage Inputs

Parameter	Value
Standard	12V +/-5% and 5V +/-5% from ATX connector
RTC	3.0V, 2.0V to 3.3V (battery), +/-20mV ripple
BattMan Supply	12V +/-5% (3A max), 5.0V +/-5% (4A max), +/-50mV ripple

1.5.3 Environmental

Most components on the LEC-BASE 2.0 carrier are selected as extended temperature range parts (-40°C to +85°C). Some components are not available in this temperature range. In these cases, the component temperature ranges are narrower. The LEC-BASE 2.0 is validated in the -40°C to +85°C range.

The overall system performance depends on the combination of module and carrier subsystems. Some SMARC modules are available in the industrial temperature range. Others are commercial temperature range parts. Similar considerations apply to any of the add-on cards or peripherals that are used with the LEC-BASE 2.0.

Table 1-4 defines the environmental conditions under which the carrier is qualified to operate and to be stored.

Table 1-4: Validated Temperature and Humidity Ranges

Parameter	Value
Temperature ▶ Operating ▶ Storage	 ▶ -40°C to +85°C ▶ -55°C to +85°C
Humidity ▶ Operating ▶ Non-operating	 ▶ 5% to 90% relative humidity, non-condensing ▶ 5% to 95% relative humidity, non-condensing

1.5.4 Mechanical

Figure 1-3 provides the mechanical dimensions and mounting hole sizes of the LEC-BASE 2.0. The LEC-BASE 2.0 can be mounted to a chassis using M4, B-head screws. Mezzanine cards can be mounted to the carrier using female-female standoffs with M2.5 threads and M2.5, B-head screws.

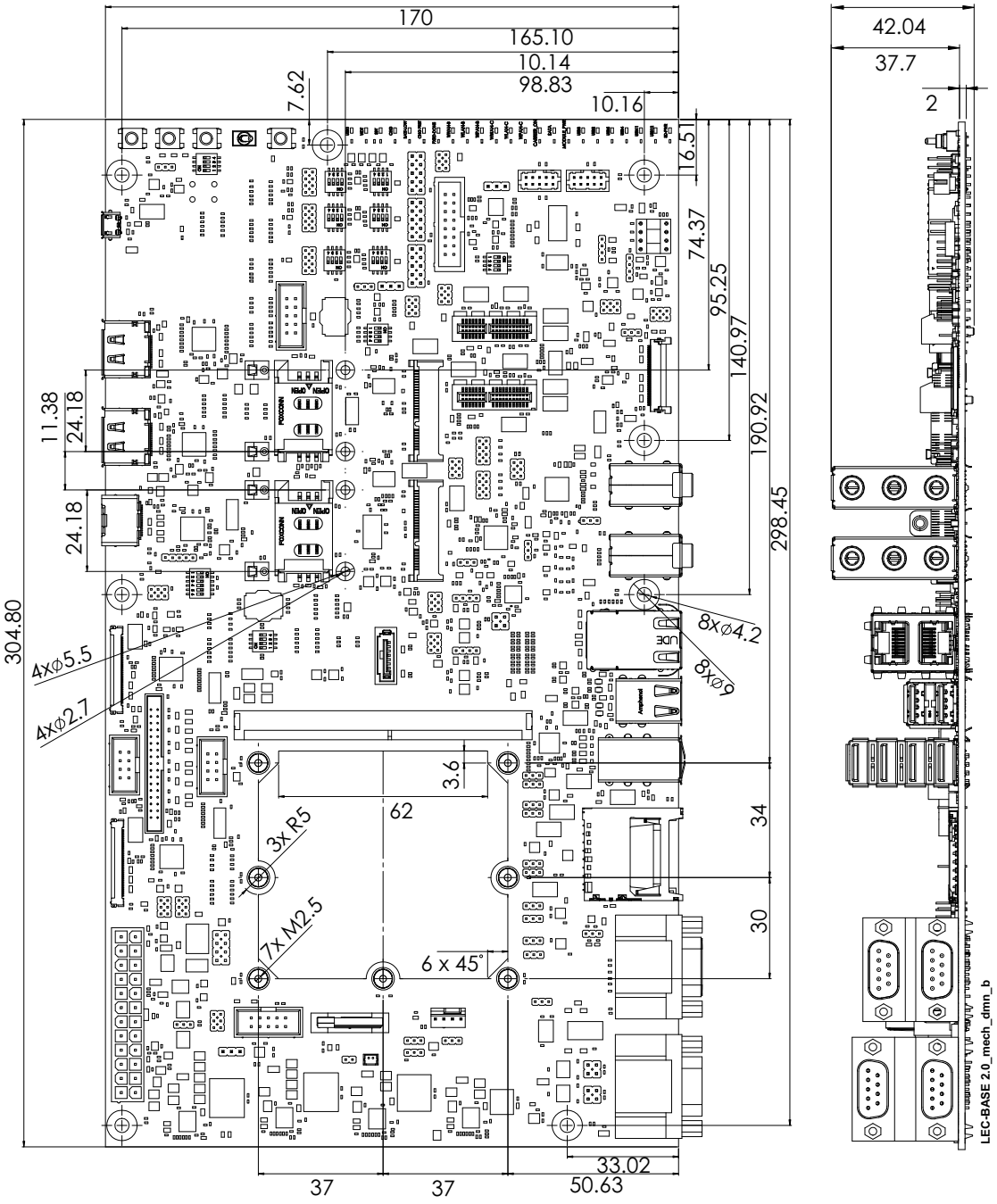


Figure 1-3: Mechanical Dimensions (Top Side)

2 Hardware

This chapter describes the physical specifications of the interface connectors, headers, LEDs, and switches on the LEC-BASE 2.0. The second section of this chapter, titled Standard Hardware References, further describes the industry standard IO hardware on the carrier.

2.1 Interface Headers, Jumper Headers, Switches, LEDs, and Connectors

This section describes and illustrates the connectors, switches, and LEDs on the LEC-BASE 2.0. Table 2-1 lists and specifies these components, providing the PCB designator, signal name, and description of each component. Figure 2-1, Figure 2-2 (PCB designator key), Figure 2-3, and Figure 2-4 appear after Table 2-1 and illustrate the locations of these user interface components.

Table 2-1: Header, Switch, LED, and Connector Descriptions

PCB Designator	Signal / Device	Pinout Link	Description
BT2	Battery Socket	“Battery Socket” on page 22	3-pin socket for CR2032 batteries that run at 3V [LOTES, AAA-BAT-038-K01, BK]
CN2	ATX Power	Table 3-12	24-pin standard ATX power input connector [ALEX, 9359-24, NATURAL]
CN25	LVDS	Table 3-19	34-pin, 2.0mm header for LVDS output [JIHVEI, 23N6850-34S10B-01G-G, BLACK]
CN105	I2C GP	Table 3-33	4-pin, 2.0mm header for I2C general purpose signals [JIH VEI, 21N12050-04S10B-01G-4/2.8-G]
CN106	I2C CAM0	Table 3-34	4-pin, 2.0mm header for I2C camera 0 signals [JIH VEI, 21N12050-04S10B-01G-4/2.8-G]
CN107	I2C CAM1	Table 3-35	4-pin, 2.0mm header for I2C camera 1 signals [JIH VEI, 21N12050-04S10B-01G-4/2.8-G]
CN108	I2C PM	Table 3-36	4-pin, 2.0mm header for I2C power management signals [JIH VEI, 21N12050-04S10B-01G-4/2.8-G]
CN109	Fan	Table 3-42	4-pin, 2.54mm header for CPU fan signals [JVE, 24W1163-04S10-01T-02]
CN110	Battery Enable	Table 3-14	2-pin, 2.0mm jumper header to enable RTC coin cell battery [JIH21N12050-02S10B-01G-4/2.8-G]
CN111	Battery Interface	Table 3-13	2-pin, 1.25mm shrouded header for external backup battery [REGO, 830-1251-02STD-3.2-6T]
CN112	Fan Voltage Select	Table 3-43	3-pin, 2.0mm jumper header to select FAN supply voltage [JIH21N12050-03S10B-01G-4/2.8-G]
CN113	LVDS Backlight 1	Table 3-21	8-pin, 2.54mm shrouded header for LVDS backlight 1 interface [JIHVEI, 23N6960-08S10B-01G-G, BLACK]
CN114	LVDS +VCC Voltage Select	Table 3-22	6-pin, 2mm jumper header for selecting display +VCC LVDS voltages [JIH21N22050-06S10B-01G-4/2.8-G]
CN116	LVDS Backlight 0	Table 3-20	8-pin, 2.54mm shrouded header for LVDS backlight 0 interface [JIHVEI, 23N6960-08S10B-01G-G, BLACK]
CN117	LVDS +VDD Voltage Select	Table 3-23	6-pin, 2.0mm jumper header for selecting display +VDD LVDS voltages [JIH21N22050-06S10B-01G-4/2.8-G]
CN118	eDP1	Table 3-27	40-pin, 0.50mm right-angle, standard connector for embedded DisplayPort1 interface [I-PEX, 20455-040E-12]

Table 2-1: Header, Switch, LED, and Connector Descriptions (Continued)

PCB Designator	Signal / Device	Pinout Link	Description
CN120	LVDS / eDP Mode Select	Table 3-24	6-pin, 2.0mm jumper header for selecting between LVDS and embedded DisplayPort display modes [NELTRON, 2208SM-06G-CR]
CN121	eDP0	Table 3-26	40-pin, 0.50mm right-angle, standard connector for embedded DisplayPort0 interface [I-PEX, 20455-040E-12]
CN122	DP++0	Table 3-31	20-pin, right-angle standard connector for Dual-Mode DisplayPort 0 signals [FOXCONN, 3VD51203-D7JJ-7H, BLACK]
CN123	HDMI	Table 3-28	19-pin, right-angle Type A, standard connector for HDMI signals [FOXCONN, QJ51191-WED5-4F]
CN124	DP++1	Table 3-32	20-pin, right-angle standard connector for Dual-Mode DisplayPort 1 signals [FOXCONN, 3VD51203-D7JJ-7H, BLACK]
CN125	HDMI / DP1 Mode Select	Table 3-30	5-pin, 2.0mm jumper header for selecting between HDMI and DisplayPort1 display modes [SAMTEC, TMM-105-03-LM-S]
CN127	CAM0_GPIO / CAM1_GPIO	Table 3-45	3-pin, 2.0mm header to connect optional CAM0 and CAM1 GPIO signals [JIH21N12050-03S10B-01G-4/2.8-G]
CN128	BattMan	Table 3-15	10-pin, 2.54 box header for BattMan smart battery signals [JIHVEI, 23N6960-10S10B-01G-G, BLACK]
CN129	BattMan SMBus Voltage Select	Table 3-16	3-pin, 2.54mm jumper header for selecting voltages for the SMBus interface toward the SMART Battery. [JIH, 21N12564-03S10B-01G-6/3-G]
CN130	IEEE 1588 Trigger	Table 3-46	4-pin, 2.54mm header for the IEEE 1588 (Precision Time Protocol) function on the module's Ethernet controller, if supported. The signal level is always 3.3V. [JIH, 21N22564-04S10B-01G-6/3-G]
CN131	GbE 0 / 1 Dual Stack	See GbE Specification	16-pin standard, RJ45 connector with LEDs for Gigabit Ethernet ports 0 and 1 [UDE, RM3-168AT9VQ, BLACK]
CN134	COM0 [bottom] / COM1 [top]	Table 3-47	9-pin standard, stacked DB9 connectors for RS232 serial ports with 2-wire and 4-wire, RX/TX and RTS/CTS support [AMPHENOL, G17H1110131EU]
CN135	CAN1 Termination Select	Table 3-55	4-pin, 2.54mm jumper header for selecting CAN1 termination schemes [JIH, 21N22564-04S10B-01G-6/3-G] NOTE: Default: 120 Ohm line termination Option: 2x 60 Ohm GND centered termination
CN136	CAN0 [bottom] / CAN1 [top]	Table 3-52	9-pin, standard dual DB9 connectors for transmitting and receiving Controller Area Network signals [FOXCONN, DM10151-H531-4F, TEAL]
CN137	CAN0 Termination Select	Table 3-53	4-pin, 2.54mm jumper header for selecting CAN0 termination schemes [JIH, 21N22564-04S10B-01G-6/3-G] NOTE: Default: 120 Ohm line termination Option: 2x 60 Ohm GND centered termination

Table 2-1: Header, Switch, LED, and Connector Descriptions (Continued)

PCB Designator	Signal / Device	Pinout Link	Description
CN138	USB11 Wake / No Wake Select	Table 3-1	3-pin, 2.0mm jumper header to select between Wake and No Wake from sleep states for the USB11 port [JIH21N12050-03S10B-01G-4/2.8-G]
CN139	USB12 Wake / No Wake Select	Table 3-2	3-pin, 2.0mm jumper header to select between Wake and No Wake from sleep states for the USB12 port [JIH21N12050-03S10B-01G-4/2.8-G]
CN140	USB2 [bottom] / USB3 [top]	See USB 3.0 Specification	18-pin, standard dual USB 3.0 connectors for USB interface ports 2 and 3 [Amphenol, GSB3112311HR, BLUE]
CN141	USB4 Wake / No Wake Select	Table 3-3	3-pin, 2.0mm jumper header to select between Wake and No Wake from sleep states for the USB4 port [JIH21N12050-03S10B-01G-4/2.8-G]
CN142	USB2 Wake / No Wake Select	Table 3-4	3-pin, 2.0mm jumper header to select between Wake and No Wake from sleep states for the USB2 port [JIH21N12050-03S10B-01G-4/2.8-G]
CN143	USB5 Wake / No Wake Select	Table 3-5	3-pin, 2.0mm jumper header to select between Wake and No Wake from sleep states for the USB5 port [JIH21N12050-03S10B-01G-4/2.8-G]
CN144	USB 4 / 5 / 11 / 12	See USB 2.0 Specification	16-pin, standard 4-stack USB 2.0 connectors for USB interface ports 4, 5, 11, and 12 [Kuon Yi, KS-004-ATB-10-L]
CN145	SPI0 Voltage Select	Table 3-56	3-pin, 2.54mm jumper header for selecting SPI0 voltages [JIH, 21N12564-03S10B-01G-6/3-G]
CN146	SPI0 Socket	Table 3-57	8-pin, 1.27mm SPI Flash socket for SPI flash memory [LOTES, ACA-SPI-004-K01, BLACK]
CN147	eSPI / SPI1 Voltage Select	Table 3-58	3-pin, 2.54mm jumper header for selecting eSPI or SPI1 voltages [JIH, 21N12564-03S10B-01G-6/3-G]
CN148	SPI0	Table 3-59	10-pin, 2.54 box header for SPI0 interface signals [JIHVEI, 23N6960-10S10B-01G-G, BLACK]
CN149	SPI0 CS0 / CS1 Select	Table 3-56	3-pin, 2.0mm jumper header to select between CS0 and CS1 for the SPI0 port [JIH21N12050-03S10B-01G-4/2.8-G]
CN150	eSPI / SPI1	Table 3-61	16-pin, 2.54 box header for eSPI or SPI1 interface signals [JIHVEI, 23N6960-10S10B-01G-G, BLACK
CN151	SD Card	Table 2-2	12-pin standard, 2.8mm slot connector for Secure Digital memory cards [TYCO, 1939115-1, BLACK]
CN152	SD Card Power Mode Select	Table 3-64	3-pin, 2mm jumper header to select power modes for the SD Card slot [JIH21N12050-03S10B-01G-4/2.8-G]
CN153	HDA	“Audio IO Jacks” on page 18	13-pin standard audio jack for three HD Audio signals: Line In (Blue), Line Out (Green), and MIC In (Pink) [FOXCONN, JA33331-HA1P-4F]
CN154	HDA Voltage Select	Table 3-65	3-pin, 2mm jumper header to select between 1.5 volts and 1.8 volts for the HD Audio interface [JIH21N12050-03S10B-01G-4/2.8-G]
CN155	I2S Audio	“Audio IO Jacks” on page 18	13-pin standard audio jack for three I2S Audio signals: Line In (Blue), Line Out (Green), and MIC In (Pink) [FOXCONN, JA33331-HA1P-4F]

Table 2-1: Header, Switch, LED, and Connector Descriptions (Continued)

PCB Designator	Signal / Device	Pinout Link	Description
CN156	Mic BIAS Select	Table 3-66	3-pin, 2.0mm jumper header to select between Internal and External Mic BIAS for the I2S Audio interface [JIH21N12050-03S10B-01G-4/2.8-G]
CN157	I2S Audio Codec Select	Table 3-67	3-pin, 2.0mm jumper header to select between SGTL5000 and TLV320 CODECs for the I2S Audio interface [JIH21N12050-03S10B-01G-4/2.8-G]
CN158	SMARC Interface	See SMARC 2.0 Specification	314-pin, MXM socket for receiving camera, graphics, and I/O signals from the SMARC module [FOXCONN, AS0B821-S55B-7H, BLACK]
CN159	USB0 Wake / No Wake Select	Table 3-6	3-pin, 2.0mm jumper header to select between Wake and No Wake from sleep states for the USB0 port [JIH21N12050-03S10B-01G-4/2.8-G]
CN160	USB0 OTG	See USB 2.0 Specification	5-pin standard, Type AB Micro-USB connector for USB 2.0 OTG host/device interface [HIROSE, ZX62D-AB-5P8]
CN162	USB3 Wake / No Wake Select	Table 3-7	3-pin, 2.0mm jumper header to select between Wake and No Wake from sleep states for the USB3 port [JIH21N12050-03S10B-01G-4/2.8-G]
CN163	GPIO 0-3 Enable	Table 3-69	8-pin, 2mm jumper header to enable GPIOs 0-3 [JVE, 21N22050-08M00B-01G-4-C]
CN167	GPIO 0-3	Table 3-68	10-pin, 2.54mm header for GPIO 0-3 signals [JIH, 21N22564-10S10B-01G-6/3-G]
CN168	GPIO 0-3 Voltage Select	Table 3-70	6-pin, 2.0mm jumper header for configuring the correct reference voltages for GPIO ports 0-3, otherwise connected to GND by the ESD clamping diodes. [NELTRON, 2208SM-06G-CR]
CN169	GPIO 4-7 Enable	Table 3-72	8-pin, 2.0mm jumper header to enable GPIOs 4-7 [JVE, 21N22050-08M00B-01G-4-C]
CN173	GPIO 4-7	Table 3-71	10-pin, 2.54mm header for GPIO 4-7 signals [JIH, 21N22564-10S10B-01G-6/3-G]
CN174	GPIO 4-7 Voltage Select	Table 3-73	6-pin, 2.0mm jumper header for configuring the correct reference voltages for GPIO ports 4-7, otherwise connected to GND by the ESD clamping diodes. [NELTRON, 2208SM-06G-CR]
CN176	GPIO 8-11 Enable	Table 3-75	8-pin, 2.0mm jumper header to enable GPIOs 8-11 [JVE, 21N22050-08M00B-01G-4-C]
CN179	GPIO 8-11	Table 3-74	10-pin, 2.54mm header for GPIO 8-11 signals [JIH, 21N22564-10S10B-01G-6/3-G]
CN180	GPIO 8-11 Voltage Select	Table 3-76	6-pin, 2.0mm jumper header for configuring the correct reference voltages for GPIO ports 8-11, otherwise connected to GND by the ESD clamping diodes. [NELTRON, 2208SM-06G-CR]
CN181	SATA0	See SATA Specification	7-pin, 1.27mm standard vertical connector for SATA0 interface [MOLEX, 67800-5005, BLACK]
CN182	SIM1	“SIM Slots” on page 21	6-pin, 2.54mm standard slot, hinge connector for Subscriber Identity Module 1 interface [REGO, 80440GFH-061-128L, BLACK]

Table 2-1: Header, Switch, LED, and Connector Descriptions (Continued)

PCB Designator	Signal / Device	Pinout Link	Description
CN183	PCIe A	Table 3-85	36-pin, 1.0mm standard connector for PCI Express x1, Port A [FOXCONN, 2EG01827-D2D-DF]
CN184	mPCIe B	"PCIe Mini Card Slot" on page 19	52-pin, 0.8mm standard, right-angle slot for PCI Express Mini Card B interface [Attend, 119A-80A00-R02]
CN185	SIM2	"SIM Slots" on page 21	6-pin, 2.54mm standard slot, hinge connector for Subscriber Identity Module 2 interface [REGO, 80440GFH-061-128L, BLACK]
CN186	PCIe D	Table 3-86	36-pin, 1.0mm standard connector for PCI Express x1, Port D [FOXCONN, 2EG01827-D2D-DF]
CN187	mPCIe B Latch	Not Applicable	Latch for fastening PCI Express Mini Card B [Attend, 119A-LATCH-80]
CN188	mPCIe C Expansion	Table 3-88	8-pin, 2mm header to expand PCI Express Mini Card C interface [JVE, 21N22050-08M00B-01G-4-C]
CN189	mPCIe B Latch	Not Applicable	Latch for fastening PCI Express Mini Card B [Attend, 119A-LATCH-80]
CN190	mPCIe C Latch	Not Applicable	Latch for fastening PCI Express Mini Card C [Attend, 119A-LATCH-80]
CN191	mPCIe C Latch	Not Applicable	Latch for fastening PCI Express Mini Card C [Attend, 119A-LATCH-80]
CN192	mPCIe C	"PCIe Mini Card Slot" on page 19	52-pin, 0.8mm standard, right-angle slot for PCI Express Mini Card C interface [Attend, 119A-80A00-R02]
CN193	mPCIe B Expansion	Table 3-87	8-pin, 2.0mm header to expand PCI Express Mini Card B interface [JVE, 21N22050-08M00B-01G-4-C]
CN194	I2C EEPROM Socket	Table 3-37	8-pin, 2.54mm socket for I2C EEPROM [Mill-Max, 110-13-308-41-001000]
CN195	I2C PM Voltage Select	Table 3-38	6-pin, 2.0mm jumper header for selecting between 1.8V, 5.0V, and 3.3V voltages for the I2C Power Management interface [NELTRON, 2208SM-06G-CR]
CN196	I2C GP Voltage Select	Table 3-39	6-pin, 2.0mm jumper header for selecting between 1.8V, 5.0V, and 3.3V voltages for the I2C General Purpose interface [NELTRON, 2208SM-06G-CR]
CN197	I2C CAM0 Voltage Select	Table 3-40	6-pin, 2.0mm jumper header for selecting between 1.8V, 5.0V, and 3.3V voltages for the I2C CAM0 interface [NELTRON, 2208SM-06G-CR]
CN198	I2C CAM1 Voltage Select	Table 3-41	6-pin, 2.0mm jumper header for selecting between 1.8V, 5.0V, and 3.3V voltages for the I2C CAM1 interface [NELTRON, 2208SM-06G-CR]
CN199	GPIO5 Fan PM Out Enable	Table 3-77	3-pin, 2.0mm jumper header to enable Fan Power Management Out on the GPIO5 port [JIH21N12050-03S10B-01G-4/2.8-G]
CN200	GPIO6 TACHO In Enable	Table 3-78	3-pin, 2.0mm jumper header to enable Tachometer In on the GPIO6 port [JIH21N12050-03S10B-01G-4/2.8-G]

Table 2-1: Header, Switch, LED, and Connector Descriptions (Continued)

PCB Designator	Signal / Device	Pinout Link	Description
CN201	PCIe ClockBuffers 0-1 Connect	Table 3-91	6-pin, 2.0mm jumper header for connecting one of the two PCIe ClockBuffers (0 or 1) to the SMBus [NELTRON, 2208SM-06G-CR]
CN202	BattMan Charger	Table 3-17	6-pin, 2.0mm header for Smart Battery charger interface [NELTRON, 2208SM-06G-CR]
CN204	Serial Voltage Mode Select	Table 3-51	3-pin, 2mm jumper header to select between +V1P8S and +V1P8_SBY for the Serial interface [JIH21N12050-03S10B-01G-4/2.8-G]
CN205	mPCIe B/C CLKREQ Enable	Table 3-89	6-pin, 2.0mm header to enable mPCIe B or C request for clock [NELTRON, 2208SM-06G-CR]
CN206	BattMan Enable	Table 3-18	3-pin, 2mm jumper header to enable the BattMan smart battery interface [JIH21N12050-03S10B-01G-4/2.8-G]
CN207	Backlight Voltage Select	Table 3-25	8-pin, 2.54mm jumper header to select between 12V and 5V for the LVDS / eDP Backlight interface [JIH, 21N22564-08S10B-01G-6/3-G]
CN208	MIPI-CSI Camera	Table 3-44	36-pin, 0.5mm FFC/FPC connector for the MIPI-CSI camera interface with SGET pinout [HIROSE, FH12A-36S-0.5SH(55)]
CN209	COM3	Table 3-50	10-pin, 2.0mm box header for serial port 3 interface signals [MOLEX, 87832-1014, BLACK]
CN210	COM2	Table 3-49	10-pin, 2.0mm box header for serial port 2 interface signals [MOLEX, 87832-1014, BLACK]
CN211	USB4 2.0 (CN144) Over-Current Detection Source Select	Table 3-8	3-pin, 2.0mm jumper header to select the source for USB4 2.0 over-current detection [JIH21N12050-03S10B-01G-4/2.8-G]
CN212	USB5 2.0 (CN144) Over-Current Detection Select	Table 3-9	3-pin, 2.0mm jumper header to select the source for USB5 2.0 over-current detection [JIH21N12050-03S10B-01G-4/2.8-G]
CN213	USB3 3.0 (CN140) Over-Current Detection Select	Table 3-10	3-pin, 2.0mm jumper header to select the source for USB3 3.0 over-current detection [JIH21N12050-03S10B-01G-4/2.8-G]
CN214	USB2 3.0 (CN140) Over-Current Detection Select	Table 3-11	3-pin, 2.0mm jumper header to select the source for USB2 3.0 over-current detection [JIH21N12050-03S10B-01G-4/2.8-G]
LED15	USB12, VBUS On	Table 3-8	Green LED indicating Vbus is applied to USB12 [LIGITEK, LG-192G-CT]
LED16	USB4, VBUS On	Not Applicable	Green LED indicating Vbus is applied to USB4 [LIGITEK, LG-192G-CT]
LED17	USB11, VBUS On	Not Applicable	Green LED indicating Vbus is applied to USB11 [LIGITEK, LG-192G-CT]
LED18	USB5, VBUS On	Not Applicable	Green LED indicating Vbus is applied to USB5 [LIGITEK, LG-192G-CT]
LED19	USB2, VBUS On	Not Applicable	Green LED indicating Vbus is applied to USB2 [LIGITEK, LG-192G-CT]

Table 2-1: Header, Switch, LED, and Connector Descriptions (Continued)

PCB Designator	Signal / Device	Pinout Link	Description
LED20	USB3, VBUS On	Not Applicable	Green LED indicating Vbus is applied to USB3 [LIGITEK, LG-192G-CT]
LED21	USB0, VBUS On	Not Applicable	Green LED indicating Vbus is applied to USB0 [LIGITEK, LG-192G-CT]
LED22	WLANB	Not Applicable	Green LED indicating wireless LAN connection on PCIe B [LIGITEK, LG-192G-CT]
LED23	WLANC	Not Applicable	Green LED indicating wireless LAN connection on PCIe C [LIGITEK, LG-192G-CT]
LED24	WPANB	Not Applicable	Green LED indicating wireless PAN (Bluetooth, Zigbee, or similar) connection on PCIe B [LIGITEK, LG-192G-CT]
LED25	WPANC	Not Applicable	Green LED indicating wireless PAN (Bluetooth, Zigbee, or similar) connection on PCIe C [LIGITEK, LG-192G-CT]
LED26	WWANC	Not Applicable	Green LED indicating wireless WAN (GSM, LTE, or similar) connection on PCIe C [LIGITEK, LG-192G-CT]
LED27	WWANB	Not Applicable	Green LED indicating wireless WAN (GSM, LTE, or similar) connection on PCIe B [LIGITEK, LG-192G-CT]
LED28	ALL DONE	Not Applicable	Green LED indicating when load for PCIe repeater EEPROM is complete (currently not used) [LIGITEK, LG-192G-CT]
LED29	SATA	Not Applicable	Yellow LED indicating SATA activity [EVERLIGHT, 19-21UYC/S350-A3/TR8]
LED30	BattMan Low	Not Applicable	Red LED indicating insufficient capacity of BattMan smart battery [LIGITEK, LG-192HRF-CT]
LED31	Power, Carrier	Not Applicable	Green LED indicating applied power to carrier [LIGITEK, LG-192G-CT]
LED32	Power, Module	Not Applicable	Green LED indicating applied power to module [LIGITEK, LG-192G-CT]
LED33	Power, SD Card	Not Applicable	Green LED indicating applied power to SD card [LIGITEK, LG-192G-CT]
LED34	WDT Time Out	Not Applicable	Red LED indicating a watchdog event from the module [LIGITEK, LG-192HRF-CT]
LED35	Carrier Standby (S3)	Not Applicable	Green LED indicating the Standby mode is active on the module (x86) [LIGITEK, LG-192G-CT]
LED36	BattMan Charging	Not Applicable	Yellow LED indicating BattMan smart battery is charging [EVERLIGHT, 19-21UYC/S350-A3/TR8]
LED37	BattMan Charger Present	Not Applicable	Green LED indicating BattMan charger is connected [LIGITEK, LG-192G-CT]
SW34	Power On, module	Not Applicable	Push-button switch to Power On or shut down the module [CONTACT, TS-A02-2, BLACK]
SW35	Reset, module	Not Applicable	Push-button switch to warm reset the module [CONTACT, TS-A02-2, BLACK]

Table 2-1: Header, Switch, LED, and Connector Descriptions (Continued)

PCB Designator	Signal / Device	Pinout Link	Description
SW36	Sleep, module	Not Applicable	Push-button switch to induce module sleep mode [CONTACT, TS-A02-2, BLACK]
SW37	LID	Not Applicable	Toggle switch to assert LID function on module [NKK, G12AP, BLACK]
SW38	Test	Not Applicable	Push-button switch to invoke test on the module [CONTACT, TS-A02-2, BLACK] NOTE: Supported only on LEC-iMX6
SW39	Boot Select	Table 3-92	4-pole, 1.27mm dip switch to select order of boot for devices on module and carrier [DIPTRONICS] DHA-04TQR, BLACK]
SW46	HDMI Configuration	Table 3-29	4-pole, 1.27mm dip switch to HDMI extender function [DIPTRONICS] DHA-04TQR, BLACK]
SW51	SPI0 Configuration	Table 3-62	4-pole, 1.27mm dip switch to configure the SPI0 socket [DIPTRONICS] DHA-04TQR, BLACK]
SW52	SPI1 Configuration	Table 3-63	4-pole, 1.27mm dip switch to configure the SPI1 interface [DIPTRONICS] DHA-04TQR, BLACK]
SW66	PLL Bandwidth Configuration	Table 3-94	2-pole, 1.6mm dip switch to configure PLL bandwidth for PCIe Clock-Buffer components [DIPTRONIC, DHNF-02-TV-T/6, HALF]
SW68	GPIO 0-3 Configuration	Table 3-79	4-pole, 1.27mm dip switch to configure the 2.2K pull up of GPIO ports 0-3 (carrier side) [DIPTRONICS] DHA-04TQR, BLACK]
SW69	GPIO 4-7 Configuration	Table 3-80	4-pole, 1.27mm dip switch to configure the 2.2K pull up of GPIO ports 4-7 (carrier side) [DIPTRONICS] DHA-04TQR, BLACK]
SW71	GPIO 8-11 Configuration	Table 3-81	4-pole, 1.27mm dip switch to configure the 2.2K pull up of GPIO ports 8-11 (carrier side) [DIPTRONICS] DHA-04TQR, BLACK]
SW72	GPIO 0-3 Configuration	Table 3-82	4-pole, 1.27mm dip switch to configure the 10K pull up of GPIO ports 0-3 (module side) [DIPTRONICS] DHA-04TQR, BLACK]
SW73	GPIO 4-7 Configuration	Table 3-83	4-pole, 1.27mm dip switch to configure the 10K pull up of GPIO ports 4-7 (module side) [DIPTRONICS] DHA-04TQR, BLACK]
SW74	GPIO 8-11 Configuration	Table 3-84	4-pole, 1.27mm dip switch to configure the 10K pull up of GPIO ports 8-11 (module side) [DIPTRONICS] DHA-04TQR, BLACK]
U174	PCIe Re-driver socket	Table 3-90	8-pin, 1.27mm socket for the I2C EEPROM [LOTES, ACA-SPI-004-K01, BLACK] NOTE: This socket is the same part as the SPI Flash socket but supports only the I2C EEPROM, not the SPI flash

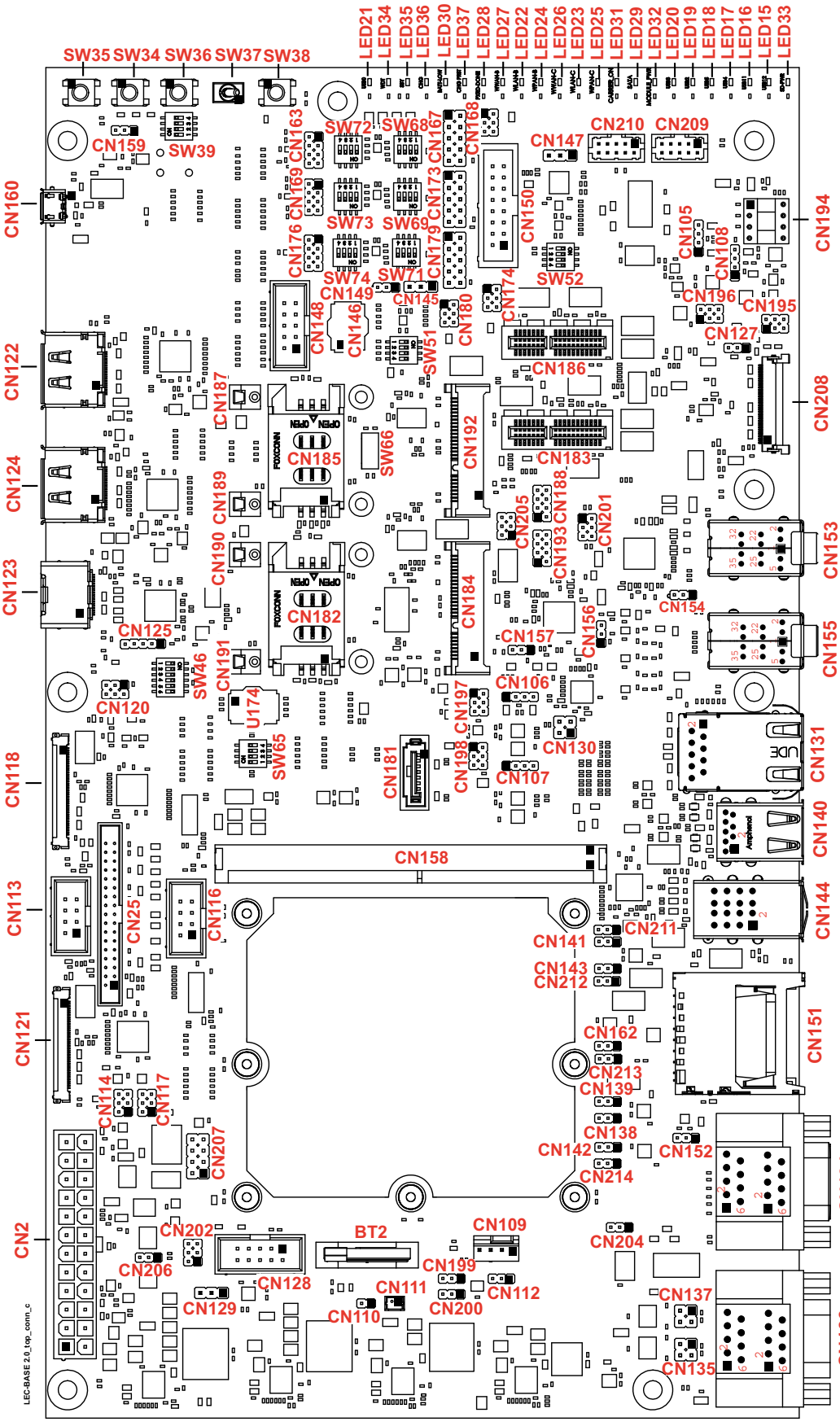


Figure 2-1: Header, Connector, Switch, and LED Locations (Top Side)

CONNECTORS:

BT2 - Battery Socket
CN2 - ATX Power Input
CN25 - LVDS, Dual-Channel Interface
CN105 - I2C_GP Interface
CN106 - I2C_CAM0 Interface
CN107 - I2C_CAM1 Interface
CN108 - I2C_PM Interface
CN109 - Fan Interface
CN110 - RTC Battery Enable
CN111 - RTC Battery Interface
CN112 - Fan Voltage Select
CN113 - LVDS Backlight 1 Interface
CN114 - LVDS +VCC Voltage Select
CN116 - LVDS Backlight 2 Interface
CN117 - LVDS +VDD Voltage Select
CN118 - eDP1 Interface
CN120 - LVDS_eDP Select
CN121 - eDP0 Interface
CN122 - DP0 Interface
CN123 - HDMI Interface
CN124 - DP1 Interface
CN125 - HDMI_DP1 Select
CN127 - CAM0_GPIO/CAM1_GPIO Select
CN128 - BattMan Interface
CN129 - BattMan Voltage Select
CN130 - Gb Ethernet-TRIGGER Select
CN131 - Gb Ethernet Stack
CN134 - COM0/COM1 Stack
CN135 - CAN1 Termination Select
CN136 - CAN0/CAN1 Stack
CN137 - CAN0 Termination Select
CN138 - USB11 Wake/NoWake Select
CN139 - USB12 Wake/NoWake Select
CN140 - USB 3.0 Stack (ports 2/3)
CN141 - USB4 Wake/NoWake Select
CN142 - USB2 Wake/NoWake Select
CN143 - USB5 Wake/NoWake Select
CN144 - USB 2.0 Stack
(ports 4/5 and 11/12)
CN145 - SPI0 Voltage Select
CN146 - SPI0 Socket
CN147 - eSPI_SPI1 Voltage Select
CN148 - SPI0 Interface
CN149 - SPI0 CS0/CS1 Select
CN150 - eSPI_SPI1 Interface
CN151 - SD-Card Slot
CN152 - SD-Card Power Mode Select
CN153 - HD Audio Stack
CN154 - HD Audio Voltage Select
CN155 - I2S Audio Stack
CN156 - External/Internal Mic Bias select
CN157 - I2S Audio CODEC select
CN158 - SMARC Interface
CN159 - USB0 Wake/NoWake Select
CN160 - USB0 2.0 OTG Interface
CN162 - USB3 Wake/NoWake Select
CN163 - GPIO 0-3 Enable
CN167 - GPIO 0-3 Interface
CN168 - GPIO 0-3 Voltage Select
CN169 - GPIO 4-7 Enable
CN173 - GPIO 4-7 Interface
CN174 - GPIO 4-7 Voltage Select
CN176 - GPIO 8-11 Enable
CN179 - GPIO 8-11 Interface
CN180 - GPIO 8-11 Voltage Select
CN181 - SATA0
CN182 - SIM1 Card Interface
CN183 - PCIe A Interface
CN184 - mPCIe B Interface
CN185 - SIM2 Card Interface
CN186 - PCIe D Interface
CN187 - mPCIe B Latch
CN188 - Expansion Interface (mPCIe C)
CN189 - mPCIe B Latch
CN190 - mPCIe C Latch
CN191 - mPCIe C Latch
CN192 - mPCIe C Interface
CN193 - Expansion Interface (mPCIe B)
CN194 - I2C EEPROM Socket
CN195 - I2C_PM Voltage Select
CN196 - I2C_GP Voltage Select
CN197 - I2C-CAM0 Voltage Select
CN198 - I2C-CAM1 Voltage Select
CN199 - GPIO5 Fan PWM_OUT Enable
CN200 - GPIO6 Fan TACHO_IN Enable
CN201 - PCIe ClockBuffers 0-1 Connect
CN202 - BattMan Charger Interface
CN204 - Serial Voltage Mode Select
CN205 - mPCIe B/C CLKREQ Enable
CN206 - BattMan Enable
CN207 - Backlight Voltage Select
CN208 - MIPI-CSI Camera Interface
CN209 - COM3 Interface
CN210 - COM2 Interface
CN211 - USB4 2.0 Over-Current Detection Source Select
CN212 - USB5 2.0 Over-Current Detection Source Select
CN213 - USB3 3.0 Over-Current Detection Source Select
CN214 - USB2 3.0 Over-Current Detection Source Select
U174 - PCIe Redriver Socket

LEDs:

LED15 - USB12, VBUS_ON
LED16 - USB4, VBUS_ON
LED17 - USB11, VBUS_ON
LED18 - USB5, VBUS_ON
LED19 - USB2, VBUS_ON
LED20 - USB3, VBUS_ON
LED21 - USB0, VBUS_ON
LED22 - WLANB
LED23 - WLANC
LED24 - WPANB
LED25 - WPANC
LED26 - WWANC
LED27 - WWANB
LED28 - ALL_DONE, PCIe
LED29 - SATA Activity
LED30 - BattMan Low
LED31 - Carrier Power
LED32 - Module Power
LED33 - SD Card Power
LED34 - WDT_Time_Out
LED35 - Carrier Standby (S3)
LED36 - BattMan Charging
LED37 - BattMan Charger Present

SWITCHES:

SW34 - Button,
Power On SMARC Module
SW35 - Button,
Reset SMARC Module
SW36 - Button,
Sleep Mode SMARC Module
SW37 - Toggle, LID
SW38 - Button, Test
SW39 - Dip Switch,
Boot Select
SW46 - Dip Switch,
HDMI Configuration
SW51 - Dip Switch,
SPI0 Configuration
SW52 - Dip Switch,
SPI1 Configuration
SW66 - Dip Switch,
PLL Bandwidth Configuration
SW68 - Dip Switch,
GPIO 0-3 2.2K PU Configuration
SW69 - Dip Switch,
GPIO 4-7 2.2K PU Configuration
SW71 - Dip Switch,
GPIO 8-11 2.2K PU Configuration
SW72 - Dip Switch,
GPIO 0-3 10K PU Configuration
SW73 - Dip Switch,
GPIO 4-7 10K PU Configuration
SW74 - Dip Switch,
GPIO 8-11 10K PU Configuration

LEC-BASE 2.0_top_conn_refkey_c

Figure 2-2: PCB Designator Key for Headers, Connectors, Switches, and LEDs

Figure 2-3 illustrates the faces of the standard interface connectors mounted along one edge of the carrier. These connectors are for CAN, Serial Port, SD Card, USB, Ethernet, Audio, and MIPI-CSI Camera (conforming to the QSeven 2.1 Specification) cable connectors.

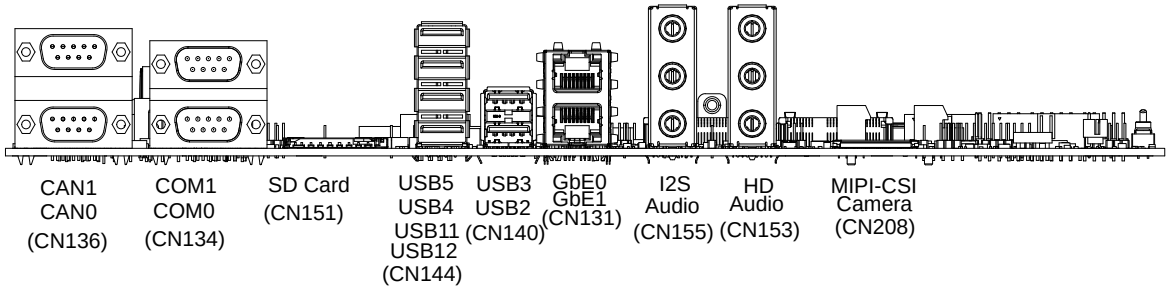


Figure 2-3: IO Panel Connector Locations

Figure 2-4 illustrates the faces of the standard interface connectors mounted along the opposite edge of the carrier shown in Figure 2-3. These connectors are for USB / OTG, DisplayPort, HDMI, and embedded DisplayPort industry-standard cable connectors.

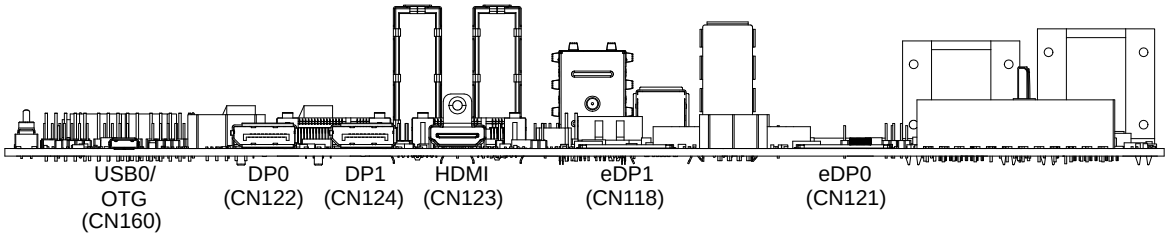


Figure 2-4: IO Panel Connector Locations (opposite side)

2.2 Standard Hardware References

This section further describes the supported features of the LEC-BASE 2.0 standard, on-board hardware.

2.2.1 Audio IO Jacks

The LEC-BASE 2.0 provides two standard audio jacks for HD (CN153) and I2S (CN155) audio. Two audio codecs support these two interfaces. Figure 2-5 depicts the three lines of the audio jacks: Line In (1 - Blue), Line Out (2 - Green), and MIC In (3 - Pink). Figure 2-6 presents the functional block diagram of I2S and HDA signals connections from the SMARC module to the audio components on the carrier.

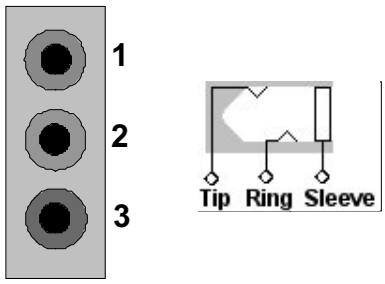


Figure 2-5: Stereo Jack Configuration

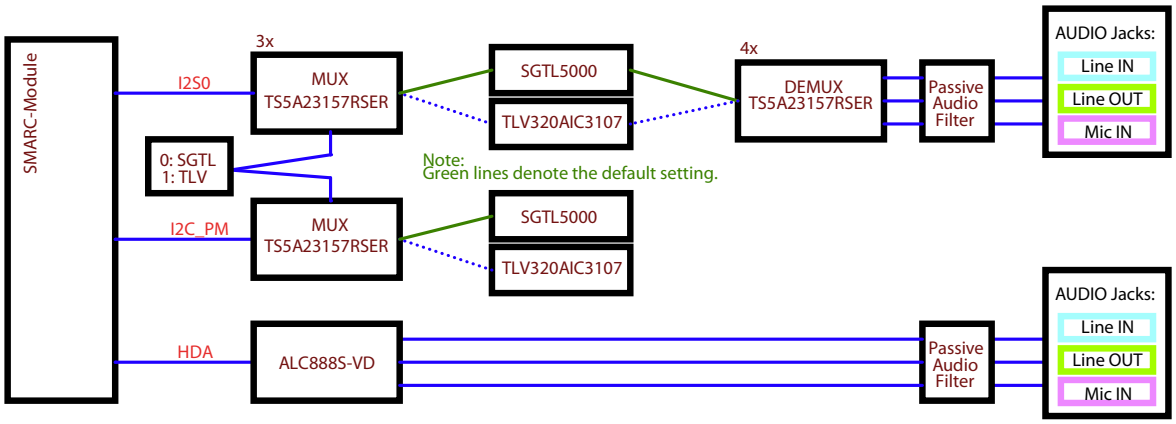


Figure 2-6: I2S/HDA Block Diagram

2.2.2 PCIe Mini Card Slot

The LEC-BASE 2.0 provides two standard PCI Express Mini Card slots. Figure 2-7 presents one mini card slot with one of the two fastening latches. Figure 2-8 illustrates the functional block diagram of the PCIe Mini Card signals and hardware on the carrier.

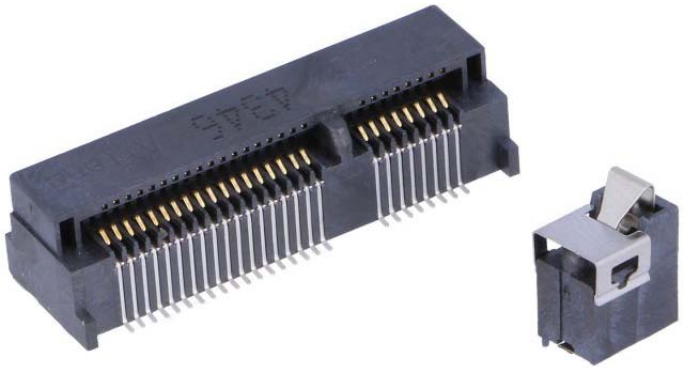


Figure 2-7: PCIe Mini Card Slot with Latch

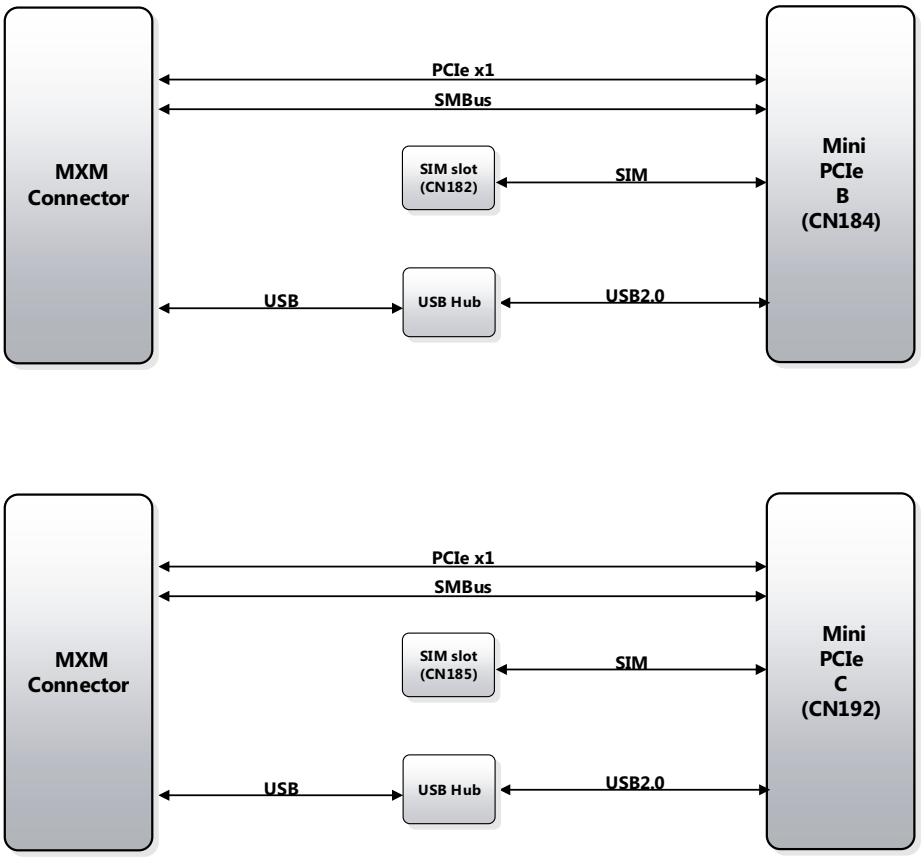


Figure 2-8: PCIe Mini Card Slot Block Diagram

2.2.3 SD Card Slot

The SD Card slot (CN151) provides the standard 4-bit, push-push interface for SD memory cards. LED5 provides indication of SD power.

> **NOTE:** UHS cards with 1.8V data signaling are supported. The card supply is always 3.3V regardless if either 1.8V signaling or 3.3V signaling is committed by both card controllers. The SoC and the SD card will agree on which standard they are compatible with and will choose the appropriate standard.

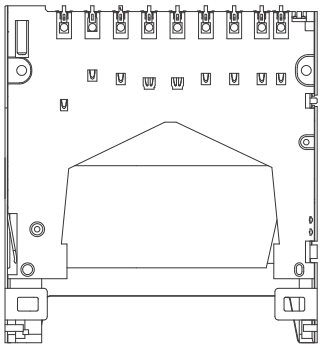
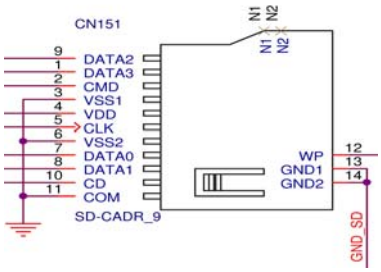


Figure 2-9: SD Card Slot

Table 2-2: SD Card Slot (CN151)

Pin #	Signal	Description	Scheme
1	SDIO_D3	SDIO data bit3	
2	SDIO_CMD	SDIO Command	
3	GND	Ground	
4	+VCC_SDIO	3.3V power supply	
5	SDIO_CK	SDIO clock	
6	GND	Ground	
7	SDIO_D0	SDIO data bit0	
8	SDIO_D1	SDIO data bit1	
9	SDIO_D2	SDIO data bit2	
10	SDIO_CD#	SDIO card detect	
11	GND	Ground	
12	SDIO_WP	SDIO write protect	

Note: Shaded table cells denote power or ground. Use jumper header CN152 to select the SD Card power mode (+V3P3_SBY or +V3P3S.)

2.2.4 SIM Slots

Two SIM slots (CN182 / CN185) provide interface for two Subscriber Identity Modules, supporting both PCIe Mini Card slots: CN182 (SIM1) supports the CN184 Mini Card slot and CN185 (SIM2) supports the CN192 Mini Card slot. Figure 2-10 illustrates the slots' hinge-type connections. Table 2-3 and Table 2-4 provide the signals for both slots.

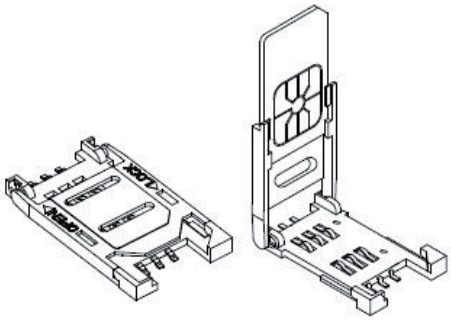
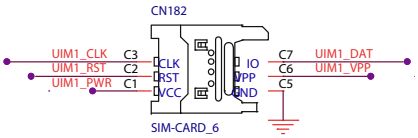


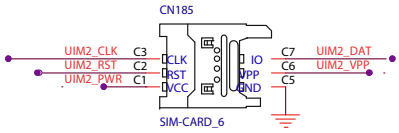
Figure 2-10: SIM Slots (CN182 / CN185)

Table 2-3: SIM1 Slot (CN182)

Pin #	Signal	Description	Scheme
C1	UM1_PWR	+1.8V or +3V VDC power supply input (depending on PCIe Mini Card; +5V is supported if supplied by the Mini Card)	
C2	UM1_RESET	Resets the card's communications	
C3	UM1_CLK	Clock signal for data communications timing	
C4	RES	Reserved	
C5	GND	Ground	
C6	UM1_VPP	Programming input voltage	
C7	UM1_DATA	I/O for serial data	
C8	RES	Reserved	

NOTE: Shaded table cells denote power or ground.

Table 2-4: SIM2 Slot (CN185)

Pin #	Signal	Description	Scheme
C1	UM2_PWR	+1.8V or +3V VDC power supply input (depending on PCIe Mini Card; +5V is supported if supplied by the Mini Card)	
C2	UM2_RESET	Resets the card's communications	
C3	UM2_CLK	Clock signal for data communications timing	
C4	RES	Reserved	
C5	GND	Ground	
C6	UM2_VPP	Programming input voltage	
C7	UM2_DATA	I/O for serial data	
C8	RES	Reserved	

NOTE: Shaded table cells denote power or ground.

2.2.5 Battery Socket

One vertical, AAA battery socket provides power for an external RTC coin cell battery. Figure 2-11 illustrates the top and side views of the socket. Table 2-5 provides the signals for the socket.

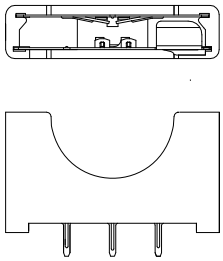


Figure 2-11: Battery Socket

Table 2-5: Battery Socket (BT2)

Pin #	Signal	Description
1	3V_BAT	+3 volts power for RTC
2	GND	Ground
3	3V_BAT	+3 volts power for RTC

Note: Shaded table cells denote power or ground. Jumper required on CN110 to enable the RTC.

A CR2032 battery may explode if incorrectly installed. Replace only with the same or equivalent type recommended by the socket manufacturer.

3 Interfaces

This section provides the pin signals for all the non-standard user interfaces on the LEC-BASE 2.0. Unless pinouts for industry standard interfaces have been modified, those pin-out tables will not appear in this manual. Signal definitions for standard interfaces such as RJ45 GbE, SATA, USB, and PCIe can be found in their respective specification datasheets.

NOTE:

The tables in this section define pin sequence using the method in the following example: A 10-pin header with two rows of pins, using odd/even numbering, where pin 2 is directly across from pin 1, is noted as **10 pins, 2 rows, odd/even pin sequence (1, 2)**. Consecutive numbering is noted, for example, as **24 pins, 2 rows, consecutive pin sequence (1, 13)**, where pin 13 is directly across from pin 1. Refer to Figure 2-1 for pin-1 locations.

3.1 USB Interfaces

All USB interfaces on the LEC-BASE 2.0 are supported through standard connectors, and their signal definitions can be found in their respective specifications. Sections 3.1.1 through 3.1.11 provide the pinout tables for all the supporting USB jumper headers on the carrier. Refer to the following block diagram for an illustration of the USB interface map on the carrier.

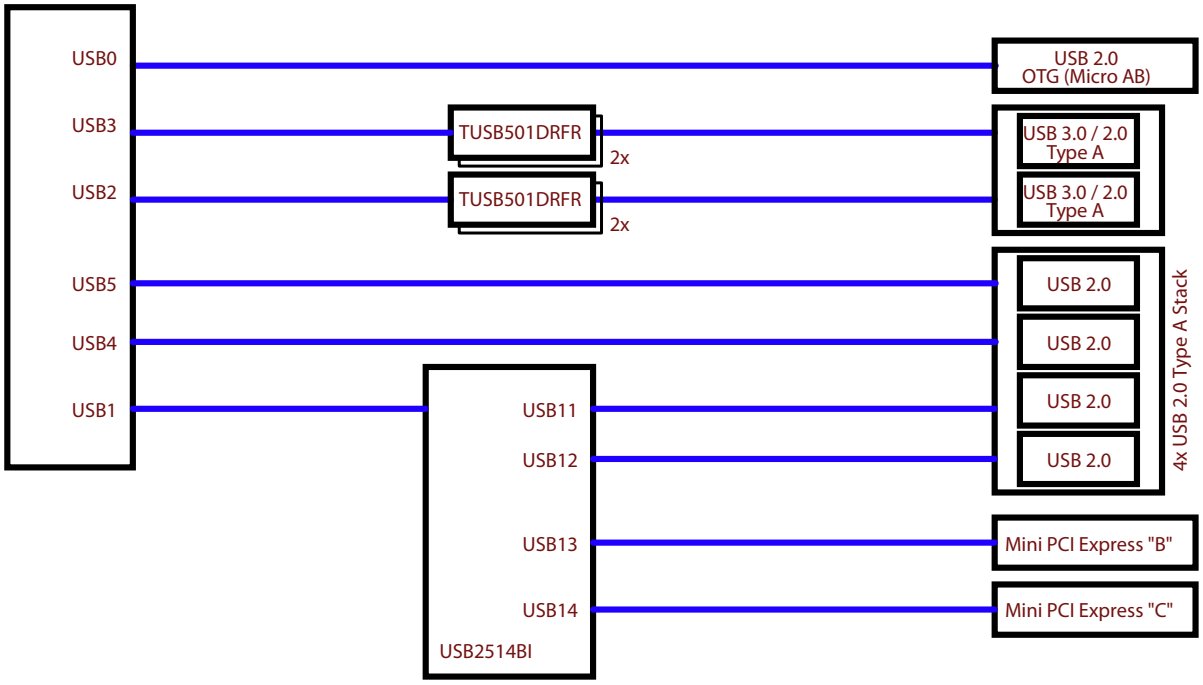


Figure 3-1: USB Mapping Block Diagram

3.1.1 USB11 Wake / No Wake Select (CN138)

Table 3-53 lists the pin signals of the USB11 Wake / No Wake select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-1: USB11 Wake / No Wake Select (CN138)

Pin #	Signal	Jumper Positions
1	+V5P0_SBY	• Jumper Installed 1-2 to enable the USB11 Wake from sleep states function [**default**] • Jumper Installed 2-3 to enable the USB11 No Wake from sleep states function
2	+V5P0_USB11	
3	+V5P0S	

3.1.2 USB12 Wake / No Wake Select (CN139)

Table 3-2 lists the pin signals of the USB12 Wake / No Wake select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-2: USB12 Wake / No Wake Select (CN139)

Pin #	Signal	Jumper Positions
1	+V5P0_SBY	• Jumper Installed 1-2 to enable the USB12 Wake from sleep states function [**default**] • Jumper Installed 2-3 to enable the USB12 No Wake from sleep states function
2	+V5P0_USB12	
3	+V5P0S	

3.1.3 USB4 Wake / No Wake Select (CN141)

Table 3-3 lists the pin signals of the USB4 Wake / No Wake select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-3: USB4 Wake / No Wake Select (CN141)

Pin #	Signal	Jumper Positions
1	+V5P0_SBY	• Jumper Installed 1-2 to enable the USB4 Wake from sleep states function • Jumper Installed 2-3 to enable the USB4 No Wake from sleep states function [**default**]
2	+V5P0_USB4	
3	+V5P0S	

3.1.4 USB2 Wake / No Wake Select (CN142)

Table 3-3 lists the pin signals of the USB2 Wake / No Wake select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-4: USB2 Wake / No Wake Select (CN142)

Pin #	Signal	Jumper Positions
1	+V5P0_SBY	• Jumper Installed 1-2 to enable the USB2 Wake from sleep states function • Jumper Installed 2-3 to enable the USB2 No Wake from sleep states function [**default**]
2	+V5P0_USB2	
3	+V5P0S	

3.1.5 USB5 Wake / No Wake Select (CN143)

Table 3-5 lists the pin signals of the USB5 Wake / No Wake select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-5: USB5 Wake / No Wake Select (CN143)

Pin #	Signal	Jumper Positions
1	+V5P0_SBY	• Jumper Installed 1-2 to enable the USB5 Wake from sleep states function [**default**] • Jumper Installed 2-3 to enable the USB5 No Wake from sleep states function
2	+V5P0_USB5	
3	+V5P0S	

3.1.6 USB0 Wake / No Wake Select (CN159)

Table 3-6 lists the pin signals of the USB0 Wake / No Wake select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-6: USB0 Wake / No Wake Select (CN159)

Pin #	Signal	Jumper Positions
1	+V5P0_SBY	• Jumper Installed 1-2 to enable the USB0 Wake from sleep states function • Jumper Installed 2-3 to enable the USB0 No Wake from sleep states function [**default**]
2	+V5P0_USB0	
3	+V5P0S	

3.1.7 USB3 Wake / No Wake Select (CN162)

Table 3-7 lists the pin signals of the USB3 Wake / No Wake select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-7: USB3 Wake / No Wake Select (CN162)

Pin #	Signal	Jumper Positions
1	+V5P0_SBY	• Jumper Installed 1-2 to enable the USB3 Wake from sleep states function • Jumper Installed 2-3 to enable the USB3 No Wake from sleep states function [**default**]
2	+V5P0_USB3	
3	+V5P0S	

3.1.8 USB4 2.0 Over-Current Detection Source Select (CN211)

Table 3-53 lists the pin signals of the USB4 2.0 Over-Current Detection Source Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-8: USB4 2.0 Over-Current Detection Source Select (CN211)

Pin #	Signal	Jumper Positions
1	USB4_EN_PU	• Jumper Installed 1-2 to enable the SoC on the Module to detect USB4 over current [**default**] • Jumper Installed 2-3 to enable the circuits on the carrier to detect USB4 over current
2	USB4_EN	
3	USB4_EN_OC#	

NOTE: The # symbol indicates the signal is Active Low.

3.1.9 USB5 2.0 Over-Current Detection Source Select (CN212)

Table 3-53 lists the pin signals of the USB5 2.0 Over-Current Detection Source Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-9: USB5 2.0 Over-Current Detection Source Select (CN212)

Pin #	Signal	Jumper Positions
1	USB5_EN_PU	• Jumper Installed 1-2 to enable the SoC on the Module to detect USB5 over current [**default**] • Jumper Installed 2-3 to enable the circuits on the carrier to detect USB5 over current
2	USB5_EN	
3	USB5_EN_OC#	

NOTE: The # symbol indicates the signal is Active Low.

3.1.10 USB3 3.0 Over-Current Detection Source Select (CN213)

Table 3-53 lists the pin signals of the USB3 3.0 Over-Current Detection Source Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-10: USB3 3.0 Over-Current Detection Source Select (CN213)

Pin #	Signal	Jumper Positions
1	USB3_EN_PU	• Jumper Installed 1-2 to enable the SoC on the Module to detect USB3 over current [**default**] • Jumper Installed 2-3 to enable the circuits on the carrier to detect USB3 over current
2	USB3_EN	
3	USB3_EN_OC#	

NOTE: The # symbol indicates the signal is Active Low.

3.1.11 USB2 3.0 Over-Current Detection Source Select (CN214)

Table 3-53 lists the pin signals of the USB2 3.0 Over-Current Detection Source Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-11: USB2 3.0 Over-Current Detection Source Select (CN214)

Pin #	Signal	Jumper Positions
1	USB2_EN_PU	• Jumper Installed 1-2 to enable the SoC on the Module to detect USB2 over current [**default**] • Jumper Installed 2-3 to enable the circuits on the carrier to detect USB2 over current
2	USB2_EN	
3	USB2_EN_OC#	

NOTE: The # symbol indicates the signal is Active Low.

3.2 Power Interfaces

This section describes the signals for all power interfaces on the carrier, including ATX, RTC battery, and Smart Battery (BattMan) input interfaces.

3.2.1 ATX Power (CN2)

Table 3-12 lists the signals of the standard ATX Power connector, which provides 24 pins, 2 rows consecutive pin sequence (1, 13) with 4.20mm pitch. Use the SW34 button switch on the carrier to apply power to the module*.

Table 3-12: ATX Power Signals (CN2)

Pin#	Signal	Description	Pin#	Signal	Description
1	+V3P3_ATX	Power Supply DC voltage	13	+V3P3_ATX	Power Supply DC voltage
2	+V3P3_ATX	Power Supply DC voltage	14	NC	Not Connected
3	GND	Ground	15	GND	Ground
4	+V5P0_ATX	Power Supply DC voltage	16	ATX_PS_ON#	Switch to turn on power supply, shorted to Ground
5	GND	Ground	17	GND	Ground
6	+V5P0_ATX	Power Supply DC voltage	18	GND	Ground
7	GND	Ground	19	GND	Ground
8	ATX_PWRGD	Status from the power supply, notifying the computer that the DC operating voltages are within the required ranges	20	NC	Not Connected
9	+V5P0_SBY	Power Supply Standby DC voltage	21	+V5P0_ATX	Power Supply DC voltage
10	+V12P0_ATX	Power Supply DC voltage	22	+V5P0_ATX	Power Supply DC voltage
11	+V12P0_ATX	Power Supply DC voltage	23	+V5P0_ATX	Power Supply DC voltage
12	+V3P3_ATX	Power Supply DC voltage	24	GND	Ground

NOTE: Shaded table cells denote power or ground. The # symbol indicates the signal is Active Low.

*As soon as an active ATX power supply is connected to the carrier, the module will be receiving power. The power button is used for starting the system power-up sequence. The module controls power up and power down of the carrier.

3.2.2 Battery Interface (CN111)

Table 3-13 lists the pin signals of the battery interface header, which provides 2 pins in a single row with 1.25mm pitch.

Table 3-13: Battery Interface (CN111)

Pin #	Signal
1	+VDD_RTC_IN
2	GND

NOTE: Shaded table cells denote power or ground.

3.2.3 Battery Enable (CN110)

Table 3-14 lists the pin signals of the RTC battery enable jumper header, which provides 2 pins in a single row with 2mm pitch.

Table 3-14: Battery Enable (CN110)

Pin #	Signal	Jumper Positions
1	+VDD_RTC_IN	• Jumper installed to connect RTC battery [**default**] • Jumper removed to disconnect RTC battery
2	+VDD_RTC_CON	

3.2.4 Smart Battery (BattMan) Interface (CN128)

Table 3-15 lists the pin signals of the Smart Battery header, which provides 10 pins in 2 rows, odd/even pin sequence (1, 2), and 2.54mm pitch.

You must configure the jumper settings as described in Table 3-15, or system damage could occur when using a BattMan power supply to Power On the carrier.

Table 3-15: Smart Battery (BattMan) Interface (CN128)

Pin #	Signal	Jumper Configurations
1	SMB_BATT_SCL (serial clock)	Make sure to set following jumper configurations before implementing a BattMan power supply to Power On the carrier: • Pins 1-2 on **CN129**, BattMan voltage select for battery-side SMBUS • Pins 2-3 on **CN206**, BattMan enable
2	SMB_BATT_SDA (serial data)	
3	BATT_PWR_BTN#	
4	BATTLOWJ	
5	BATT_PS_ON (ATX power supply)	
6	Not Connected	
7	+V12P0_ATX (12-volt power)	
8	+V5P0_SBY (5-volt standby power)	
9	SMB_ALERT# (SMBus alert)	
10	GND	

NOTE: The voltage level of this interface is determined by the CN129 jumper header (default 5V for BattMan supply.) Shaded table cells denote power or ground.

3.2.5 BattMan SMBus Voltage Select (CN129)

Table 3-16 lists the pin signals of the BattMan SMBus voltage select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-16: BattMan SMBus Voltage Select (CN129)

Pin #	Signal	Jumper Positions
1	+V5P0_SBY	• Jumper Installed 1-2 - 5-volt +VCC_SMB_BATT [**default**] • Jumper Installed 2-3 - 3.3-volt +VCC_SMB_BATT
2	+VCC_SMB_BATT	
3	+V3PS_SBY	

3.2.6 BattMan Charger Interface (CN202)

Table 3-17 lists the pin signals of the BattMan Charger interface, which provides 6 pins in two rows with odd/even pin sequence (1,2) and 2.00mm pitch.

Table 3-17: BattMan Charger Interface (CN202)

Pin #	Signal	Pin #	Signal
1	BATMAN.BATLOW# (1.8V logic)	2	BATMAN.CHARGER_PRSNT# (1.8V logic)
3	GND	4	GND
5	BATMAN.CHARGING# (1.8V logic)	6	GND

NOTE: Shaded table cells denote ground. The # symbol indicates the signal is Active Low.

3.2.7 BattMan Enable (CN206)

Table 3-18 lists the pin signals of the BattMan enable jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-18: BattMan Enable (CN206)

Pin #	Signal	Jumper Positions
1	GND	• Jumper on 1-2 disables BattMan support [**default**] • Jumper on 2-3 enables BattMan support
2	EN_VR50_BATT	
3	+V5P0_SBY	

3.3 Display Interfaces

The LEC-BASE 2.0 supports four display interfaces, with the capacity to use three of them, simultaneously. This section provides the pinout tables for all four interfaces including the pinout tables for all support interfaces and jumper headers. The following list presents the four display interfaces.

- LVDS
- eDP (embedded DisplayPort)
- HDMI
- DP++ (Dual-Mode DisplayPort)

3.3.1 LVDS (CN25)

Table 3-19 lists the pin signals of the LVDS header which provides 34-pins, 2 rows, odd/even pin sequence (1, 2) with 2.00mm pitch. Channel A pins are connected directly to the LVDS interface at the SMARC connector. Channel B pins are connected to selected LCD pins on the SMARC connector.

Table 3-19: LVDS Interface Pin Signals (CN25)

Pin #	Signal	Description	SMARC Signal
1	LVDS_DDC_DAT	System Management Data	I2C_LCD_DAT
2	LVDS_DDC_CLK	System Management Clock	I2C_LCD_DAT
3	+VDD_LVDS	Panel Power [use CN114 and CN117 jumper headers to select voltages and +VCC display modes]	N/A
4	+VDD_LVDS_EDID*	Panel EDID Power [use R551 and R1391 solder jumpers to select voltages +V3P3_SBY (R551 [default]) or +VDD_PANEL (R1391)] *	N/A
5	GND	Ground	GND
6	LVDS_A0_N	Data Negative Output - Channel A	LVDS0_0-
7	LVDS_A0_P	Data Positive Output - Channel A	LVDS0_0+
8	LVDS_VDDEN	Panel Power Enable	LCD_VDD_EN
9	LVDS_A1_N	Data Negative Output - Channel A	LVDS0_1-
10	LVDS_A1_P	Data Positive Output - Channel A	LVDS0_1+
11	LVDS_BKLT_EN	Panel Backlight Enable	LCD_BKLT_EN
12	LVDS_A2_P	Data Positive Output - Channel A	LVDS0_2+
13	LVDS_A2_N	Data Negative Output - Channel A	LVDS0_2-
14	NC	Not Connected	
15	LVDS_A_CK_N	Clock Negative - Channel A	LVDS0_CK-
16	LVDS_A_CK_P	Clock Positive - Channel A	LVDS0_CK+
17	+VDD_LVDS	Panel Power [use CN114 and CN117 jumper headers to select voltages and +VCC display modes]	N/A
18	LVDS_A3_P	Data Positive Output - Channel A	LVDS0_3+
19	LVDS_A3_N	Data Negative Output - Channel A	LVDS0_3-
20	GND	Ground	
21	LVDS_B0_N	Data Negative Output - Channel B	LVDS1_0-
22	LVDS_B0_P	Data Positive Output - Channel B	LVDS1_0+

Table 3-19: LVDS Interface Pin Signals (CN25) (Continued)

Pin #	Signal	Description	SMARC Signal
23	GND	Ground	
24	LVDS_B1_N	Data Negative Output - Channel B	LVDS1_1-
25	LVDS_B1_P	Data Positive Output - Channel B	LVDS1_1+
26	GND	Ground	
27	LVDS_B2_N	Data Negative Output - Channel B	LVDS1_2-
28	LVDS_B2_P	Data Positive Output - Channel B	LVDS1_2+
29	GND	Ground	
30	LVDS_B_CK_P	Clock Positive - Channel B	LVDS1_CK+
31	LVDS_B_CK_N	Clock Negative - Channel B	LVDS1_CK-
32	NC	Not Connected	
33	LVDS_B3_P	Data Positive - Channel B	LVDS1_3+
34	LVDS_B3_N	Data Negative - Channel B	LVDS1_3-

NOTE: The shaded table cells denote power or ground.

* If using an LVDS panel without EDID-ROM, disconnect pin 4 by removing the R551 solder jumper.

3.3.2 LVDS Backlight 0 (CN116)

Table 3-20 lists the pin signals of the LVDS Backlight 0 interface, which provides 8 pins, 2 rows, with odd/even pin sequence (1, 2) and 2.54mm pitch.

Table 3-20: LVDS Backlight 0 (CN116)

Pin #	Signal
1	GND
2	+VDD_PANEL (VDD fixed voltages 3.3V or 5V selected at CN117; or switch to +VCC_PANEL mode at CN117 (3-4) and select VCC voltages at CN114).
3	LVDS_BKLT0_CTRL
4	GND
5	LVDS_BKLT0_EN
6	GND
7	Not Connected
8	+VCC_BKLT (backlight voltage, controlled by chipset and selected at CN207)

NOTE: The shaded table cells denote Ground or Power.

Never select +12V for +VCC_Panel (jumper on pins 3-4) at CN114 while in +VDD_Panel mode (jumper on 1-2 or 5-6 at CN117.) Doing so will destroy the LVDS control circuitry

3.3.3 LVDS Backlight 1 (CN113)

Table 3-21 lists the pin signals of the LVDS Backlight 1 interface, which provides 8 pins, 2 rows, with odd/even pin sequence (1, 2) and 2.54mm pitch.

Table 3-21: LVDS Backlight 1 (CN113)

Pin #	Signal
1	GND
2	+VDD_PANEL (VDD fixed voltages 3.3V or 5V selected at CN117; or switch to +VCC_PANEL mode at CN117 (3-4) and select VCC voltages at CN114)
3	LVDS_BKLT1_CTRL
4	GND
5	LVDS_BKLT1_EN
6	GND
7	Not Connected
8	+VCC_BKLT (backlight voltage, controlled by chipset and selected at CN207)

NOTE: The shaded table cells denote Ground or Power.

Never select +12V for +VCC_Panel (jumper on pins 3-4) at CN114 while in +VDD_Panel mode (jumper on 1-2 or 5-6 at CN117.) Doing so will destroy the LVDS control circuitry.

3.3.4 LVDS VCC Voltage Select (CN114)

Table 3-22 lists the pin signals of the LVDS VCC Voltage Select jumper header, which provides 6 pins in two rows with odd/even pin sequence (1,2) and 2mm pitch.

Table 3-22: LVDS VCC Voltage Select Signals (CN114)

Pin #	Signal	Pin #	Signal	Jumper Positions
1	+VLCD_3P3	2	+VCC_PANEL_IN	• Pins 1-2 for selecting +3.3V LVDS VCC panel voltage [**default**] • Pins 3-4 for selecting +12V LVDS VCC panel voltage • Pins 5-6 for selecting +5V LVDS VCC panel voltage
3	+VLCD_12P0	4	+VCC_PANEL_IN	
5	+VLCD_5P0	6	+VCC_PANEL_IN	

NOTE: A jumper must be placed on pins 3-4 of header CN117 to enable VCC mode.

3.3.5 LVDS VDD Voltage Select (CN117)

Table 3-22 lists the pin signals of the LVDS VDD Voltage Select jumper header, which provides 6 pins in two rows with odd/even pin sequence (1,2) and 2mm pitch.

Table 3-23: LVDS Voltage Select Signals (CN117)

Pin #	Signal	Pin #	Signal	Jumper Positions
1	+VLCD_3P3	2	+VDD_PANEL_IN	• Pins 1-2 for selecting +3.3V LVDS VDD panel voltage • Pins 3-4 for enabling LVDS VCC mode [**default**] • Pins 5-6 for selecting +5V LVDS VDD panel voltage
3	+VCC_PANEL	4	+VDD_PANEL_IN	
5	+VLCD_5P0	6	+VDD_PANEL_IN	

NOTE: Move jumper to 1-2 or 5-6 to enable VDD mode.

3.3.6 LVDS / eDP Mode Select (CN120)

Table 3-22 lists the pin signals of the LVDS / EDP Mode Select jumper header, which provides 6 pins in two rows with odd/even pin sequence (1,2) and 2mm pitch.

Table 3-24: LVDS / eDP mode Select (CN120)

Pin #	Signal	Pin #	Signal	Jumper Positions
1	LVDS_eDP_SEL_R*	2	Not Connected	• Pins 1-3 for selecting eDP mode • Pins 4-6 for selecting LVDS mode [**default**]
3	LVDS_eDP_SEL	4	LVDS_eDP_SEL	
5	Not Connected	6	GND	

* Pin-1 signal = +V3P3S with 4.7K PU

3.3.7 Backlight Voltage Select (CN207)

Table 3-25 lists the pin signals of the Backlight Voltage select jumper header, which provides 6 pins in two rows with odd/even pin sequence (1,2) and 2.54mm pitch.

Table 3-25: Backlight Voltage Select (CN207)

Pin #	Signal	Pin #	Signal	Jumper Positions
1	+VLCD_12P0	2	+VCC_BKL_IN	• Jumpers on 1-2 and 3-4 selects 12V supply to backlight (both jumpers needed in case of high-powered backlights) [**default**] • Jumper on 7-8 selects 5V supply to backlight
3	+VLCD_12P0	4	+VCC_BKL_IN	
5	Not Connected	6	Not Connected	
7	+VLCD_5P0	8	+VCC_BKL_IN	

3.3.8 eDP0 (CN121)

Table 3-26 lists the pin signals of the embedded DisplayPort 0 connector, which provides 40-pins, single row with 0.5mm pitch.

Table 3-26: eDP0 Video Signals (CN121)

Pin #	Signal	Description
1	NC	Not Connected
2	eDP0_BKLT_PWR	Backlight power (5V / 12V [selected at CN59])
3	eDP0_BKLT_PWR	Backlight power (5V / 12V [selected at CN59])
4	eDP0_BKLT_PWR	Backlight power (5V / 12V [selected at CN59])
5	eDP0_BKLT_PWR	Backlight power (5V / 12V [selected at CN59])
6	NC	Not Connected
7	NC	Not Connected
8	eDP0_BKLT_PWM	Backlight brightness via pulse width modulation (PWM)

Table 3-26: eDP0 Video Signals (CN121) (Continued)

Pin #	Signal	Description
9	eDP0_BKLT_ENABLE	Backlight power enable
10	eDP0_BKLT_GND	Backlight ground
11	eDP0_BKLT_GND	Backlight ground
12	eDP0_BKLT_GND	Backlight ground
13	eDP0_BKLT_GND	Backlight ground
14	eDP0_HPD	Hot Plug Detect
15	eDP0_LCD_GND	LCD ground
16	eDP0_LCD_GND	LCD ground
17	eDP0_LCD_GND	LCD ground
18	eDP0_LCD_GND	LCD ground
19	NC	Not Connected
20	eDP0_LCD_VCC	LCD power (3.3V / 5V / 12V)
21	eDP0_LCD_VCC	LCD power (3.3V / 5V / 12V)
22	eDP0_LCD_VCC	LCD power (3.3V / 5V / 12V)
23	eDP0_LCD_VCC	LCD power (3.3V / 5V / 12V)
24	eDP0_HS_GND	High-Speed Ground
25	eDP0_AUX_n	Auxiliary differential pair - negative
26	eDP0_AUX_p	Auxiliary differential pair - positive
27	eDP0_HS_GND	High-Speed Ground
28	eDP0_TX0_p	Lane 0 Display Port primary channel differential pair 0 - positive
29	eDP0_TX0_n	Lane 0 Display Port primary channel differential pair 0 - negative
30	eDP0_HS_GND	High-Speed Ground
31	eDP0_TX1_p	Lane 1 Display Port primary channel differential pair 1 - positive
32	eDP0_TX1_n	Lane 1 Display Port primary channel differential pair 1 - negative
33	eDP0_HS_GND	High-Speed Ground
34	eDP0_TX2_p	Lane 2 Display Port primary channel differential pair 2 - positive
35	eDP0_TX2_n	Lane 2 Display Port primary channel differential pair 2 - negative
36	eDP0_HS_GND	High-Speed Ground
37	eDP0_TX3_p	Lane 3 Display Port primary channel differential pair 3 - positive
38	eDP0_TX3_n	Lane 3 Display Port primary channel differential pair 3 - negative
39	eDP0_HS_GND	High-Speed Ground
40	NC	Not Connected

NOTE: The shaded table cells denote power or ground.

3.3.9 eDP1 (CN118)

Table 3-27 lists the pin signals of the embedded DisplayPort 1 connector, which provides 40-pins, single row with 0.5mm pitch.

Table 3-27: eDP1 Video Signals (CN118)

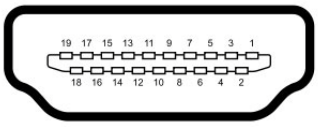
Pin #	Signal	Description
1	NC	Not Connected
2	eDP1_BKLT_PWR	Backlight power (5V / 12V [selected at CN207])
3	eDP1_BKLT_PWR	Backlight power (5V / 12V [selected at CN207])
4	eDP1_BKLT_PWR	Backlight power (5V / 12V [selected at CN207])
5	eDP1_BKLT_PWR	Backlight power (5V / 12V [selected at CN207])
6	NC	Not Connected
7	NC	Not Connected
8	eDP1_BKLT_PWM	Backlight brightness via pulse width modulation (PWM)
9	eDP1_BKLT_ENABLE	Backlight power enable
10	eDP1_BKLT_GND	Backlight ground
11	eDP1_BKLT_GND	Backlight ground
12	eDP1_BKLT_GND	Backlight ground
13	eDP1_BKLT_GND	Backlight ground
14	eDP1_HPD	Hot Plug Detect
15	eDP1_LCD_GND	LCD ground
16	eDP1_LCD_GND	LCD ground
17	eDP1_LCD_GND	LCD ground
18	eDP1_LCD_GND	LCD ground
19	NC	Not Connected
20	eDP1_LCD_VCC	LCD power (3.3V / 5V / 12V)
21	eDP1_LCD_VCC	LCD power (3.3V / 5V / 12V)
22	eDP1_LCD_VCC	LCD power (3.3V / 5V / 12V)
23	eDP1_LCD_VCC	LCD power (3.3V / 5V / 12V)
24	eDP1_HS_GND	High-Speed Ground
25	eDP1_AUX_n	Auxiliary differential signal - negative
26	eDP1_AUX_p	Auxiliary differential signal - positive
27	eDP1_HS_GND	High-Speed Ground
28	eDP1_TX0_p	Lane 0 Display Port primary channel differential signal 0 - positive
29	eDP1_TX0_n	Lane 0 Display Port primary channel differential signal 0 - negative
30	eDP1_HS_GND	High-Speed Ground
31	eDP1_TX1_p	Lane 1 Display Port primary channel differential signal 1 - positive
32	eDP1_TX1_n	Lane 1 Display Port primary channel differential signal 1 - negative
33	eDP1_HS_GND	High-Speed Ground
34	eDP1_TX2_p	Lane 2 Display Port primary channel differential signal 2 - positive
35	eDP1_TX2_n	Lane 2 Display Port primary channel differential signal 2 - negative
36	eDP1_HS_GND	High-Speed Ground
37	eDP1_TX3_p	Lane 3 Display Port primary channel differential signal 3 - positive
38	eDP1_TX3_n	Lane 3 Display Port primary channel differential signal 3 - negative
39	eDP1_HS_GND	High-Speed Ground
40	NC	Not Connected

NOTE: The shaded table cells denote power or ground.

3.3.10 HDMI (CN123)

Table 3-31 lists the pin signals of the HDMI interface, which provides a 19-pin, standard two-row connector with 0.5mm pitch.

Table 3-28: HDMI Signals (CN123)

Pin #	Signal	Description	Pin Sequence
1	HDMI_D2_P	Data2 differential signal - Positive	 HDMI Type A Plug Connector
2	GND	Data2 Ground	
3	HDMI_D2_N	Data2 differential signal - Negative	
4	HDMI_D1_P	Data1 differential signal - Positive	
5	GND	Data1 Ground	
6	HDMI_D1_N	Data1 differential signal - Negative	
7	HDMI_D0_P	Data0 differential signal - Positive	
8	GND	Data0 Ground	
9	HDMI_D0_N	Data0 differential signal - Negative	
10	HDMI_CK_P	Clock - Positive	
11	GND	Clock Ground	
12	HDMI_CK_N	Clock - Negative	
13	HDMI_CEC	Consumer Electronics Control bus	
14	NC	Not Connected	
15	HDMI_SCL	I2C Serial Clock for DDC	
16	HDMI_SDA	I2C Serial Data for DDC	
17	GND	DDC / CEC Ground	
18	HDMI_+5V	5 Volts Power	
19	HDMI_HPD	Hot Plug Detect	

NOTE: The shaded table cells denote power or ground.

3.3.11 HDMI Configuration Switch (SW46)

Table 3-29 lists the pin signals of the HDMI configuration dip switch, which provides 4 poles, 8 pin positions with 1.27mm pitch.

Table 3-29: HDMI Configuration Switch (SW46)

Position	Signal	Position	Signal
1 (off)	HDMI_EQ5 [**Default**]	8 (on)	HDMI_EQ5_10K_H (+V3P3S)
2 (off)	HDMI_EQ5 [**Default**]	7 (on)	+V3P3S
3 (off)	HDMI_EQ5	6 (on)	GND [**Default**]
4 (off)	HDMI_EQ5 [**Default**]	5 (on)	HDMI_EQ5_10K_L (GND)

Only one ON Position allowed at the same time among poles 1-4
Config 1: 1-Off, 2-Off, 3-On, 4-Off = +0.0dB
Config 2: 1-Off, 2-Off, 3-Off, 4-On = +2.0dB
Config 3: 1-Off, 2-Off, 3-Off, 4-Off = +3.5dB
Config 4: 1-On, 2-Off, 3-Off, 4-Off = +9.0dB
Config 5: 1-Off, 2-On, 3-Off, 4-Off = +7.0dB

3.3.12 HDMI / DP1 Mode Select (CN125)

Table 3-30 lists the pin signals of the HDMI/DP1 Mode Select jumper header, which provides 5 pins in a single row with 2.00mm pitch.

Table 3-30: HDMI / DP1 Mode Select (CN125)

Pin #	Signal	Jumper Positions
1	HDMI_DP1_SEL_H	• Jumper Installed on 1-2 - DisplayPort mode • Jumper Installed on 2-3 - HDMI mode • Jumper Installed on 4-5 - Controlled by HDMI, CN123 Connector [**default**]
2	HDMI_DP1_SEL2	
3	GND	
4	HDMI_HPD_G	
5	HDMI_HDP	

When a jumper is installed in the default position on pins 3-4, the HDMI connector will determine the mode. In this case, if the HDMI connector is occupied, the HDMI mode is enabled. If the HDMI connector is not occupied, the DP mode is enabled.

3.3.13 DisplayPort++ 0 (CN122)

Table 3-31 lists the pin signals of the DisplayPort++ 0 connector, which provides 20-pins, single row with 0.5mm pitch.

Table 3-31: DisplayPort++ 0 Signals (CN122)

Pin #	Signal	Description
1	DP0_LANE0_P	Lane 0 DisplayPort primary channel differential signal - positive
2	GND	Ground
3	DP0_LANE0_N	Lane 0 DisplayPort primary channel differential signal - negative
4	DP0_LANE1_P	Lane 1 DisplayPort primary channel differential signal - positive
5	GND	Ground
6	DP0_LANE1_N	Lane 1 DisplayPort primary channel differential signal - negative
7	DP0_LANE2_P	Lane 2 DisplayPort primary channel differential signal - positive
8	GND	Ground
9	DP0_LANE2_N	Lane 2 DisplayPort primary channel differential signal - negative
10	DP0_LANE3_P	Lane 3 DisplayPort primary channel differential signal - positive
11	GND	Ground
12	DP0_LANE3_N	Lane 3 DisplayPort primary channel differential signal - negative
13	DP0_AUX_SEL	DisplayPort auxiliary signal pulled to ground for dual mode
14	DP0_CEC	Not Supported
15	DP0_AUX_P	DisplayPort auxiliary channel differential signal - positive
16	GND	Ground
17	DP0_AUX_N	DisplayPort auxiliary channel differential signal - negative
18	DP0_HDP	DisplayPort Hot Plug Detect
19	GND	Ground
20	+3V3S_DP0	DisplayPort Power

NOTE: The shaded table cells denote power or ground.

3.3.14 DisplayPort++ 1 (CN124)

Table 3-31 lists the pin signals of the DisplayPort++ 1 connector, which provides 20-pins, single row with 0.5mm pitch.

Table 3-32: DisplayPort++ 1 Signals (CN124)

Pin #	Signal	Description
1	DP1_LANE0_P	Lane 0 DisplayPort primary channel differential signal - positive
2	GND	Ground
3	DP1_LANE0_N	Lane 0 DisplayPort primary channel differential signal - negative
4	DP1_LANE1_P	Lane 1 DisplayPort primary channel differential signal - positive
5	GND	Ground
6	DP1_LANE1_N	Lane 1 DisplayPort primary channel differential signal - negative
7	DP1_LANE2_P	Lane 2 DisplayPort primary channel differential signal - positive
8	GND	Ground
9	DP1_LANE2_N	Lane 2 DisplayPort primary channel differential signal - negative
10	DP1_LANE3_P	Lane 3 DisplayPort primary channel differential signal - positive
11	GND	Ground
12	DP1_LANE3_N	Lane 3 DisplayPort primary channel differential signal - negative
13	DP1_AUX_SEL	DisplayPort auxiliary signal pulled to ground for dual mode
14	DP1_CEC	Not Supported
15	DP1_AUX_P	DisplayPort auxiliary channel differential signal - positive
16	GND	Ground
17	DP1_AUX_N	DisplayPort auxiliary channel differential signal - negative
18	DP1_HDP	DisplayPort Hot Plug Detect
19	GND	Ground
20	+3V3S_DP0	DisplayPort Power

NOTE: The shaded table cells denote power or ground.

3.4 I2C Interfaces

The LEC-BASE 2.0 supports I2C interfaces for General Purpose, Camera, and Power Management. This section provides the pinout tables for all I2C interfaces including the pinout tables for all support interfaces and jumper headers.

3.4.1 I2C GP (CN105)

Table 3-33 lists the pin signals of the I2C GP header, which provides 4 pins in a single row with 2.00mm pitch.

Table 3-33: I2C GP (CN105)

Pin #	Signal
1	I2C_GP_CK
2	Ground
3	+VCC_I2C_GP
4	I2C_GP_DAT

NOTE: Shaded table cells denote ground or power. Use CN196 to select voltages. Current draw must not exceed 300mA.

3.4.2 I2C CAM0 (CN106)

Table 3-33 lists the pin signals of the I2C CAM0 header, which provides 4 pins in a single row with 2.00mm pitch.

Table 3-34: I2C CAM0 (CN106)

Pin #	Signal
1	I2C_CAM0_CK
2	Ground
3	+VCC_CAM0_GP
4	I2C_CAM0_DAT

NOTE: Shaded table cells denote ground or power. Use CN197 to select voltages. Current draw must not exceed 300mA.

3.4.3 I2C CAM1 (CN107)

Table 3-33 lists the pin signals of the I2C CAM1 header, which provides 4 pins in a single row with 2.00mm pitch.

Table 3-35: I2C CAM1 (CN107)

Pin #	Signal
1	I2C_CAM1_CK
2	Ground
3	+VCC_CAM1_GP
4	I2C_CAM1_DAT

NOTE: Shaded table cells denote ground or power. Use CN198 to select voltages. Current draw must not exceed 300mA.

3.4.4 I2C PM (CN108)

Table 3-33 lists the pin signals of the I2C PM header, which provides 4 pins in a single row with 2.00mm pitch.

Table 3-36: I2C PM (CN108)

Pin #	Signal
1	I2C_PM_CK
2	Ground
3	+VCC_PM_GP
4	I2C_PM_DAT

NOTE: Shaded table cells denote ground or power. Use CN195 to select voltages. Current draw must not exceed 300mA.

3.4.5 I2C EEPROM Socket (CN194)

Table 3-37 lists the pin signals of the I2C EEPROM socket, which provides 8 pins in two rows with consecutive pin sequence (1,8) and 2.54mm pitch.

Table 3-37: I2C EEPROM Socket (CN194)

Pin #	Signal	Pin #	Signal
1	CR_I2C_A0	8	GND
2	CR_I2C_A1	7	CR_I2C_WP#
3	CR_I2C_A2	6	I2C_PMI2C.PM_CK
4	GND	5	I2C_PMI2C.PM_DAT

NOTE: Shaded table cells denote power or ground.

3.4.6 I2C_PM Voltage Select (CN195)

Table 3-38 lists the pin signals of the I2C_PM Voltage Select jumper header, which provides 6 pins in two rows with odd/even pin sequence (1,2) and 2.00mm pitch.

Table 3-38: I2C_PM Voltage Select (CN195)

Pin #	Signal	Pin #	Signal	Jumper Positions
1	+V1P8S	2	+VCC_I2C_PM	• Jumper on 1-2 selects 1.8V for the I2C_PM interface [**default**] • Jumper on 3-4 selects 5.0V for the I2C_PM interface • Jumper on 5-6 selects 3.3V for the I2C_PM interface
3	+V5P0S_FS_PM	4	+VCC_I2C_PM	
5	+V3P3S	6	+VCC_I2C_PM	

NOTE: Draw current must not be above 300mA. To disable voltage output, install a jumper on either 2-4 or 4-6.

3.4.7 I2C_GP Voltage Select (CN196)

Table 3-39 lists the pin signals of the I2C_GP Voltage Select jumper header, which provides 6 pins in two rows with odd/even pin sequence (1,2) and 2.00mm pitch.

Table 3-39: I2C_GP Voltage Select (CN196)

Pin #	Signal	Pin #	Signal	Jumper Positions
1	+V1P8S	2	+VCC_I2C_GP	• Jumper on 1-2 selects 1.8V for the I2C_GP interface [**default**] • Jumper on 3-4 selects 5.0V for the I2C_GP interface • Jumper on 5-6 selects 3.3V for the I2C_GP interface
3	+V5P0S_FS_GP	4	+VCC_I2C_GP	
5	+V3P3S	6	+VCC_I2C_GP	

NOTE: Draw current must not be above 300mA. To disable voltage output, install a jumper on either 2-4 or 4-6.

3.4.8 I2C_CAM0 Voltage Select (CN197)

Table 3-40 lists the pin signals of the I2C_CAM0 Voltage Select jumper header, which provides 6 pins in two rows with odd/even pin sequence (1,2) and 2.00mm pitch.

Table 3-40: I2C_CAM0 Voltage Select (CN197)

Pin #	Signal	Pin #	Signal	Jumper Positions
1	+V1P8S	2	+VCC_I2C_CAM0	• Jumper on 1-2 selects 1.8V for the I2C_CAM0 interface [**default**] • Jumper on 3-4 selects 5.0V for the I2C_CAM0 interface • Jumper on 5-6 selects 3.3V for the I2C_CAM0 interface
3	+V5P0S_FCAM0	4	+VCC_I2C_CAM0	
5	+V3P3S	6	+VCC_I2C_CAM0	

NOTE: Draw current must not be above 300mA. To disable voltage output, install a jumper on either 2-4 or 4-6.

3.4.9 I2C_CAM1 Voltage Select (CN198)

Table 3-41 lists the pin signals of the I2C_CAM1 Voltage Select jumper header, which provides 6 pins in two rows with odd/even pin sequence (1,2) and 2.00mm pitch.

Table 3-41: I2C_CAM1 Voltage Select (CN198)

Pin #	Signal	Pin #	Signal	Jumper Positions
1	+V1P8S	2	+VCC_I2C_CAM1	• Jumper on 1-2 selects 1.8V for the I2C_CAM1 interface [**default**] • Jumper on 3-4 selects 5.0V for the I2C_CAM1 interface • Jumper on 5-6 selects 3.3V for the I2C_CAM1 interface
3	+V5P0S_FCAM1	4	+VCC_I2C_CAM1	
5	+V3P3S	6	+VCC_I2C_CAM1	

NOTE: Draw current must not be above 300mA. To disable voltage output, install a jumper on either 2-4 or 4-6.

3.5 Fan Interface

This section provides the pinout tables for both the CPU Fan interface and the Fan interface voltage select jumper header.

3.5.1 Fan I/O (CN109)

Table 3-42 lists the pin signals of the CPU fan header, which provides 4 pins in a single row with 2.54mm pitch.

Table 3-42: Fan (CN109)

Pin #	Signal
1	GND
2	+V_FAN
3	FAN_TACH_IN (measures fan speed)
4	FAN_PWM_OUT (sets fan speed)

NOTE: Shaded table cells denote power or ground. Use CN112 to select voltage.

3.5.2 Fan Voltage Select (CN112)

Table 3-43 lists the pin signals of the Fan Voltage Select jumper header, which provides 3 pins in a single row with 2mm pitch.

Table 3-43: Fan Voltage Select (CN112)

Pin #	Signal	Jumper Positions
1	+V12P0_ATX	• Jumper installed on pins 1-2 to select 12-volt fan voltage [**default**] • Jumper installed on pins 2-3 to select 5-volt fan voltage
2	+V_FAN	
3	+V5P0A	

3.6 Camera Interfaces

This section describes the MIPI-CSI and GPIO Camera interfaces. The primary camera interface is the MIPI-CSI interface, which complies with the MIPI-CSI 2.0 specification and allows dual-role usage of the I2C camera interfaces for other I2C functions if no camera is in use. The GPIO Camera interface is used for user-specified camera add-on cards.

3.6.1 MIPI-CSI Camera Interface (CN208)

Table 3-44 lists the pin signals of the MIPI-CSI camera interface, which provides 36 pins, 1 row, consecutive sequence with 0.02" (0.50mm) pitch.

Table 3-44: MIPI-CSI Camera Interface Signals (CN208)

Pin #	Signal	Description
1	+VCAM33_OUT	3.3 volts +/-5% to power the camera device (output)
2	+VCAM33_OUT	3.3 volts +/-5% to power the camera device (output)
3	CSI1.RX0_P	CSI1 Data Lane 0+
4	CSI1.RX0_N	CSI1 Data Lane 0-
5	GND	Ground
6	CSI1.RX1_P	CSI1 Data Lane 1+
7	CSI1.RX1_N	CSI1 Data Lane 1-
8	GND	Ground
9	CSI1.RX2_P	CSI1 Data Lane 2+
10	CSI1.RX2_N	CSI1 Data Lane 2-
11	CSI1_CAM1_RST#	Camera 1 Reset (active low; CMOS 1.8V; output)
12	CSI1.RX3_P	CSI1 Data Lane 3+
13	CSI1.RX3_N	CSI1 Data Lane 3-
14	GND	Ground
15	CSI1.CK_P	CSI1 Differential Clock+ (Strobe; D-PHY; input)
16	CSI1.CK_N	CSI1 Differential Clock- (Strobe; D-PHY; input)
17	GND	Ground
18	CSI1.TX_P/ I2C_CAM1_CK	Camera 1 Control Interface Clock (I2C-like interface; CMOS 1.8V OD; output) NOTE: The CSI1.TX_P signal is currently not supported by SMARC modules because it is part of the MIPI-CSI 3 specification, which is not currently supported by the SMARC 2.0 specification.
19	CSI1.TX_N/ I2C_CAM1_DAT	Camera 1 Control Interface Data (I2C-like interface; CMOS 1.8V OD; input/output) NOTE: The CSI1.TX_N signal is currently not supported by SMARC modules because it is part of the MIPI-CSI 3 specification, which is not currently supported by the SMARC 2.0 specification.

Table 3-44: MIPI-CSI Camera Interface Signals (CN208) (Continued)

Pin #	Signal	Description
20	CSI1.CAM1_PWR#	Camera 1 Power Enable (active low; CMOS 1.8V; output)
21	CAM_MCK_OUT	Master Clock (may be used by cameras to drive internal PLL; frequency range: 6 - 27MHz; CMOS 1.8V; output)
22	CSI0.CAM0_PWR#	Camera 0 Enable (active low; CMOS 1.8V OD; output)
23	CSI0.TX_P/ I2C_CAM0_CK	Camera 0 Control Interface Clock (I2C-like interface; CMOS 1.8V OD; input/output) NOTE: The CSI0.TX_P signal is currently not supported by SMARC modules because it is part of the MIPI-CSI 3 specification, which is not currently supported by the SMARC 2.0 specification.
24	CSI0.TX_N/ I2C_CAM0_DAT	Camera 0 Control Interface Data (I2C-like interface; CMOS 1.8V OD; input/output) NOTE: The CSI0.TX_N signal is currently not supported by SMARC modules because it is part of the MIPI-CSI 3 specification, which is not currently supported by the SMARC 2.0 specification.
25	GND	Ground
26	CSI0_CLK_P	CSI0 Differential Clock+ (Strobe; D-PHY; input)
27	CSI0_CLK_N	CSI0 Differential Clock- (Strobe; D-PHY; input)
28	GND	Ground
29	CSI0.RX0_P	CSI0 Data Lane 0+ (D-PHY; input)
30	CSI0.RX0_N	CSI0 Data Lane 0- (D-PHY; input)
31	CSI0_CAM0_RST#	Camera 0 Reset (active low; CMOS 1.8V; output
32	CSI0_RX1_P	CSI0 Data Lane 1+ (D-PHY; input)
33	CSI0_RX1_N	CSI0 Data Lane 1- (D-PHY; input)
34	GND	
35	CAM0_GPIO	GPIO for Camera 0 (CMOS 1.8V; input/output)
36	CAM1_GPIO	GPIO for Camera 1 (CMOS 1.8V; input/output)

NOTE: The gray table cells denote ground or power. The # symbol indicates the signal is Active Low.

3.6.2 GPIO Camera Interface (CN127)

Table 3-45 lists the pin signals of the GPIO Camera Interface header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-45: GPIO Camera Interface (CN127)

Pin #	Signal
1	CAM0_GPIO
2	GND
3	CAM1_GPIO

These two GPIOs follow the SGET Q7 specification 2.1. They can be used by camera add-on cards for user-specified camera functions. Not supported by the ADLINK LEC-BASE 2.0 camera add-on card.

3.7 IEEE 1588 Trigger Interface (CN130)

Table 3-46 lists the pin signals of the IEEE 1588 Precision Time Protocol trigger interface, which provides 4 pins in two rows with odd/even pin sequence (1,2) and 2.54mm pitch.

Table 3-46: IEEE 1588 Trigger Interface (CN130)

Pin #	Signal	Pin #	Signal
1	GBE_TRIGGER.1	2	GND
3	GBE_TRIGGER.0	4	GND

NOTE: These pins provide circuitry to trigger the IEEE 1588 Precision Time Protocol function on the module's Ethernet controller, if supported, at 3.3V signal level.

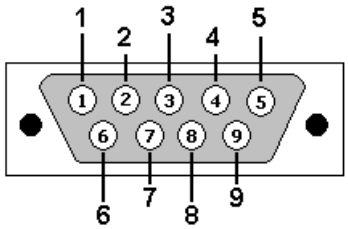
3.8 Serial Interfaces

This section describes the signals of the dual, standard DB9 serial port connectors for RS232 connectivity.

3.8.1 COM0 (CN134 [top])

Table 3-47 lists the signals of the COM0, 4-wire RS232 interface, which provides a standard dual DB9 connector.

Table 3-47: COM0 Signals (CN134 [top])

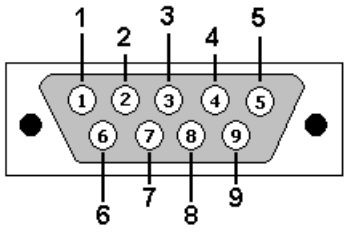
Pin #	Signal	Pin Sequence
1	Not Connected	
2	COM0_RX	
3	COM0_TX	
4	Not Connected	
5	GND	
6	Not Connected	
7	COM0_RTS#	
8	COM0_CTS#	
9	Not Connected	

NOTE: Shaded table cell denotes ground. The # symbol indicates the signal is Active Low.

3.8.2 COM1 (CN134 [bottom])

Table 3-48 lists the signals of the COM1, 2-wire RS232 interface, which provides a standard DB9 connector.

Table 3-48: COM1 Signals (CN134 [bottom])

Pin #	Signal	Pin Sequence
1	Not Connected	
2	COM1_RX	
3	COM1_TX	
4	Not Connected	
5	GND	
6	Not Connected	
7	Not Connected	
8	Not Connected	
9	Not Connected	

NOTE: Shaded table cell denotes ground. The # symbol indicates the signal is Active Low.

3.8.3 Serial 2 (COM2) Interface (CN210)

Table 3-49 lists the pin signals of the 4-wire Serial 2 interface, which provides 10 pins in two rows with odd/even pin sequence (1,2) and 2.00mm pitch.

Table 3-49: Serial 2 (COM2) Interface (CN210)

Pin #	Signal	Pin #	Signal
1	TP59	2	TP60
3	RX2	4	RTS2#
5	TX2	6	CTS2#
7	TP61	8	TP62
9	GND	10	TP63

NOTE: Shaded table cell denotes ground. The # symbol indicates the signal is Active Low.

3.8.4 Serial 3 (COM3) Interface (CN209)

Table 3-50 lists the pin signals of the 2-wire Serial 3 interface, which provides 10 pins in two rows with odd/even pin sequence (1,2) and 2.00mm pitch.

Table 3-50: Serial 3 (COM3) Interface (CN209)

Pin #	Signal	Pin #	Signal
1	TP64	2	TP65
3	RX3	4	TP66
5	TX3	6	TP67
7	TP68	8	TP69
9	GND	10	TP70

NOTE: Shaded table cell denotes ground.

3.8.5 Serial Voltage Mode Select (CN204)

Table 3-51 lists the pin signals of the Serial Voltage Mode select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-51: Serial Voltage Mode Select (CN204)

Pin #	Signal	Jumper Positions
1	+V1P8S	• Jumper Installed 1-2 selects +V1P8S Serial Voltage mode [**default**] • Jumper Installed 2-3 selects +V1P8S_SBY Serial Voltage mode
2	+VCCA_SERIAL	
3	+V1P8S_SBY	

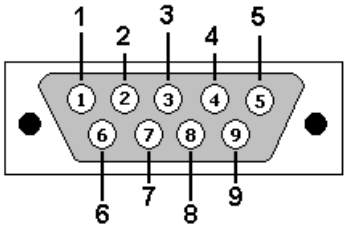
3.9 CAN Interfaces (Controller Area Network)

This section describes the signals of the dual, standard DB9 CAN port connectors for Controller Area Network connectivity.

3.9.1 CAN0 (CN136 [top])

Table 3-52 lists the signals of the Controller Area Network interface, CAN0, which provides a standard DB9 connector.

Table 3-52: CAN0 Signals (CN136 [top])

Pin #	Signal	Pin Sequence
1	Not Connected	
2	CAN0_L	
3	GND_CAN	
4	Not Connected	
5	Not Connected	
6	GND_CAN	
7	CAN0_H	
8	Not Connected	
9	Not Connected	

NOTE: These pins are connected over the CAN transceiver to the CAN0 SMARC connector interface (pins P143 and P144.) Shaded table cells denote ground.

3.9.2 CAN0 Termination (CN137)

Table 3-53 lists the pin signals of the CAN0 Termination jumper header, which provides 4 pins in two rows with odd/even pin sequence (1,2) and 2.54mm pitch.

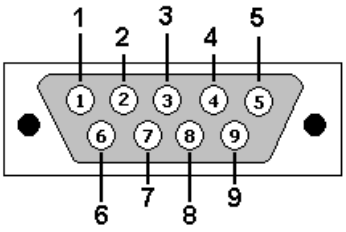
Table 3-53: CAN0 Termination (CN137)

Pin #	Signal	Pin #	Signal	Jumper Positions
1	CAN0_TH	2	GND	• Pins 1-3 and 2-4 for selecting 120 Ohm line termination [**default**] • Pins 1-2 and 3-4 for selecting 2x 60Ohm, GND-centered termination
3	CAN0_TL	4	GND	

3.9.3 CAN1 (CN136 [bottom])

Table 3-54 lists the signals of the Controller Area Network interface, CAN1, which provides a standard DB9 connector.

Table 3-54: CAN1 Signals (CN136 [bottom])

Pin #	Signal	Pin Sequence
1	Not Connected	
2	CAN1_L	
3	GND_CAN	
4	Not Connected	
5	Not Connected	
6	GND_CAN	
7	CAN1_H	
8	Not Connected	
9	Not Connected	

NOTE: These pins are connected over the CAN transceiver to the CAN1 SMARC connector interface (pins P145 and P146.) Shaded table cell denotes ground.

3.9.4 CAN1 Termination (CN135)

Table 3-55 lists the pin signals of the CAN1 Termination jumper header, which provides 4 pins in two rows with odd/even pin sequence (1,2) and 2.54mm pitch.

Table 3-55: CAN1 Termination (CN135)

Pin #	Signal	Pin #	Signal	Description
1	CAN1_TH	2	GND	• Pins 1-3 and 2-4 for selecting 120 Ohm line termination [**default**] • Pins 1-2 and 3-4 for selecting 2x 60Ohm, GND-centered termination
3	CAN1_TL	4	GND	

3.10 SPI Interfaces

3.10.1 SPI0 Voltage Select (CN145)

Table 3-56 lists the pin signals of the SPI0 Voltage Select jumper header, which provides 3 pins in a single row with 2.54mm pitch.

Table 3-56: SPI0 Voltage Select (CN145)

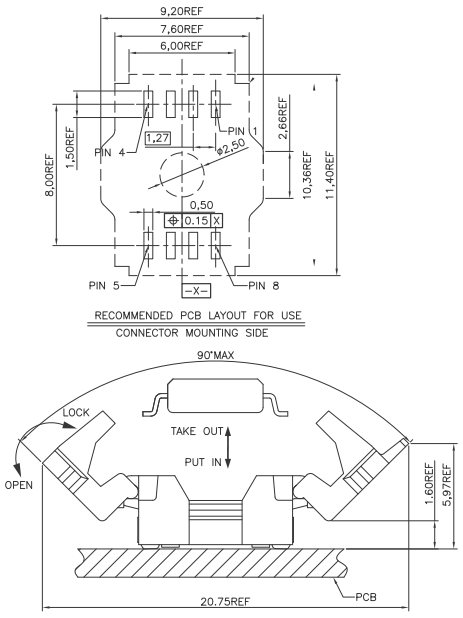
Pin #	Signal	Jumper Positions
1	+V1P8S	• Jumper Installed 1-2 to select 1.8V for +VCC_SPI0 [**default**] • Jumper Installed 2-3 to select 3.3V for +VCC_SPI0
2	+VCC_SPI	
3	+V3P3S	

3.10.2 SPI0 Flash Socket (CN146)

Table 3-22 lists the pin signals of the SPI0 Flash socket, which provides 8 pins in two rows with consecutive pin sequence (1,8) and 1.27mm pitch.

Table 3-57: SPI0 Flash Socket (CN146)

Pin #	Signal	Pin #	Signal
1	SPI0_SKT_CS#	8	+VCC_SPI0
2	SPI0_MISO	7	SPI0_SKT_HOLD#
3	SPI0_SKT_WP#	6	SPI0_CLK
4	GND	5	SPI0_MOSI



NOTE: Shaded table cells denote power or ground.

3.10.3 eSPI / SPI1 Voltage Select (CN147)

Table 3-58 lists the pin signals of the eSPI / SPI1 Voltage Select jumper header, which provides 3 pins in a single row with 2.54mm pitch.

Table 3-58: eSPI / SPI1 Voltage Select (CN147)

Pin #	Signal	Jumper Positions
1	+V1P8S	• Jumper Installed 1-2 to select 1.8V for +VCC_SPI1 [**default**] • Jumper Installed 2-3 to select 3.3V for +VCC_SPI1
2	+VCC_SPI1	
3	+V3P3S	

3.10.4 SPI0 Interface (CN148)

Table 3-59 lists the pin signals of the SPI0 interface, which provides 8 pins in two rows with odd/ even pin sequence (1,2) and 2.54mm pitch.

Table 3-59: SPI0 Interface (CN148)

Pin #	Signal	Pin #	Signal
1	SPI0_PH_HOLD#	2	SPI0_PH_WP#
3	SPI0_CS0#	4	SPI0_CS1#
5	GND	6	+VCC_SPI0
7	SPI0_CLK	8	Not Connected
9	SPI0_MOSI	10	SPI0_MISO

NOTE: Shaded table cells denote power or ground. The # symbol indicates the signal is Active Low.

3.10.5 SPI0 CS0/CS1 Select (CN149)

Table 3-60 lists the pin signals of the SPI0 CS0/ CS1 Select jumper header, which provides 3 pins in a single row with 2.54mm pitch.

Table 3-60: SPI0 CS0/CS1 Select (CN149)

Pin #	Signal	Jumper Positions
1	SPI0_CS0#	• Jumper Installed 1-2 to select SPI0_CS0# on socket [**default**] • Jumper Installed 2-3 to select SPI0_CS1# on socket
2	SPI0_SKT_CS#	
3	SPI0_CS1#	

NOTE: The # symbol indicates the signal is Active Low.

3.10.6 eSPI / SPI1 Interface (CN150)

Table 3-59 lists the pin signals of the eSPI / SPI1 interface, which provides 16 pins in two rows with odd/even pin sequence (1,2) and 2.54mm pitch.

Table 3-61: eSPI / SPI1 Interface (CN150)

Pin #	Signal	Pin #	Signal
1	SPI1_PH_HOLD#	2	SPI1_PH_WP#
3	SPI1_CS0#	4	SPI1_CS1#
5	GND	6	+VCC_SPI1
7	SPI1_CLK	8	GND
9	SPI1_IO0_MOSI	10	SPI1_IO1_MISO
11	SPI1_IO3	12	SPI1_IO2
13	ESPI_ALERT0#	14	ESPI_ALERT1#
15	ESPI_RESET#	16	GND

NOTE: Shaded table cells denote power or ground. The # symbol indicates the signal is Active Low.

3.10.7 SPI0 Configuration Switch (SW51)

Table 3-62 lists the pin signals of the SPI0 configuration dip switch, which provides 4 poles, 8 pin positions with 1.27mm pitch.

Table 3-62: SPI0 Configuration Switch (SW51)

Position	Signal	Position	Signal
1 (off)	SPI0_SKT_HOLD# [**Default**]	8 (on)	GND
2 (off)	SPI0_SKT_WP# [**Default**]	7 (on)	GND
3 (off)	SPI0_PH_HOLD# [**Default**]	6 (on)	GND
4 (off)	SPI0_PH_WP# [**Default**]	5 (on)	GND

NOTE: The # symbol indicates the signal is Active Low.

3.10.8 SPI1 Configuration Switch (SW52)

Table 3-63 lists the pin signals of the SPI1 configuration dip switch, which provides 4 poles, 8 pin positions with 1.27mm pitch.

Table 3-63: SPI1 Configuration Switch (SW52)

Position	Signal	Position	Signal
1 (off)	SPI1_HOLD# [**Default**]	8 (on)	GND
2 (off)	SPI1_WP# [**Default**]	7 (on)	GND
3 (off)	Not Connected [**Default**]	6 (on)	GND
4 (off)	Not Connected [**Default**]	5 (on)	GND

NOTE: The # symbol indicates the signal is Active Low.

3.11 SD Card Power Mode Select (CN152)

Table 3-64 lists the pin signals of the SD Card Power Mode Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-64: SD Card Power Mode Select (CN152)

Pin #	Signal	Jumper Positions
1	+V3P3_SBY	• Jumper Installed 1-2 to select the SD Card +V3.3 Standby power mode • Jumper Installed 2-3 to select the SD Card +V3.3S power mode [**default**]
2	SDIO.PWR_EN	
3	+V3P3S	

3.12 Audio Interfaces

Two audio interfaces (HD and I2S) on the LEC-BASE 2.0 are supported through standard connectors, and their signal definitions can be found in the Standard Hardware References section of Chapter 2. This section provides the pinout tables for all the supporting audio jumper headers.

3.12.1 HDA Voltage Select (CN154)

Table 3-65 lists the pin signals of the HD Audio Voltage Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-65: HDA Voltage Select (CN154)

Pin #	Signal	Jumper Positions
1	+V1P8S	• Jumper Installed 1-2 to select +VDDIO_HDA +V1.8 voltage • Jumper Installed 2-3 to select +VDDIO_HDA +V1.5 voltage [**default**]
2	+VDDIO_HDA_SRC	
3	+V1P5S	

3.12.2 External / Internal Mic BIAS Select (CN156)

Table 3-66 lists the pin signals of the External / Internal Mic BIAS Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-66: External / Internal Mic BIAS Select (CN156)

Pin #	Signal	Jumper Positions
1	MIC_BIAS	• Jumper Installed 1-2 to select Internal Mic BIAS • Jumper Installed 2-3 to select External Mic BIAS [**default**]
2	MICIN_CON	
3	MIC_BBIAS_EXT	

3.12.3 I2S Audio CODEC Select (CN157)

Table 3-67 lists the pin signals of the I2S Audio CODEC Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-67: I2S Audio CODEC Select (CN157)

Pin #	Signal	Jumper Positions
1	GND	• Jumper Installed 1-2 to select SGTL5000 CODEC [**default**] • Jumper Installed 2-3 to select TLV320 CODEC
2	TLVSEL_SGTLSEL#	
3	+3.3V	

3.13 GPIO Interfaces

Twelve GPIO ports support general purpose IO signals on three header interfaces. This section defines the signals of all three headers as well as the signals of all GPIO support jumper headers.

3.13.1 GPIO 0-3 Interface (CN167)

Table 3-68 lists the pin signals of the GPIO 0-3 interface, which provides 10 pins in two rows with odd/even pin sequence (1,2) and 2.54mm pitch.

Table 3-68: GPIO 0-3 Interface (CN167)

Pin #	Signal	Pin #	Signal
1	+V1P8S	2	GND
3	GPIO00	4	GND
5	GPIO01	6	GND
7	GPIO02	8	GND
9	GPIO03	10	+VGPIO0

NOTE: Shaded table cells denote power or ground.

3.13.2 GPIO 0-3 Enable (CN163)

Table 3-69 lists the pin signals of the GPIO 0-3 enable jumper header, which provides 8 pins in two rows with odd/even pin sequence (1,2) and 2.00mm pitch.

Table 3-69: GPIO 0-3 Enable (CN163)

Pin #	Signal	Pin #	Signal	Jumper Positions
1	GPIO00_R	2	GPIO.00	• Jumper on 1-2 enables GPIO0 • Jumper on 3-4 enables GPIO1 • Jumper on 5-6 enables GPIO2 • Jumper on 7-8 enables GPIO3 • All jumpers installed [**default**]
3	GPIO01_R	4	GPIO.01	
5	GPIO02_R	6	GPIO.02	
7	GPIO03_R	8	GPIO.03	

NOTE: The default setting for this header is all jumpers installed.

3.13.3 GPIO 0-3 Voltage Select (CN168)

Table 3-70 lists the pin signals of the GPIO 0-3 Voltage Select jumper header, which provides 6 pins in two rows with odd/even pin sequence (1,2) and 2.00mm pitch.

Table 3-70: GPIO 0-3 Voltage Select (CN168)

Pin #	Signal	Pin #	Signal	Jumper Positions
1	GND	2	+VGPIO0	• Jumper on 1-2 selects 0V for GPIO 0-3 [**default**] • Jumper on 3-4 selects 3.3V for GPIO 0-3 • Jumper on 5-6 selects 1.8V for GPIO 0-3
3	+V3P3S	4	+VGPIO0	
5	+V1P8S	6	+VGPIO0	

NOTE: Draw current must not be above 300mA.

3.13.4 GPIO 4-7 Interface (CN173)

Table 3-71 lists the pin signals of the GPIO 4-7 interface, which provides 10 pins in two rows with odd/even pin sequence (1,2) and 2.54mm pitch.

Table 3-71: GPIO 4-7 Interface (CN173)

Pin #	Signal	Pin #	Signal
1	+V1P8S	2	GND
3	GPIO04	4	GND
5	GPIO05	6	GND
7	GPIO06	8	GND
9	GPIO07	10	+VGPIO1

NOTE: Shaded table cells denote power or ground.

3.13.5 GPIO 4-7 Enable (CN169)

Table 3-72 lists the pin signals of the GPIO 4-7 enable jumper header, which provides 8 pins in two rows with odd/even pin sequence (1,2) and 2.00mm pitch.

Table 3-72: GPIO 4-7 Enable (CN169)

Pin #	Signal	Pin #	Signal	Jumper Positions
1	GPIO04_R	2	GPIO.04	• Jumper on 1-2 enables GPIO4 • Jumper on 3-4 enables GPIO5 [**default**] • Jumper on 5-6 enables GPIO6 [**default**] • Jumper on 7-8 enables GPIO7 [**default**]
3	GPIO05_R	4	GPIO.05	
5	GPIO06_R	6	GPIO.06	
7	GPIO07_R	8	GPIO.07	

NOTE: The default setting for this header is all jumpers installed.

If the HDA CODEC is being used, the GPIO4 port must remain disabled by keeping the jumper parked on pin 1 or pin 2. If a PWM controlled fan with tacho-function is used, the GPIO6 jumper must be set to park position.

3.13.6 GPIO 4-7 Voltage Select (CN174)

Table 3-73 lists the pin signals of the GPIO 4-7 Voltage Select jumper header, which provides 6 pins in two rows with odd/even pin sequence (1,2) and 2.00mm pitch.

Table 3-73: GPIO 4-7 Voltage Select (CN174)

Pin #	Signal	Pin #	Signal	Jumper Positions
1	GND	2	+VGPIO1	• Jumper on 1-2 selects 0V for GPIO 4-7 [**default**] • Jumper on 3-4 selects 3.3V for GPIO 4-7 • Jumper on 5-6 selects 1.8V for GPIO 4-7
3	+V3P3S	4	+VGPIO1	
5	+V1P8S	6	+VGPIO1	

NOTE: Draw current must not be above 300mA.

3.13.7 GPIO 8-11 Interface (CN179)

Table 3-74 lists the pin signals of the GPIO 8-11 interface, which provides 10 pins in two rows with odd/even pin sequence (1,2) and 2.54mm pitch.

Table 3-74: GPIO 8-11 Interface (CN179)

Pin #	Signal	Pin #	Signal
1	+V1P8S	2	GND
3	GPIO08	4	GND
5	GPIO09	6	GND
7	GPIO10	8	GND
9	GPIO11	10	+VGPIO2

NOTE: Shaded table cells denote power or ground.

3.13.8 GPIO 8-11 Enable (CN176)

Table 3-75 lists the pin signals of the GPIO 8-11 enable jumper header, which provides 8 pins in two rows with odd/even pin sequence (1,2) and 2.00mm pitch.

Table 3-75: GPIO 8-11 Enable (CN176)

Pin #	Signal	Pin #	Signal	Jumper Positions
1	GPIO08_R	2	GPIO.08	• Jumper on 1-2 enables GPIO8 [**default**] • Jumper on 3-4 enables GPIO9 [**default**] • Jumper on 5-6 enables GPI10 [**default**] • Jumper on 7-8 enables GPI11 [**default**]
3	GPIO09_R	4	GPIO.09	
5	GPIO010_R	6	GPIO.10	
7	GPIO011_R	8	GPIO.11	

NOTE: The default setting for this header is all jumpers installed.

3.13.9 GPIO 8-11 Voltage Select (CN180)

Table 3-76 lists the pin signals of the GPIO 8-11 Voltage Select jumper header, which provides 6 pins in two rows with odd/even pin sequence (1,2) and 2.00mm pitch.

Table 3-76: GPIO 8-11 Voltage Select (CN180)

Pin #	Signal	Pin #	Signal	Jumper Positions
1	GND	2	+VGPIO2	• Jumper on 1-2 selects 0V for GPIO 8-11 [**default**] • Jumper on 3-4 selects 3.3V for GPIO 8-11 • Jumper on 5-6 selects 1.8V for GPIO 8-11
3	+V3P3S	4	+VGPIO2	
5	+V1P8S	6	+VGPIO2	

NOTE: Draw current must not be above 300mA.

3.13.10 GPIO5 Fan Power Management Enable (CN199)

Table 3-77 lists the pin signals of the GPIO5 Fan PWM Out enable jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-77: GPIO5 Fan PWM Out Enable (CN199)

Pin #	Signal	Jumper Positions
1	FAN.PWM_OUT	• Jumper Installed on 1-2 disconnects GPIO5 from Fan Power Management • Jumper Installed on 2-3 connects GPIO5 to Fan Power Management [**default**]
2	FAN.PWM_OUT	
3	PWM_OUT	

NOTE: For headers CN199 and CN200 to function correctly, the jumpers on pins 5-6 and 7-8 of header CN169 must be in parked positions, which will inactivate for use the GPIO5 and GPIO6 ports.

3.13.11 GPIO6 Fan Tachometer Enable (CN200)

Table 3-78 lists the pin signals of the GPIO6 Fan Tacho In enable jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-78: GPIO6 Fan Tacho_In Enable (CN200)

Pin #	Signal	Jumper Positions
1	FAN.TACHO_IN	• Jumper Installed on 1-2 disconnects GPIO6 from Fan Tachometer • Jumper Installed on 2-3 connects GPIO6 to Fan Tachometer [**default**]
2	FAN.TACHO_IN	
3	TACHO_IN	

NOTE: For headers CN199 and CN200 to function correctly, the jumpers on pins 5-6 and 7-8 of header CN169 must be in parked positions, which will inactivate for use the GPIO5 and GPIO6 ports.

3.13.12 GPIO 0-3, 2.2K PU Configuration Switch (SW68)

Table 3-79 lists the pin signals of the GPIO 0-3, 2.2K PU configuration dip switch, which provides 4 poles, 8 pin positions with 1.27mm pitch.

Table 3-79: GPIO 0-3, 2.2K PU Configuration Switch (SW68)

Position	Signal	Position	Signal
1 (off)	+VGPIO0 [**Default**]	8 (on)	PU_GPIO00 (2.2K)
2 (off)	+VGPIO0 [**Default**]	7 (on)	PU_GPIO01 (2.2K)
3 (off)	+VGPIO0 [**Default**]	6 (on)	PU_GPIO02 (2.2K)
4 (off)	+VGPIO0 [**Default**]	5 (on)	PU_GPIO03 (2.2K)

NOTE: The 2.2K PUs are placed at the user end, near CN167, and the 10K PUs are placed near the module. The level shift circuit is placed between the 2K and 10K PUs.

3.13.13 GPIO 4-7, 2.2K PU Configuration Switch (SW69)

Table 3-80 lists the pin signals of the GPIO 4-7, 2.2K PU configuration dip switch, which provides 4 poles, 8 pin positions with 1.27mm pitch.

Table 3-80: GPIO 4-7, 2.2K PU Configuration Switch (SW69)

Position	Signal	Position	Signal
1 (off)	+VGPIO1 [**Default**]	8 (on)	PU_GPIO04 (2.2K)
2 (off)	+VGPIO1 [**Default**]	7 (on)	PU_GPIO05 (2.2K)
3 (off)	+VGPIO1 [**Default**]	6 (on)	PU_GPIO06 (2.2K)
4 (off)	+VGPIO1 [**Default**]	5 (on)	PU_GPIO07 (2.2K)

NOTE: The 2.2K PUs are placed at the user end, near CN173, and the 10K PUs are placed near the module. The level shift circuit is placed between the 2K and 10K PUs.

3.13.14 GPIO 8-11, 2.2K PU Configuration Switch (SW71)

Table 3-81 lists the pin signals of the GPIO 8-11, 2.2K PU configuration dip switch, which provides 4 poles, 8 pin positions with 1.27mm pitch.

Table 3-81: GPIO 8-11, 2.2K PU Configuration Switch (SW71)

Position	Signal	Position	Signal
1 (off)	+VGPIO2 [**Default**]	8 (on)	PU_GPIO08 (2.2K)
2 (off)	+VGPIO2 [**Default**]	7 (on)	PU_GPIO09 (2.2K)
3 (off)	+VGPIO2 [**Default**]	6 (on)	PU_GPIO10 (2.2K)
4 (off)	+VGPIO2 [**Default**]	5 (on)	PU_GPIO11 (2.2K)

NOTE: The 2.2K PUs are placed at the user end, near CN179, and the 10K PUs are placed near the module. The level shift circuit is placed between the 2K and 10K PUs.

3.13.15 GPIO 0-3, 10K PU Configuration Switch (SW72)

Table 3-82 lists the pin signals of the GPIO 0-3, 10K PU configuration dip switch, which provides 4 poles, 8 pin positions with 1.27mm pitch.

Table 3-82: GPIO 0-3, 10K PU Configuration Switch (SW72)

Position	Signal	Position	Signal
1 (off)	+V1P8S [**Default**]	8 (on)	PU_GPIO00 (10K)
2 (off)	+V1P8S [**Default**]	7 (on)	PU_GPIO01 (10K)
3 (off)	+V1P8S [**Default**]	6 (on)	PU_GPIO02 (10K)
4 (off)	+V1P8S [**Default**]	5 (on)	PU_GPIO03 (10K)

NOTE: The 2.2K PUs are placed at the user end, near CN167, and the 10K PUs are placed near the module. The level shift circuit is placed between the 2K and 10K PUs.

3.13.16 GPIO 4-7, 10K PU Configuration Switch (SW73)

Table 3-83 lists the pin signals of the GPIO 4-7, 10K PU configuration dip switch, which provides 4 poles, 8 pin positions with 1.27mm pitch.

Table 3-83: GPIO 4-7, 10K PU Configuration Switch (SW73)

Position	Signal	Position	Signal
1 (off)	+V1P8S [**Default**]	8 (on)	PU_GPIO04 (10K)
2 (off)	+V1P8S [**Default**]	7 (on)	PU_GPIO05 (10K)
3 (off)	+V1P8S [**Default**]	6 (on)	PU_GPIO06 (10K)
4 (off)	+V1P8S [**Default**]	5 (on)	PU_GPIO07 (10K)

NOTE: The 2.2K PUs are placed at the user end, near CN173, and the 10K PUs are placed near the module. The level shift circuit is placed between the 2K and 10K PUs.

3.13.17 GPIO 8-11, 10K PU Configuration Switch (SW74)

Table 3-84 lists the pin signals of the GPIO 8-11, 10K PU configuration dip switch, which provides 4 poles, 8 pin positions with 1.27mm pitch.

Table 3-84: GPIO 8-11, 10K PU Configuration Switch (SW74)

Position	Signal	Position	Signal
1 (off)	+V1P8S [**Default**]	8 (on)	PU_GPIO08 (10K)
2 (off)	+V1P8S [**Default**]	7 (on)	PU_GPIO09 (10K)
3 (off)	+V1P8S [**Default**]	6 (on)	PU_GPIO10 (10K)
4 (off)	+V1P8S [**Default**]	5 (on)	PU_GPIO11 (10K)

NOTE: The 2.2K PUs are placed at the user end, near CN179, and the 10K PUs are placed near the module. The level shift circuit is placed between the 2K and 10K PUs.

3.14 PCIe Interfaces

This section provides the signal definitions of the PCI Express interfaces on the carrier. Refer to PCIe Mini Card Slot section in Chapter 2 for information on the standard PCIe Mini Card interface.

3.14.1 PCIe A x1 (CN183)

Table 3-85 lists the signals for the PCIe A x1 connector, which provides 36 pins, two rows, consecutive pin sequence (1, 13) with 1.00mm pitch.

Table 3-85: PCIe A x1 (CN183)

Pin	Signal	Pin	Signal
B1	+V12P0_ATX	A1	GND
B2	+V12P0_ATX	A2	+V12P0_ATX
B3	+V12P0_ATX	A3	+V12P0_ATX
B4	GND	A4	GND
B5	SMB_PCIE_A_CLK	A5	Not Connected
B6	SMB_PCIE_A_DAT	A6	Not Connected
B7	GND	A7	Not Connected
B8	+3VP3S	A8	Not Connected
B9	Not Connected	A9	+3VP3S

Table 3-85: PCIe A x1 (Continued) (CN183) (Continued)

Pin	Signal	Pin	Signal
B10	+3VP3_SBY	A10	+3VP3S
B11	PCIE_WAKE_A#	A11	PCIE_A_RST#
B12	Not Connected	A12	GND
B13	GND	A13	REFCLK_A_P
B14	PCIE_A_TXC_P	A14	REFCLK_A_N
B15	PCIE_A_TXC_N	A15	GND
B16	GND	A16	PCIE_A_RX_P
B17	PCIE_PRSNT_A#	A17	PCIE_A_RX_N
B18	GND	A18	GND

NOTE: Shaded table cells denote power or ground. The # symbol indicates the signal is Active Low.

3.14.2 PCIe D x1 (CN186)

Table 3-86 lists the signals for the PCIe D x1 connector, which provides 36 pins, two rows, consecutive pin sequence (1, 13) with 1.00mm pitch.

Table 3-86: PCIe D x1 (CN186)

Pin	Signal	Pin	Signal
B1	+V12P0_ATX	A1	GND
B2	+V12P0_ATX	A2	+V12P0_ATX
B3	+V12P0_ATX	A3	+V12P0_ATX
B4	GND	A4	GND
B5	SMB_PCIE_D_CLK	A5	Not Connected
B6	SMB_PCIE_D_DAT	A6	Not Connected
B7	GND	A7	Not Connected
B8	+3VP3S	A8	Not Connected
B9	Not Connected	A9	+3VP3S
B10	+3VP3_SBY	A10	+3VP3S
B11	PCIE_WAKE_D#	A11	PCIE_D_RST#
B12	Not Connected	A12	GND
B13	GND	A13	REFCLK_D_P
B14	PCIE_D_TXC_P	A14	REFCLK_D_N
B15	PCIE_D_TXC_N	A15	GND
B16	GND	A16	PCIE_D_RX_P
B17	PCIE_PRSNT_D#	A17	PCIE_D_RX_N
B18	GND	A18	GND

NOTE: Shaded table cells denote power or ground. The # symbol indicates the signal is Active Low

3.14.3 Expansion Interface - mPCIe B (CN193)

Table 3-87 lists the pin signals of the mini PCIe B expansion interface, which provides 8 pins in two rows with odd/even pin sequence (1,2) and 2.00mm pitch.

Table 3-87: Expansion Interface - mPCIe B (CN193)

Pin #	Signal	Pin #	Signal
1	COEX_B1 (user defined)	2	GND
3	COEX_B2 (user defined)	4	GND
5	W_DISABLE_B1# (wireless disable)	6	GND
7	W_DISABLE_B2# (wireless disable)	8	GND

NOTE: Shaded table cells denote ground. The # symbol indicates the signal is Active Low.

3.14.4 Expansion Interface - mPCIe C (CN188)

Table 3-88 lists the pin signals of the mini PCIe C Expansion interface, which provides 8 pins in two rows with odd/even pin sequence (1,2) and 2.00mm pitch.

Table 3-88: Expansion Interface - mPCIe C (CN188)

Pin #	Signal	Pin #	Signal
1	COEX_C1 (user defined)	2	GND
3	COEX_C2 (user defined)	4	GND
5	W_DISABLE_C1# (wireless disable)	6	GND
7	W_DISABLE_C2# (wireless disable)	8	GND

NOTE: Shaded table cells denote ground. The # symbol indicates the signal is Active Low.

3.14.5 mPCIe B/C CLKREQ Enable (CN205)

Table 3-89 lists the pin signals of the mPCIe B/C CLKREQ enable jumper header, which provides 6 pins in two rows with odd/even pin sequence (1,2) and 2.00mm pitch.

Table 3-89: mPCIe B/C CLKREQ Enable (CN205)

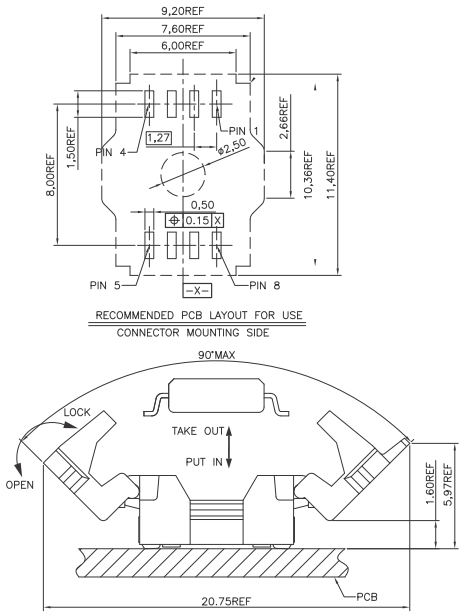
Pin #	Signal	Pin #	Signal	Jumper Positions
1	CLKREQ_B#	2	GND	• Jumper on 1-2 enables mPCIe B request for clock • Jumper on 5-6 enables mPCIe C request for clock • Jumpers on 1-3 and 4-6 disables manual clock request [**default**]
3	Not Connected	4	Not Connected	
5	CLKREQ_C#	6	GND	

3.14.6 PCIe Re-Driver Socket (U174)

Table 3-90 lists the pin signals of the PCIe Re-driver socket, which provides 8 pins in two rows with consecutive pin sequence (1,8) and 1.27mm pitch.

Table 3-90: PCIe Re-driver Socket (U174)

Pin #	Signal	Pin #	Signal
1	PCIE_RD_ROM_A0	8	+V3P3S
2	PCIE_RD_ROM_A1	7	PCIE_RD_ROM_WP
3	PCIE_RD_ROM_A2	6	RD_ROM_SCL
4	GND	5	IRD_ROM_SDA



NOTE: Shaded table cells denote power or ground. A 2Kb (256 x 8-bit) EEPROM is recommended.

3.15 Miscellaneous Interfaces

3.15.1 SMBus ClockBuffers 0-1 Connect (CN201)

Table 3-91 lists the pin signals of the SMBus ClockBuffers 0-1 connect jumper header, which provides 6 pins in two rows with odd/even pin sequence (1,2) and 2.00mm pitch.

Table 3-91: SMBus ClockBuffers 0-1 Connect (CN201)

Pin #	Signal	Pin #	Signal	Jumper Positions
1	SMBus_CB0_DAT	2	SMBus_CB0_CK	• Jumpers on 1-3 and 2-4 connects ClockBuffer 0 to the SMBus [**default**] • Jumpers on 3-5 and 4-6 connects ClockBuffer 1 to the SMBus
3	SMB_SYS_SDA	4	SMB_SYS_SCL	
5	SMBus_CB1_DAT	6	SMBus_CB1_CK	

NOTE: Only one of the two ClockBuffers (0 or 1) can be connected (at-a-time) to the SMBus.

3.15.2 Boot Select Switch (SW39)

Table 3-92 lists the pin signals of the Boot Select dip switch, which provides 4 poles, 8 pin positions with 1.27mm pitch. Refer to Table 3-93 for the Boot Select Switch configuration settings.

Table 3-92: Boot Select Switch (SW39)

Position	Signal	Position	Signal
1 (off)	PM.BOOT_SEL0# [**Default**]	8 (on)	GND
2 (off)	PM.BOOT_SEL1# [**Default**]	7 (on)	GND
3 (off)	PM.BOOT_SEL2# [**Default**]	6 (on)	GND
4 (off)	PM.FORCE_RECOV# [**Default**]	5 (on)	GND

NOTE: The # symbol indicates the signal is Active Low.

Table 3-93: Boot Select Switch SW39 Configuration Settings

BOOT Select (ON = GND OFF = FLOAT)	SEL2#	SEL1#	SEL0#	RECOV#
Carrier SATA	ON	ON	ON	OFF
Carrier SD Card	ON	ON	OFF	OFF
Carrier eSPI (CS0#)	ON	OFF	ON	OFF
Carrier SPI (CS0#)	ON	OFF	OFF	OFF
Module Device (NOR, NAND)	OFF	ON	ON	OFF
Remote Boot (GBE, Serial)	OFF	ON	OFF	OFF
Module eMMC Flash	OFF	OFF	ON	OFF
Module SPI [**Default**]	OFF	OFF	OFF	OFF
Recovery	OFF	OFF	OFF	ON

NOTE: The # symbol indicates the signal is Active Low. The blue shaded table cells indicate the “ON” switch position.

3.15.3 PLL Bandwidth Configuration Switch (SW66)

Table 3-94 lists the pin signals of the PLL Bandwidth configuration dip switch for PCIe Clock-Buffer components, providing 2 poles and 4 pin positions.

Table 3-94: PLL Bandwidth Configuration Switch (SW66)

Position	Signal	Position	Signal
1 (off)	PLL_BW_CB0 (3.3V High Bandwidth) [**Default**]	4 (on)	PLL_BWR_CB0 (0V Low Bandwidth)
2 (off)	PLL_BW_CB1 (3.3V High Bandwidth) [**Default**]	3 (on)	PLL_BWR_CB1 (0V Low Bandwidth)

NOTE: This switch configures the PLL Bandwidth of the PCI-Express Clock-Buffer components. The default setting is recommended (High). Both switches must be either OFF or ON at the same time.

Appendix A Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed in Table A-1 below. Requests for support through Ask an Expert are given the highest priorities, and usually will be addressed within one working day.

- ADLINK Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the ADLINK web site at to **http://askanexpert.adlinktech.com**. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.

ADLINK strongly suggests that you register with the web site. By creating a profile on the ADLINK web site, you will have a portal page called “My ADLINK”, unique to you with access to exclusive services and account information.

- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to the My Question area where you can check status, update your request, and access other features.
- Download Service – This service is also free and available 24 hours a day using the web site link shown in Table A-1. For certain downloads such as technical documents and software, you must register online before you can log in to this service.

Table A-1: Technical Support Contact Information

Method	Contact Information
Ask an Expert	**http://askanexpert.adlinktech.com**
Web Site	**https://emb.adlinktech.com**
Standard Mail	**ADLINK Technology, Inc.** Address: 9F, No.166 Jian Yi Road, Zhonghe District New Taipei City 235, Taiwan 新北市中和區建一路 166 號 9 樓 Tel: +886-2-8226-5877 Fax: +886-2-8226-5717 Email: service@adlinktech.com **Ampro ADLINK Technology, Inc.** Address: 5215 Hellyer Avenue, #110 San Jose, CA 95138, USA Tel: +1-408-360-0200 Toll Free: +1-800-966-5200 (USA only) Fax: +1-408-360-0222 Email: info@adlinktech.com **ADLINK Technology (China) Co., Ltd.** Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203) 300 Fang Chun Rd., Zhangjiang Hi-Tech Park Pudong New Area, Shanghai, 201203 China Tel: +86-21-5132-8988 Fax: +86-21-5132-3588 Email: market@adlinktech.com

Table A-1: Technical Support Contact Information (Continued)

Method	Contact Information
	ADLINK Technology GmbH Address: Hans-Thoma-Strasse 11 D-68163 Mannheim, Germany Tel: +49-621-43214-0 Fax: +49-621 43214-30 Email: emea@adlinktech.com Please visit the contact page using the web site link shown above for information on how to contact the ADLINK regional office nearest you.