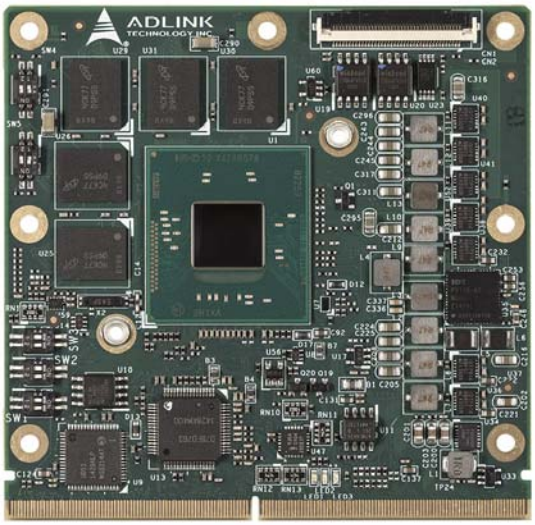
LEC-BT

(Low Energy Computer on Module)

Technical Reference

P/N 50-1Z166-1020

Rev 3.00



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Preface

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Revision History

Revision	Reason for Change	Date
1.00	Initial Release	Feb/16
2.00	Updated AFB signals in Table 3-2; removed PCAM signals from Table 3-2; added section 4 Utilities; updated block diagram	Feb/16
3.00	Added Electrical Specifications table to chapter 1 to define input voltage as a fixed 5V supply	Aug/16

ADLINK Technology, Incorporated
www.adlinktech.com

Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

Environmental Responsibility

ADLINK is committed to fulfill its social responsibility to global environmental preservation through compliance with the European Union's Restriction of Hazardous Substances (RoHS) directive and Waste Electrical and Electronic Equipment (WEEE) directive. Environmental protection is a top priority for ADLINK. We have enforced measures to ensure that our products, manufacturing processes, components, and raw materials have as little impact on the environment as possible. When products are at their end of life, our customers are encouraged to dispose of them in accordance with the product disposal and/or recovery programs prescribed by their nation or company.

Important Safety Instructions

For user safety, please read and follow all **Instructions**, **WARNINGs**, **CAUTIONs,** and **NOTEs** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

Table of Contents

1 Overview

This manual presents a general overview of the LEC-BT. After reviewing this document you should understand the following perspectives of the LEC-BT.

- Feature Overview
- Hardware Functions
- Interface Definitions
- Utility Definitions
- Contact Information

NOTE: Refer to http://www.sget.org/standards/smarc.html for SMARC specifications. Please refer to BSP readme documents in the Quick Drive for BSP installation instructions.

1.1 Block Diagram

Figure 1-1 represents the component functions of the module.

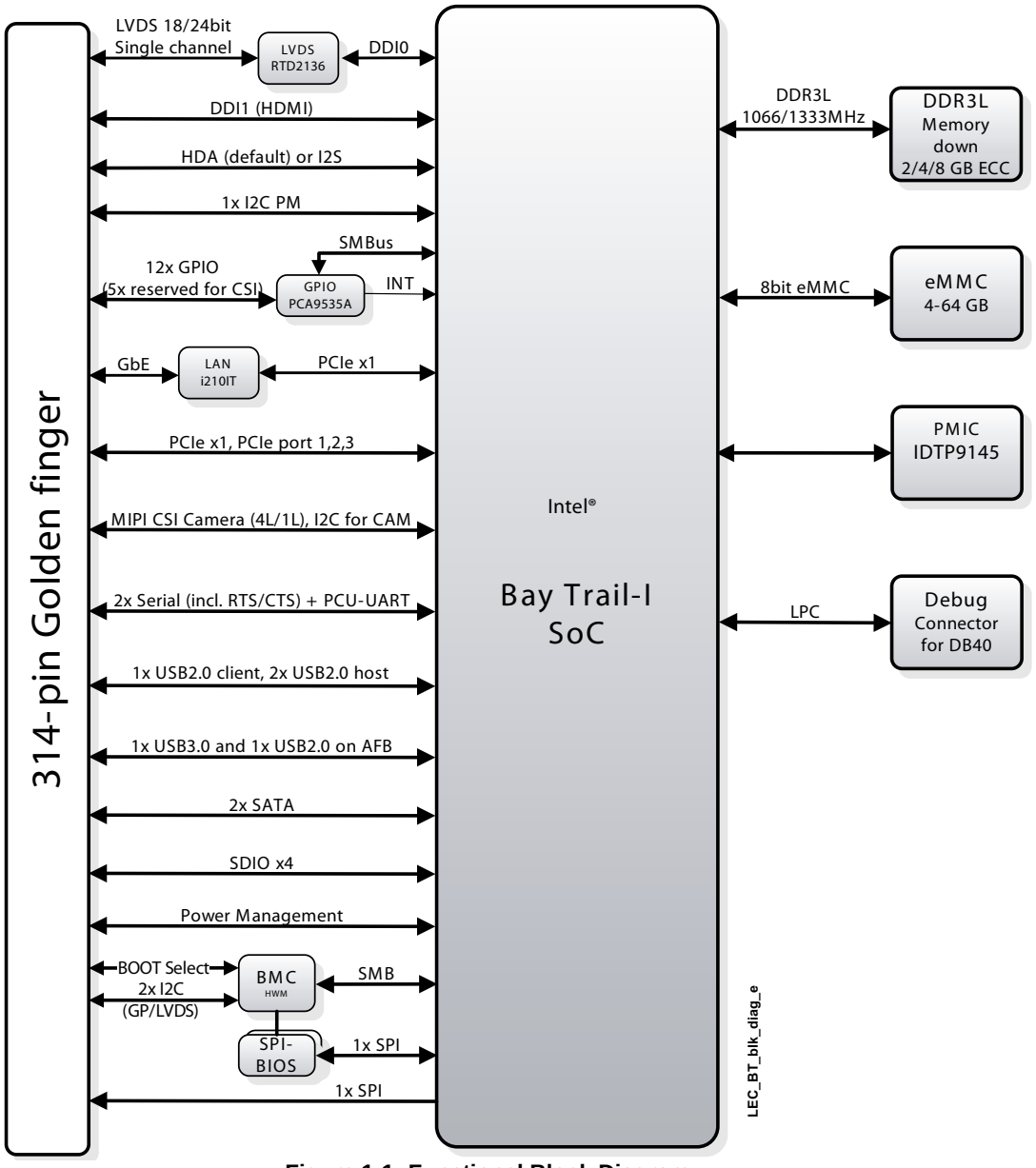


Figure 1-1: Functional Block Diagram

1.2 Major Components (ICs)

Table 1-1 lists the major integrated circuits on the LEC-BT, including a brief description of each IC. Figure 1-2 shows the locations of the major ICs.

Table 1-1: Major Integrated Circuit Descriptions and Functions

Chip Type	Mfg.	Model	Description	Function
CPU (U1)	Intel	• E3845 (quad core, 10W, 1.91GHz) • E3826 (dual core, 7W, 1.46GHz) • E3815 (single core, 5W, 1.46GHz) • E3805 (dual core, 3W, headless, 1.33GHz)	Atom, 22nm SoC (System on Chip) with Intel 64 architecture	Integrates Processor Core, Graphics and Memory Controller Hub, and I/O Hub
Ethernet Controller (U9)	Intel	WGI210IT SLIXT	Single-port Gigabit Ethernet controller	Integrates GbE MAC, PHY, and SGMII/SerDes to enable 10T/ 100TX/1000T Ethernet signals using the PCIe x1 bus
DDR3L SDRAM (U24, U25, U26, U27, U28, U29, U30 [ECC], U31, U32)	Micron Intelligent Memory	• MT41K256M8RH-125 (2GB model) • MT41K512M8RH-125 (4GB model) • IM8G08D3FBBG-15EI (8GB model)	On-board DDR3L, 1.35V • 2Gb, 32Mx8x8 • 4Gb, 64Mx8x8 • 8Gb, 128Mx8x8 System Memory	Provides high-speed data transfer
eMMC, NAND Flash (U48 - on bottom side)	Micron	MTFC8GLVEA-4M-IT	MultiMediaCard Controller and NAND Flash Memory up to 64GB	Provides communication and mass data storage capabilities

Key:
U1 - CPU
U9 - Ethernet Controller
U25 - DDR3L SDRAM
U26 - DDR3L SDRAM
U29 - DDR3L SDRAM
U30 - DDR3L SDRAM (ECC)
U31 - DDR3L SDRAM

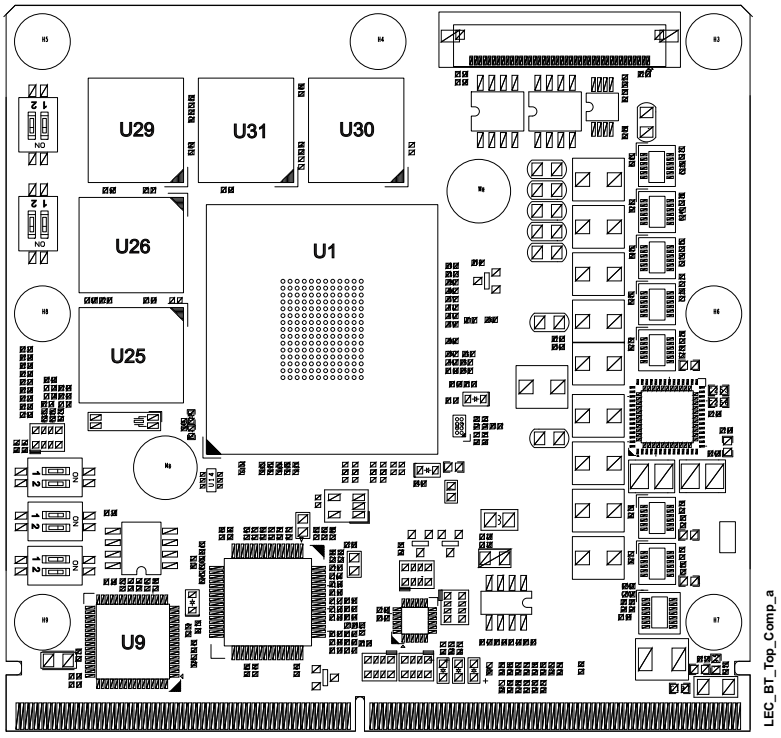


Figure 1-2: Component Locations (Top Side)

Key:
U24 - DDR3L SDRAM
U27 - DDR3L SDRAM
U28 - DDR3L SDRAM
U32 - DDR3L SDRAM
U48 - NAND Flash

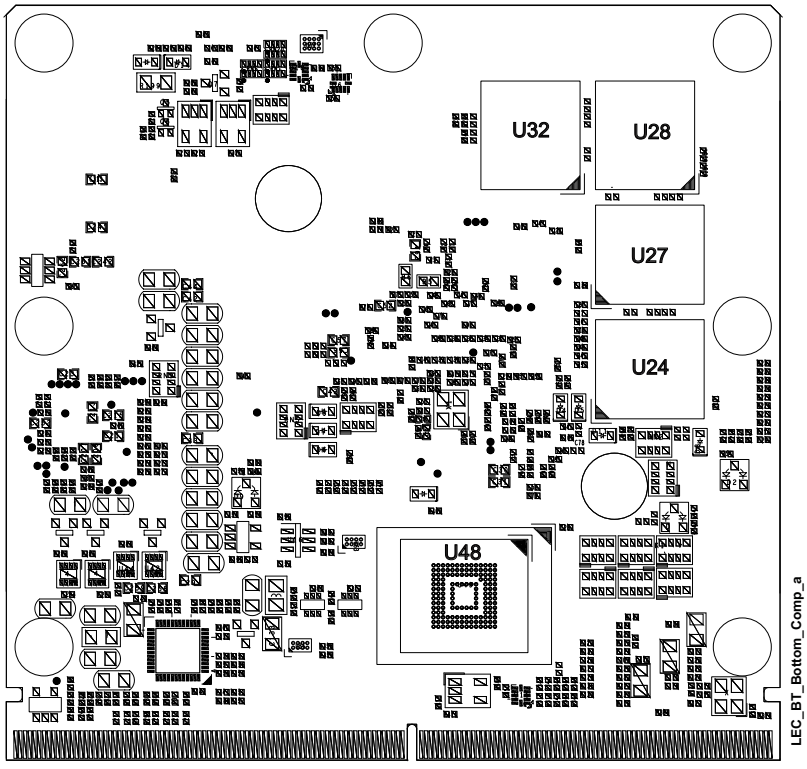


Figure 1-3: Component Locations (Bottom Side)

1.3 Connectors, Switches, and LEDs

Table 1-2 describes the connectors, switches, and LEDs shown in Figure 1-4.

Table 1-2: Module Connector Description

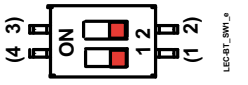
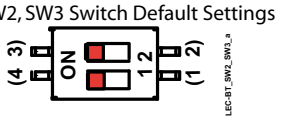
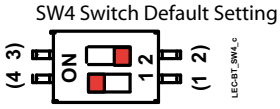
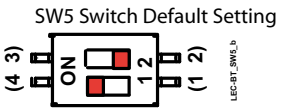
Connector#	Board Access	Description
GF1 – SMARC P-S	Top/ Bottom	314-pin, MXM edge connector for routing Camera, Graphics, and I/O signals from the module to the baseboard
CN1	Top	40-pin, DB40 connector for debug card
SW1, SW2, SW3 – 4-pin dip switches for enabling/ disabling CSI1 camera, 4L, Data 0-3 [default=ON/ON]	Top	**SW1-SW3 CSI1 Settings**: ▶ One-lane CSI1 configuration (CSI1-D0) - Set SW1, SW2, and SW3 to ON/ON ▶ Two-lane CSI1 configuration (CSI1-D0 and CSI1-D1) - Set SW1 to OFF/OFF and leave SW2 and SW3 ON/ON [factory default] ▶ Three-lane CSI1 configuration (CSI1-D0, CSI1-D1, and CSI1-D2) - Set SW1, SW2 to OFF/OFF and leave SW3 ON/ON ▶ Four-lane CSI1 configuration (CSI1-D0, CSI1-D1, CSI1-D2, and CSI1-D3) - Set SW1, SW2, and SW3 to OFF/OFF SW1 Switch Default Setting  SW2, SW3 Switch Default Settings 
SW4	Top	4-pin dip switch for: • Loading BIOS setup defaults at Boot Up (2=off [default], 3=on) • Selecting 18/24 bit LVDS modes (1=18bit [default], 4=24bit) SW4 Switch Default Setting 

Table 1-2: Module Connector Description (Continued)

SW5	Top	4-pin dip switch for: • BIOS_SELECT (1=BIOS2 [blue LED blinks fast], 4=BIOS1 [default]) • WDT Disable (2=off [BMC switches to BIOS2 when BIOS1 not detected-default], 3=on [disables BIOS Detection Watchdog]) 
LED1	Top	Blue LED indicating system status activities for HW Reset, SW Reset, Power Up, Power Down, Reset Button, Power Button, and Exception Blink Codes
LED2	Top	Green LED for Power On
LED3	Top	Red LED for Watchdog Activity

Key:
CN1 - DB40 Debug
GF1A - SMARC Interface 1A
GF1B - SMARC Interface 1B
LED1 - System Status (Blue)
LED2 - Power On (Green)
LED3 - Watchdog Activity (Red)
SW1 - CSI1_D1
SW2 - CSI1_D2
SW3 - CSI1_D3
SW4 - BIOS Defaults and LVDS 18/24 Bit Select
SW5 - BIOS 1-2 Select and Watchdog Disable

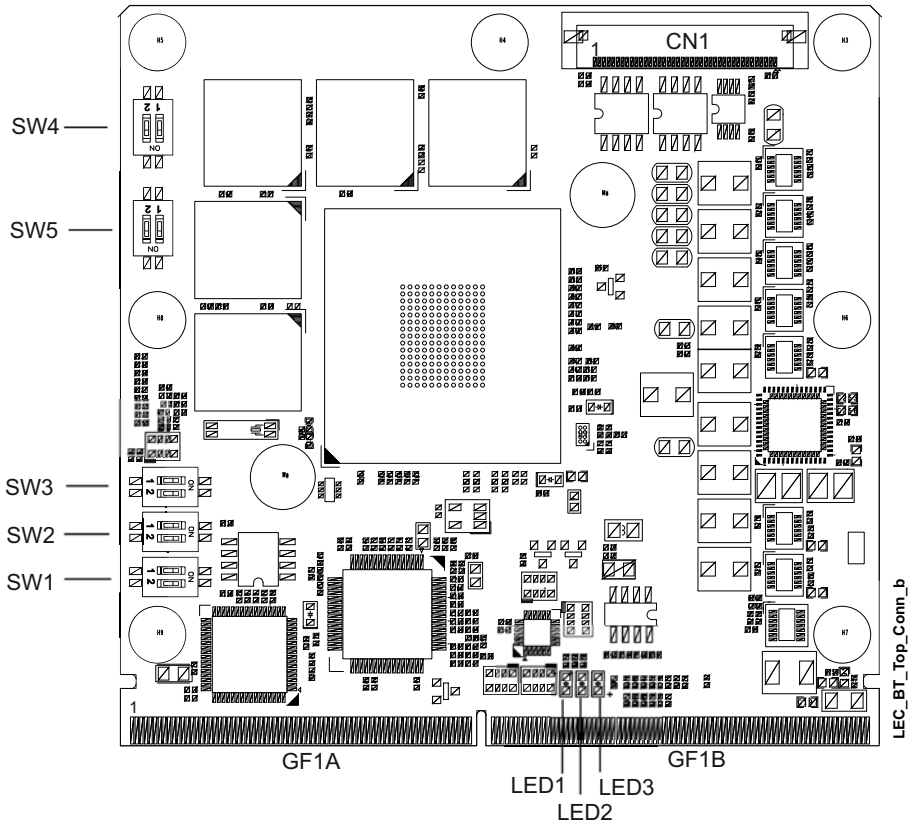


Figure 1-4: Connector Locations (Top Side)

1.4 Specifications

1.4.1 Physical Specifications

Table 1-3 lists the physical dimensions of the module.

Table 1-3: Weight and Footprint Dimensions

Item	Dimension	
Weight	0.02 kg (0.05 lb)	Overall height is measured from the upper board surface to the top of the highest permanent component (CN1 connector) on the upper board surface. This measurement does not include the cooling solution, which can vary. The cooling solution will probably increase this dimension.
Height (overall)	2.50 mm (0.098 inches)	
Board thickness	1.27 mm (0.05 inches)	
Width	80.00 mm (3.15 inches)	
Length	82.00 mm (3.23 inches)	

1.4.2 Mechanical Specifications

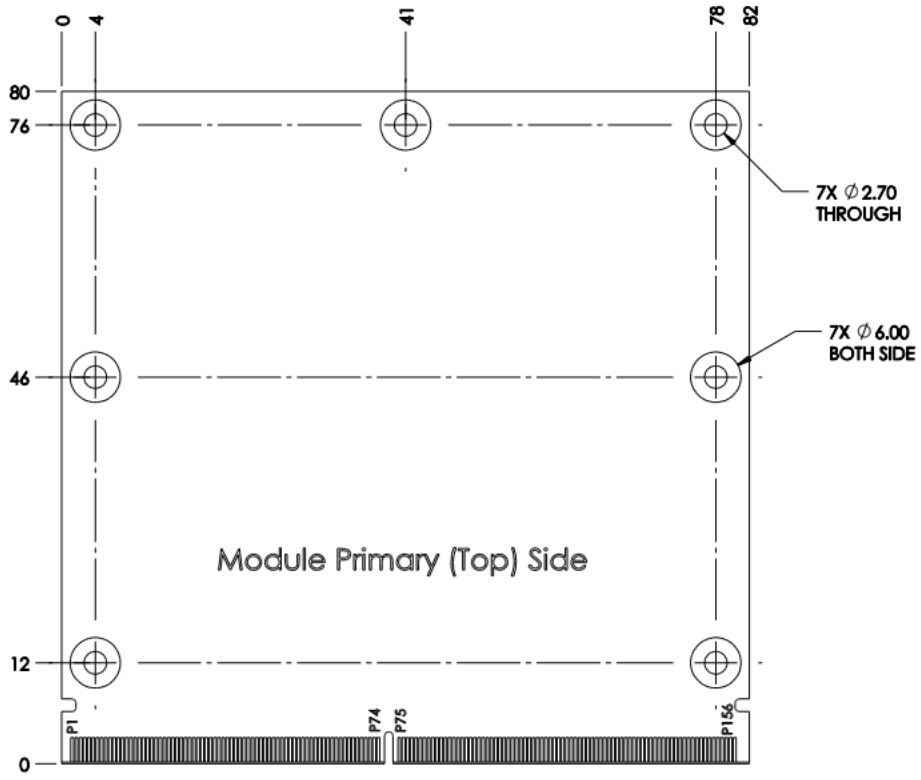


Figure 1-5: Mechanical Dimensions (Top Side)

NOTE: All dimensions are given in millimeters.

1.4.3 Electrical Specifications

Table 1-4 specifies the electrical characteristics of the module.

Table 1-4: Electrical Specifications

Parameter	Value
Voltage Input	
Standard	▶ Fixed 5-Volt Supply (+4.75V DC min to +5.25V DC max)
RTC	▶ 3.0V, 2.0V to 3.3V (battery)
Power States	▶ C1-C6 processor power states ▶ S0 (active), S4 (suspend-to-disk), S5 (soft-off and wake-on-LAN), and S5 ECO (wake on USB S3/ S4, WOL S3/S4/S5) system power states

1.4.4 Power Specifications

Table 1-5 provides the power requirements for this module.

Table 1-5: Power Supply Requirements

Parameter	E3815 (5W) Characteristics	E3826 (7W) Characteristics	E3845 (10W) Characteristics
Input Type	Regulated DC voltage	Regulated DC voltage	Regulated DC voltage
In-rush Voltage & Current	0.55A (2.75W) @ 5V	0.65A (3.25W) @ 5V	0.85A (4.25W) @ 5V
Typical Idle Voltage & Current	0.66A (3.30W) @ 5V	0.65A (3.25W) @ 5V	0.77A (3.85W) @ 5V
Intel TAT (Intel Thermal Analysis Tool) Voltage & Current	1.18A (5.90W) @ 5V	1.60A (8.00W) @ 5V	2.52A (12.60W) @ 5V

Operating configurations:

- ▶ In-rush operating configuration - Typical under Windows 8.1
- ▶ Idle operating configuration - Typical under Windows 8.1
- ▶ Intel TAT (Thermal Analysis Tool) operating configuration - Typical under Windows 8.1

1.4.5 Environmental Specifications

Table 1-6 provides the most efficient operating and storage condition ranges required for this module.

Table 1-6: Environmental Requirements

Parameter	Conditions
Temperature	
Standard	0° to +60° C (+32° to +140° F)
Extended	–40° to +85° C (–40° to +185° F)
Storage	–55° to +85° C (–67° to +185° F)
Humidity	
Operating	5% to 90% relative humidity, non-condensing
Non-operating	5% to 95% relative humidity, non-condensing

1.4.6 Thermal/Cooling Requirements

The LEC-BT is designed to operate at its maximum CPU speed and requires a thermal solution. ADLINK offers a heat spreader as one part of the cooling solution.

> CAUTION: The optional heat spreader plate requires another form of cooling, such as a fan. A heat spreader plate is not a complete thermal solution for the LEC-BT.
>
> The overall system design must keep the ICs within their operating temperature specifications.

2 Hardware

2.1 CPU

The LEC-BT product family offers multiple versions of the Intel Atom E3800 Series CPU (SoC): the E3805 (Dual Core, headless), the E3815 (Single Core), the E3826 (Dual Core), and the E3845 (Quad Core). E3800 CPUs feature the Intel 64 Architecture and are manufactured based on Intel's 22-nanometer technology. Refer to the CPU data sheet at:

http://www.intel.com/content/dam/www/public/us/en/documents/datasheets/atom-e3800-family-datasheet.pdf

2.2 Memory

The LEC-BT employs one channel of 64-bit DDR3L on-board memory. Nine SDRAM memory chips provide up to 8GB of low voltage non-ECC (and ECC in one of the nine chips), unbuffered system memory. Refer to the SDRAM data sheet at:
http://www.micron.com/parts/dram/ddr3-sdram/mt41k512m8rh-125

2.3 eMMC NAND Flash

The Intel E3800 SoC supports one single, 8-bit eMMC interface, which can used to support the onboard eMMC NAND flash device. If the onboard eMMC NAND flash device is being supported, the eMMC pins on the MXM SMARC connector are not supported.

A custom configuration can be provided if the eMMC flash device will not be used. In this case the eMMC signals will be routed to the SDMMC SMARC pins, available for use by the baseboard.

The module supports NAND chips with capacities from 4GB to 64GB. The default capacity is 8GB. Refer to the NAND Flash data sheet at:
http://www.micron.com/parts/nand-flash/managed-nand/mtfc8glvea-4m-it

and the SMARC specification at:
http://www.sget.org/standards/smarc.html

3 Interfaces

This section provides descriptions of the interfaces and signals within the SMARC P-S (Primary-Secondary) connector. Refer to the SMARC specification at: http://www.sget.org/standards/smarc.html for definitions of the SMARC interfaces. The SMARC P-S (Primary-Secondary) connector provides the following interfaces:

- LVDS
- HDMI
- Camera CSIO
- Audio
- PCIe
- Gb Ethernet
- USB 2.0
- USB 3.0
- SATA
- I2C
- SPI
- Serial
- I2S
- SD/SDIO
- eMMC
- GPIO
- AFB
- Debug

NOTE: ADLINK Technology Inc. only supports the features/options tested and listed in this manual. The main chips used in the LEC-BT may provide more features or options than are listed for the LEC-BT, but some of these features or options are not supported on the module and will not function as specified in the chip documentation.

3.1 18/24 Bit LVDS LCD

The LVDS interface is connected to the DDI0 interface of the SoC, while the translation is made by a DisplayPort™-to-LVDS converter. (Refer to the Realtek RTD2136R-CG, DisplayPort-to-LVDS converter data sheet.)

NOTE: Backlight Enable, Display Enable, and PWMOUT are controlled from the BIOS setup.

3.2 HDMI (High-Definition Multimedia Interface)

The default setup defines the DDI1 port as HDMI and provides the following signals:

- 1 Clock pair
- 3 Data pairs
- Service signals

The HDMI interface is compliant with the HDMI 1.4 specification.

3.3 Camera (CSI)

The LEC-BT brings out two ports from the SoC for an MIPI-CSI 2.0 (serial) camera interface. Port 1 receives input through the CSI0 pins on the SMARC connector, supporting one clock lane and one data lane. Port 2 receives input through the CSI1 pins on the SMARC connector, supporting one clock lane and four data lanes. Each lane operates at up to 1GT/s and supports approximately 800 Mbit/s of actual pixels.

3.4 Audio (HDA)

The SoC provides an HDA controller, which communicates with internal or external CODECs over the Intel HDA serial link. HDA signals are brought out through the I2S2 pins on the SMARC connector and are multiplexed with LPE_I2S audio signals. When HDA is active, LPE audio is disabled.

3.5 PCI Express (PCIe)

The CPU features four PCIe x1 ports, and the LEC-BT module uses three of them for the PCIe interface and one of them for the Gigabit Ethernet interface. The PCIe interface supports the PCIe Base Specification 2.0 with a maximum signal rate of 5 GT/s and can be configured to support PCIe edge cards or Express Cards.

3.6 Gigabit Ethernet

The on-board Intel I210IT Ethernet controller uses PCIe x1 (v2.1) bus signals from the CPU to enable 10T/100TX/1000T operation through integrated MAC, PHY, and SGMII/SerDes interfaces.

3.7 USB Ports

The USB interface originates from two host controllers on the SoC that provide four USB 2.0 ports and one USB 3.0 port.

3.7.1 USB2.0

Three of the four USB 2.0 ports use the USB 0-2 pins on the SMARC connector (0 = client; 1 = host; 2 = host.) The fourth USB 2.0 port is routed through the AFB-DIFF2 pins on the SMARC connector, which map to the USB_DP/N [0] pins on the SoC.

3.7.2 USB 3.0

The USB 3.0 port uses the AFB_DIFF 0-1 pins on the SMARC connector, which map to the USB3_TX/RX pins on the SoC. See Table 3-3.

3.8 SATA

The SATA interface provides two ports, one through the SATA0 pins (P48, P49, P51, and P52) and one through the SATA1, AFB pins (S71, S72, S74, and S75) on the SMARC connector. The interface supports 1.5Gb/s and 3.0Gb/s.

3.9 I2C Bus

The LEC-BT provides four interfaces through the I2C bus for General Purpose, Power Management, Camera, and LCD video I2C signals with operating speeds up to 400kHz. All I2C interfaces have 1.8V pull ups with 2.2k resistors.

Table 3-1: I2C Signal Map

SMARC Connector I2C Pins	Map To:
S5 / S7	SOC: SIO_I2C1
S48 / S49	BMC: I2C_GP
P105 / P106	SoC: DDI1_DDC (HDMI)
P121 / P122	SoC: SMB (DATA / CLK)
S139 / S140	BMC or RTD2136 LVDS_DID

3.10 SPI

The LEC-BT implements the SPI1 controller from the SoC (the SPI0 controller is not connected). The SPI1 controller connects to the SMARC connector at pins P54, P56, P57, and P58 (pin P55 is not connected), which support two SPI Flash devices on the module for BIOS storage. Consequently, the SPI0 pins P43, P44, P45, P46 on the SMARC connector are not connected.

3.11 Serial (UART)

The LEC-BT provides three serial interfaces: Two ports are high-speed, 4-wire ports (with TX/RX and RTS#/CTS#), and one port is 2-wire (with TX/RX only.)

3.12 I2S (Audio)

The LEC-BT supports an I2S audio interface as an alternate configuration to the default HD Audio interface. The I2S signals are supported through the I2S0 pins on the SMARC connector, and a programmable voltage regulator is used to switch between the I2S (1V8) and HDA (1V5). The default is HDA, and the change to I2S mode is be made through the LPE Audio BIOS setting. The I2S1 pins are not connected.

3.13 SD/SDIO Interface

Four parallel data lines comprise the SD/SDIO interface, supporting SD Card sockets.

3.14 eMMC Interface

The LEC-BT provides one 8-bit eMMC interface port, brought out from the SoC through the SDMMC pins on the SMARC connector. If the eMMC NAND chip on the module is being used, the SDMMC pins will not be available for the baseboard.

3.15 GPIO

The LEC-BT provides 12 GPIO signals from the PCA9535A GPIO expander on the module. The GPIO signals can be utilized for General Purpose IOs as well as camera reset, camera power, and HDA reset.

Table 3-1: GPIO Default Settings

SMARC Connector Pin	Default Function
GPIO0	CAM0_PWR#
GPIO1	CAM1_PWR#
GPIO2	CAM0_RST#
GPIO3	CAM1_RST#
GPIO4	HDA_RST#
GPIO5	GPIO
GPIO6	GPIO
GPIO7	GPIO
GPIO8	GPIO
GPIO9	GPIO
GPIO10	GPIO
GPIO11	GPIO

3.16 AFB (Alternate Function Block)

The module supports certain AFB pins that are dedicated for specific functions. Table 3-2 provides the map from the AFB signal on the module to its designated function signal on the SoC.

Table 3-2:AFB Pin Map to SoC

Pin	AFB Signal	SoC Signal
S17	AFB0_OUT	Intel SoC_PMC_SLP_S3#
S18	AFB1_OUT	Intel SoC_PMC_SLP_S4#
S19	AFB2_OUT	Intel SoC_PMC_SUS_STAT#
S20	AFB3_IN	Not connected
S21	AFB4_IN	Not connected
S22	AFB5_IN	Not connected
S23	AFB6_PTIO	EN_OC# for USB SS on AFB
S24	AFB7_PTIO	PCU_SMB_ALERT#
S55	AFB8_PTIO	Not connected
S56	AFB9_PTIO	Not connected
S62	AFB_DIFF0+	USB3.0_TX+
S63	AFB_DIFF0-	USB3.0_TX-
S65	AFB_DIFF1+	USB3.0_RX+
S66	AFB_DIFF1-	USB3.0_RX-
S68	AFB_DIFF2+	USB_DP [0]
S69	AFB_DIFF2-	USB_DN [0]
S71	AFB_DIFF3+	SATA_TXP [1]
S72	AFB_DIFF3-	SATA_TXN [1]
S74	AFB_DIFF4+	SATA_RXP [1]
S75	AFB_DIFF4-	SATA_RXN [1]

3.17 LPC Debug

A 40-pin, front flip, DB40 connector allows access to debug and update the BIOS, BMC, and OS code on the module. (Refer to “Debug (DB40)” on page 21.)

3.18 SMARC Interface Signals

Table 3-3 provides the pin signals for the SMARC P-S connector. Refer to the SMARC specification at http://www.sget.org/standards/smarc.html for definitions of the SMARC signals.

Table 3-3: SMARC P-S Connector (GF1) Signal Descriptions

Pin #	Primary (Top Side)	Pin #	Secondary (Bottom Side)
		S1	Not connected
P1	Not connected	S2	Not connected
P2	GND	S3	GND
P3	CSI1_CK+ (CSI1 differential clock inputs.)	S4	Not connected
P4	CSI1_CK- (CSI1 differential clock inputs.)	S5	I2C_CAM_CK (Serial / Parallel camera support link - I2C clock)
P5	Not connected	S6	Not connected
P6	Not connected	S7	I2C_CAM_DAT (Serial / Parallel camera support link - I2C data)
P7	CSI1_D0+ (CSI1 differential data inputs.)	S8	CSI0_CK+ (CSI0 differential clock inputs.)
P8	CSI1_D0- (CSI1 differential data inputs.)	S9	CSI0_CK- (CSI0 differential clock inputs.)
P9	GND	S10	GND
P10	CSI1_D1+ (CSI1 differential data inputs.)	S11	CSI0_D0+ (CSI0 differential data inputs.)
P11	CSI1_D1- (CSI1 differential data inputs.)	S12	CSI0_D0- (CSI0 differential data inputs.)
P12	GND	S13	GND
P13	CSI1_D2+ (CSI1 differential data inputs.)	S14	Not connected
P14	CSI1_D2- (CSI1 differential data inputs.)	S15	Not connected
P15	GND	S16	GND
P16	CSI1_D3+ (CSI1 differential data inputs.)	S17	AFB0_OUT (General purpose AFB output; maps to PMC_SLP_S3# on the SOC)
P17	CSI1_D3- (CSI1 differential data inputs.)	S18	AFB1_OUT (General purpose AFB output; maps to PMC_SLP_S4# on the SOC)
P18	GND	S19	AFB2_OUT (General purpose AFB output; maps to PMC_SUS_STAT# on the SOC)
P19	GBE_MDI3- (Bi-directional transmit/ receive pair 3 to magnetics [Media Dependent Interface])	S20	Not connected
P20	GBE_MDI3+(Bi-directional transmit/ receive pair 3 to magnetics [Media Dependent Interface])	S21	Not connected
P21	GBE_LINK100# (Link Speed Indication LED for 100Mbps; able to sink 24mA or more carrier LED current)	S22	Not connected
P22	GBE_LINK1000# (Link Speed Indication LED for 1000Mbps; able to sink 24mA or more carrier LED current)	S23	AFB6_PTIO (EN_OC# for USB SS)
P23	GBE_MDI2- (Bi-directional transmit/ receive pair 2 to magnetics [Media Dependent Interface])	S24	AFB7_PTIO (PCU_SMB_ALERT#)
P24	GBE_MDI2+ (Bi-directional transmit/ receive pair 2 to magnetics [Media Dependent Interface])	S25	GND

Table 3-3: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

P25	GBE_LINK_ACT# (Link / Activity Indication LED Driven low on Link [10, 100 or 1000 mbps] Blinks on Activity; able to sink 24mA or more Carrier LED current)	S26	SDMMC_D0 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P26	GBE_MDI1- (Bi-directional transmit/ receive pair 1 to magnetics [Media Dependent Interface])	S27	SDMMC_D1 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P27	GBE_MDI1+ (Bi-directional transmit/ receive pair 1 to magnetics [Media Dependent Interface])	S28	SDMMC_D2 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P28	GBE_CTREF(Center-Tap reference voltage for GBE0 Carrier board Ethernet magnetic [if required by the Module GBE PHY])	S29	SDMMC_D3 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P29	GBE0_MDI0- (Bi-directional transmit/ receive pair 0 to magnetics [Media Dependent Interface])	S30	SDMMC_D4 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P30	GBE0_MDI0+ (Bi-directional transmit/ receive pair 0 to magnetics [Media Dependent Interface])	S31	SDMMC_D5 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P31	Not connected	S32	SDMMC_D6 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P32	GND	S33	SDMMC_D7 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P33	SDIO_WP (SDIO card Write Protect; 10K pull-up to 3.3V)	S34	GND
P34	SDIO_CMD (SDIO card Command line)	S35	SDMMC_CK (clock)
P35	SDIO_CD# (SDIO Card Detect; 10K pull-up to 3.3V)	S36	SDMMC_CMD (command line)
P36	SDIO_CK (SDIO card Clock)	S37	SDMMC_RST# (Reset signal to eMMC device)
P37	SDIO_PWR_EN (SDIO card Power Enable)	S38	Not connected
P38	GND	S39	I2S0_LRCK (Left & Right audio synchronization clock)
P39	SDIO_D0 (SDIO card 4-bit data path)	S40	I2S0_SDOUT (Digital audio output)
P40	SDIO_D1 (SDIO card 4-bit data path)	S41	I2S0_SDIN (Digital audio input)
P41	SDIO_D2 (SDIO card 4-bit data path)	S42	I2S0_CK (Digital audio clock)
P42	SDIO_D3 (SDIO card 4-bit data path)	S43	Not connected
P43	Not connected	S44	Not connected
P44	Not connected	S45	Not connected
P45	Not connected	S46	Not connected
P46	Not connected	S47	GND
P47	GND	S48	I2C_GP_CK (I2C General Purpose clock signal)
P48	SATA0_TX+ (Differential SATA 0 transmit data Pair; 0.1 uF 0402 capacitor on module)	S49	I2C_GP_DAT I2C (General Purpose data signal)

Table 3-3: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

P49	SATA0_TX- (Differential SATA 0 transmit data Pair; 0.1 uF 0402 capacitor on module)	S50	I2S2_LRCK (Left & Right audio synchronization clock)
P50	GND	S51	I2S2_SDOUT (Digital audio output)
P51	SATA0_RX+ (Differential SATA 0 receive data Pair; 0.1 uF 0402 capacitor on module)	S52	I2S2_SDIN (Digital audio input)
P52	SATA0_RX- (Differential SATA 0 receive data Pair; 0.1 uF 0402 capacitor on module)	S53	I2S2_CK (Digital audio clock)
P53	GND	S54	SATA_ACT# (Active low SATA activity indicator If implemented, able to sink 24mA or more Carrier LED current)
P54	SPI1_CS0# (SPI1 Master Chip Select 0 output)	S55	Not connected
P55	Not connected	S56	Not connected
P56	SPI1_CK (SPI1 Master Clock output)	S57	Not connected
P57	SPI1_DIN (SPI1 Master Data input [input to CPU, output from SPI device])	S58	Not connected
P58	SPI1_DO (SPI1 Master Data output [output from CPU, input to SPI device])	S59	Not connected
P59	GND	S60	Not connected
P60	USB0+ (Differential USB0 data pair)	S61	GND
P61	USB0- (Differential USB0 data pair)	S62	AFB_DIFF0+ (maps to USB3_TX_P on the SOC)
P62	USB0_EN_OC# (Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up is present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.12.4 of *SMARC Specification.*)	S63	AFB_DIFF0- (maps to USB3_TX_N on the SOC)
P63	Not connected	S64	GND
P64	Not connected	S65	AFB_DIFF1+ (maps to USB3_RX_P on the SOC)
P65	USB1+ (Differential USB1 data pair)	S66	AFB_DIFF1- (maps to USB3_RX_N on the SOC)
P66	USB1- (Differential USB1 data pair)	S67	GND
P67	USB1_EN_OC# (Pulled low by Module OD driver to disable USB1 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up is present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.12.4 of *SMARC Specification.*)	S68	AFB_DIFF2+ (maps to USB_D0_P on the SOC)
P68	GND	S69	AFB_DIFF2- (maps to USB_D0_N on the SOC)
P69	USB2+ (Differential USB2 data pair)	S70	GND
P70	USB2- (Differential USB2 data pair)	S71	AFB_DIFF3+ (maps to SATA_TX1_P on the SOC)

Table 3-3: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

P71	USB2_EN_OC# (Pulled low by Module OD driver to disable USB2 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up ***shall*** be present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.12.4 of *SMARC Specification*.)	S72	AFB_DIFF3- (maps to SATA_TX1_N on the SOC)
P72	PCIE_C_PRSNT# (PCIe Port C present input. Pulled up or terminated on Module)	S73	GND
P73	PCIE_B_PRSNT# (PCIe Port B present input. Pulled up or terminated on Module)	S74	AFB_DIFF4+ (maps to SATA_RX1_P on the SOC)
P74	PCIE_A_PRSNT# (PCIe Port A present input. Pulled up or terminated on Module)	S75	AFB_DIFF4- (maps to SATA_RX1_N on the SOC)
	Key		Key
P75	PCIE_A_RST# (PCIe Port A reset output)	S76	PCIE_B_RST# (PCIe Port B reset output, active low)
P76	PCIE_C_CKREQ# (PCIe Port C clock request input. Pulled up or terminated on Module)	S77	PCIE_C_RST# (PCIe Port A reset output, active low)
P77	PCIE_B_CKREQ# (PCIe Port B clock request input. Pulled up or terminated on Module)	S78	PCIE_C_RX+ (Differential PCIe Link C receive data pair 0. No coupling caps on Module)
P78	PCIE_A_CKREQ# (PCIe Port A clock request input. Pulled up or terminated on Module)	S79	PCIE_C_RX- (Differential PCIe Link C receive data pair 0. No coupling caps on Module)
P79	GND	S80	GND
P80	PCIE_C_REFCK+ (Differential PCIe Link C reference clock output. DC coupled)	S81	PCIE_C_TX+ (Differential PCIe Link C transmit data pair 0. Series coupling caps are on the Module. Caps are 0402 package 0.1uF)
P81	PCIE_C_REFCK- (Differential PCIe Link C reference clock output. DC coupled)	S82	PCIE_C_TX- (Differential PCIe Link C transmit data pair 0. Series coupling caps are on the Module. Caps are 0402 package 0.1uF)
P82	GND	S83	GND
P83	PCIE_A_REFCK+ (Differential PCIe Link A reference clock output. DC coupled)	S84	PCIE_B_REFCK+ (Differential PCIe Link B reference clock output; DC coupled)
P84	PCIE_A_REFCK- (Differential PCIe Link A reference clock output. DC coupled)	S85	PCIE_B_REFCK- (Differential PCIe Link B reference clock output; DC coupled)
P85	GND	S86	GND
P86	PCIE_A_RX+ (Differential PCIe Link A receive data pair 0. No coupling caps on Module)	S87	PCIE_B_RX+ (Differential PCIe Link B receive data pair 0. No coupling caps on Module)
P87	PCIE_A_RX- (Differential PCIe Link A receive data pair 0. No coupling caps on Module)	S88	PCIE_B_RX- (Differential PCIe Link B receive data pair 0. No coupling caps on Module)
P88	GND	S89	GND
P89	PCIE_A_TX+ (Differential PCIe Link A transmit data pair 0. Series coupling capacitors are on the Module. 0.1 uF 0402 capacitor are on module)	S90	PCIE_B_TX+ (Differential PCIe Link B transmit data pair 0. Series coupling caps are on the Module Caps are 0402 package 0.1uF)

Table 3-3: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

P90	PCIE_A_TX- (Differential PCIe Link A transmit data pair 0. Series coupling capacitors are on the Module. 0.1 uF 0402 capacitor are on module)	P91	PCIE_B_TX- (Differential PCIe Link B transmit data pair 0. Series coupling caps are on the Module Caps are 0402 package 0.1uF)
P91	GND	S92	GND
P92	HDMI_D2+ (TMDS / HDMI data 2 differential pair)	S93	Not connected
P93	HDMI_D2- (TMDS / HDMI data 2 differential pair)	S94	Not connected
P94	GND	S95	Not connected
P95	HDMI_D1+ (TMDS / HDMI data 1 differential pair)	S96	Not connected
P96	HDMI_D1- (TMDS / HDMI data 1 differential pair)	S97	Not connected
P97	GND	S98	Not connected
P98	HDMI_D0+ (TMDS / HDMI data 0 differential pair)	S99	Not connected
P99	HDMI_D0- (TMDS / HDMI data 0 differential pair)	S100	Not connected
P100	GND	S101	GND
P101	HDMI_CK+ (TMDS / HDMI clock output differential pair)	S102	Not connected
P102	HDMI_CK- (TMDS / HDMI clock output differential pair)	S103	Not connected
P103	GND	S104	Not connected
P104	HDMI_HPD (HDMI Hot Plug Detect input)	S105	Not connected
P105	HDMI_CTRL_CK (I2C clock line dedicated to HDMI)	S106	Not connected
P106	HDMI_CTRL_DAT (I2C data line dedicated to HDMI)	S107	Not connected
P107	HDMI_CEC (HDMI Consumer Electronics Control, 1 – wire peripheral control interface)	S108	Not connected
P108	GPIO0 / CAM0_PWR# [default] (Camera 0 Power Enable, active low output)	S109	Not connected
P109	GPIO1 / CAM1_PWR# [default] (Camera 1 Power Enable, active low output)	S110	GND
P110	GPIO2 / CAM0_RST# [default] (Camera 0 Reset, active low output)	S111	Not connected
P111	GPIO3 / CAM1_RST# [default] (Camera 1 Reset, active low output)	S112	Not connected
P112	GPIO4 / HDA_RST# [default] (HD Audio Reset, active low output)	S113	Not connected
P113	GPIO5 (General Purpose IO)	S114	Not connected
P114	GPIO6 (General Purpose IO)	S115	Not connected
P115	GPIO7 (General Purpose IO)	S116	Not connected
P116	GPIO8 (General Purpose IO)	S117	Not connected
P117	GPIO9 (General Purpose IO)	S118	Not connected
P118	GPIO10 (General Purpose IO)	S119	GND
P119	GPIO11 (General Purpose IO)	S120	Not connected
P120	GND	P121	Not connected

Table 3-3: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

P121	I2C_PM_CK (Power management I2C bus clock)	S122	Not connected
P122	I2C_PM_DAT(Power management I2C bus data)	S123	Not connected
P123	BOOT_SEL0# (Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier.)	S124	GND
P124	BOOT_SEL1# (Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier.)	S125	LVDS0+ (LVDS LCD data channel differential pair)
P125	BOOT_SEL2# (Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier.)	S126	LVDS0- (LVDS LCD data channel differential pair)
P126	RESET_OUT# (General purpose reset output to Carrier board.)	S127	LCD_BKLT_EN (High enables panel backlight)
P127	RESET_IN# (Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise. Pulled up on Module. Driven by OD part on Carrier.)	S128	LVDS1+ (LVDS LCD data channel differential pair)
P128	POWER_BTN# (Power-button input from Carrier board. Carrier to float the line in inactive state. Active low, level sensitive. De-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.)	S129	LVDS1- (LVDS LCD data channel differential pair)
P129	SER0_TX (Asynchronous serial port data out)	S130	GND
P130	SER0_RX (Asynchronous serial port data in)	S131	LVDS2+ (LVDS LCD data channel differential pair)
P131	SER0_RTS# (Request to Send handshake line for SER0)	S132	LVDS2- (LVDS LCD data channel differential pair)
P132	SER0_CTS# (Clear to Send handshake line for SER0)	S133	LCD_VDD_EN (High enables panel VDD)
P133	GND	S134	LVDS_CK+ (LVDS LCD differential clock pair)
P134	SER1_TX (Asynchronous serial port data out)	S135	LVDS_CK- (LVDS LCD differential clock pair)
P135	SER1_RX (Asynchronous serial port data in)	S136	GND
P136	SER2_TX (Asynchronous serial port data out)	S137	LVDS3+ (LVDS LCD data channel differential pair)
P137	SER2_RX (Asynchronous serial port data in)	S138	LVDS3- (LVDS LCD data channel differential pair)
P138	SER2_RTS# (Request to Send handshake line for SER2)	S139	I2C_LCD_CK (I2C clock – to read LCD display EDID EEPROMs)
P139	SER2_CTS# (Clear to Send handshake line for SER2)	S140	I2C_LCD_DAT (I2C data – to read LCD display EDID EEPROMs)
P140	Not connected	S141	LCD_BKLT_PWM (Display backlight PWM control)
P141	Not connected	S142	Not connected
P142	GND	S143	GND
P143	Not connected	S144	RSVD / EDP_HPD (Reserved for future eDP Hot Plug Detect pin)

Table 3-3: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

P144	Not connected	S145	WDT_TIME_OUT# (Watchdog Timer Output)
P145	Not connected	S146	PCIE_WAKE (PCIe wake up interrupt to host – common to PCIe; links A, B, C – pulled up or terminated on Module)
P146	Not connected	S147	VDD_RTC (Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based Lithium cell or Super Cap. See ***Section 7.3 RTC Voltage Rail*** of the SMARC specification for an important safety note on the implementation of lithium backup batteries.)
P147	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S148	LID# (Lid open/close indication to Module. Low indicates lid closure, which system ***may*** use to initiate a sleep state. Carrier to float the line in inactive state. Active low, level sensitive. De-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.)
P148	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S149	SLEEP# (Sleep indicator from Carrier board; sourced from user Sleep button or Carrier logic. Carrier to float the line in inactive state. Active low, level sensitive; de-bounced on the Module. Pulled up on Module. Driven by OD part on Carrier.)
P149	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S150	VIN_PWR_BAD# (Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) ***is not*** enabled while this signal is held low by the Carrier. Pulled up on Module. Driven by OD part on Carrier.)
P150	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S151	CHARGING# (Held low by Carrier during battery charging. Carrier to float the line when charge is complete. Pulled up on Module. Driven by OD part on Carrier.)
P151	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S152	CHARGER_PRSNT# (Held low by Carrier if DC input for battery charger is present. Pulled up on Module. Driven by OD part on Carrier.)
P152	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S153	CARRIER_STBY# (The Module drives this signal low when the system is in a standby power state)
P153	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S154	CARRIER_PWR_ON (Carrier board circuits [apart from power management and power path circuits] ***are*** powered up until the Module asserts the CARRIER_PWR_ON signal)

Table 3-3: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

P154	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S155	FORCE_RECOV# (Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when the Force Recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based Force Recovery function, then a low on the Module FORCE_RECOV# pin ***may*** invoke the SOC native Force Recovery mode – such as over a Serial Port. Pulled up on Module. Driven by OD part on Carrier.)
P155	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S156	BATLOW# (Battery low indication to Module. Carrier to float the line in inactive state. Pulled up on Module. Driven by OD part on Carrier.)
P156	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S157	TEST# (Held low by Carrier to invoke Module vendor specific test function(s). Pulled up on Module. Driven by OD part on Carrier.)
		S158	GND

3.19 Debug (DB40)

Table 3-4 lists the pin signals of the CN1 connector, which provides 40 pins, 1 row, consecutive sequence with 0.02" (0.50mm) pitch.

Table 3-4: Debug Interface Signals (CN1)

Pin #	Signal
1	RESVD
2	SMC_STATUS
3	BIOS_MODE
4	SEL_BIOS
5	POSTWDT_DIS#
6	SUS_S5#
7	SUS_S4#
8	SUS_S3#
9	CB_PWROK
10	CB_RESET#
11	SYS_RESET#
12	PWRBTN#
13	SMC_OCD0B
14	SMC_OCD0A
15	SMC_CLK
16	SMC_DATA
17	SMC_RESET_IN#
18	SMC_FLMD0
19	SMC_RXD6
20	SMC_TXD6
21	GND3
22	3V3_DUAL

Table 3-4: Debug Interface Signals (CN1) (Continued)

23	3V3_SMC1
24	LPC_AD0
25	LPC_AD1
26	LPC_AD2
27	LPC_AD3
28	LPC_FRAME#
29	CLK33_LPC
30	RST#
31	BIOS_DIS0
32	GND2
33	LPC_3V3
34	SPI_BIOS_CLK
35	SPI_BIOS_MOSI
36	SPI_BIOS_MISO
37	SPI_BIOS_CS1#
38	SPI_BIOS_CS0#
39	GND1
40	VCC_SPI_IN

NOTE: The gray table cells denote ground.

4 Utilities

4.1 BIOS

The LEC-BT features an AMI BIOS. The default settings provide a “ready to run” system, even without a BIOS setup backup battery.

The BIOS is located in flash memory and can be easily updated with software under DOS.

All setup changes of the BIOS are stored in the CMOS RAM.

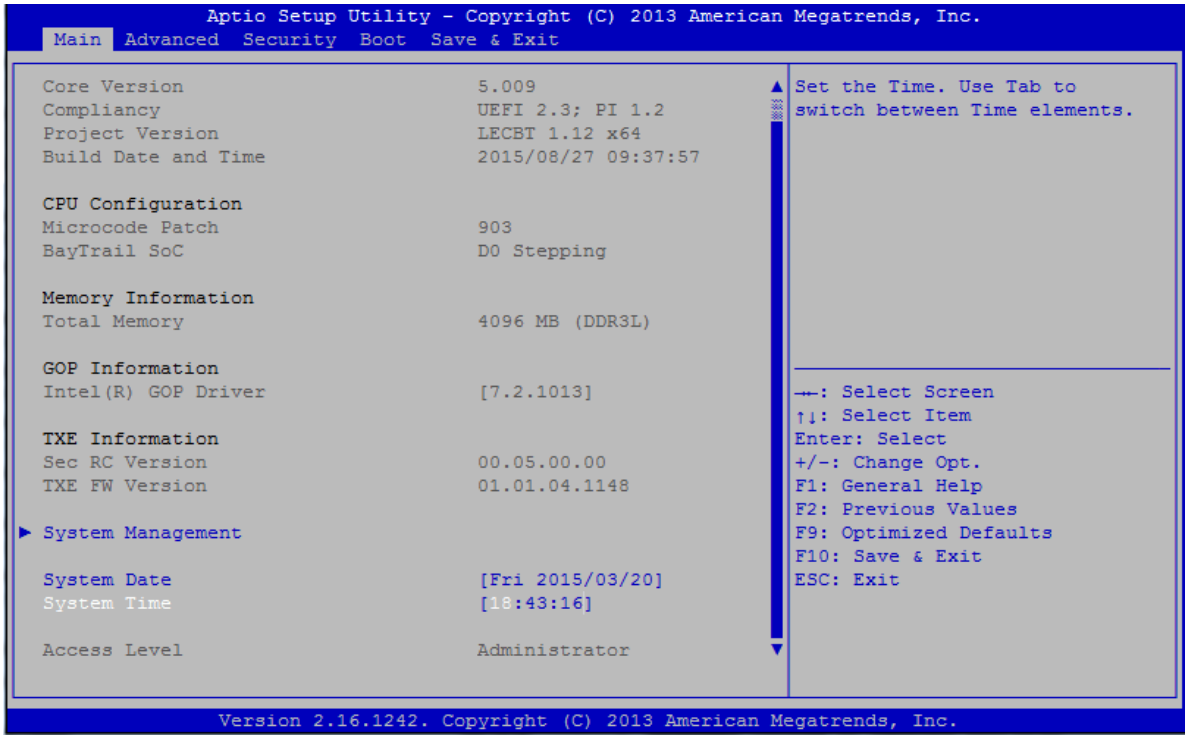
The soldered battery will provide power to store that information for over two years without board activation.

4.1.1 Configuring the BIOS

- Pressing <DEL> during power up starts the BIOS setup utility.
- Pressing <F11> during power up starts the boot menu.
- Pressing <END> during power up returns settings to default.

4.1.2 Main screen of the BIOS

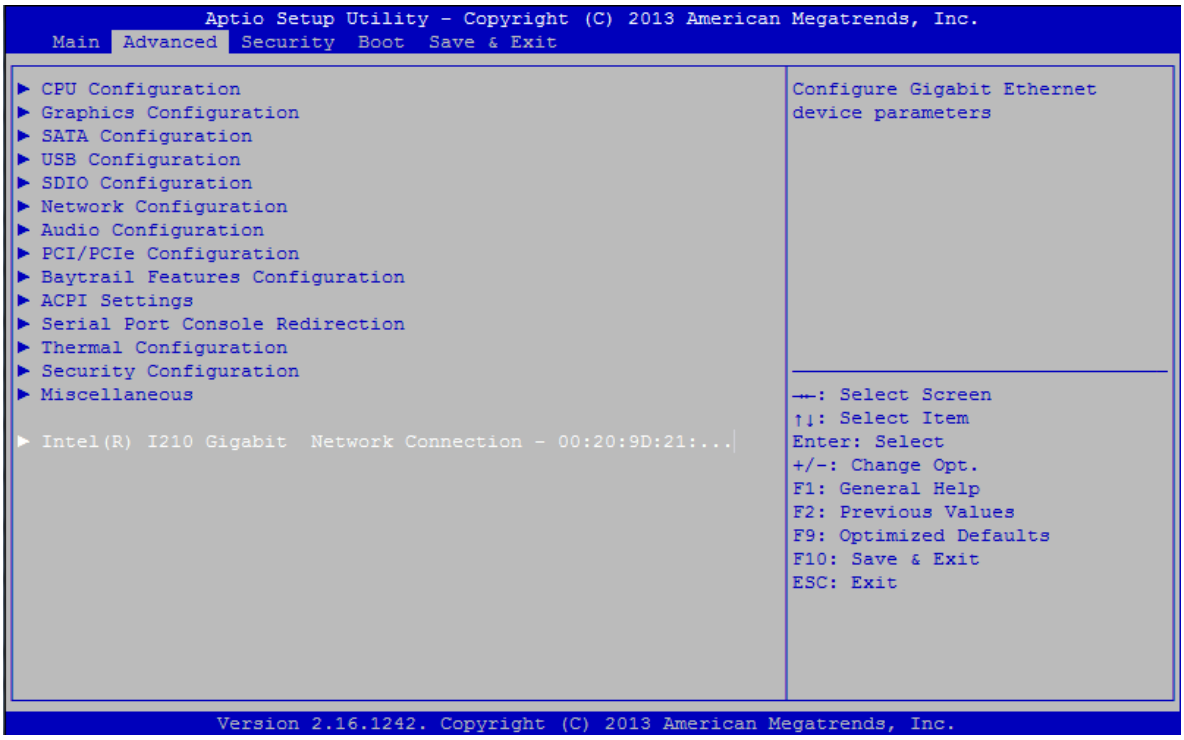
The main screen of the BIOS SETUP UTILITY provides an overview of the BIOS version, the clock speed, installed memory, memory speed, date and time, and other system information. The date and time can be configured by the user.



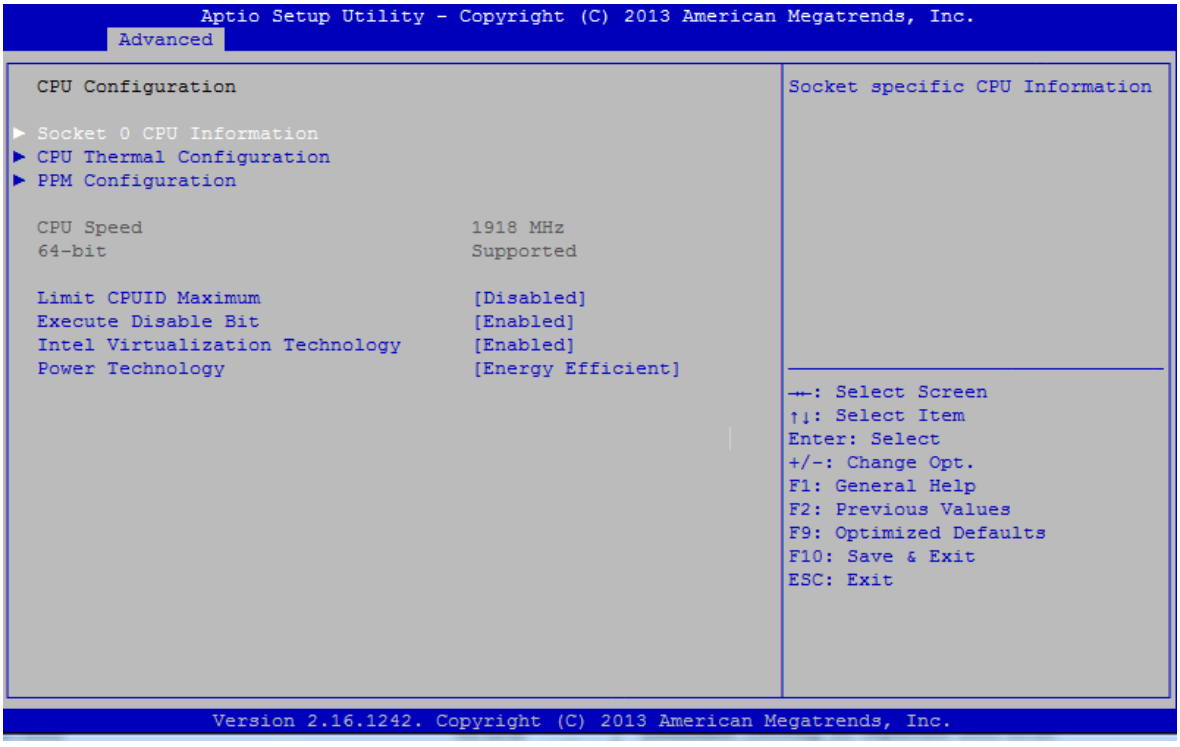
4.1.3 Advanced Settings screen

The main screen of “Advanced Settings” provides configuration settings for CPU, Graphics, SATA, USB, SDIO, Network, Audio, PCI/PCIe, Devices, ACPI, Serial, Thermal, Security, Miscellaneous, and SIO.

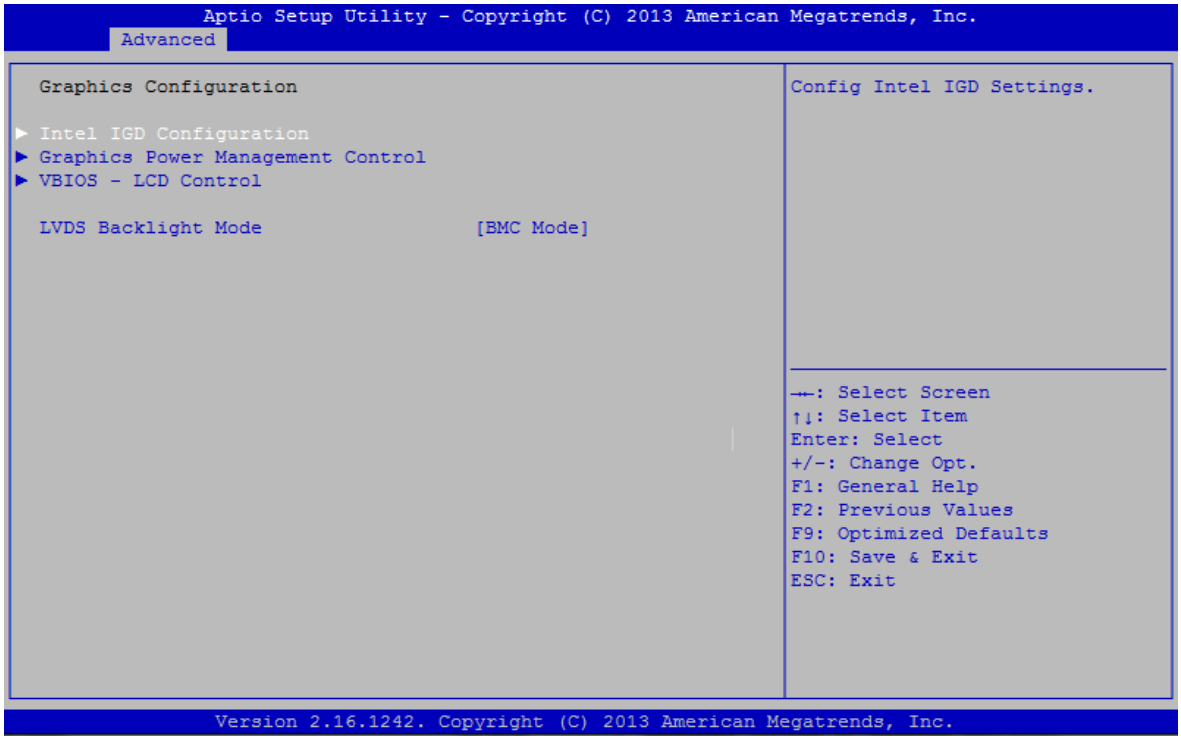
Inappropriate values for any of the following advanced settings below may cause the system to malfunction.



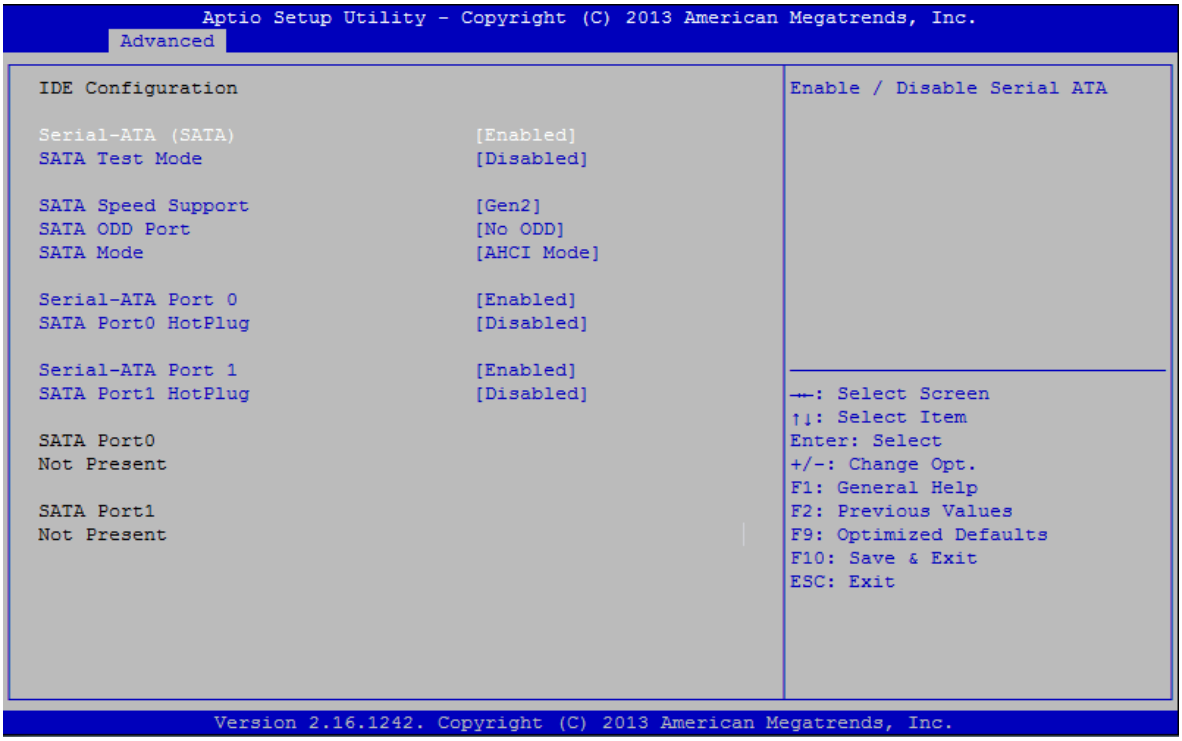
Advanced > CPU



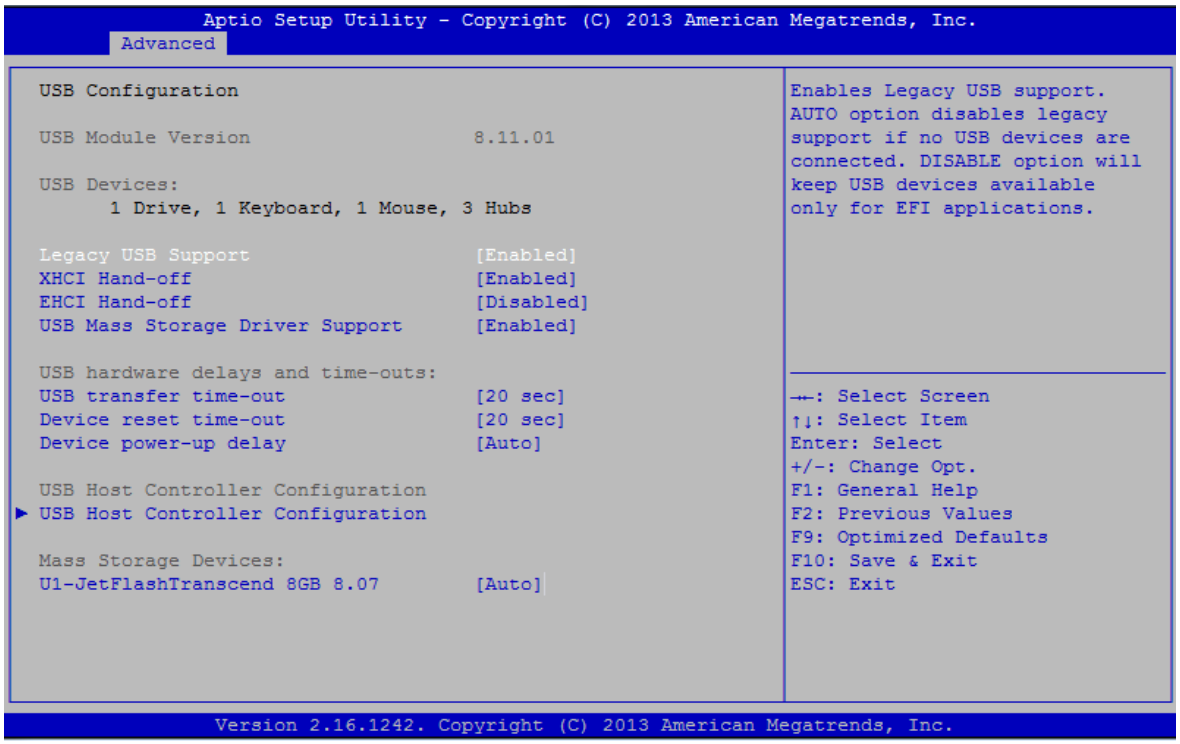
Advanced > Graphics



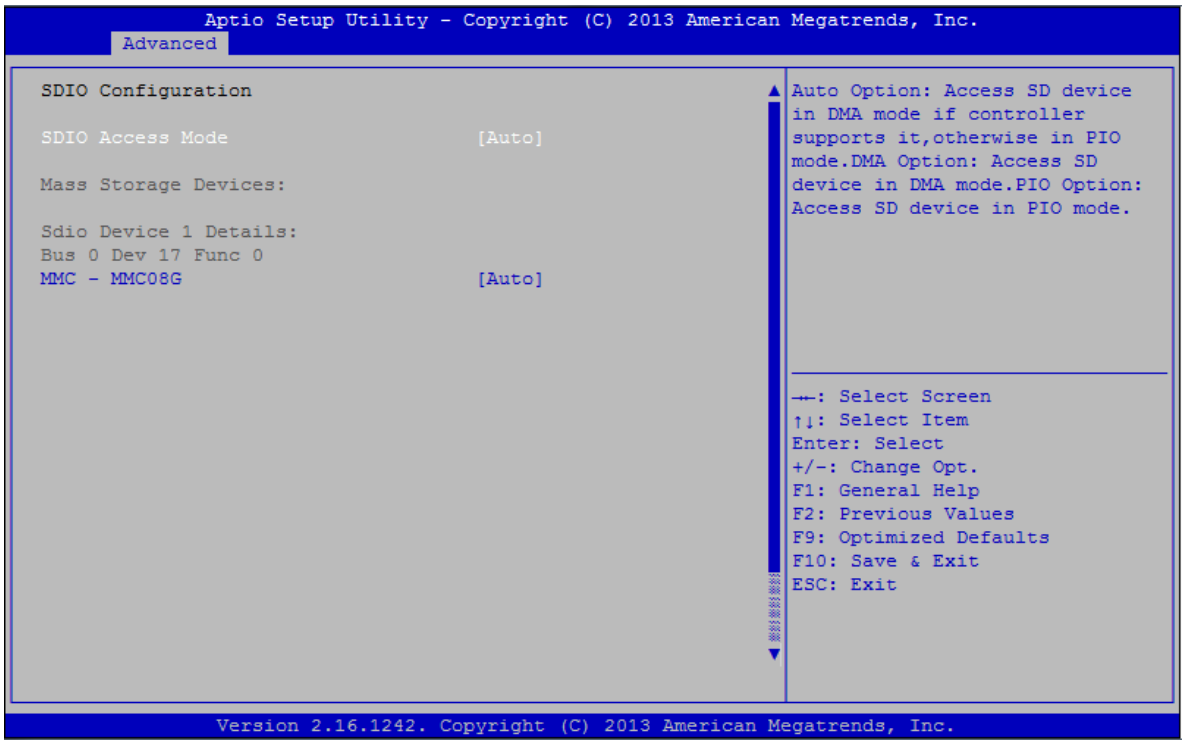
Advanced > SATA



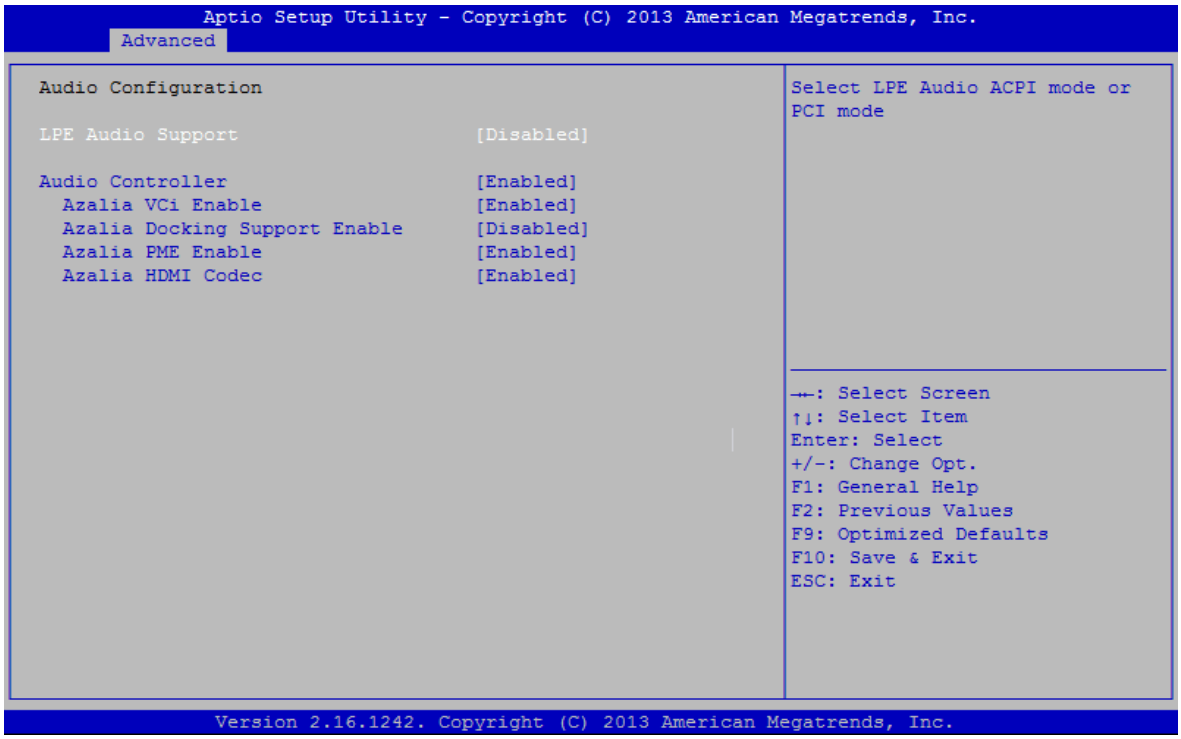
Advanced > USB



Advanced > SDIO

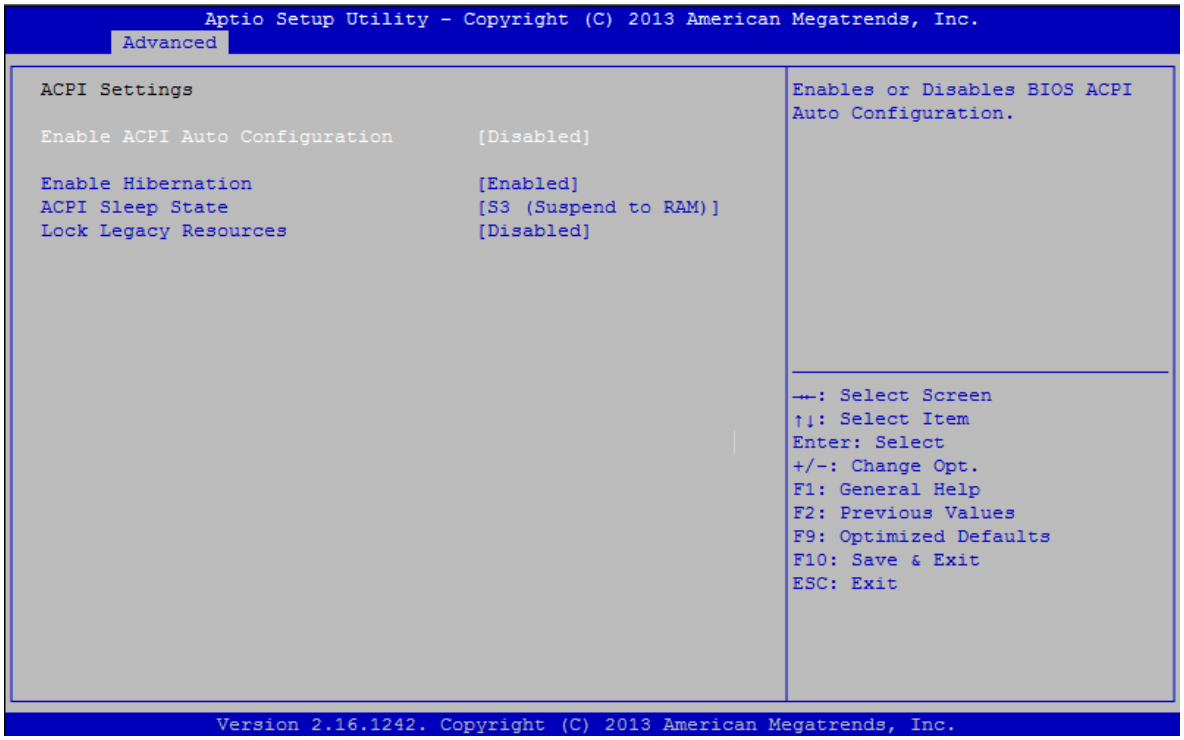


Advanced > Audio

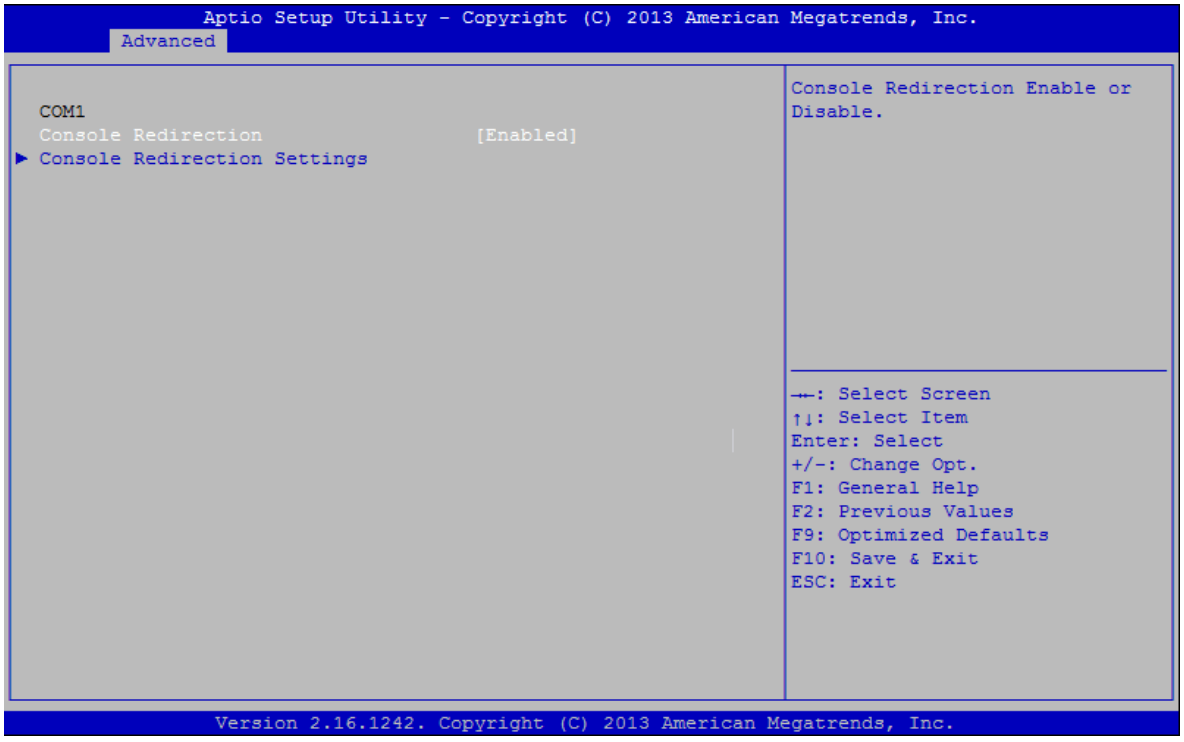


Advanced > PCI-PCIe

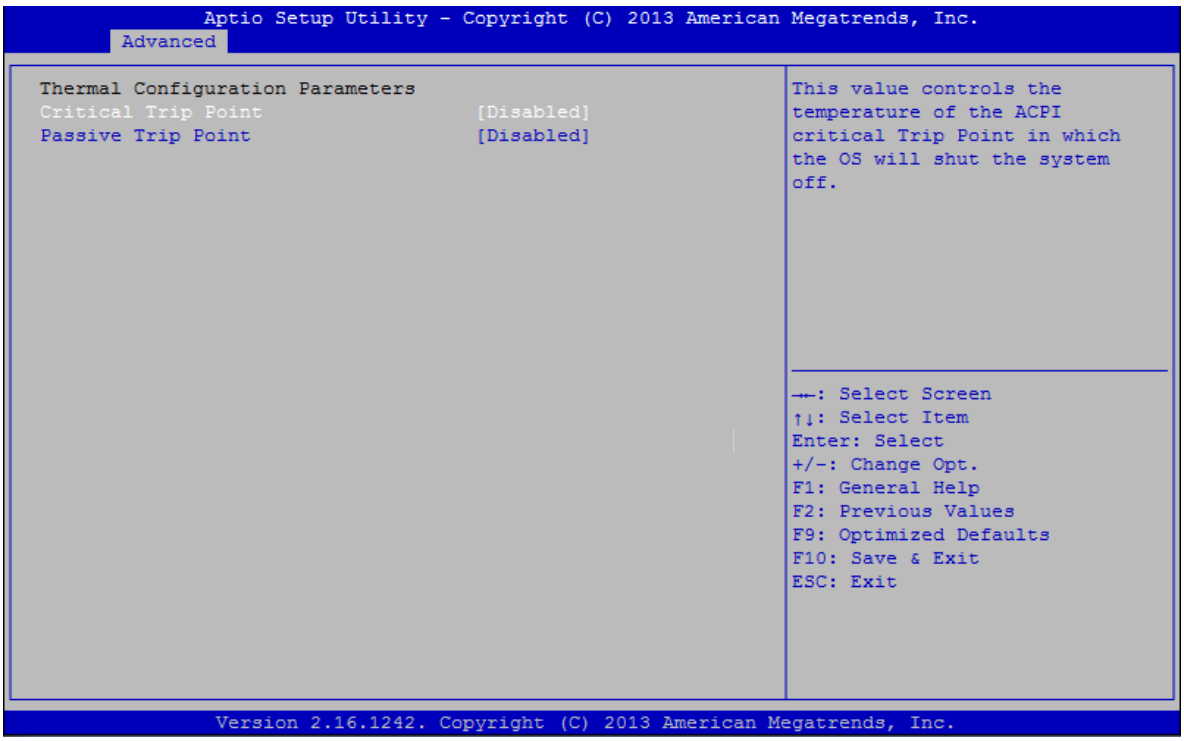
Advanced > ACPI



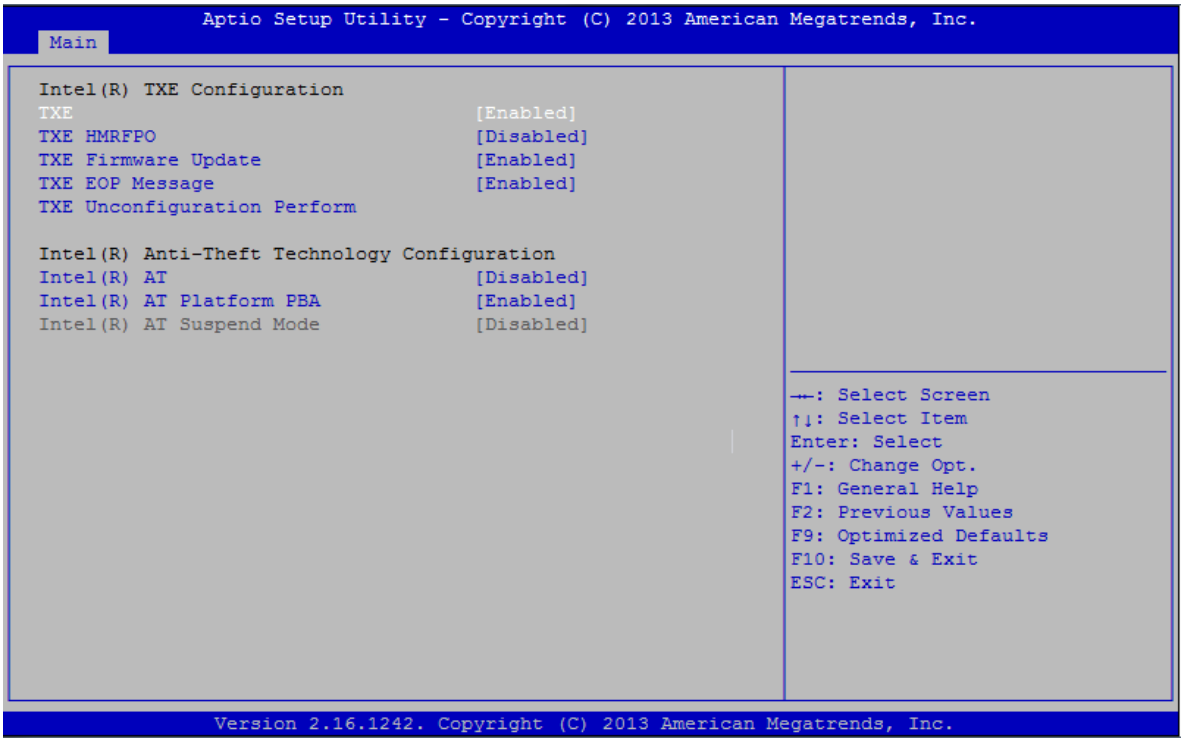
Advanced > Serial



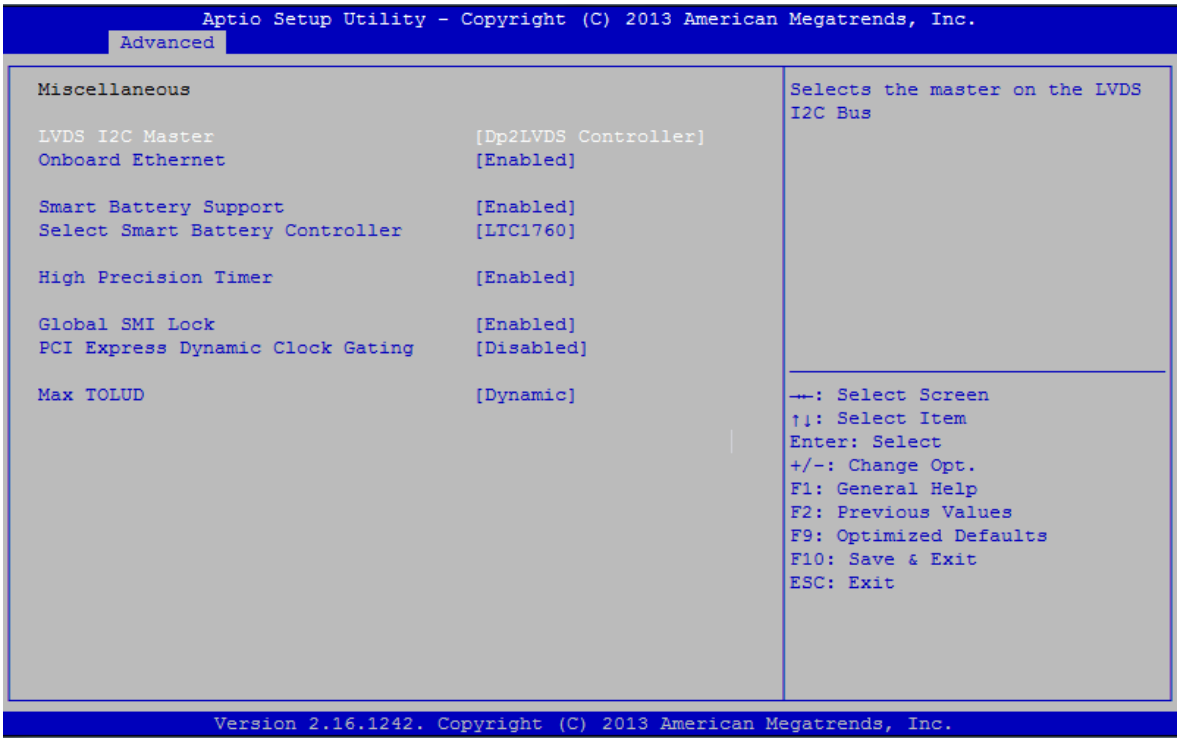
Advanced > Thermal



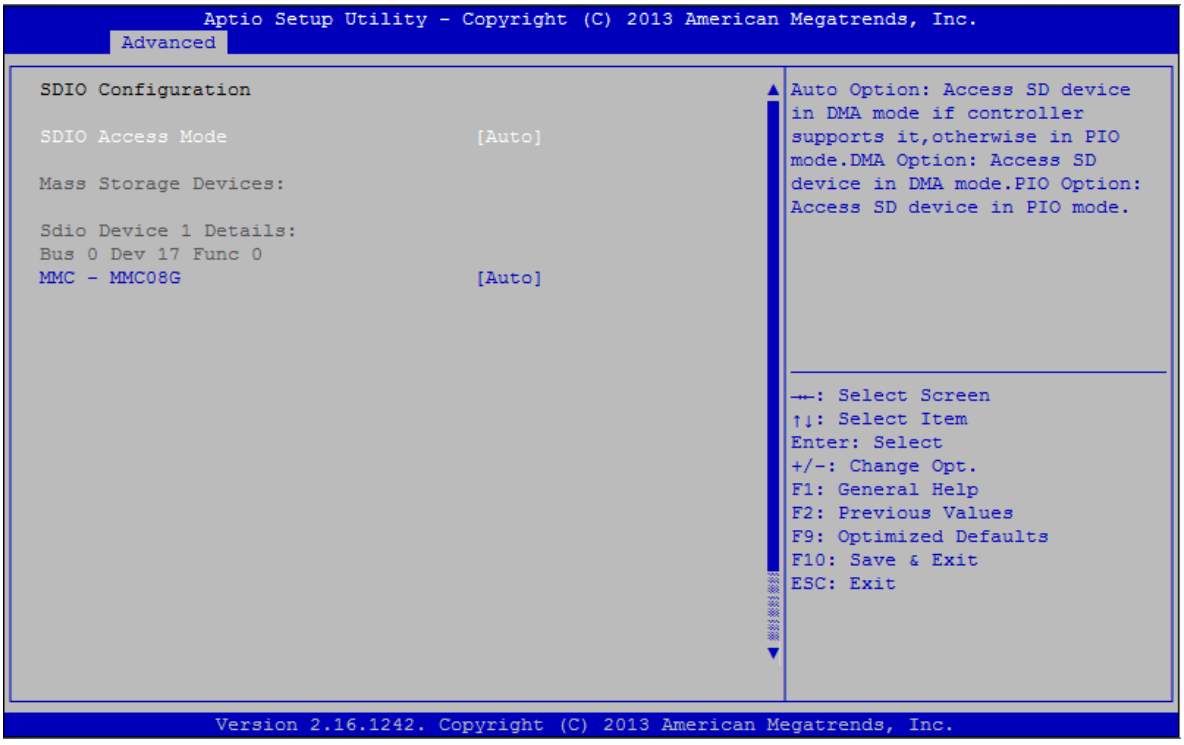
Advanced > Security



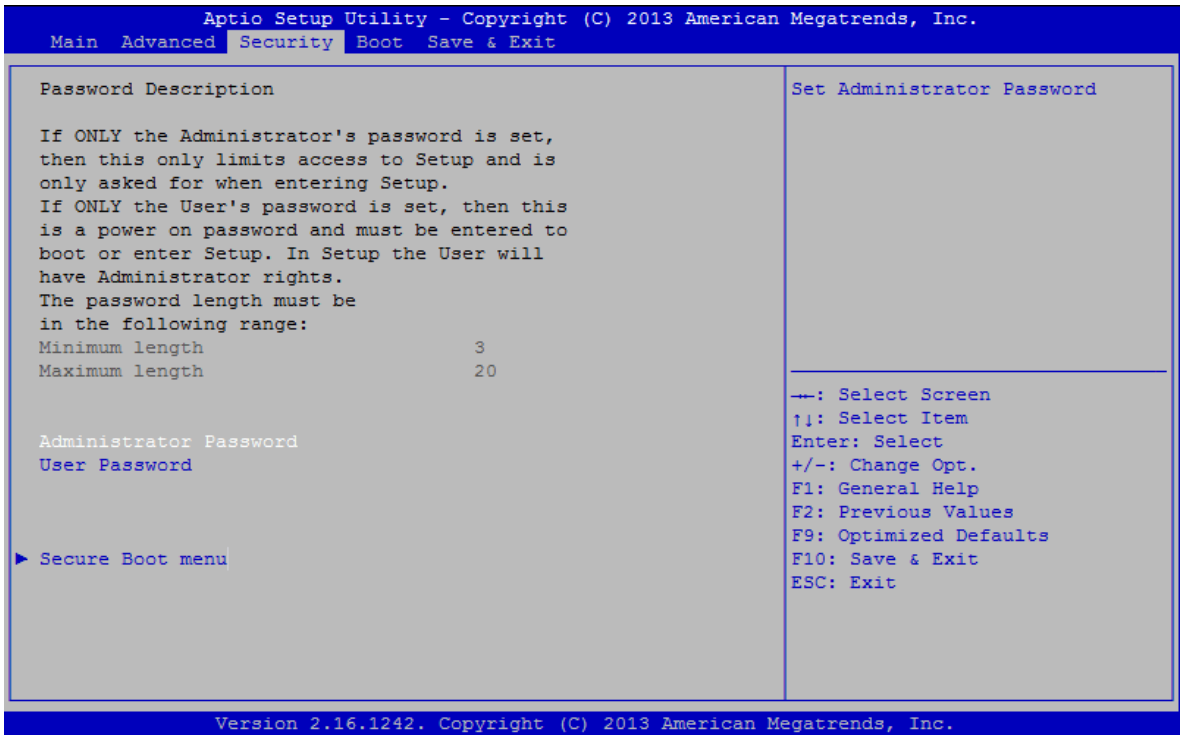
Advanced > Miscellaneous



Advanced > SDIO

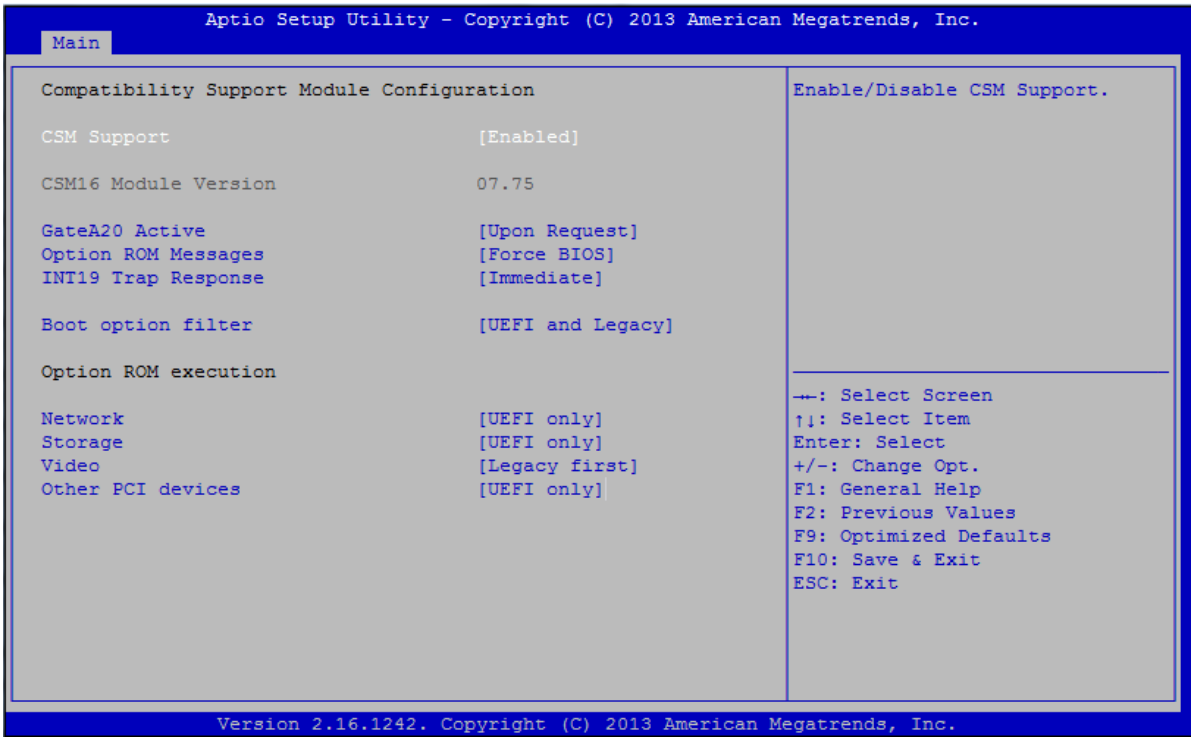


4.1.4 Security screen

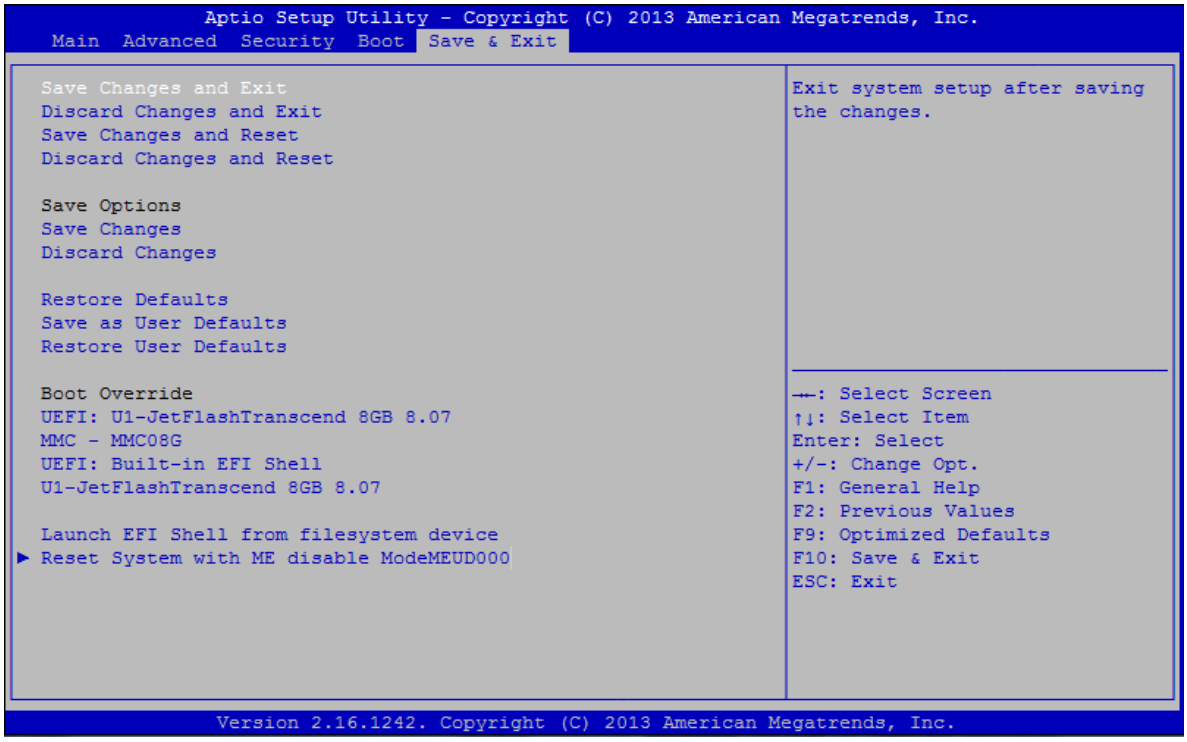


4.1.5 Boot screen

If more than one drive is attached to the LEC-BT, you can select from the first “Boot Configuration” screen the boot order in which the drives are scanned for a bootable OS image.



4.1.6 Save & Exit screen



4.2 SEMA functions

Under the management of the BMC chip (Board Management Controller), the SEMA utility (Smart Embedded Management Agent) provides system control and failure protection—counting, monitoring, and measuring hardware and software events, from which the SoC can trigger corrective commands. The optional SEMA Cloud utility not only controls local events on the module but system client events on the Internet of Things (IoT.) Refer to the following bullets for a list of SEMA functions.

- Total operating hours counter
  Counts the time the module has been run in minutes.
- On-time minutes counter
  Counts the seconds since last system start.
- Temperature monitoring of CPU and Board temperature
  Minimum and maximum temperature values of CPU and board are stored in flash.
- Power monitor
  Reads the current drawn by the board and reports the nominal operating voltage.
- Power cycles counter
- Boot counter
  Boot counter is increased after a HW- or SW-Reset or after a successful power-up.
- Watchdog Timer
  Set / Reset / Disable Watchdog Timer.
- System Restart Cause
  Power loss / Watchdog / External Reset.
- Flash area
  1kB Flash area for customer data
- Protected Flash area
  128 Bytes for Keys, ID's, etc. can be stored in a write- and clear-protectable region.
- Board Identify
  Vendor / Board / Serial number

The SEMA Tools are available for Windows and Linux. SEMA functionality can also be used in applications. Refer to the SEMA software manual and technical manual on the ADLINK web site for more information.

4.2.1 Board Specific SEMA functions

Voltages

The BMC of the LEC-BT implements a Voltage Monitor and samples several Onboard Voltages. The Voltages can be read by calling the SEMA function, “Get Voltages”. The function returns a 16-bit value divided in Hi-Byte (MSB) and Lo-Byte (LSB).

Table 4-1: BMC Voltage Monitor Values

ADC Channel	Voltage Name	Voltage Formula [V]
0	---	---
1	+V1.0S	(MSB<<8 + LSB) * 3.3 / 1024
2	+V1.2S	(MSB<<8 + LSB) * 3.3 / 1024
3	+V1.8S	(MSB<<8 + LSB) * 3.3 / 1024
4	+V3.3S	(MSB<<8 + LSB) * 1.100 * 3.3 / 1024
5	+V1.5S	(MSB<<8 + LSB) * 3.3 / 1024
6	+V5.0A	(MSB<<8 + LSB) * 1.833 * 3.3 / 1024

Table 4-1: BMC Voltage Monitor Values (Continued)

7	(MAINCURRENT)	Use Main Current Function

Main Current

The BMC of the LEC-BT implements a Current Monitor. The current can be read by calling the SEMA function “Get Main Current”. The function returns four 16-bit values divided in Hi-Byte (MSB) and Lo-Byte (LSB). These four values represent the last four currents drawn by the board. The values are sampled every 250ms. The order of the four values is NOT in relationship to time. The access to the BMC may increase the drawn current of the whole system. In this case, you still have three samples without the influence of the read access.

Main Current = (MSB_n<<8 + LSB_n) * 8.06mA

TS#-Events

TS# is activated by a temperature sensor when a device reaches its critical temperature and released when the device is back in its normal temperature range. This counter gives the user information about temperature or cooling issues. This counter is cleared when the system is removed from power. The LEC-BT only monitors the board temperature and does not support TS#-Events.

Exception Blink Codes

In the case of an error, the BMC shows a blink code on the STATUS-LED (LED1). This error code is also reported by the BMC Flags register. The Exception Code is not stored in the Flash storage and is cleared when the power is removed. Therefore, the “Clear Exception Code”-Command is not supported.

Table 4-2: Exception Blink Codes

Exception Blink Code	Error Message
0	NOERROR
2	NO_SUSCLK
3	NO_SLP_S5
4	NO_SLP_S3
5	RESET_FAIL
6	
7	POWER_FAIL
8	LOW_VIN
9	NO_PWRGD_ATX
10	NO_PWRGD_1V0S
11	NO_PWRGD_1V2S
13	NO_PWRGD_1V8S
14	NO_PWRGD_3V3S
15	NO_PWRGD_1V5S

BMC Flags

The BMC Flags register returns the last detected exception code since power up.

4.3 Watchdog Timer

The LEC-BT features three separate Watchdog Timers. One of them is integrated in the SoC and two are provided by the BMC (managed by the SEMA).

The SoC Watchdog can be configured in the BIOS or by programming the Watchdog registers. If this function is used by user application, the application has to provide all logging functionality if desired.

The BMC Watchdog activations are caused by under voltage protection. The Watchdog LED flashes after restart but only if the power supply reaches 4.2V.

4.4 Temperature Sensors

The LEC-BT supports two temperature sensor functions. One is offered from the SoC and one from a dedicated chip (Texas Instruments LM73) on the board.

The SoC temperature sensors can be configured by programming the appropriate SoC registers. Refer to the Thermal Management chapter in the Intel Atom E3800 data sheet for more information. The on-board LM73 temperature sensor is managed by the BMC and is configured through the SEMA utility.

4.5 Programming Examples

Programming examples can be provided based on a Linux operating system, upon request.

Appendix A Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed in Table A-1 below. Requests for support through Ask an Expert are given the highest priorities, and usually will be addressed within one working day.

- ADLINK Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the ADLINK web site at http://www.adlinktech.com/AAE/. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.

ADLINK strongly suggests that you register with the web site. By creating a profile on the ADLINK web site, you will have a portal page called “My ADLINK”, unique to you with access to exclusive services and account information.

- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to the My Question area where you can check status, update your request, and access other features.
- Download Service – This service is also free and available 24 hours a day at http://www.adlinktech.com. For certain downloads such as technical documents and software, you must register online before you can log in to this service.

Table A-1: Technical Support Contact Information

Method	Contact Information
Ask an Expert	http://www.adlinktech.com/AAE/
Web Site	http://www.adlinktech.com
Standard Mail	**ADLINK Technology, Inc.** Address: 9F, No.166 Jian Yi Road, Zhonghe District New Taipei City 235, Taiwan 新北市中和區建一路 166 號 9 樓 Tel: +886-2-8226-5877 Fax: +886-2-8226-5717 Email: service@adlinktech.com **Ampro ADLINK Technology, Inc.** Address: 5215 Hellyer Avenue, #110 San Jose, CA 95138, USA Tel: +1-408-360-0200 Toll Free: +1-800-966-5200 (USA only) Fax: +1-408-360-0222 Email: info@adlinktech.com **ADLINK Technology (China) Co., Ltd.** Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203) 300 Fang Chun Rd., Zhangjiang Hi-Tech Park Pudong New Area, Shanghai, 201203 China Tel: +86-21-5132-8988 Fax: +86-21-5132-3588 Email: market@adlinktech.com

Table A-1: Technical Support Contact Information (Continued)

ADLINK Technology Beijing
Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室(100085)
Rm. 801, Power Creative E, No. 1 Shang Di East Rd.
Beijing, 100085 China
Tel: +86-10-5885-8666
Fax: +86-10-5885-8626
Email: market@adlinktech.com

ADLINK Technology Shenzhen
Address: 深圳市南山区科技园南区高新南七道 数字技术园
A1 栋 2 楼 C 区 (518057)
2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7
High-Tech Industrial Park S., Shenzhen, 518054 China
Tel: +86-755-2643-4858
Fax: +86-755-2664-6353
Email: market@adlinktech.com

LiPPERT ADLINK Technology GmbH
Address: Hans-Thoma-Strasse 11
D-68163 Mannheim, Germany
Tel: +49-621-43214-0
Fax: +49-621 43214-30
Email: emea@adlinktech.com

PENTA ADLINK Technology GmbH
Ulrichsbergerstrasse 17
94469 Deggendorf, Germany
Tel: +49 (0) 991 290 94 – 10
Fax: +49 (0) 991 290 94 - 29
Email: emea@adlinktech.com

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91940 Les Ulis, France
Tel: +33 (0) 1 60 12 35 66
Fax: +33 (0) 1 60 12 35 66
Email: france@adlinktech.com

ADLINK Technology Japan Corporation
Address: 〒101-0045 東京都千代田区神田鍛冶町 3-7-4
神田 374 ビル 4F
KANDA374 Bldg. 4F, 3-7-4 Kanda Kajicho,
Chiyoda-ku, Tokyo 101-0045, Japan
Tel: +81-3-4455-3722
Fax: +81-3-5209-6013
Email: japan@adlinktech.com

ADLINK Technology, Inc. (Korean Liaison Office)
Address: 경기도 성남시 분당구 수내로 46 번길 4 경동빌딩 2 층
(수내동 4-4 번지) (우) 463-825
2F, Kyungdong B/D, 4 Sunae-ro 46 beon-gil
Bundang-gu, Seongnam-si, Gyeonggi-do, Korea, 13595
Toll Free +82-80-800-0585
Tel +82-31-786-0585
Fax +82-31-786-0583
Email: korea@adlinktech.com

Table A-1: Technical Support Contact Information (Continued)

	ADLINK Technology Singapore Pte. Ltd. Address: 84 Genting Lane #07-02A, Cityneon Design Centre Singapore 349584 Tel: +65-6844-2261 Fax: +65-6844-2263 Email: singapore@adlinktech.com **ADLINK Technology Singapore Pte. Ltd. (Indian Liaison Office)** Address: #50-56, First Floor, Spearhead Towers Margosa Main Road (between 16th/17th Cross) Malleswaram, Bangalore - 560 055, India Tel: +91-80-65605817, +91-80-42246107 Fax: +91-80-23464606 Email: india@adlinktech.com **ADLINK Technology, Inc. (Israeli Liaison Office)** Address: 27 Maskit St., Corex Building PO Box 12777 Herzliya 4673300, Israel Tel: +972-54-632-5251 Fax: +972-77-208-0230 Email: israel@adlinktech.com **ADLINK Technology, Inc. (UK Liaison Office)** Tel: +44 774 010 59 65 Email: UK@adlinktech.com