LEC-PX30

User's Guide

22/01/2020

Rev. 0.7

Corrected engineering version

Preface

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Safety Instructions

For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

Conventions

The following conventions may be used throughout this manual, denoting special levels of information

Note: This information adds clarity or specifics to text and illustrations.

Caution: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

Warning: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

Revision History

Revision	Description	Date	Author
0.6	Engineering version	22/8/2019	JB
0.7	Corrected engineering version, mechanical and SMARC to controller table	6/9/2019	JB

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1. Introduction

Warning: this is an EA (early available) engineering manual, meaning contents might properly reflect the actual or final version of this product

1.1 The SMARC Formfactor

The SMARC ("Smart Mobility ARChitecture") is a versatile small form factor computer on Module definition targeting applications that require low power, low costs, and high performance. The Modules will typically use ARM SOCs similar or the same as those used in many familiar devices such as tablet computers and smart phones. Alternative low power SOCs and CPUs, such as tablet oriented X86 devices and other RISC CPUs may be used as well. The Module power envelope is typically under 6W.

Two Module sizes are defined: 82 mm x 50 mm and 82 mm x 80 mm.

The Module PCBs have 314 edge fingers that mate with a low profile 314 pin 0.5 mm pitch right angle connector (the connector is sometimes identified as a 321 pin connector, but 7 pins are lost to the key).

The Modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE and a single channel LVDS display transmitter are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

SGeT STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

SMARC module and carrier specifications are available online at: https://www.sget.org/standards/smarc.html

2. Specifications

2.1 Core System

SoC

Rockchip PX30 with Quad-core ARM Cortex-A35 CPU TrustZone technology support ARMv8 Cryptography Extensions"

Memory

1GB or 2GB DDR3L at 1066/1333 MHz, memory down (non ECC)

L2 Cache

256KB unified system L2 cache

IoT security

CryptoAuthentication™ Device, Microchip ATECC608A

Cryptographic co-processor with secure hardware-based key storage for sign-verify authentication provides Internet of Things (IoT) Protected

Storage for up to 16 keys, certificates or data ECDH: FIPS SP800-56A Elliptic Curve Diffie-Hellman NIST standard P256

elliptic curve support SHA-256 & HMAC hash including off-chip context save/restore AES-128: encrypt/decrypt, galois field multiply for GCM"

2.2 Video

LEC-PX30 standard display support is limited to either 4-lane MIPI DSI or single channel 24-bit LVDS. DSI and LVDS are multiplexed and either of them can simply be enabled at boot time. HDMI panel support up to 1920x1080 resolution can be achieved by using a simple bridge on the carrier. A reference design based on ADV7335 "MIPI/DSI Receiver with HDMI Transmitter" is available

GPU Core:

Mali-G31

GPU Feature Support

Supports DirectX 11 FL9_3, OpenGLES 1.1/ 2.0 / 3.2, Vulkan 1.0, OpenCL 2.0

Full Profile Video decoding: H.264 up to 1080p@60fps, H.265/HEVC up to 1080p@60fps

MPEG-4, ISO/IEC 14496-2, SP@L0-3, ASP@L0-5, up to 1080p@60fps VP8, up to 1080p@60fps

Video Encoding: H.264 video encoder at BP/MP/HP@level 4.2 1920x1080@30fps, 1x 1080p@30fps or 2x 720p@30fps encoding

MIPI DSI

MIPI DSI 4 lanes at max. 1080p@60fps display output (default, multiplexed with LVDS signal)

LVDS

LVDS single channel 24-bit at max. 1280x800@60fps (multiplexed with MIPI DSI signal)

Camera

MIPI CSI RX Interface

- Compatible with the MIPI Alliance Interface specification v1.0

- Up to 4 data lanes, 1.0Gbps maximum data rate per lane, supporting MIPI-HS, MIPI-LP mode

2.3 Audio

Supports ES8316 codec for high performance and low power multi-bit deltasigma audio ADC and DAC (located on carrier)

2.4 Dual Ethernet

Primary LAN

MAC 10/100 Ethernet Controller on SoC

Supports 10/100-Mbps data transfer rates, both full-duplex and half-duplex

Secondary LAN

MAC/PHY 10/100 Ethernet Controller on LAN9514 via USB 2.0

Supports 10/100-Mbps data transfer rates, both full-duplex and half-duplex

2.5 Extension busses

USB

4x USB 2.0, 1x USB OTG

UART

Two UART interfaces SER0 and SER2 (TX/X/CTS/RTS), 64-byte FIFO and support for 5-bit, 6-bit, 7-bit, 8-bit data transmit or receive

CAN bus

Supports CAN2.0B only or mixed CAN2.0B and CAN FD mode, data bit rate up to 8 Mbps

SPI

2x SPI (one occupied by SPI-to-CAN controller)

I2S

2x I2S interfaces with audio resolution from 16-bits to 32-bits and sample rate up to 192KHz (see Audio Codec support)

I2C

Four I2C interfaces

- Support for 7-bit and 10-bit address mode

- Software programmable clock frequency of 100 kbit/s in Standard-mode,

400 kbit/s in the Fast-mode or 1 Mbit/s in Fast-mode Plus

GPIO

12x GPIO with interrupt, one GPIO with PWM

2.6 System Storage

SDIO

1x SDIO (4-bit) compatible with SD3.0, MMC ver. 4.51

eMMC

8, 16, 32 or 64 GB (build option)

Compatible with eMMC specification 4.41, 4.51, 5.0 and 5.1

2.7 SEMA® Board Management Controller

Voltage/current monitoring, boot configuration, logistics and forensic

information, flat panel control, watchdog timer

2.8 Debug Header

30-pin multipurpose flat cable connector for use with optional DB-30 debug module Provides JTAG, BMC access; UART, power test points; diagnostic LEDs, Power, Reset, Boot configuration

2.9 Power

Supply Voltage

4.75 V – 5.25 V

Rise Time

TBD

2.10 Mechanical and Environmental

Form Factor

SGET SMARC Specifications v2.1 (2.1 is currently under approval by SGET)

Dimension

SMARC short size module, 82mm x 50mm

Operating Temperature

Standard: 0°C to +60°C

Rugged: -20°C to +85°C (optional)

Humidity

5-90% RH operating, non-condensing

5-95% RH storage (and operating with conformal coating)

Shock and Vibration

IEC 60068-2-64 and IEC-60068-2-27, MIL-STD-202 F, Method 213B, Table 213-I,

Condition A and Method 214A, Table 214-I, Condition D

3. Block Diagram

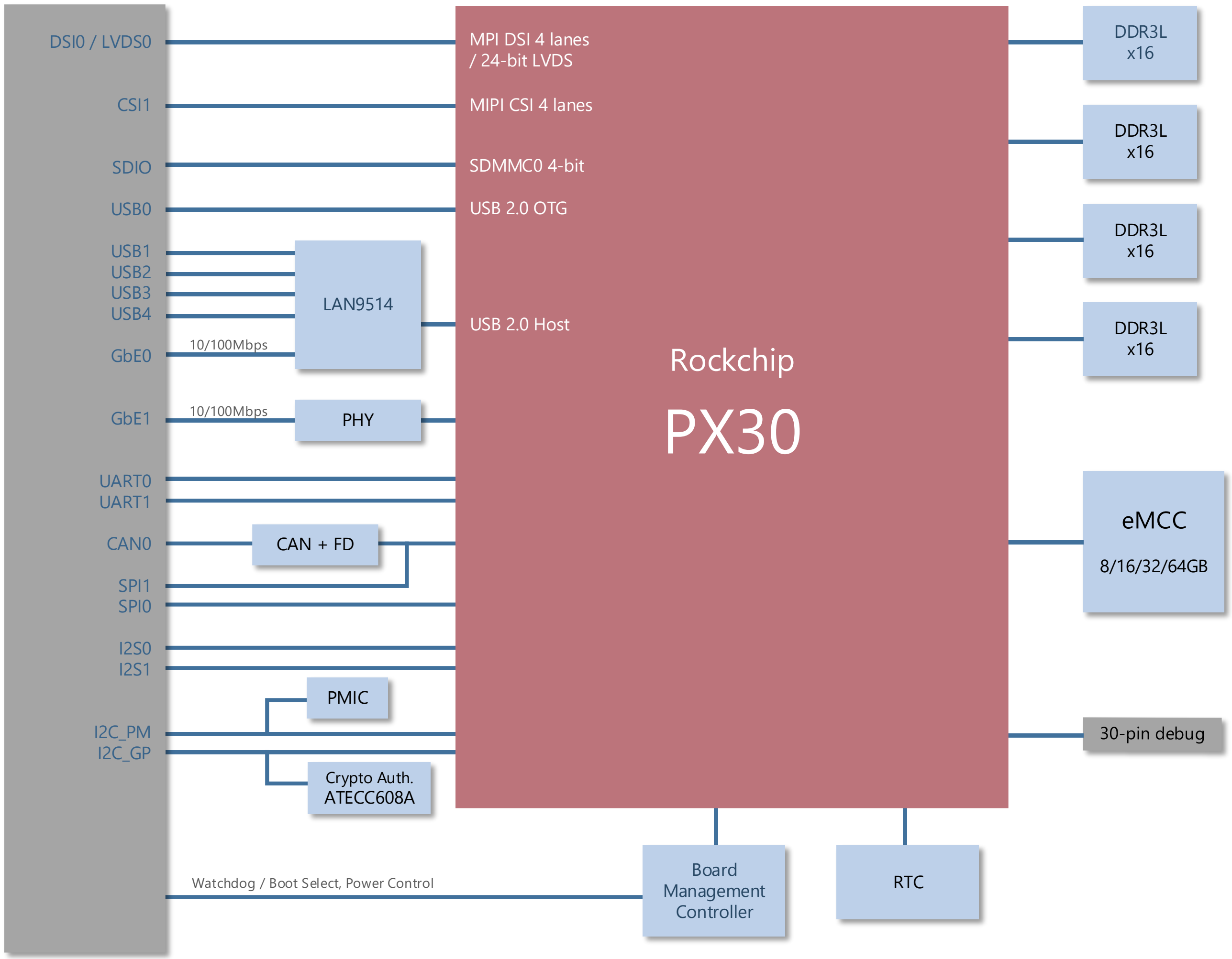

Figure 1 – Module function diagram

4. Pinout and Signal Descriptions

4.1 Pin Summary

The below table is a comprehensible list of all signal pins on the MXM 3 connector in the standard specification SMARC 2.1. Those signals not supported on LEC-PX30 are strikethrough ~~STRIKETHROUGH~~

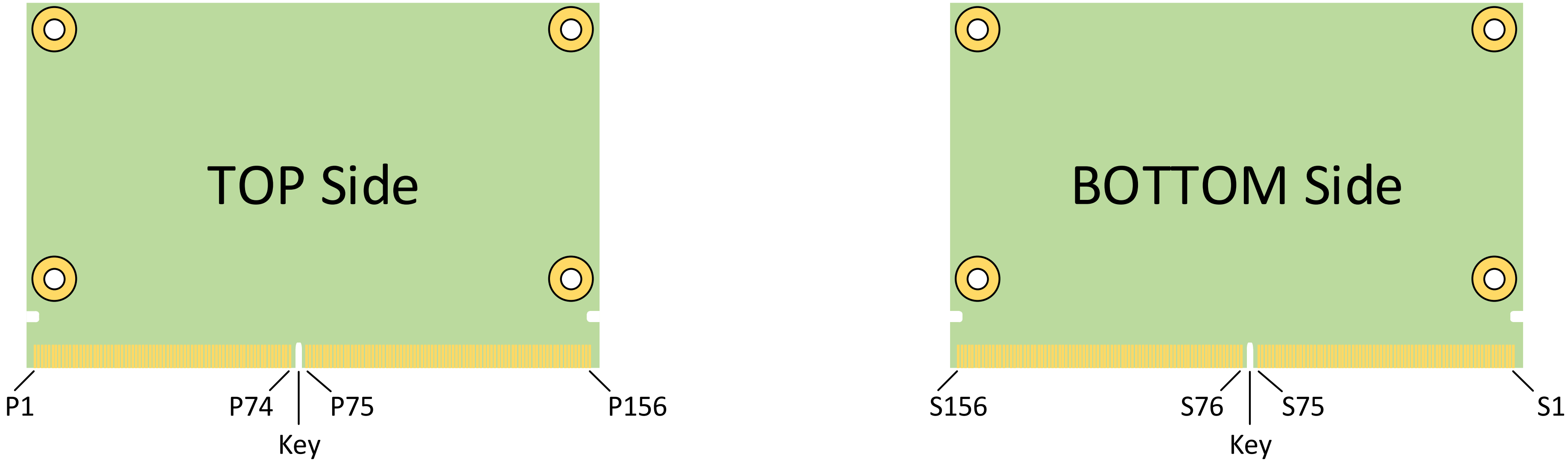

Figure 2 – Module top/botom side pin numbering

P-Pin	Primary (Top) Side
P1	~~SMB_ALERT_1V8#~~
P2	GND
P3	CSI1_CK+
P4	CSI1_CK-
P5	~~GBE1_SDP~~
P6	~~GBE0_SDP~~
P7	CSI1_RX0+
P8	CSI1_RX0-
P9	GND
P10	CSI1_RX1+
P11	CSI1_RX1-
P12	GND
P13	CSI1_RX2+
P14	CSI1_RX2-
P15	GND
P16	CSI1_RX3+
P17	CSI1_RX3-
P18	GND
P19	~~GBE0_MDI3-~~
P20	~~GBE0_MDI3+~~
P21	GBE0_LINK100#
P22	~~GBE0_LINK1000#~~
P23	~~GBE0_MDI2-~~
P24	~~GBE0_MDI2+~~
P25	GBE0_LINK_ACT#
P26	GBE0_MDI1-
P27	GBE0_MDI1+
P28	GBE0_CTREF
P29	GBE0_MDI0-
P30	GBE0_MDI0+
P31	~~SPI0_CS1#~~
P32	GND
P33	SDIO_WP
P34	SDIO_CMD

S-Pin	Secondary (Bottom) Side
S1	~~CSI1_TX+~~ / I2C_CAM1_CK
S2	~~CSI1_TX-~~ / I2C_CAM1_DAT
S3	GND
S4	RSVD
S5	~~CSI0_TX-~~ / ~~I2C_CAM0_CK~~
S6	CAM_MCK
S7	~~CSI0_TX+~~ / ~~I2C_CAM0_DAT~~
S8	~~CSI0_CK+~~
S9	~~CSI0_CK-~~
S10	GND
S11	~~CSI0_RX0+~~
S12	~~CSI0_RX0-~~
S13	GND
S14	~~CSI0_RX1+~~
S15	~~CSI0_RX1-~~
S16	GND
S17	GBE1_MDI0+
S18	GBE1_MDI0-
S19	GBE1_LINK100#
S20	GBE1_MDI1+
S21	GBE1_MDI1-
S22	~~GBE1_LINK1000#~~
S23	~~GBE1_MDI2+~~
S24	~~GBE1_MDI2-~~
S25	GND
S26	~~GBE1_MDI3+~~
S27	~~GBE1_MDI3-~~
S28	~~GBE1_CTREF~~
S29	~~PCIE_D_TX+~~ / ~~SERDES_1_TX+~~
S30	~~PCIE_D_TX-~~ / ~~SERDES_1_TX-~~
S31	GBE1_LINK_ACT#
S32	~~PCIE_D_RX+~~ ~~/ SERDES_1_RX+~~
S33	~~PCIE_D_RX-~~ / ~~SERDES_1_RX-~~
S34	GND
S35	USB4+

P-Pin	Primary (Top) Side
P35	SDIO_CD#
P36	SDIO_CK
P37	SDIO_PWR_EN
P38	GND
P39	SDIO_D0
P40	SDIO_D1
P41	SDIO_D2
P42	SDIO_D3
P43	SPI0_CS0#
P44	SPI0_CK
P45	SPI0_DIN
P46	SPI0_DO
P47	GND
P48	~~SATA_TX+~~
P49	~~SATA_TX-~~
P50	GND
P51	~~SATA_RX+~~
P52	~~SATA_RX-~~
P53	GND
P54	~~ESPI_CS0# /~~ SPI1_CS0#
P55	~~ESPI_CS1# /~~ SPI1_CS1#
P56	~~ESPI_CK /~~ SPI1_CK
P57	~~ESPI_IO_1 /~~ SPI1_DIN
P58	~~ESPI_IO_0 /~~ SPI1_DO
P59	GND
P60	USB0+
P61	USB0-
P62	USB0_EN_OC#
P63	USB0_VBUS_DET
P64	USB0_OTG_ID
P65	USB1+
P66	USB1-
P67	USB1_EN_OC#
P68	GND
P69	USB2+

S-Pin	Secondary (Bottom) Side
S36	USB4-
S37	~~USB3_VBUS_DET~~
S38	AUDIO_MCK
S39	I2S0_LRCK
S40	I2S0_SDOUT
S41	I2S0_SDIN
S42	I2S0_CK
S43	~~ESPI_ALERT0#~~
S44	~~ESPI_ALERT1#~~
S45	~~MDIO_CLK~~
S46	~~MDIO_DAT~~
S47	GND
S48	I2C_GP_CK
S49	I2C_GP_DAT
S50	~~HDA_SYNC~~ / I2S2_LRCK
S51	~~HDA_SDO~~ / I2S2_SDOUT
S52	~~HDA_SDI~~ / I2S2_SDIN
S53	~~HDA_CK~~ / I2S2_CK
S54	~~SATA_ACT#~~
S55	~~USB5_EN_OC#~~
S56	~~ESPI_IO_2~~
S57	~~ESPI_IO_3~~
S58	~~ESPI_RESET#~~
S59	~~USB5+~~
S60	~~USB5-~~
S61	GND
S62	~~USB3_SSTX+~~
S63	~~USB3_SSTX-~~
S64	GND
S65	~~USB3_SSRX+~~
S66	~~USB3_SSRX-~~
S67	GND
S68	USB3+
S69	USB3-
S70	GND

P-Pin	Primary (Top) Side
P70	USB2-
P71	USB2_EN_OC#
P72	RSVD
P73	RSVD
P74	USB3_EN_OC#
	Key
P75	~~PCIE_A_RST#~~
P76	USB4_EN_OC#
P77	~~PCIE_B_CKREQ#~~
P78	~~PCIE_A_CKREQ#~~
P79	GND
P80	~~PCIE_C_REFCK+~~
P81	~~PCIE_C_REFCK-~~
P82	GND
P83	~~PCIE_A_REFCK+~~
P84	~~PCIE_A_REFCK-~~
P85	GND
P86	~~PCIE_A_RX+~~
P87	~~PCIE_A_RX-~~
P88	GND
P89	~~PCIE_A_TX+~~
P90	~~PCIE_A_TX-~~
P91	GND
P92	~~HDMI_D2+ / DP1_LANE0+~~
P93	~~HDMI_D2- / DP1_LANE0-~~
P94	GND
P95	~~HDMI_D1+ / DP1_LANE1+~~
P96	~~HDMI_D1- / DP1_LANE1-~~
P97	GND
P98	~~HDMI_D0+~~ / ~~DP1_LANE2+~~
P99	~~HDMI_D0-~~ / ~~DP1_LANE2-~~
P100	GND
P101	~~HDMI_CK+~~ / ~~DP1_LANE3+~~
P102	~~HDMI_CK-~~ / ~~DP1_LANE3-~~

S-Pin	Secondary (Bottom) Side
S71	~~USB2_SSTX+~~
S72	~~USB2_SSTX-~~
S73	GND
S74	~~USB2_SSRX+~~
S75	~~USB2_SSRX-~~
	Key
S76	~~PCIE_B_RST#~~
S77	~~PCIE_C_RST#~~
S78	~~PCIE_C_RX+~~ / ~~SERDES_2_RX+~~
S79	~~PCIE_C_RX-~~ / ~~SERDES_2_RX-~~
S80	GND
S81	~~PCIE_C_TX+~~ / ~~SERDES_2_TX+~~
S82	~~PCIE_C_TX-~~ / ~~SERDES_2_TX-~~
S83	GND
S84	~~PCIE_B_REFCK+~~
S85	~~PCIE_B_REFCK-~~
S86	GND
S87	~~PCIE_B_RX+~~
S88	~~PCIE_B_RX-~~
S89	GND
S90	~~PCIE_B_TX+~~
S91	~~PCIE_B_TX-~~
S92	GND
S93	~~DP0_LANE0+~~
S94	~~DP0_LANE0-~~
S95	~~DP0_AUX_SEL~~
S96	~~DP0_LANE1+~~
S97	~~DP0_LANE1-~~
S98	~~DP0_HPD~~
S99	~~DP0_LANE2+~~
S100	~~DP0_LANE2-~~
S101	GND
S102	~~DP0_LANE3+~~
S103	~~DP0_LANE3-~~

P-Pin	Primary (Top) Side
P103	GND
P104	~~HDMI_HPD~~ / ~~DP1_HPD~~
P105	~~HDMI_CTRL_CK~~ / ~~DP1_AUX+~~
P106	~~HDMI_CTRL_DAT~~ /
P107	~~DP1_AUX_SEL~~
P108	GPIO0 / ~~CAM0_PWR#~~
P109	GPIO1 / CAM1_PWR#
P110	GPIO2 / ~~CAM0_RST#~~
P111	GPIO3 / CAM1_RST#
P112	GPIO4 ~~/ HDA_RST#~~
P113	GPIO5 / PWM_OUT
P114	GPIO6 ~~/ TACHIN~~
P115	GPIO7
P116	GPIO8
P117	GPIO9
P118	GPIO10
P119	GPIO11
P120	GND
P121	I2C_PM_CK
P122	I2C_PM_DAT
P123	BOOT_SEL0#
P124	BOOT_SEL1#
P125	BOOT_SEL2#
P126	RESET_OUT#
P127	RESET_IN#
P128	POWER_BTN#
P129	SER0_TX
P130	SER0_RX
P131	~~SER0_RTS#~~
P132	~~SER0_CTS#~~
P133	GND
P134	~~SER1_TX~~
P135	~~SER1_RX~~
P136	SER2_TX
P137	SER2_RX
P138	SER2_RTS#

S-Pin	Secondary (Bottom) Side
S104	~~USB3_OTG_ID~~
S105	~~DP0_AUX+~~
S106	~~DP0_AUX-~~
S107	~~LCD1_BKLT_EN~~
S108	~~LVDS1_CK+~~ / ~~eDP1_AUX+ /~~
S109	~~LVDS1_CK-~~ / ~~eDP1_AUX- /~~
S110	GND
S111	~~LVDS1_0+~~ / ~~eDP1_TX0+~~ / ~~DSI1_D0+~~
S112	~~LVDS1_0-~~ / ~~eDP1_TX0-~~ / ~~DSI1_D0-~~
S113	~~eDP1_HPD~~ / ~~DSI1_TE~~
S114	~~LVDS1_1+~~ / ~~eDP1_TX1+~~ / ~~DSI1_D1+~~
S115	~~LVDS1_1-~~ / ~~eDP1_TX1-~~ / ~~DSI1_D1-~~
S116	~~LCD1_VDD_EN~~
S117	~~LVDS1_2+~~ / ~~eDP1_TX2+~~ / ~~DSI1_D2+~~
S118	~~LVDS1_2-~~ / ~~eDP1_TX2-~~ / ~~DSI1_D2-~~
S119	GND
S120	~~LVDS1_3+~~ / ~~eDP1_TX3+~~ / ~~DSI1_D3+~~
S121	~~LVDS1_3-~~ / ~~eDP1_TX3-~~ / ~~DSI1_D3-~~
S122	~~LCD1_BKLT_PWM~~
S123	GPIO13
S124	GND
S125	LVDS0_0+ / ~~eDP0_TX0+~~ / DSI0_D0+
S126	LVDS0_0- / ~~eDP0_TX0-~~ / DSI0_D0-
S127	LCD0_BKLT_EN
S128	LVDS0_1+ / ~~eDP0_TX1+~~ / DSI0_D1+
S129	LVDS0_1- / ~~eDP0_TX1-~~ / DSI0_D1-
S130	GND
S131	LVDS0_2+/ ~~eDP0_TX2+~~ / DSI0_D2+
S132	LVDS0_2- / ~~eDP0_TX2-~~ / DSI0_D2-
S133	LCD0_VDD_EN
S134	LVDS0_CK+/~~eDP0_AUX~~/ DSI0_CLK+
S135	LVDS0_CK-/~~eDP0_AUX-~~/ DSI0_CLK-
S136	GND
S137	LVDS0_3+ / ~~eDP0_TX3+~~ / DSI0_D3+
S138	LVDS0_3- / ~~eDP0_TX3-~~ / DSI0_D3-
S139	I2C_LCD_CK

P-Pin	Primary (Top) Side
P139	SER2_CTS#
P140	~~SER3_TX~~
P141	~~SER3_RX~~
P142	GND
P147	VDD_IN
P148	VDD_IN
P149	VDD_IN
P150	VDD_IN
P151	VDD_IN
P152	VDD_IN

S-Pin	Secondary (Bottom) Side
S140	I2C_LCD_DAT
S141	LCD0_BKLT_PWM
S142	GPIO12
S143	GND
S148	LID#
S149	SLEEP#
S150	VIN_PWR_BAD#
S151	~~CHARGING#~~
S152	~~CHARGER_PRSNT#~~
S153	CARRIER_STBY#

P-Pin	Primary (Top) Side
P143	CAN0_TX
P144	CAN0_RX
P145	~~CAN1_TX~~
P146	~~CAN1_RX~~
P153	VDD_IN
P154	VDD_IN
P155	VDD_IN
P156	VDD_IN

S-Pin	Secondary (Bottom) Side
S144	~~eDP0_HPD~~ / ~~DSI0_TE~~
S145	WDT_TIME_OUT#
S146	~~PCIE_WAKE#~~
S147	~~VDD_RTC~~
S154	CARRIER_PWR_ON
S155	FORCE_RECOV#
S156	BATLOW#
S157	TEST#
S158	GND

Note: ~~STRIKETHROUGH~~ strike-through entries are not supported functions on this product

Note: Both LVDS0 and DSI0 (default) are supported, either function can be enabled at boot time in the DTS (Device Tree)

4.2 Signal Terminology Descriptions

Meaning of the terms used for signal description tables

Term	Description
I	Input to the module
O	Output from the module
O OD	Open drain output from the module
I OD	Open drain input to the module, with mandatory PU (pull up) on module
OD	Open drain
I/O	Bi-directional Input/Output
PU	PU (pull-up) resistor on module
PD	PD (pull-down) resistor on module
VDD_IN	Main power source from carrier to module
CMOS	Logic input or output
GBE MDI	Differential analog signaling for Gigabit Media Dependent Interface
LVDS DP	Low Voltage Differential Signal for DisplayPort interface
LVDS D-PHY	Low Voltage Differential Signal for MIPI CSI-2 cameras and DSI displays
LVDS M-PHY	Low Voltage Differential Signal for MIPI CSI-3 cameras
LVDS LCD	Low Voltage Differential Signal for LCD displays
LVDS PCIE	Low Voltage Differential Signal for PCIe
LVDS SATA	Low Voltage Differential Signal for SATA
TMDS HDMI	Transition Minimized Differential Signal for HDMI displays
USB	DC coupled differential signaling for traditional (non-Superspeed) USB signals
USB SS	Differential signal for SuperSpeed USB signals
USB VBUS 5V	5V tolerant input for USB VBUS detection
3.3V	3.3V Power Domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
1.8V	1.8V Power Domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
3.3Vsb	3.3V Power Domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)
1.8Vsb	1.8V Power Domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)

4.3 Signal Description by function

4.3.1 The First Display Interface

This is a group of 30-pins that is split into a channel 0 and channel 1 and can support either dual channel LVDS ports, 2 separate single channel LVDS ports, 2 MIPI DSI ports of 4 lanes each or 2 eDP ports 4 lanes each. A mix of different display type such as DSI and eDP is also permitted.

Pin #	LVDS Name	MIPI DSI Name	eDP Name
S125	LVDS0_0+	DSI0_D0+	~~eDP0_TX0+~~
S126	LVDS0_0-	DSI0_D0-	~~eDP0_TX0-~~
S128	LVDS0_1+	DSI0_D1+	~~eDP0_TX1+~~
S129	LVDS0_1 -	DSI0_D1-	~~eDP0_TX1-~~
S131	LVDS0_2+	DSI0_D2+	~~eDP0_TX2+~~
S132	LVDS0_2-	DSI0_D2-	~~eDP0_TX2-~~
S137	LVDS0_3+	DSI0_D3+	~~eDP0_TX3+~~
S138	LVDS0_3-	DSI0_D3-	~~eDP0_TX3-~~
S134	LVDS0_CK+	DSI0_CLK+	~~eDP0_AUX+~~
S135	LVDS0_CK-	DSI0_CLK-	~~eDP0_AUX-~~
S133	LCD0_VDD_EN	LCD0_VDD_EN	~~LCD0_VDD_EN~~
S127	LCD0_BKLT_EN	LCD0_BKLT_EN	~~LCD0_BKLT_EN~~
S141	LCD0_BKLT_PWM	LCD0_BKLT_PWM	~~LCD0_BKLT_PWM~~
S144		DSI0_TE	~~eDP0_HPD~~
S139	I2C_LCD_CK	I2C_LCD_CK	~~I2C_LCD_CK~~
S140	I2C_LCD_DAT	I2C_LCD_DAT	~~I2C_LCD_DAT~~

Pin #	LVDS Name	MIPI DSI Name	eDP Name
S111	~~LVDS1_0+~~	~~DSI1_D0+~~	~~eDP1_TX0+~~
S112	~~LVDS1_0-~~	~~DSI1_D0-~~	~~eDP1_TX0-~~
S114	~~LVDS1_1+~~	~~DSI1_D1+~~	~~eDP1_TX1+~~
S115	~~LVDS1_1 -~~	~~DSI1_D1-~~	~~eDP1_TX1-~~
S117	~~LVDS1_2+~~	~~DSI1_D2+~~	~~eDP1_TX2+~~
S118	~~LVDS1_2-~~	~~DSI1_D2-~~	~~eDP1_TX2-~~
S120	~~LVDS1_3+~~	~~DSI1_D3+~~	~~eDP1_TX3+~~
S121	~~LVDS1_3-~~	~~DSI1_D3-~~	~~eDP1_TX3-~~
S108	~~LVDS1_CK+~~	~~DSI1_CLK+~~	~~eDP1_AUX+~~
S109	~~LVDS1_CK-~~	~~DSI1_CLK-~~	~~eDP1_AUX-~~
S116	~~LCD1_VDD_EN~~	~~LCD1_VDD_EN~~	~~LCD1_VDD_EN~~
S107	~~LCD1_BKLT_EN~~	~~LCD1_BKLT_EN~~	~~LCD1_BKLT_EN~~
S122	~~LCD1_BKLT_PWM~~	~~LCD1_BKLT_PWM~~	~~LCD1_BKLT_PWM~~
S113		~~DSI1_TE~~	~~eDP1_HPD~~

Above tables for LVDS, DSI and eDP describe signals that are supported on this product. Unsupported signals are crossed out (~~STRIKETHROUGH~~) or in case multiplexed (either or) this will be described in the NOTES of the signal description tables by type.

Note: DSI0 mode or LVDS0 can be selected at boot time through DVT (device tree), DSI0 is default

4.3.1.1 LVDS0 mode

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
LVDS0_0+ LVDS0_0- LVDS0_1+ LVDS0_1 - LVDS0_2+ LVDS0_2- LVDS0_3+ LVDS0_3-	S125 S126 S128 S129 S131 S132 S137 S138	Primary LVDS channel differential pair data lines	O LVDS LCD		Runtime		
LVDS0_CK+ LVDS0_CK-	S134 S135	Primary LVDS channel differential pair clock lines	O LVDS LCD		Runtime		
LCD0_VDD_EN	S133	Primary LVDS channel power enable, active high	O CMOS	1.8V	Runtime		
LCD0_BKLT_EN	S127	Primary LVDS channel backlight enable, active high	O CMOS	1.8V	Runtime		
LCD0_BKLT_PWM	S141	Primary LVDS channel brightness control through pulse width modulation (PWM)	O CMOS	1.8V	Runtime		
I2C_LCD_DAT	S140	DDC data line used for flat panel detection and control	I/O OD CMOS	1.8V	Runtime	PU 2k2	
I2C_LCD_CK	S139	DDC clock line used for flat panel detection and control	O OD CMOS	1.8V	Runtime	PU 2k2	

4.3.1.2 DSI0 mode

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
DSI0_D0+ DSI0_D0- DSI0_D1+ DSI0_D1- DSI0_D2+ DSI0_D2- DSI0_D3+ DSI0_D3-	S125 S126 S128 S129 S131 S132 S137 S138	Primary DSI panel differential pair data lines	O LVDS D-PHY		Runtime		
DSI0_CLK+ DSI0_CLK-	S134 S135	Primary DSI panel differential pair clock lines.	O LVDS D-PHY		Runtime		
LCD0_VDD_EN	S133	Primary panel power enable, active high	O CMOS	1.8V	Runtime		
LCD0_BKLT_EN	S127	Primary panel backlight enable, active high	O CMOS	1.8V	Runtime		
LCD0_BKLT_PWM	S141	Primary panel brightness control through pulse width modulation (PWM)	O CMOS	1.8V	Runtime		
DSI0_TE	S144	Primary DSI panel tearing effect sigal	I CMOS	1.8V	Runtime		
I2C_LCD_DAT	S140	DDC data line used for flat panel detection and control	I/O OD CMOS	1.8V	Runtime	PU 2k2	
I2C_LCD_CK	S139	DDC clock line used for flat panel detection and control	O OD CMOS	1.8V	Runtime	PU 2k2	

4.3.2 Second & Third Display Interface

All the below signals on Second Interface are not supported

Pin #	HDMI signal names	DP++ signal names
P92 P93 P95 P96 P98 P99	~~HDMI_D2+~~ ~~HDMI_D2-~~ ~~HDMI_D1+~~ ~~HDMI_D1-~~ ~~HDMI_D0+~~ ~~HDMI_D0-~~	~~DP1_LANE0+~~ ~~DP1_LANE0-~~ ~~DP1_LANE1+~~ ~~DP1_LANE1-~~ ~~DP1_LANE2+~~ ~~DP1_LANE2-~~
P101 P102	~~HDMI_CK+~~ ~~HDMI_CK-~~	~~DP1_LANE3+~~ ~~DP1_LANE3-~~
S105	~~HDMI_CTRL_CK~~	~~DP1_AUX+~~
S106	~~HDMI_CTRL_DAT~~	~~DP1_AUX-~~
P104	~~HDMI_HPD~~	~~DP1_HPD~~
P107	-	~~DP1_AUX_SEL~~

All the below signals on Third Interface are not supported

Pin #	DP++ signal names
P92 P93 P95 P96 P98 P99	~~DP0_LANE0+~~ ~~DP0_LANE0-~~ ~~DP0_LANE1+~~ ~~DP0_LANE1-~~ ~~DP0_LANE2+~~ ~~DP0_LANE2-~~
P101 P102	~~DP0_LANE3+~~ ~~DP0_LANE3-~~
S105	~~DP0_AUX+~~
S106	~~DP0_AUX-~~
P104	~~DP0_HPD~~
P107	~~DP0_AUX_SEL~~

Note: HDMI support with a resolution of up to 1920x1080 can be implemented through a DSI to HDMI on the IPi-SMARC carrier, a reference design based on Analog Devices' ADV7533 MIPI/DSI Receiver with HDMI Transmitter is available on request

4.3.3 MIPI Cameras

4.3.3.1 MIPI CSI0

Not supported

4.3.3.2 MIPI CSI1

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CSI1_RX0+ CSI1_RX0- CSI1_RX1+ CSI1_RX1- CSI1_RX2+ CSI1_RX2- CSI1_RX3+ CSI1_RX3-	P7 P8 P10 P11 P13 P14 P16 P17	CSI1 differential input (point to point)	I LVDS D-PHY / I LVDS M-PHY		Runtime		
CSI1_CK+ CSI1_CK-	P3 P4	CSI1 differential clock input (point to point)	I LVDS D-PHY		Runtime		
I2C_CAM1_DAT / CSI1_TX-	S2	I2C data for serial camera data support link or differential data lane	I/O OD CMOS / O LVDS M-PHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 mode uses I2C_CAM1_DAT MIPI-CSI 3.0 mode uses CSI1_TX-
I2C_CAM1_CK / CSI1_TX+	S1	I2C clock for serial camera data support link or differential data lane	O OD CMOS / O LVDS M-PHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 mode uses I2C_CAM1_CK MIPI-CSI 3.0 mode uses CSI1_TX+
CAM1_PWR# / GPIO1	P109	Camera 0 Power Enable, active low output.	O CMOS	1.8V	Runtime		CAM1_PWR# is default, GPIO1 can be enabled through DVT
CAM1_RST# / GPIO3	P111	Camera 0 reset, active low output	O CMOS	1.8V	Runtime		CAM1_PWR# is default, GPIO3 can be enabled through DVT
CAM_MCK	S6	Master clock output	O CMOS	1.8V	Runtime		

4.3.4 Audio

4.3.4.1 I2S0 / I2S2

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
I2S0_LRCK	S39	I2S0 Left & Right synchronization clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
I2S0_SDOUT	S40	I2S0 Digital audio Output	O CMOS	1.8V	Runtime		
I2S0_SDIN	S41	I2S0 Digital audio Input	I CMOS	1.8V	Runtime		
I2S0_CK	S42	I2S0 Digital audio clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
I2S2_LRCK / ~~HDA_SYNC~~	S50	I2S2 Left & Right synchronization clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
I2S2_SDOUT/ ~~HDA_SDO~~	S51	I2S2 Digital audio Output	O CMOS	1.8V	Runtime		
I2S2_SDIN/ ~~HDA_SDI~~	S52	I2S2 Digital audio Input	I CMOS	1.8V	Runtime		
I2S2_CK/ ~~HDA_CK~~	S53	I2S2 Digital audio clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
AUDIO_MCK	S38	Master clock output to I2S codec(s)	O CMOS	1.8V	Runtime		

Note: I2S1 signalling has been removed during update to SMARC 2.0 specification

4.3.5 USB

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
USB0+ USB0-	P60 P61	USB differential data pairs for port 0	I/O USB	USB	Runtime		From SOC
~~USB0_EN_OC#~~	P62	~~USB over-current sense for port 0~~	~~I/O OD CMOS~~	~~3.3Vsb / 3.3V~~	Runtime	~~PU 10k~~	~~Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.~~
USB0_VBUS_DET	P63	USB port 0 host power detection, when this port is used as a device.	I USB VBUS 5V	USB VBUS 5V	Runtime		Can be connected to a USB client port VBUS pin
USB0_OTG_ID	P64	Input pin to announce OTG device insertion on USB 2.0 port	I CMOS	3.3Vsb / 3.3V	Runtime		
USB1+ USB1-	P65 P66	USB differential data pairs for port 1	I/O USB	USB	Runtime		From USB HUB, alternatively USB HUB can be removed, and USB 2.0 Host directly routed to SOC
USB1_EN_OC#	P67	USB over-current sense for port 1	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB2+ USB2-	P69 P70	USB differential data pairs for port 2	I/O USB	USB	Runtime		From USB HUB
~~USB2_SSRX+~~ ~~USB2_SSRX-~~	~~S74~~ ~~S75~~	~~Receive signal differential pairs for SuperSpeed on port 2~~	~~I~~ ~~USB SS~~	~~USB SS~~	Runtime	-	USB 3.0 mode not supported
~~USB2_SSTX+~~ ~~USB2_SSTX-~~	~~S71~~ ~~S72~~	~~Transmit signal differential pairs for SuperSpeed on port 2~~	~~O~~ ~~USB SS~~	~~USB SS~~	Runtime	-	USB 3.0 mode not supported
USB2_EN_OC#	P71	USB over-current sense for port 2	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.

USB3+ USB3-	S68 S69	USB differential data pairs for port 3	I/O USB	USB	Runtime		From USB HUB
~~USB3_SSRX+~~ ~~USB3_SSRX-~~	~~S65~~ ~~S66~~	~~Receive signal differential pairs for SuperSpeed on port 3~~	~~I~~ ~~USB SS~~	~~USB SS~~	Runtime		USB 3.0 mode not supported
~~USB3_SSTX+~~ ~~USB3_SSTX-~~	~~S62~~ ~~S63~~	~~Transmit signal differential pairs for SuperSpeed on port 3~~	~~O~~ ~~USB SS~~	~~USB SS~~	Runtime		USB 3.0 mode not supported
USB3_EN_OC#	P74	USB over-current sense for port 3	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
~~USB3_VBUS_DET~~	S37	~~USB port 3 host power detection, when this port is used as a device.~~	~~I~~ ~~USB VBUS 5V~~	~~USB VBUS 5V~~	Runtime		
~~USB3_OTG_ID~~	S104	~~Input pin to announce OTG device insertion on USB 3.0 port~~	~~I~~ ~~CMOS~~	~~3.3Vsb / 3.3V~~	Runtime		
USB4+ USB4-	S35 S36	USB differential data pairs for port 4	I/O USB	USB	Runtime		From USB HUB
USB4_EN_OC#	P76	USB over-current sense for port 4	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.

Note: USB 3 & 4 ports will only be active in final design

4.3.6 PCIe and SerDes pin sharing

4.3.6.1 PCIe Ports

This design does not support PCIe ports

4.3.7 SATA

This design does not support SATA ports

4.3.8 LAN

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- ~~GBE0_MDI2+~~ ~~GBE0_MDI2-~~ ~~GBE0_MDI3+~~ ~~GBE0_MDI3-~~	P30 P29 P27 P26 P24 P23 P20 P19	10/100 Mbps Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1. The MDI can operate in 100, and 10Mbit/sec modes. 100 10 MDI[0]+/- TX+/- TX+/- MDI[1]+/- RX+/- RX+/-	GBE MDI		Runtime		Twisted pair signals for external transformer.
GBE0_LINK100#	P21	Link Speed Indication LED for GBE 0 100Mbps	O OD CMOS	3.3V	Runtime		Shall be able to sink 24mA or more Carrier LED current
~~GBE0_LINK1000#~~	P22	~~Link Speed Indication LED for GBE 0 1000Mbps~~	O OD CMOS	3.3V	Runtime		Shall be able to sink 24mA or more Carrier LED current
GBE0_LINK_ACT#	P25	Link / Activity Indication LED Driven low on Link (10, 100 mbps) Blinks on Activity	O OD CMOS	3.3V	Runtime		Shall be able to sink 24mA or more Carrier LED current
GBE0_CTREF	P28	Center-Tap reference voltage for Carrier board Ethernet magnetic (if required by the Module GBE PHY)	Analog	0 to 3.3V max	Runtime		
~~GBE0_SDP~~	P6	~~IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol)~~	~~IO CMOS~~	~~3.3V~~	Runtime	-	-
GBE1_MDI0+ GBE1_MDI0- GBE1_MDI1+ GBE1_MDI1- ~~GBE1_MDI2+~~ ~~GBE1_MDI2-~~ ~~GBE1_MDI3+~~ ~~GBE1_MDI3-~~	S17 S18 S20 S21 S23 S24 S26 S27	10/100 Mbps Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1. The MDI can operate in 100, and 10Mbit/sec modes. 100 10 MDI[0]+/- TX+/- TX+/- MDI[1]+/- RX+/- RX+/-	GBE MDI		Standby		Twisted pair signals for external transformer.

GBE1_LINK100#	S19	Link Speed Indication LED for GBE 1 100Mbps	O OD CMOS	3.3V	Runtime		Shall be able to sink 24mA or more Carrier LED current
~~GBE1_LINK1000#~~	S22	~~Link Speed Indication LED for GBE 1 1000Mbps~~	O OD CMOS	3.3V	Runtime		Shall be able to sink 24mA or more Carrier LED current
GBE1_LINK_ACT#	S31	Link / Activity Indication LED Driven low on Link (10, 100 mbps) Blinks on Activity	O OD CMOS	3.3V	Runtime		Shall be able to sink 24mA or more Carrier LED current
GBE1_CTREF	S28	Center-Tap reference voltage for Carrier board Ethernet magnetic \`(if required by the Module GBE PHY)\`	Analog	0 to 3.3V max	Runtime		
~~GBE1_SDP~~	P5	~~IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol)~~	IO CMOS	3.3V	Runtime		

4.3.9 SDIO

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SDIO_D0 SDIO_D1 SDIO_D2 SDIO_D3	P39 P40 P41 P42	SDIO Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
SDIO_WP	P33	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I OD CMOS	3.3V	Runtime	PU 10k	Pulled up on module
SDIO_CMD	P34	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
SDIO_CD#	P35	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	I OD CMOS	3.3V	Runtime	PU 10k	Pulled up on module
SDIO_CK	P36	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	O CMOS	1.8V or 3.3V	Runtime		
SDIO_PWR_EN	P37	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	O CMOS	3.3V	Runtime		should be driven low in STB Mode by the module

4.3.10

4.3.11 SPI

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SPI0_CS0#	P43	SPI0 Master Chip Select 0	O CMOS	1.8V	Runtime		This signal can be used to select carrier SPI as boot device
~~SPI0_CS1#~~	P31	~~SPI0 Master Chip Select 1~~	~~O CMOS~~	~~1.8V~~	Runtime		
SPI0_CK	P44	SPI0 Clock	O CMOS	1.8V	Runtime		
SPI0_DIN	P45	SPI0 Master input / Slave output	I CMOS	1.8V	Runtime		also referred to as MISO
SPI0_DO	P46	SPI0 Master output / Slave input	O CMOS	1.8V	Runtime		also referred to as MOSI
SPI1_CS0#	P54	SPI1 Master Chip Select 0	O CMOS	1.8V	Runtime		
SPI1_CS1#	P55	SPI1 Master Chip Select 1	O CMOS	1.8V	Runtime		
SPI1_CK	P56	SPI1 Clock	O CMOS	1.8V	Runtime		
SPI1_DIN	P57	SPI1 Master input / Slave output	I CMOS	1.8V	Runtime		also referred to as MISO
SPI1_DO	P58	SPI1 Master output / Slave input	O CMOS	1.8V	Runtime		also referred to as MOSI

Note: SPI0 is free to use on the carrier but support only one device through CS0

SPI1 supports a CAN bus controller on the module through CS0, that leaves CS1 free for a device on the carrier

4.3.12 GPIO

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GPIO0 / ~~CAM0_PWR#~~	P108	General purpose I/O pin 0.	I/O CMOS	1.8V	Runtime	PU 470K on the Module.	Camera 0 is not supported
GPIO1 / ~~CAM1_PWR#~~	P109	General purpose I/O pin 1.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	Default use is is GPIO1 alternative use is Camera 1 Power Enable - active low, through DTS
GPIO2 / CAM0_RST#	P110	General purpose I/O pin 2.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	Camera 0 is not supported
GPIO3 / CAM1_RST#	P111	General purpose I/O pin 3.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	Default use is GPIO3, alternative use is Camera 1 Reset - active low, through DTS
GPIO4 / ~~HDA_RST#~~	P112	General purpose I/O pin 4.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO5 / PWM_OUT	P113	General purpose I/O pin 5.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	Default is GPIO mode, alternate use is PWM output
GPIO6	P114	General purpose I/O pin 6.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO7	P115	General purpose I/O pin 7.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO8	P116	General purpose I/O pin 8.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO9	P117	General purpose I/O pin 9.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO10	P118	General purpose I/O pin 10.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO11	P119	General purpose I/O pin 11.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO12	S142	General purpose I/O pin 12	I/O CMOS	1.8V	Runtime	PU 470K on the Module	advised as INT signal to I2C GPIO expander on carrier.
GPIO13	S123	General purpose I/O pin 13	I/O CMOS	1.8V	Runtime	PU 470K on the Module	

4.3.13 UART

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SER0_TX	P129	Asynchronous serial data output port 0	O CMOS	1.8V	Runtime		
SER0_RX	P130	Asynchronous serial data input port 0	I CMOS	1.8V	Runtime		
SER0_RTS#	P131	"Request to Send" handshake line for port 0	O CMOS	1.8V	Runtime		
SER0_CTS#	P132	"Clear to Send" handshake line for port 0	I CMOS	1.8V	Runtime		
~~SER1_TX~~	P134	~~Asynchronous serial data output port 1~~	~~O CMOS~~	~~1.8V~~	~~Runtime~~		
~~SER1_RX~~	P135	~~Asynchronous serial data input port 1~~	~~I CMOS~~	~~1.8V~~	~~Runtime~~		
SER2_TX	P136	Asynchronous serial data output port 2	O CMOS	1.8V	Runtime		
SER2_RX	P137	Asynchronous serial data input port 2	I CMOS	1.8V	Runtime		
SER2_RTS#	P138	"Request to Send" handshake line for port 2	O CMOS	1.8V	Runtime		
SER2_CTS#	P139	"Clear to Send" handshake line for port 2	I CMOS	1.8V	Runtime		
~~SER3_TX~~	P140	~~Asynchronous serial data output port 3~~	~~O CMOS~~	~~1.8V~~	~~Runtime~~		
~~SER3_RX~~	P141	~~Asynchronous serial data input port 3~~	~~I CMOS~~	~~1.8V~~	~~Runtime~~		

4.3.14 CAN bus

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CAN0_TX	P143	CAN port 0 Transmit output	O CMOS	1.8V	Runtime		
CAN0_RX	P144	CAN port 0 Receive input	I CMOS	1.8V	Runtime		
~~CAN1_TX~~	P145	~~CAN port 1 Transmit output~~	~~O CMOS~~	~~1.8V~~	~~Runtime~~		
~~CAN1_RX~~	P146	~~CAN port1 Receive input~~	~~I CMOS~~	~~1.8V~~	~~Runtime~~		

4.3.15 Miscellaneous

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
TEST#	S157	Held low by Carrier to invoke Module vendor specific test function(s).	I CMOS	[1.8 to 5]Vsb / 5.25V	Runtime	PU on Module. Driven by OD on Carrier	Module must implement PU but actual value is depended on particular module design. Carrier Board should leave this pin floating for normal operation
WDT_TIME_OUT#	S145	Watch-Dog-Timer Output, low active.	O CMOS	1.8V	Runtime		Driven only during runtime
PWM_OUT / GPIO5	P113	Pulse Width Modulation (PWM) output	I/O CMOS	1.8V	Runtime	PU 470K on the Module	GPIO5 is the default pin configuration

4.3.16 Power and System Management

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
BATLOW#	S156	Battery low indication to Module. Carrier to float the line in inactive state.	I OD CMOS	TBD	Runtime	PU 4.7K	Driven by OD on Carrier. Pulled up on module.
CARRIER_PWR_ON	S154	Carrier board circuits (apart from power management and power path circuits) should not be powered up until the Module asserts the CARRIER_PWR_ON signal.	O CMOS	TBD	-		On x86 designs this pin should utilize the RSM_RST# signal.
CARRIER_STBY#	S153	The Module shall drive this signal low when the system is in a standby power state.	O CMOS	TBD	-		On x86 designs this pin should utilize the SUS_S3# signal.
CHARGER_PRSNT#	S152	Held low by Carrier if DC input for battery charger is present.	I OD CMOS	TBD	Standby	PU 100K	Driven by OD on Carrier. Pulled up on module.
CHARGING#	S151	Held low by Carrier during battery charging. Carrier to float the line when charge is complete.	I OD CMOS	TBD	Standby	PU 68K	Driven by OD on Carrier. Pulled up on module.
VIN_PWR_BAD#	S150	Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) shall not be enabled while this signal is held low by the Carrier.	I OD CMOS	TBD	Standby	PU 10K	Driven by OD on Carrier Module must implement PU but actual value is depended on particular module design.
SLEEP#	S149	Sleep indicator from Carrier board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state.Active low, level sensitive. Should be de-bounced on the Module.	I OD CMOS	TBD	Standby	PU 4.7K	Driven by OD on Carrier. Pulled up on module.
LID#	S148	Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module.	I OD CMOS	TBD	Standby	PU 4.7K	Driven by OD on Carrier. Pulled up on module.
POWER_BTN#	P128	Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module.	I OD CMOS	TBD	Standby	PU 10K	Driven by OD on Carrier. Pulled up on module.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
RESET_OUT#	P126	General purpose reset output to Carrier board.	O CMOS	TBD	Standby	PU 10K	
RESET_IN#	P127	Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise.	I OD CMOS	TBD	Standby	PU 10K	Driven by OD on Carrier. Pulled up on module.
I2C_PM_DAT	P122	Power management I2C bus DATA	I/O OD CMOS	TBD	Standby	PU 2.2K	On x86 systems these serve as SMB DATA. Pulled up on module.
I2C_PM_CK	P121	Power management I2C bus CLK	O OD CMOS	TBD	Standby	PU 2.2K	On x86 systems these serve as SMB CLK. Pulled up on module.
~~SMB_ALERT_1V8#~~	P1	~~SMBus Alert# (interrupt) signal~~	~~I OD CMOS~~	TBD	~~Standby~~	~~PU 2.2K~~	~~only used on x86 design~~

4.3.17 Boot Select

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
BOOT_SEL0# BOOT_SEL1# BOOT_SEL2#	P123 P124 P125	Input straps determine the Module boot	I OD CMOS	1.8V	Standby	PU 4.7K	Driven by OD on Carrier. Pulled up on module. Only booting from EMMC and SDcard is supported
~~FORCE_RECOV#~~	S155		~~I OD~~ ~~CMOS~~	~~1.8V~~	~~Runtime~~	~~PU 10K~~ -	~~Driven by OD on Carrier.~~ ~~Pulled up on module.~~ ~~Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based Force Recovery functions, then a low on the Module FORCE_RECOV# pin may invoke the SOC native Force Recovery mode – such as over a Serial Port. For x86 systems this signal may be used to load BIOS defaults. Pulled up on Module. Driven by OD part on Carrier.~~

4.3.18 Power

Name	Pin #	Description	I/O Type	Power Rail / Tolerance	PU / PD	Comments
VDD_IN	P147, P148, P149, P150, P151, P152, P153, P154, P155, P156	Module power input voltage 4.75 min to 5.25V max	P Not defined within Signal Terminolgy Descriptions. Should we define a specific rail?	4.75V to 5.25V / 5V		
GND	P2, P9, P12, P15, P18, P32, P38, P47, P50, P53, P59, P68, P79, P82, P85, P88, P91, P94, P97, P100, P103, P120, P133, P142, S3, S10, S16, S25, S34, S47, S61, S64, S67, S70, S73, S80, S83, S86, S89, S92, S101, S110, S119, S124, S130, S136, S143, S158	Module signal and power return, and GND reference	P Not defined within Signal Terminolgy Descriptions. Should we define a specific rail?	Ground		
VDD_RTC	S147	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based Lithium cell or Super Cap.	P Not defined within Signal Terminolgy Descriptions. Should we define a specific rail?	[2 to 3.25] / 3.25V		

4.4 SMARC pin to controller mapping

Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	I/O Mux default	Power Rail
P1	SMB_ALERT_1V8#	-	-	-	-	-	-	-
P2	GND	-	-	-	-	-	-	-
P3	CSI1_CK+	In	-	CSI	PX30	MIPI_CSI_CLKP	-	VCC_1V0
P4	CSI1_CK-	In	-	CSI	PX30	MIPI_CSI_CLKN	-	VCC_1V0
P5	GBE1_SDP	-	-	-	-		-	-
P6	GBE0_SDP	-	-	-	-		-	-
P7	CSI1_RX0+	In	-	CSI	PX30	MIPI_CSI_DP0	-	VCC_1V0
P8	CSI1_RX0-	In	-	CSI	PX30	MIPI_CSI_DN0	-	VCC_1V0
P9	GND	-	-	-	-		-	-
P10	CSI1_RX1+	In	-	CSI	PX30	MIPI_CSI_DP1	-	VCC_1V0
P11	CSI1_RX1-	In	-	CSI	PX30	MIPI_CSI_DN1	-	VCC_1V0
P12	GND	-	-	-	-		-	-
P13	CSI1_RX2+	In	-	CSI	PX30	MIPI_CSI_DP2	-	VCC_1V0
P14	CSI1_RX2-	In	-	CSI	PX30	MIPI_CSI_DN2	-	VCC_1V0
P15	GND	-	-	-	-	-	-	-
P16	CSI1_RX3+	In	-	CSI	PX30	MIPI_CSI_DP3	-	VCC_1V0
P17	CSI1_RX3-	In	-	CSI	PX30	MIPI_CSI_DN3	-	VCC_1V0
P18	GND	-	-	-	-	-	-	-
P19	GBE0_MDI3-	-	-	-	-	-	-	-
P20	GBE0_MDI3+	-	-	-	-	-	-	-
P21	GBE0_LINK100#	Out/OD	-	-	DP83822	LED_1	-	VCC3V3_SYS
P22	GBE0_LINK1000#	-	-	-	-	-	-	-
P23	GBE0_MDI2-	-	-	-	-	-	-	-
P24	GBE0_MDI2+	-	-	-	-	-	-	-
P25	GBE0_LINK_ACT#	Out/OD	-	-	DP83822	LED_0	-	VCC3V3_SYS
P26	GBE0_MDI1-	Bi-Dir	-	-	DP83822	RD_M	-	3.3VA1
P27	GBE0_MDI1+	Bi-Dir	-	-	DP83822	RD_P	-	3.3VA1

P28	GBE0_CTREF	-	-	-	-	-	-	-
P29	GBE0_MDI0-	Bi-Dir	-	-	DP83822	TD_M	-	3.3VA1
P30	GBE0_MDI0+	Bi-Dir	-	-	DP83822	TD_P	-	3.3VA1
P31	SPI0_CS1#	-	-	-	-	-	-	-
P32	GND	-	-	-	-	-	-	-
P33	SDIO_WP	In	-	CMOS/ VDD_IO	PX30	GPIO0_A5_d	ALT6/ALT6	VCC3V0_PMU
P34	SDIO_CMD	Bi-Dir	-	CMOS/ VDD_IO	PX30	SDMMC0_CMD	ALT0/ALT0	VCCIO_SD_1V8
P35	SDIO_CD#	In	-	CMOS/ VDD_IO	PX30	SDMMC0_DETN	ALT6/ALT6	VCC3V0_PMU
P36	SDIO_CK	Out	-	CMOS/ VDD_IO	PX30	SDMMC0_CLKO	ALT0/ALT0	VCCIO_SD_1V8
P37	SDIO_PWR_EN	Out	-	CMOS/ VDD_IO	PX30	GPIO0_A2_d	ALT6/ALT6	VCC3V0_PMU
P38	GND	-	-	-	-	-	-	-
P39	SDIO_D0	Bi-Dir	-	CMOS/ VDD_IO	PX30	SDMMC0_D0	ALT0/ALT0	VCCIO_SD_1V8
P40	SDIO_D1	Bi-Dir	-	CMOS/ VDD_IO	PX30	SDMMC0_D1	ALT0/ALT0	VCCIO_SD_1V8
P41	SDIO_D2	Bi-Dir	-	CMOS/ VDD_IO	PX30	SDMMC0_D2	ALT0/ALT0	VCCIO_SD_1V8
P42	SDIO_D3	Bi-Dir	-	CMOS/ VDD_IO	PX30	SDMMC0_D3	ALT0/ALT0	VCCIO_SD_1V8
P43	SPI0_CS0#	Out	-	CMOS/ VDD_IO	PX30	SPI0_CSN	ALT2/ALT2	VCCIO_FLASH
P44	SPI0_CK	Out	-	CMOS/ VDD_IO	PX30	SPI0_CLK	ALT2/ALT2	VCCIO_FLASH
P45	SPI0_DIN	In	-	CMOS/ VDD_IO	PX30	SPI0_RXD	ALT2/ALT2	VCCIO_FLASH
P46	SPI0_DO	Out	-	CMOS/ VDD_IO	PX30	SPI0_TXD	ALT2/ALT2	VCCIO_FLASH
P47	GND	-	-	-	-	-	-	-
P48	SATA_TX+	-	-	-	-	-	-	-
P49	SATA_TX-	-	-	-	-	-	-	-
P50	GND	-	-	-	-	-	-	-
P51	SATA_RX+	-	-	-	-	-	-	-
P52	SATA_RX-	-	-	-	-	-	-	-
P53	GND	-	-	-	-	-	-	-
P54	ESPI_CS0# / SPI1_CS0#	Out	-	CMOS/ VDD_IO	PX30	SPI1_CSN0	ALT2/ALT2	VCC1V8_DVP
P55	ESPI_CS1# / SPI1_CS1#	Out	-	CMOS/ VDD_IO	PX30	SPI1_CSN1	ALT2/ALT2	VCC1V8_DVP
P56	ESPI_CK / SPI1_CK	Out	-	CMOS/ VDD_IO	PX30	SPI1_CLK	ALT2/ALT2	VCC1V8_DVP
P57	ESPI_IO_1 / SPI1_DIN	In	-	CMOS/ VDD_IO	PX30	SPI1_MISO	ALT2/ALT2	VCC1V8_DVP
P58	ESPI_IO_0 / SPI1_DO	Out	-	CMOS/ VDD_IO	PX30	SIP1_MOSI	ALT2/ALT2	VCC1V8_DVP
P59	GND	-	-	-	-	-	-	-
P60	USB0+	Bi-Dir	-	USB	PX30	OTG_DP	-	USB_AVDD

P61	USB0-	Bi-Dir	-	USB	PX30	OTG_DM	-	USB_AVDD
P62	USB0_EN_OC#	In	PU-10K	CMOS/ VDD_IO	PX30	GPIO0_A1_d	-	VCC3V0_PMU
P63	USB0_VBUS_DET	PWR	-	CMOS/ VDD_IO	PX30	USB_DET	-	VCC3V0_PMU
P64	USB0_OTG_ID	In	-	CMOS/ VDD_IO	PX30	USB_ID	-	VCC3V0_PMU
P65	USB1+	Bi-Dir	-	USB	LAN9514	USBDP2	-	-
P66	USB1-	Bi-Dir	-	USB	LAN9514	USBDM2	-	-
P67	USB1_EN_OC#	In	PU-10K	CMOS/ VDD_IO	LAN9514	PRTCTL2	-	+3.3V
P68	GND	-	-	-	-	-	-	-
P69	USB2+	Bi-Dir	-	USB	LAN9514	USBDP3	-	-
P70	USB2-	Bi-Dir	-	USB	LAN9514	USBDM3	-	-
P71	USB2_EN_OC#	Bi-Dir	PU-10K	CMOS/ VDD_IO	LAN9514	PRTCTL3	-	+3.3V
P72	RSVD	-	-	-	-	-	-	-
P73	RSVD	-	-	-	-	-	-	-
P74	USB3_EN_OC#	In	PU-10K	CMOS/ VDD_IO	LAN9514	PRTCTL4	-	+3.3V
P75	PCIE_A_RST#	-	-	-	-	-	-	-
P76	USB4_EN_OC#	In	PU-10K	CMOS/ VDD_IO	LAN9514	PRTCTL5	-	+3.3V
P77	PCIE_B_CKREQ#	-	-	-	-	-	-	-
P78	PCIE_A_CKREQ#	-	-	-	-	-	-	-
P79	GND	-	-	-	-	-	-	-
P80	PCIE_C_REFCK+	-	-	-	-	-	-	-
P81	PCIE_C_REFCK-	-	-	-	-	-	-	-
P82	GND	-	-	-	-	-	-	-
P83	PCIE_A_REFCK+	-	-	-	-	-	-	-
P84	PCIE_A_REFCK-	-	-	-	-	-	-	-
P85	GND	-	-	-	-	-	-	-
P86	PCIE_A_RX+	-	-	-	-	-	-	-
P87	PCIE_A_RX-	-	-	-	-	-	-	-
P88	GND	-	-	-	-	-	-	-
P89	PCIE_A_TX+	-	-	-	-	-	-	-
P90	PCIE_A_TX-	-	-	-	-	-	-	-
P91	GND	-	-	-	-	-	-	-
P92	HDMI_D2+ / DP1_LANE0+	-	-	-	-	-	-	-

P93	HDMI_D2- / DP1_LANE0-	-	-	-	-	-	-	-
P94	GND	-	-	-	-	-	-	-
P95	HDMI_D1+ / DP1_LANE1+	-	-	-	-	-	-	-
P96	HDMI_D1- / DP1_LANE1-	-	-	-	-	-	-	-
P97	GND	-	-	-	-	-	-	-
P98	HDMI_D0+ / DP1_LANE2+	-	-	-	-	-	-	-
P99	HDMI_D0- / DP1_LANE2-	-	-	-	-	-	-	-
P100	GND	-	-	-	-	-	-	-
P101	HDMI_CK+ / DP1_LANE3+	-	-	-	-	-	-	-
P102	HDMI_CK- / DP1_LANE3-	-	-	-	-	-	-	-
P103	GND	-	-	-	-	-	-	-
P104	HDMI_HPD / DP1_HPD	-	-	-	-	-	-	-
P105	HDMI_CTRL_CK / DP1_AUX+	-	-	-	-	-	-	-
P106	HDMI_CTRL_DAT / DP1_AUX-	-	-	-	-	-	-	-
P107	DP1_AUX_SEL	-	-	-	-	-	-	-
P108	GPIO0 / CAM0_PWR#	Bi-Dir	Serial-0R	CMOS/ VDD_IO	PX30	GPIO3_C0_d	ALT5/ALT5	VCC1V8_DVP
P109	GPIO1 / CAM1_PWR#	Bi-Dir	Serial-0R	CMOS/ VDD_IO	PX30	GPIO3_C1_d	ALT5/ALT5	VCC1V8_DVP
P110	GPIO2 / CAM0_RST#	Bi-Dir	Serial-0R	CMOS/ VDD_IO	PX30	GPIO3_C2_d	ALT5/ALT5	VCC1V8_DVP
P111	GPIO3 / CAM1_RST#	Bi-Dir	Serial-0R	CMOS/ VDD_IO	PX30	GPIO3_C3_d	ALT5/ALT5	VCC1V8_DVP
P112	GPIO4 / HDA_RST#	Bi-Dir	PU-470K	CMOS/ VDD_IO	PX30	GPIO3_C4_d	-	VCC1V8_DVP
P113	GPIO5 / PWM_OUT	Bi-Dir	PU-470K	CMOS/ VDD_IO	PX30	GPIO3_C5_d	-	VCC1V8_DVP
P114	GPIO6 / TACHIN	Bi-Dir	PU-470K	CMOS/ VDD_IO	PX30	GPIO3_C6_d	-	VCC1V8_DVP
P115	GPIO7	Bi-Dir	-	CMOS/ VDD_IO	PX30	GPIO3_B2_d	ALT5/ALT5	VCC1V8_DVP
P116	GPIO8	Bi-Dir	PU-470K	CMOS/ VDD_IO	PX30	GPIO_B0_d	-	VCC1V8_DVP
P117	GPIO9	Bi-Dir	PU-470K	CMOS/ VDD_IO	PX30	GPIO3_B5_d	-	VCC1V8_DVP
P118	GPIO10	Bi-Dir	PU-470K	CMOS/ VDD_IO	PX30	GPIO3_D1_d	-	VCC1V8_DVP
P119	GPIO11	Bi-Dir	PU-470K	CMOS/ VDD_IO	PX30	GPIO3_D12_d	-	VCC1V8_DVP
P120	GND	-	-	-	-	-	-	-
P121	I2C_PM_CK	Out	PU-2k2	CMOS/ VDD_IO	PX30	I2C0_SCL	ALT6/ALT6	VCC_1V8
P122	I2C_PM_DAT	Bi-Dir	PU-2k2	CMOS/ VDD_IO	PX30	I2C0_SDA	ALT6/ALT6	VCC_1V8
P123	BOOT_SEL0#	In	PU-4k7	CMOS/ VDD_IO	BMC	PB3	-	+1V8SMC
P124	BOOT_SEL1#	In	PU-4k7	CMOS/ VDD_IO	BMC	PB5	-	+1V8SMC
P125	BOOT_SEL2#	In	PU-4k7	CMOS/ VDD_IO	BMC	PA2	-	+1V8SMC

P126	RESET_OUT#	In	PU-10K	CMOS/ VDD_IO	BMC	P140	-	+1V8SMC
P127	RESET_IN#	In	PU-10K	CMOS/ VDD_IO	BMC	P140	-	+1V8SMC
P128	POWER_BTN#	In	PU-10K	CMOS/ VDD_IO	BMC	P31	-	+1V8SMC
P129	SER0_TX	Out	-	CMOS/ VDD_IO	PX30	UART2_TX_M1	ALT1/ALT1	VCC_RMII
P130	SER0_RX	In	-	CMOS/ VDD_IO	PX30	UART2_RX_M1	ALT1/ALT1	VCC_RMII
P131	SER0_RTS#	-	-	-	-	-	-	-
P132	SER0_CTS#	-	-	-	-	-	-	-
P133	GND	-	-	-	-	-	-	-
P134	SER1_TX	-	-	-	-	-	-	-
P135	SER1_RX	-	-	-	-	-	-	-
P136	SER2_TX	Out	-	CMOS/ VDD_IO	PX30	UART1_TX	ALT4/ALT4	VCC_1V8
P137	SER2_RX	In	-	CMOS/ VDD_IO	PX30	UART1_RX	ALT4/ALT4	VCC_1V8
P138	SER2_RTS#	Out	-	CMOS/ VDD_IO	PX30	UART1_RTS	ALT4/ALT4	VCC_1V8
P139	SER2_CTS#	In	-	CMOS/ VDD_IO	PX30	UART1_CTS	ALT4/ALT4	VCC_1V8
P140	SER3_TX	-	-	-	-	-	-	-
P141	SER3_RX	-	-	-	-	-	-	-
P142	GND	-	-	-	-	-	-	-
P143	CAN0_TX	Out	-	CMOS/ VDD_IO	MCP2517FD	TXCAN_3V3	ALT2/ALT2	VCC1V8_DVP
P144	CAN0_RX	In	-	CMOS/ VDD_IO	MCP2517FD	RXCAN_3V3	ALT2/ALT2	VCC1V8_DVP
P145	CAN1_TX	-	-	-	-	-	-	-
P146	CAN1_RX	-	-	-	-	-	-	-
P147	VDD_IN	-	-	-	-	-	-	-
P148	VDD_IN	-	-	-	-	-	-	-
P149	VDD_IN	-	-	-	-	-	-	-
P150	VDD_IN	-	-	-	-	-	-	-
P151	VDD_IN	-	-	-	-	-	-	-
P152	VDD_IN	-	-	-	-	-	-	-
P153	VDD_IN	-	-	-	-	-	-	-
P154	VDD_IN	-	-	-	-	-	-	-
P155	VDD_IN	-	-	-	-	-	-	-
P156	VDD_IN	-	-	-	-	-	-	-
S1	CSI1_TX+ / I2C_CAM1_CK	Out	-	CMOS/ VDD_IO	PX30	I2C2_SCL	-	VCC_RMII

S2	CSI1_TX- / I2C_CAM1_DAT	Bi-Dir	-	CMOS/ VDD_IO	PX30	I2C2_SDA	-	VCC_RMII
S3	GND	-	-	-	-	-	-	-
S4	RSVD	-	-	-	-	-	-	-
S5	CSI0_TX- / I2C_CAM0_CK	-	-	-	-	-	-	-
S6	CAM_MCK	Out	-	CMOS/ VDD_IO	PX30	GPIO2_B3_d	ALT0/ALT0	VCC_RMII
S7	CSI0_TX+ / I2C_CAM0_DAT	-	-	-	-	-	-	-
S8	CSI0_CK+	-	-	-	-	-	-	-
S9	CSI0_CK-	-	-	-	-	-	-	-
S10	GND	-	-	-	-	-	-	-
S11	CSI0_RX0+	-	-	-	-	-	-	-
S12	CSI0_RX0-	-	-	-	-	-	-	-
S13	GND	-	-	-	-	-	-	-
S14	CSI0_RX1+	-	-	-	-	-	-	-
S15	CSI0_RX1-	-	-	-	-	-	-	-
S16	GND	-	-	-	-	-	-	-
S17	GBE1_MDI0+	Bi-Dir	-	-	LAN9514	TXP	-	-
S18	GBE1_MDI0-	Bi-Dir	-	-	LAN9514	TXN	-	-
S19	GBE1_LINK100#	Out/OD	-	-	LAN9514	nSPD_LED	-	VCC3V3_SYS
S20	GBE1_MDI1+	Bi-Dir	-	-	LAN9514	RXP	-	-
S21	GBE1_MDI1-	Bi-Dir	-	-	LAN9514	RXN	-	-
S22	GBE1_LINK1000#	-	-	-	-	-	-	-
S23	GBE1_MDI2+	-	-	-	-	-	-	-
S24	GBE1_MDI2-	-	-	-	-	-	-	-
S25	GND	-	-	-	-	-	-	-
S26	GBE1_MDI3+	-	-	-	-	-	-	-
S27	GBE1_MDI3-	-	-	-	-	-	-	-
S28	GBE1_CTREF	-	-	-	-	-	-	-
S29	PCIE_D_TX+ / SERDES_1_TX+	-	-	-	-	-	-	-
S30	PCIE_D_TX- / SERDES_1_TX-	-	-	-	-	-	-	-
S31	GBE1_LINK_ACT#	Out/OD	-	-	LAN9514	nLNKA_LED	ALT1/ALT1	VCC3V3_SYS
S32	PCIE_D_RX+ / SERDES_1_RX+	-	-	-	-	-	-	-
S33	PCIE_D_RX- / SERDES_1_RX-	-	-	-	-	-	-	-
S34	GND	-	-	-	-	-	-	-

S35	USB4+	Out	-	USB	LAN9514	USBDP5	-	-
S36	USB4-	Bi-Dir	-	USB	LAN9514	USBDM5	-	-
S37	USB3_VBUS_DET	-	-	-	-	-	-	-
S38	AUDIO_MCK	Out	-	CMOS/ VDD_IO	PX30	I2S1_2CH_MCLK	ALT0/ALT0	VCC_1V8
S39	I2S0_LRCK	Bi-Dir	-	CMOS/ VDD_IO	PX30	I2S1_2CH_LRCK_TXRX	-	VCC_1V8
S40	I2S0_SDOUT	Out	-	CMOS/ VDD_IO	PX30	I2S1_2CH_SDO	-	VCC_1V8
S41	I2S0_SDIN	In	-	CMOS/ VDD_IO	PX30	I2S1_2CH_SDI	-	VCC_1V8
S42	I2S0_CK	Bi-Dir	-	CMOS/ VDD_IO	PX30	I2S1_2CH_SCKL	-	VCC_1V8
S43	ESPI_ALERT0#	-	-	-	-	-	-	-
S44	ESPI_ALERT1#	-	-	-	-	-	-	-
S45	MDIO_CLK	-	-	-	-	-	-	-
S46	MDIO_DAT	-	-	-	-	-	-	-
S47	GND	-	-	-	-	-	-	-
S48	I2C_GP_CK	Out	PU-2.2K	-	PX30	I2C1_SCL	ALT6/ALT6	VCC_1V8
S49	I2C_GP_DAT	Bi-Dir	PU-2.2K	-	PX30	I2C1_SDA	ALT6/ALT6	VCC_1V8
S50	HDA_SYNC / I2S2_LRCK	Bi-Dir	-	-	PX30	I2S0_2CH_LRCK_TXRX	-	VCC1V8_DVP
S51	HDA_SDO / I2S2_SDOUT	Out	-	-	PX30	I2S0_2CH_SDO	-	VCC1V8_DVP
S52	HDA_SDI / I2S2_SDIN	In	-	-	PX30	I2S0_2CH_SDI	-	VCC1V8_DVP
S53	HDA_CK / I2S2_CK	Bi-Dir	-	-	PX30	I2S0_2CH_SCKL	-	VCC1V8_DVP
S54	SATA_ACT#	-	-	-	-	-	-	-
S55	USB5_EN_OC#	-	-	-	-	-	-	-
S56	ESPI_IO_2	-	-	-	-	-	-	-
S57	ESPI_IO_3	-	-	-	-	-	-	-
S58	ESPI_RESET#	-	-	-	-	-	-	-
S59	USB5+	-	-	-	-	-	-	-
S60	USB5-	-	-	-	-	-	-	-
S61	GND	-	-	-	-	-	-	-
S62	USB3_SSTX+	-	-	-	-	-	-	-
S63	USB3_SSTX-	-	-	-	-	-	-	-
S64	GND	-	-	-	-	-	-	-
S65	USB3_SSRX+	-	-	-	-	-	-	-
S66	USB3_SSRX-	-	-	-	-	-	-	-

S67	GND	-	-	-	-	-	-	-
S68	USB3+	Bi-Dir	-	USB	LAN9514	USBDP4	-	-
S69	USB3-	Bi-Dir	-	USB	LAN9514	USBDM4	-	-
S70	GND	-	-	-	-	-	-	-
S71	USB2_SSTX+	-	-	-	-	-	-	-
S72	USB2_SSTX-	-	-	-	-	-	-	-
S73	GND	-	-	-	-	-	-	-
S74	USB2_SSRX+	-	-	-	-	-	-	-
S75	USB2_SSRX-	-	-	-	-	-	-	-
S76	PCIE_B_RST#	-	-	-	-	-	-	-
S77	PCIE_C_RST#	-	-	-	-	-	-	-
S78	PCIE_C_RX+ / SERDES_2_RX+	-	-	-	-	-	-	-
S79	PCIE_C_RX- / SERDES_2_RX-	-	-	-	-	-	-	-
S80	GND	-	-	-	-	-	-	-
S81	PCIE_C_TX+ / SERDES_2_TX+	-	-	-	-	-	-	-
S82	PCIE_C_TX- / SERDES_2_TX-	-	-	-	-	-	-	-
S83	GND	-	-	-	-	-	-	-
S84	PCIE_B_REFCK+	-	-	-	-	-	-	-
S85	PCIE_B_REFCK-	-	-	-	-	-	-	-
S86	GND	-	-	-	-	-	-	-
S87	PCIE_B_RX+	-	-	-	-	-	-	-
S88	PCIE_B_RX-	-	-	-	-	-	-	-
S89	GND	-	-	-	-	-	-	-
S90	PCIE_B_TX+	-	-	-	-	-	-	-
S91	PCIE_B_TX-	-	-	-	-	-	-	-
S92	GND	-	-	-	-	-	-	-
S93	DP0_LANE0+	-	-	-	-	-	-	-
S94	DP0_LANE0-	-	-	-	-	-	-	-
S95	DP0_AUX_SEL	-	-	-	-	-	-	-
S96	DP0_LANE1+	-	-	-	-	-	-	-
S97	DP0_LANE1-	-	-	-	-	-	-	-
S98	DP0_HPD	-	-	-	-	-	-	-
S99	DP0_LANE2+	-	-	-	-	-	-	-

S100	DP0_LANE2-	-	-	-	-	-	-	-
S101	GND	-	-	-	-	-	-	-
S102	DP0_LANE3+	-	-	-	-	-	-	-
S103	DP0_LANE3-	-	-	-	-	-	-	-
S104	USB3_OTG_ID	-	-	-	-	-	-	-
S105	DP0_AUX+	-	-	-	-	-	-	-
S106	DP0_AUX-	-	-	-	-	-	-	-
S107	LCD1_BKLT_EN	-	-	-	-	-	-	-
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	-	-	-	-	-	-	-
S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	-	-	-	-	-	-	-
S110	GND	-	-	-	-	-	-	-
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	-	-	-	-	-	-	-
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	-	-	-	-	-	-	-
S113	eDP1_HPD / DSI1_TE	-	-	-	-	-	-	-
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	-	-	-	-	-	-	-
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	-	-	-	-	-	-	-
S116	LCD1_VDD_EN	-	-	-	-	-	-	-
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	-	-	-	-	-	-	-
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	-	-	-	-	-	-	-
S119	GND	-	-	-	-	-	-	-
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	-	-	-	-	-	-	-
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	-	-	-	-	-	-	-
S122	LCD1_BKLT_PWM	-	-	-	-	-	-	-
S123	GPIO13	Bi-Dir	Serial-33R	CMOS/ VDD_IO	PX30	GPIO3_A0_d	ALT1/ALT1	VCC1V8_DVP
S124	GND	-	-	-	-	-	-	-

S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	Out	-	LVDS	PX30	LVDS_TX0P	-	MIPI_DSI
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	Out	-	LVDS	PX30	LVDS_TX1N	-	MIPI_DSI
S127	LCD0_BKLT_EN	Out	Serial-0R	CMOS/ VDD_IO	PX30	GPIO0_B7_d	ALT5/ALT5	VCC_1V8
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	Out	-	LVDS	PX30	LVDS_TX1P	-	MIPI_DSI
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	Out	-	LVDS	PX30	LVDS_TX1N	-	MIPI_DSI
S130	GND	-	-	-	-	-	-	-
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	Out	-	LVDS	PX30	LVDS_TX2P	-	MIPI_DSI
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	Out	-	LVDS	PX30	LVDS_TX2N	-	MIPI_DSI
S133	LCD0_VDD_EN	Out	-	CMOS/ VDD_IO	PX30	GPIO3_A4_d	ALT5/ALT5	VCC1V8_DVP
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	Out	-	LVDS	PX30	LVDS_CLKP	-	MIPI_DSI
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	Out	-	LVDS	PX30	LVDS_CLKN	-	MIPI_DSI
S136	GND	-	-	-	-	-	-	-
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	Out	-	LVDS	PX30	LVDS_TX3P	-	MIPI_DSI
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	Out	-	LVDS	PX30	LVDS_TX3N	-	MIPI_DSI
S139	I2C_LCD_CK	Out	PU-2.2K	CMOS/ VDD_IO	PX30	I2C2_SCL	ALT6/ALT6	VCC_RMII
S140	I2C_LCD_DAT	Bi-Dir	PU-2.2K	CMOS/ VDD_IO	PX30	I2C2_SDA	ALT6/ALT6	VCC_RMII
S141	LCD0_BKLT_PWM	Out	Serial-33R	CMOS/ VDD_IO	PX30	GPIO0_C0_d	ALT4/ALT4	VCC_1V8
S142	GPIO12	Bi-Dir	-	-	PX30	GPIO3_C7_d	-	VCC1V8_DVP
S143	GND	-	-	-	-	-	-	-
S144	eDP0_HPD / DSI0_TE	-	-	-	-	-	-	-
S145	WDT_TIME_OUT#	Out	-	CMOS/ VDD_IO	BMC	P10	-	+1V8SMC
S146	PCIE_WAKE#	-	-	-	-	-	-	-
S147	VDD_RTC	-	-	-	RTC	-	-	-
S148	LID#	In	PU-4.7K	CMOS/ VDD_IO	BMC	PB0	ALT5/ALT5	+1V8SMC
S149	SLEEP#	In	PU-4.7K	CMOS/ VDD_IO	PX30	GPIO1_C4_u	ALT5/ALT5	VCC_1V8
S150	VIN_PWR_BAD#	In	PU-10K	CMOS/ VDD_IO	BMC	P33	-	+1V8SMC

S151	CHARGING#	Out	PU-68K	CMOS/ VDD_IO	PX30	GPIO1_C5_d	ALT5/ALT5	VCC_1V8
S152	CHARGER_PRSNT#	Out	PU-100K	CMOS/ VDD_IO	PX30	GPIO1_C6_u	ALT5/ALT5	VCC_1V8
S153	CARRIER_STBY#	Out	-	CMOS/ VDD_IO	BMC	P53	-	+1V8SMC

5. Software Support

5.1.1 Early Access

5.1.2 Yocto

5.1.3 Ubuntu

6. Mechanical and Thermal

6.1 Module dimensions

6.2 Thermal Solutions

6.2.1 Heatspreader : HTS

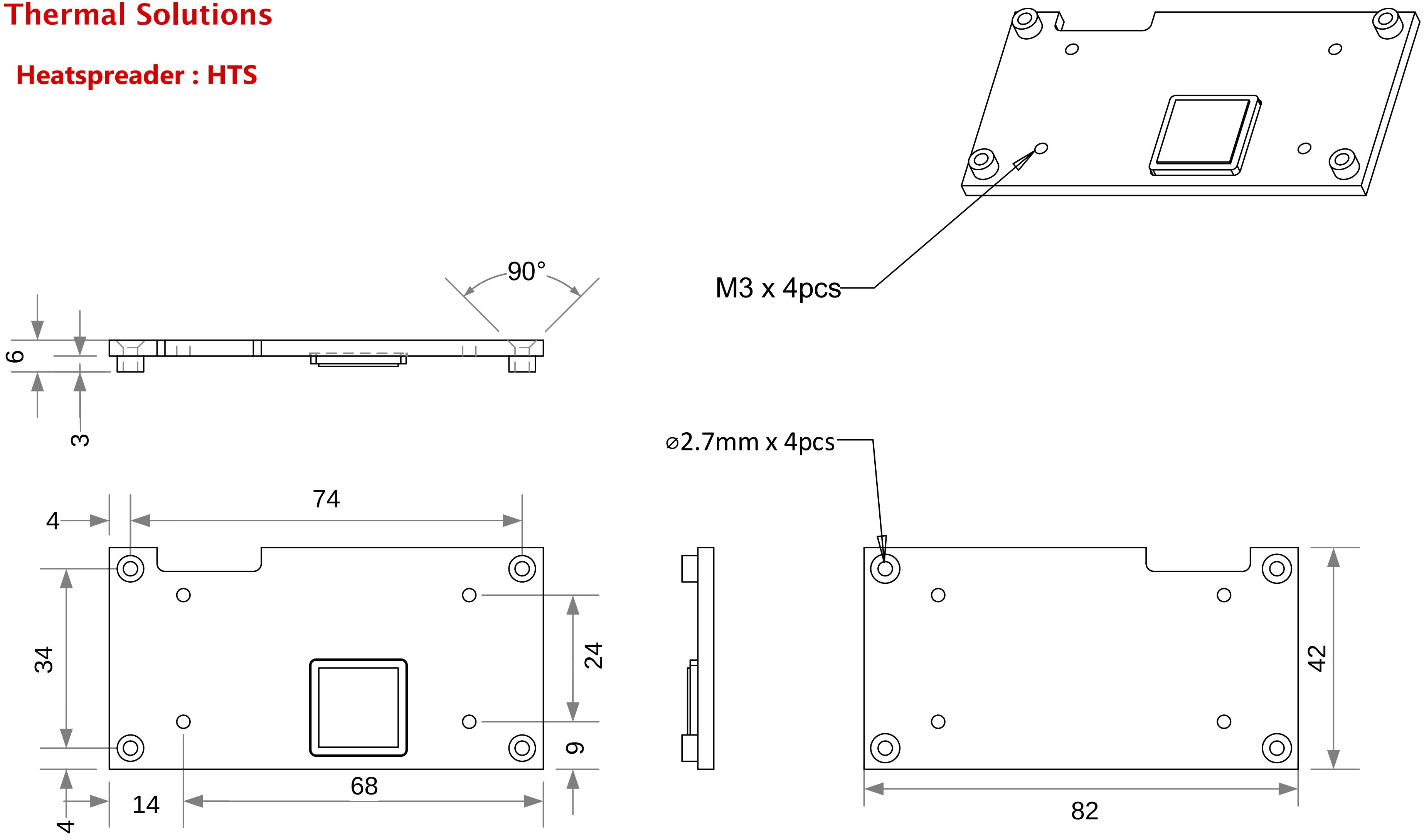

Figure 3 – Heatspreader HTS-sPX30

6.2.2 Heatsink : THS

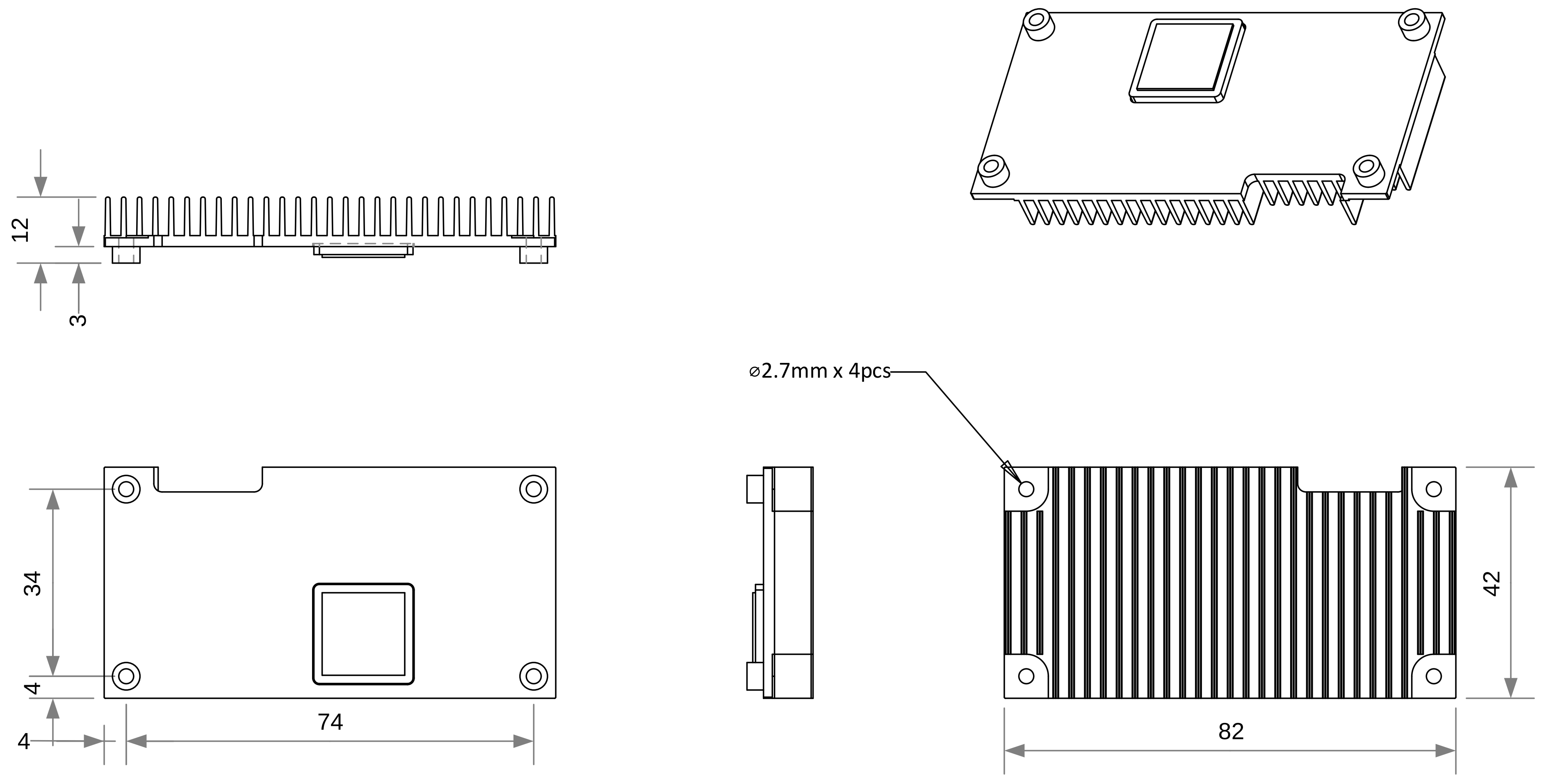

Figure 4 – Heatsink THS-sPX30