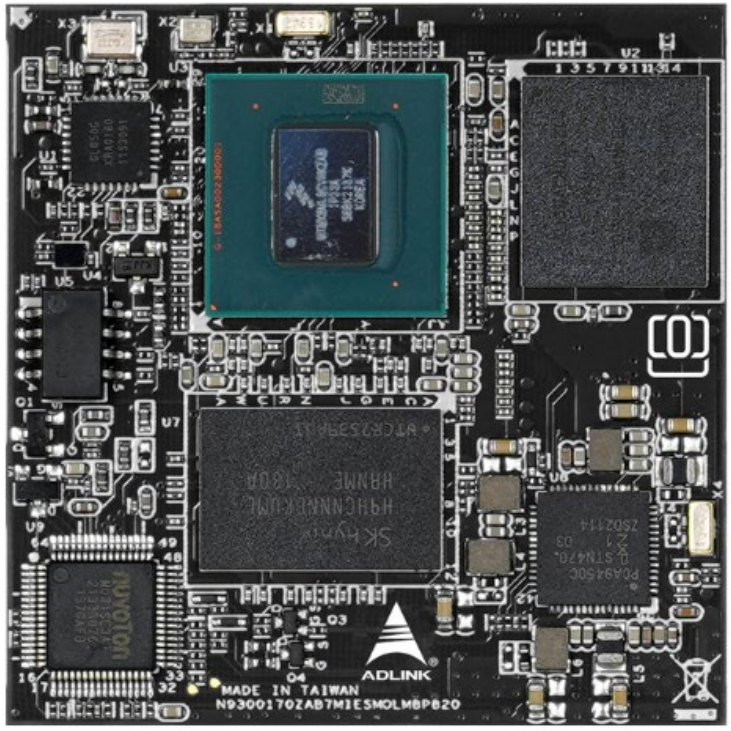
# OSM-IMX8MP

User's Guide




OPEN STANDARD MODULE™

Revision: Rev. 0.1 Preliminary
Date: 2024-05-30
Part Number: 50M-76100-1000

ADLINK LEADING EDGE COMPUTING

# Revision History

| Revision | Description | Date | Author |
|---|---|---|---|
| 0.1 | Preliminary release | 2024-05-30 | AL |

# Preface

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## Safety Instructions

For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

Read these safety instructions carefully.

- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

## Conventions

The following conventions may be used throughout this manual, denoting special levels of information.

**Note**: This information adds clarity or specifics to text and illustrations.

**Caution**: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

**Warning**: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

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# 1. Introduction

## 1.1. The OSM Form factor

The OSM ("Open Standard Module™") specification allows the development, production, and distribution of embedded modules for the most popular MCU32, ARM and x86 architectures. For a growing number of IoT applications, this standard helps combine the advantages of modular embedded computing with increasing requirements for costs, space, and interfaces.

The modules are used as building blocks for portable and stationary embedded systems. They consist of the core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies. The modules are employed with application-specific carrier boards that implement other features such as audio CODECs, touch controllers, wireless devices, PHY's, and other related features. This modular approach allows for scalability, fast time to market, and upgradability while still maintaining low costs, low power consumption, and small physical size.

SGeT STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

OSM module and carrier specifications are available online at: https://sget.org/standards/osm/

# 2. Specifications

## 2.1. Core System

### CPU

4x / 2x ARM Cortex-A53 @ | 1x Cortex M7 | 2.3 TOPS NPU

ARM Cortex-A53 MP Core processors are high-performance and optimized for low power.

### Memory

The chip has a single 32-bit DRAM controller.

- LPDDR4, soldered down
- 32-bit DRAM interface

### L2 Cache

512KB system L2 cache

### Security

Arm® TrustZone® EdgeLock® secure enclave

## 2.2. Video

### 2.2.1 GPU

**GPU Core**

Vivante GC7000UL

**Graphics Feature Support**

GC7000UL (2 shaders), OpenGL ES 2.0/3.0/3.1,

Vulkan, OpenCL 1.2; GC380 (2D)

### 2.2.2 Display Interface Support

**MIPI DSI**

1x MIPI DSI 4 lane Compliant to MIPI-DSI standard v1.2

Maximum resolution 1080p60 with 24-bit RGB

**LVDS**

2-channel LVDS port, up to 1920x1080p60 resolution

**HDMI**

HDMI 2.0a complaint, up to 1920x1080p60 / 3840x2160p30

## 2.3. Camera

One 4-lane MIPI CSI2 camera input

## 2.4. Audio

I2S to carrier

## 2.5. Dual Wired Ethernet

**Primary LAN**

MAC 10/100/1000 Ethernet Controller on SoC

Supports 10/100/1000-Mbps data transfer rates, both full-duplex and half-duplex

**Secondary LAN**

MAC 10/100/1000 Ethernet Controller on SoC

Supports 10/100/1000-Mbps data transfer rates, both full-duplex and half-duplex

## 2.6. Expansion Busses

**USB**: 2x USB 2.0, 2x USB 3.0

**UART**: 4 UART interfaces

**CANbus**: 2x CAN Supports CAN FD mode, data bit rate up to 8 Mbps

**SPI**: 2x SPI

**I2S**: 1x I2S interface with audio resolution from 16-bits to 32-bits and sample rate up to 192KHz (see Audio Codec support)

**ADC**: 2x ADC

**PWM**: 4x PWM

**I2C**: 2x I2C interfaces

- Support 7-bit mode
- Software programmable clock frequency of 100 kbit/s in Standard-mode, 400 kbit/s in Fast-mode, or 1 Mbit/s in Fast-mode Plus.

**GPIO**: 8x GPIO

## 2.7. System Storage

**SDIO**

2x SDIO (4-bit), compatible with SD3.0

**eMMC**

32, 64, 128 GB (built-in storage options)

## 2.8. Program Header

JTAG solder points

## 2.9. FAN Control

None, only passive cooling is needed.

## 2.10. Power

**Power Modes**

ON / OFF / SUSPEND

Power on / off behavior same as x86 AT (always boot)

**Voltage Input**

5.0V +/- 5%

**Operating Temperatures (vs power input)**

| | | |
|---|---|---|
| Standard Operating Temperature: | 0 to 60°C | Commercial grade BOM (memory, eMMC, SOC) |
| Extreme Rugged Operating Temperature: | -40 to 85°C | Industrial grade BOM (memory, eMMC, SOC) |

## 2.11. Mechanical and Environmental

**Form Factor and Specification**

OSM R1.1 Size-L

**Environmental Humidity**

Derating for two different BOMs

- 5-90% RH operating, non-condensing
- 5-95% RH storage (and operating with conformal coating)

**EMI**

EN55022 Class B inside an enclosure

**Shock and Vibration**

HALT Testing, including test report confirming extended operating temperature range during and after vibration. A separate shock test report to MIL-STD-202F, Method 213B, Table 213-I, Condition A.

IN ADDITION: When installed on a baseboard, the device shall operate under 18 sawtooth mechanical shocks (3 shocks in each direction) with a peak acceleration of 40g for a duration of 18 msec each and 75g for a duration of 6 msec each.

**Capable of supporting random vibration**: MIL-STD-202F, Method 214A, Table 214-I, Condition D. If HALT testing shows equal or better performance, a separate vibration test report is not necessary.

**MTBF**

300,000 hrs. (at 40°C), 100,000 hrs. (at 85°C)

Two different BOM: 0-60°C and -40-85°C

# 3. Block Diagram

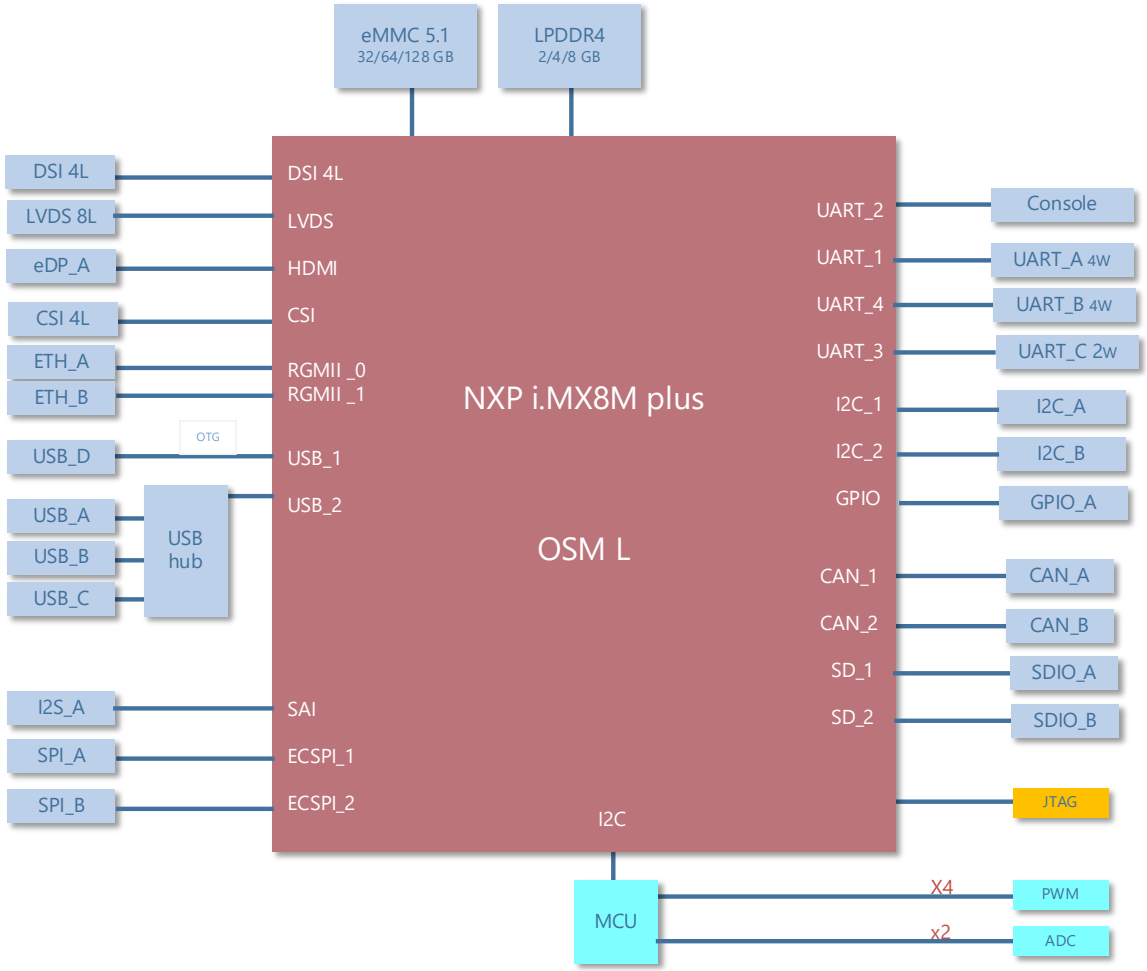


**Figure 1 – Module function diagram**

# 4. Pinout and Signal Descriptions

## 4.1. Pin Summary

- Size-0 – "Zero": 30 mm x 15 mm
- Size-S – "Small": 30 mm x 30 mm
- Size-M – "Medium": 30 mm x 45 mm
- Size-L – "Large": 45 mm x 45 mm

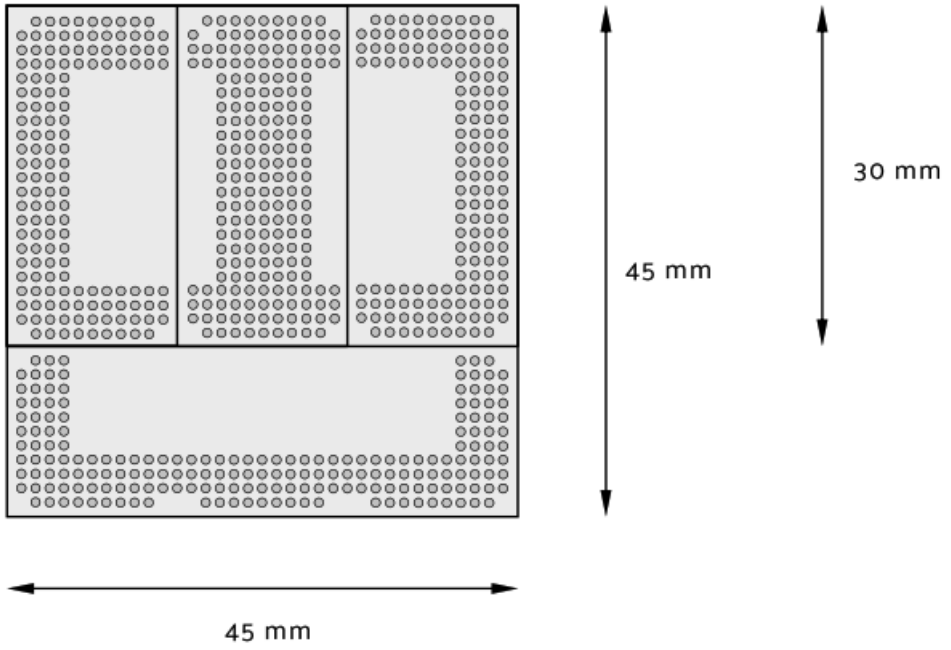


**Figure 2 – Module size grid**

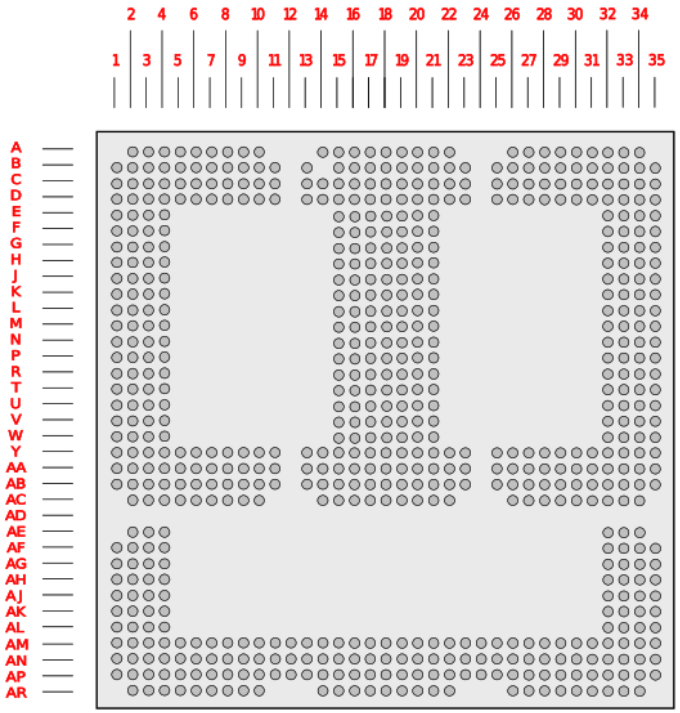


Figure 21: Contact Grid (all sizes) (view from top, through the module)

**Figure 3 – Module pinout grid**

## 4.2. Signal Terminology Descriptions

The following information provides descriptions of the terms used in the signal description table:

| Term | | Description |
|---|---|---|
| I | | Input to the module |
| O | | Output from the module |
| I/O | | Bi-directional input/output |
| OD | | Open drain |
| PU | | PU (pull-up) resistor |
| PD | | PD (pull-down) resistor |
| CMOS | | Logic input or output |
| GBE MDI | | Differential analogue signaling for gigabit media dependent interface |
| DP | | Low voltage differential signal for DisplayPort interface |
| D-PHY | | Low voltage differential signal for MIPI CSI-2 cameras and DSI displays |
| M-PHY | | Low voltage differential signal for MIPI CSI-3 cameras |
| LVDS | | Low voltage differential signal for LCD displays |
| PCIE | | Low voltage differential signal for PCIe |
| SATA | | Low voltage differential signal for SATA |
| TMDS HDMI | | Transition minimized differential signal for HDMI displays |
| USB | | DC coupled differential signaling for traditional (non-SuperSpeed) USB signals |
| USB SS | | Differential signal for SuperSpeed USB signals |
| USB VBUS 5V | | 5V tolerant input for USB VBUS detection |
| VDD_IN | | Main power source from carrier to module |
| 3.3V | | 3.3V power domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e., both signals are high) |
| 1.8V | | 1.8V power domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e., both signals are high) |
| 3.3Vsb | | 3.3V standby power domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#) |
| 1.8Vsb | | 1.8V standby power domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#) |
| Sleep | | Module is in its lowest power state |
| Runtime | | Module is full on. CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e., both signals are high) |
| | | |

## 4.3. Signal Description by Function

### 4.3.1 LVDS Display Interface

For information on LVDS support for a single-channel with 4 lanes, please refer to the details below:

| Contact Name | Contact Acronym | Functional Description | I/O Type | I/O Level | PU / PD | Comments |
|---|---|---|---|---|---|---|
| LVDS_I2C_CLK | AM11 | DDC clock line used for flat panel detection and control | O OD CMOS | 1.8V | PU 2k2 | |
| LVDS_I2C_DAT | AM12 | DDC data line used for flat panel detection and control | I/O OD CMOS | 1.8V | PU 2k2 | |
| LVDS_VDD_EN | AN14 | LVDS channel power enable, active high | O CMOS | 1.8V | | |
| LVDS_BL_PWM | AN22 | LVDS channel brightness control through pulse width modulation | O CMOS | 1.8V | | |
| LVDS_BL_EN | AN23 | LVDS channel backlight enable, active high | O CMOS | 1.8V | | |
| LVDS_A_CLK_P | AN13 | LVDS channel A differential pair clock lines | O LVDS LCD | | | |
| LVDS_A_CLK_N | AN12 | LVDS channel A differential pair clock lines | O LVDS LCD | | | |
| LVDS_A_LANE0_P | AP18 | LVDS channel A differential pair data lines | O LVDS LCD | | | |
| LVDS_A_LANE0_N | AP17 | LVDS channel A differential pair data lines | O LVDS LCD | | | |
| LVDS_A_LANE1_P | AR16 | LVDS channel A differential pair data lines | O LVDS LCD | | | |
| LVDS_A_LANE1_N | AR15 | LVDS channel A differential pair data lines | O LVDS LCD | | | |
| LVDS_A_LANE2_P | AP15 | LVDS channel A differential pair data lines | O LVDS LCD | | | |
| LVDS_A_LANE2_N | AP14 | LVDS channel A differential pair data lines | O LVDS LCD | | | |
| LVDS_A_LANE3_P | AP12 | LVDS channel A differential pair data lines | O LVDS LCD | | | |
| LVDS_A_LANE3_N | AP11 | LVDS channel A differential pair data lines | O LVDS LCD | | | |

#### 4.3.1.1. DSI0 Mode

| Contact Name | Contact Acronym | Functional Description | I/O Type | I/O Level | PU / PD | Comments |
|---|---|---|---|---|---|---|
| DSI_DATA0_N | AB11 | DSI differential output (point to point) | O LVDS D-PHY | | | |
| DSI_DATA0_P | AB10 | DSI differential output (point to point) | O LVDS D-PHY | | | |
| DSI_DATA1_N | AC9 | DSI differential output (point to point) | O LVDS D-PHY | | | |
| DSI_DATA1_P | AC8 | DSI differential output (point to point) | O LVDS D-PHY | | | |
| DSI_DATA2_N | AC6 | DSI differential output (point to point) | O LVDS D-PHY | | | |
| DSI_DATA2_P | AC5 | DSI differential output (point to point) | O LVDS D-PHY | | | |
| DSI_DATA3_N | AB5 | DSI differential output (point to point) | O LVDS D-PHY | | | |
| DSI_DATA3_P | AB4 | DSI differential output (point to point) | O LVDS D-PHY | | | |
| DSI_CLOCK_N | AB8 | DSI differential clock output (point to point) | O LVDS D-PHY | | | |
| DSI_CLOCK_P | AB7 | DSI differential clock output (point to point) | O LVDS D-PHY | | | |
| DSI_TE | AA3 | DSI panel tearing effect signal | I CMOS | 1.8V | | |
| DISP_VDD_EN / GPIO_C_4 | F3 | Primary display power enable, active high | O CMOS | 1.8V | | |
| DISP_BL_EN / GPIO_C_5 | F4 | Primary display backlight enable, active high | O CMOS | 1.8V | | |
| DISP_BL_PWM / PWM_0 | E18 | Primary display brightness control through pulse width modulation | O CMOS | 1.8V | | |

### 4.3.1.2. eDP0 / eDP1 Mode

**N/A**

### 4.3.1.3. HDMI MODE (to eDP A)

| Contact Name | Contact Acronym | Functional Description | I/O Type | I/O Level | PU / PD | Comments |
|---|---|---|---|---|---|---|
| eDP_A_LANE0_P | A30 | Primary 4-lane eDP differential pair data lines | O LVDS DP | | | AC coupled off module |
| eDP_A_LANE0_N | A31 | Primary 4-lane eDP differential pair data lines | O LVDS DP | | | AC coupled off module |
| eDP_A_LANE1_P | B31 | Primary 4-lane eDP differential pair data lines | O LVDS DP | | | AC coupled off module |
| eDP_A_LANE1_N | B32 | Primary 4-lane eDP differential pair data lines | O LVDS DP | | | AC coupled off module |
| eDP_A_LANE2_P | A33 | Primary 4-lane eDP differential pair data lines | O LVDS DP | | | AC coupled off module |
| eDP_A_LANE2_N | A34 | Primary 4-lane eDP differential pair data lines | O LVDS DP | | | AC coupled off module |
| eDP_A_LANE3_P | B34 | Primary 4-lane eDP differential pair data lines | O LVDS DP | | | AC coupled off module |
| eDP_A_LANE3_N | B35 | Primary 4-lane eDP differential pair data lines | O LVDS DP | | | AC coupled off module |
| eDP_A_AUX_P | C33 | Primary bidirectional eDP channel used for link management and device control | I/O LVDS DP | | PD 100k | AC coupled off module |
| eDP_A_AUX_N | C34 | Primary bidirectional eDP channel used for link management and device control | I/O LVDS DP | | PD 100k | AC coupled off module |
| eDP_A_AUX_SEL | D32 | Strapping signal to enable either HDMI or DP output | I CMOS | 1.8V | PD 1M | Pulled to GND on Carrier for DP operation in dual mode (DP++) implementations. Driven to 1.8V on carrier for HDMI mode module must tolerate high level in stand-by mode. |
| eDP_A_BL_HPD | D33 | Detection of hot plug / unplug of the primary eDP display and notification of the link layer. | I CMOS | 1.8V | PD 1M | Module must tolerate high level in stand-by mode. |
| eDP_A_BL_EN | D31 | Primary eDP panel backlight enabled, active high | O CMOS | 1.8V | | |
| eDP_A_BL_PWM | C31 | Primary eDP panel brightness control through pulse width modulation | O CMOS | 1.8V | | |

#### 4.3.1.4. eDP_B

**N/A**

### 4.3.2 MIPI Camera Support

#### 4.3.2.1. CSI (4 lanes)

| Contact Name | Contact Acronym | Functional Description | I/O Type | I/O Level | PU / PD | Comments |
|---|---|---|---|---|---|---|
| CSI_DATA0_N | C1 | CSI differential input (point to point) | I LVDS D-PHY/ I LVDS M-PHY | | | |
| CSI_DATA0_P | B1 | CSI differential input (point to point) | I LVDS D-PHY / I LVDS M-PHY | | | |
| CSI_DATA1_N | A2 | CSI differential input (point to point) | I LVDS D-PHY / I LVDS M-PHY | | | |
| CSI_DATA1_P | A3 | CSI differential input (point to point) | I LVDS D-PHY / I LVDS M-PHY | | | |
| CSI_DATA2_N | A5 | CSI differential input (point to point) | I LVDS D-PHY / I LVDS M-PHY | | | |
| CSI_DATA2_P | A6 | CSI differential input (point to point) | I LVDS D-PHY / I LVDS M-PHY | | | |
| CSI_DATA3_N | B6 | CSI differential input (point to point) | I LVDS D-PHY / I LVDS M-PHY | | | |
| CSI_DATA3_P | B7 | CSI differential input (point to point) | I LVDS D-PHY / I LVDS M-PHY | | | |
| CSI_CLOCK_N | B3 | CSI differential clock input (point to point) | I LVDS D-PHY | | | |
| CSI_CLOCK_P | B4 | CSI differential clock input (point to point) | I LVDS D-PHY | | | |
| CAM_MCK | C2 | Master clock output | O CMOS | 1.8V | | |
| I2C_CAM_SDA / CSI_TX_N | C3 | I2C data for serial camera data support link or differential data lane | I/O OD CMOS / O LVDS M- PHY | 1.8V | PU 2.2K | MIPI-CSI 2.0 mode uses I2C_CAM_SDA |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | | | MIPI-CSI 3.0 mode uses CSI_TX_N |
| I2C_CAM_SCL / CSI_TX_P | C4 | I2C clock for serial camera data support link or differential data lane | I/O OD CMOS | 1.8V | PU 2.2K | MIPI-CSI 2.0 mode uses I2C_CAM_SCL |
| | | | / O LVDS M-PHY | | | MIPI-CSI 3.0 mode uses CSI_TX_P |
| CAM_PWR / GPIO_C_6 | G3 | Camera 0 Power Enable, active high output. | O CMOS | 1.8V | | |
| CAM_RST# / GPIO_C_7 | G4 | Camera 0 reset, active low output | O CMOS | 1.8V | | |

## 4.3.3 Audio Interfaces

### 4.3.3.1. I2S0

| Contact Name | Contact Acronym | Functional Description | I/O Type | I/O Level (Size-0 only, optional) | I/O Level (>Size-0) | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| I2S_A_DATA_IN | V21 | I2S A Digital audio Input | I/O CMOS | VCC_OUT_IO | 1.8V | | |
| I2S_A_DATA_OUT | W21 | I2S A Digital audio Output | I/O CMOS | VCC_OUT_IO | 1.8V | | |
| I2S_B_DATA_IN | V19 | I2S B Digital audio Input | I/O CMOS | VCC_OUT_IO | 1.8V | | |
| I2S_B_DATA_OUT | W19 | I2S B Digital audio Output | I/O CMOS | VCC_OUT_IO | 1.8V | | |
| I2S_MCLK | V18 | Master clock output to I2S codec(s) | I/O CMOS | VCC_OUT_IO | 1.8V | | |
| I2S_LRCLK | W18 | I2S Left & Right synchronization clock | I/O CMOS | VCC_OUT_IO | 1.8V | | Module Output - if CPU acts in Master Mode. Module Input - if CPU acts in Slave Mode. |
| I2S_BITCLK | W20 | I2S Digital audio clock | I/O CMOS | VCC_OUT_IO | 1.8V | | Module Output - if CPU acts in Master Mode. Module Input if CPU acts in Slave Mode. |

### 4.3.4 USB Ports

| Contact Name | Contact Acronym | Functional Description | I/O Type | I/O Level | PU / PD | Comments |
|---|---|---|---|---|---|---|
| USB_A_D_N | AB13 | USB differential data pairs for port A | I/O USB | USB | | |
| USB_A_D_P | AC14 | USB differential data pairs for port A | I/O USB | USB | | |
| USB_A_ID | AB14 | Input Contact to announce OTG device insertion on USB 2.0 port | I OD CMOS | 1.8V | PU 10k | |
| USB_A_OC# | AC15 | USB over-current for port A | I OD CMOS | 1.8V | PU 10k | |
| USB_A_VBUS | AB16 | USB port 0 port power detection | I USB VBUS 5V | USB VBUS 5V | | |
| USB_A_EN | AC16 | Power enable for USB VBUS voltage | O CMOS | 1.8V | | |
| USB_B_D_N | AB23 | USB differential data pairs for port B | I/O USB | USB | | |
| USB_B_D_P | AC22 | USB differential data pairs for port B | I/O USB | USB | | |
| USB_B_ID | AB22 | Input Contact to announce OTG device insertion on USB 2.0 port | I OD CMOS | 1.8V | PU 10k | |
| USB_B_OC# | AC21 | USB over-current for port B | I OD CMOS | 1.8V | PU 10k | |
| USB_B_VBUS | AB20 | USB port 0 port power detection | I USB VBUS 5V | USB VBUS 5V | | |
| USB_B_EN | AC20 | Power enable for USB VBUS voltage | O CMOS | 1.8V | | |
| Contact Name | Contact Acronym | Functional Description | I/O Type | I/O Level | PU / PD | Comments |
| USB_C_D_N | D11 | USB differential data pairs for port C | I/O USB | USB | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| USB_C_D_P | D10 | USB differential data pairs for port C | I/O USB | USB | | |
| USB_C_ID | D9 | Input Contact to announce OTG device insertion on USB 2.0 port | I OD CMOS | 1.8V | PU 10k | |
| USB_C_OC# | C8 | USB over-current for port C | I OD CMOS | 1.8V | PU 10k | |
| USB_C_VBUS | C9 | USB port 0 port power detection | I USB VBUS 5V | USB VBUS 5V | | |
| USB_C_EN | C10 | Power enable for USB VBUS voltage | O CMOS | 1.8V | | |
| USB_C_SSTX_N | A9 | Transmit signal differential pairs for SuperSpeed on port C | O USB SS | USB SS | | AC coupled off module |
| USB_C_SSTX_P | A8 | Transmit signal differential pairs for SuperSpeed on port C | O USB SS | USB SS | | AC coupled off module |
| USB_C_SSRX_N | B11 | Receive signal differential pairs for SuperSpeed on port C | I USB SS | USB SS | | AC coupled off module |
| USB_C_SSRX_P | B10 | Receive signal differential pairs for SuperSpeed on port C | I USB SS | USB SS | | AC coupled off module |
| Contact Name | Contact Acronym | Functional Description | I/O Type | I/O Level | PU / PD | Comments |
| USB_D_D_N | D26 | USB differential data pairs for port D | I/O USB | USB | | |
| USB_D_D_P | D25 | USB differential data pairs for port D | I/O USB | USB | | |
| USB_D_ID | D27 | Input Contact to announce OTG device insertion on USB 2.0 port | I OD CMOS | 1.8V | PU 10k | |

| | | | | | | |
|---|---|---|---|---|---|---|
| USB_D_OC# | C28 | USB over-current for port D | I OD CMOS | 1.8V | PU 10k | |
| USB_D_VBUS | C27 | USB port 0 port power detection | I USB VBUS 5V | USB VBUS 5V | | |
| USB_D_EN | C26 | Power enable for USB VBUS voltage | O CMOS | 1.8V | | |
| USB_D_SSTX_N | A28 | Transmit signal differential pairs for SuperSpeed on port D | O USB SS | USB SS | | AC coupled off module |
| USB_D_SSTX_P | A27 | Transmit signal differential pairs for SuperSpeed on port D | O USB SS | USB SS | | AC coupled off module |
| USB_D_SSRX_N | B26 | Receive signal differential pairs for SuperSpeed on port D | I USB SS | USB SS | | AC coupled off module |
| USB_D_SSRX_P | B25 | Receive signal differential pairs for SuperSpeed on port D | I USB SS | USB SS | | AC coupled off module |

### 4.3.5 PCIe

| Contact Name | Contact Acronym | Functional Description | I/O Type | I/O Level | PU / PD | Comments |
|---|---|---|---|---|---|---|
| PCIe_A_HSI0_P | AB1 | Differential PCIe link A receive data pair | I LVDS PCIE | | | AC coupled off module |
| PCIe_A_HSI0_N | AB2 | Differential PCIe link A receive data pair | I LVDS PCIE | | | AC coupled off module |
| PCIe_A_HSO0_P | AC2 | Differential PCIe link A transmit data pair | O LVDS PCIE | | | AC coupled off module |
| PCIe_A_HSO0_N | AC3 | Differential PCIe link A transmit data pair | O LVDS PCIE | | | AC coupled off module |
| PCIe_CLKREQ# | W2 | PCIe reference clock request | I OD CMOS | 1.8V | PU 10k | |
| PCIe_A_PERST# | V2 | PCIe Port A reset output | O CMOS | 1.8V | | |
| PCIe_REFCLK_P | W1 | Differential PCIe reference clock output | O LVDS PCIE | | | |
| PCIe_REFCLK_N | Y1 | Differential PCIe reference clock output | O LVDS PCIE | | | |
| PCIe_WAKE# | T2 | PCIe wake up interrupt to host –<br>common to PCIe links A, B, C, D | I OD CMOS | 1.8V | PU 10k | |
| PCIe_SMDAT | U1 | System management I2C bus DATA | I/O OD CMOS | 1.8V | PU 2k2 | |
| PCIe_SMCLK | T1 | System management I2C bus CLK | O OD CMOS | 1.8V | PU 2k2 | |
| PCIe_SM_ALERT# | R2 | SMBus Alert# (interrupt) signal | I OD CMOS | 1.8V | PU 2k2 | |

## 4.3.6 Dual LAN ports

### 4.3.6.1. GBE0 (RGMii)

| Contact Name | Contact Acronym | Functional Description | I/O Type | I/O Level | PU / PD | Comments |
|---|---|---|---|---|---|---|
| ETH_A_(R)(G)MII_CRS | E16 | Carrier Sense port A | I CMOS | 1.8V/2.5V/3.3V | | |
| ETH_A_(R)(G)MII_COL | F15 | Collision detection for ( at half speed only) port A | I CMOS | 1.8V/2.5V/3.3V | | |
| ETH_A_(S)(R)(G)MII_TXD0 | H15 | Transmit data bit 0 (transmitted first) port A | O CMOS | 1.8V/2.5V/3.3V | | _P when used as differential |
| ETH_A_(S)(R)(G)MII_TXD1 | G15 | Transmit data bit 1 port A | O CMOS | 1.8V/2.5V/3.3V | | _N when used as differential |
| ETH_A_(S)(R)(G)MII_TXD2 | H16 | Transmit data bit 2 port A | O CMOS | 1.8V/2.5V/3.3V | | _P when used as differential |
| ETH_A_(S)(R)(G)MII_TXD3 | G16 | Transmit data bit 3 port A | O CMOS | 1.8V/2.5V/3.3V | | _N when used as differential |
| ETH_A_(R)(G)MII_TX_EN(_ER) | K16 | Transmit enable (Error) port A | O CMOS | 1.8V/2.5V/3.3V | | |
| ETH_A_(R)(G)MII_TX_CLK | J15 | Transmit clock port A | I/O CMOS | 1.8V/2.5V/3.3V | | |
| ETH_A_(S)(R)(G)MII_RXD0 | K15 | Receive data bit 0 (received first) port A | I CMOS | 1.8V/2.5V/3.3V | | _P when used as differential |
| ETH_A_(S)(R)(G)MII_RXD1 | L15 | Receive data bit 1 port A | I CMOS | 1.8V/2.5V/3.3V | | _N when used as differential |
| ETH_A_(R)(G)MII_RXD2 | N15 | Receive data bit 2 port A | I CMOS | 1.8V/2.5V/3.3V | | |
| ETH_A_(R)(G)MII_RXD3 | P15 | Receive data bit 3 port A | I CMOS | 1.8V/2.5V/3.3V | | |
| ETH_A_(R)(G)MII_RX_ER | L16 | Receive error port A | I CMOS | 1.8V/2.5V/3.3V | | |
| ETH_A_(R)(G)MII_RX_DV(_ER) | M15 | Receive data valid port A | I CMOS | 1.8V/2.5V/3.3V | | |
| ETH_A_(R)(G)MII_RX_CLK | R15 | Receive clock port A | I/O CMOS | 1.8V/2.5V/3.3V | | |
| ETH_A_SDP | N16 | Ethernet port A System Defined Contact | O CMOS | 1.8V/2.5V/3.3V | | |
| ETH_MDIO | T15 | Management bus data signal for Ethernet | I/O CMOS | 1.8V/2.5V/3.3V | | Can be used for all ETH ports or for A exclusively |
| ETH_MDC | T16 | Management bus clock signal for Ethernet | O CMOS | 1.8V/2.5V/3.3V | | Can be used for all ETH ports or for A exclusively |
| ETH_IOPWR | M17 | ETH voltage. It is used to provide the IO Voltage Level for all Ethernet interfaces. | P | 1.8V/2.5V/3.3V | | Minimum current: 100mA |

#### 4.3.6.2. GBE1 (RGMii)

| Contact Name | Contact Acronym | Functional Description | I/O Type | I/O Level | PU / PD | Comments |
|---|---|---|---|---|---|---|
| ETH_B_(R)(G)MII_CRS | D2 | Carrier Sense port B | I CMOS | 1.8V/2.5V/3.3V | | |
| ETH_B_(R)(G)MII_COL | E1 | Collision detection (at half speed only) port B | I CMOS | 1.8V/2.5V/3.3V | | |
| ETH_B_(S)(R)(G)MII_TXD0 | G1 | Transmit data bit 0 (transmitted first) port B | O CMOS | 1.8V/2.5V/3.3V | | _P when used as differential |
| ETH_B_(S)(R)(G)MII_TXD1 | F1 | Transmit data bit 1 port B | O CMOS | 1.8V/2.5V/3.3V | | _N when used as differential |
| ETH_B_(S)(R)(G)MII_TXD2 | G2 | Transmit data bit 2 port B | O CMOS | 1.8V/2.5V/3.3V | | _P when used as differential |
| ETH_B_(S)(R)(G)MII_TXD3 | F2 | Transmit data bit 3 port B | O CMOS | 1.8V/2.5V/3.3V | | _N when used as differential |
| ETH_B_(R)(G)MII_TX_EN(_ER) | J2 | Transmit enable (Error) port B | O CMOS | 1.8V/2.5V/3.3V | | |
| ETH_B_(R)(G)MII_TX_CLK | H1 | Transmit clock port B | I/O CMOS | 1.8V/2.5V/3.3V | | |
| ETH_B_(S)(R)(G)MII_RXD0 | J1 | Receive data bit 0 (received first) port B | I CMOS | 1.8V/2.5V/3.3V | | _P when used as differential |
| ETH_B_(S)(R)(G)MII_RXD1 | K1 | Receive data bit 1 port B | I CMOS | 1.8V/2.5V/3.3V | | _N when used as differential |
| ETH_B_(R)(G)MII_RXD2 | M1 | Receive data bit 2 port B | I CMOS | 1.8V/2.5V/3.3V | | |
| ETH_B_(R)(G)MII_RXD3 | N1 | Receive data bit 3 port B | I CMOS | 1.8V/2.5V/3.3V | | |
| ETH_B_(R)(G)MII_RX_ER | K2 | Receive error port B | I CMOS | 1.8V/2.5V/3.3V | | |
| ETH_B_(R)(G)MII_RX_DV(_ER) | L1 | Receive data valid (Error) port B | I CMOS | 1.8V/2.5V/3.3V | | |
| ETH_B_(R)(G)MII_RX_CLK | P1 | Receive clock port B | I/O CMOS | 1.8V/2.5V/3.3V | | |
| ETH_B_SDP | M2 | Ethernet port B System Defined Contact | O CMOS | 1.8V/2.5V/3.3V | | |
| ETH_B_MDIO | C7 | Management bus data signal for Ethernet B | I/O CMOS | 1.8V/2.5V/3.3V | | Optional use |
| ETH_B_MDC | C6 | Management bus clock signal for Ethernet B | O CMOS | 1.8V/2.5V/3.3V | | Optional use |

### 4.3.7 SDIO Card (4-bit)

The Carrier SDIO Card ***can*** be selected as the boot device.

| Contact Name | Contact Acronym | Functional Description | I/O Type | I/O Level | PU / PD | Comments |
|---|---|---|---|---|---|---|
| SDIO_A_CMD | E20 | SDIO A Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode. | I/O CMOS | 1.8V or 3.3V | | |
| SDIO_A_CLK | F21 | SDIO A Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. | O CMOS | 1.8V or 3.3V | | |
| SDIO_A_D0 | G20 | SDIO A Data lines. These signals operate in push-pull mode. | I/O CMOS | 1.8V or 3.3V | | |
| SDIO_A_D1 | G21 | SDIO A Data lines. These signals operate in push-pull mode. | I/O CMOS | 1.8V or 3.3V | | |
| SDIO_A_D2 | H20 | SDIO A Data lines. These signals operate in push-pull mode. | I/O CMOS | 1.8V or 3.3V | | |
| SDIO_A_D3 | H21 | SDIO A Data lines. These signals operate in push-pull mode. | I/O CMOS | 1.8V or 3.3V | | |
| SDIO_A_CD# | J21 | SDIO A Card Detect. This signal indicates when a SDIO/MMC card is present. | I OD CMOS | 1.8V or 3.3V | PU 10k | |

| | | | | | | |
|---|---|---|---|---|---|---|
| SDIO_A_WP | D20 | SDIO A Write Protect. This signal denotes the state of the write- protect tab on SD cards. | I OD CMOS | 1.8V or 3.3V | PU 10k | Tie to GND on carrier, if not used |
| SDIO_A_PWR_EN | D21 | SDIO A Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device. | O CMOS | 1.8V or 3.3V | | |
| SDIO_A_IOPWR | C20 | SDIO A Voltage. It is used to provide the IO Voltage Level | P | 1.8V or 3.3V | | Minimum current: 100mA |
| SDIO_B_CLK | K20 | SDIO B Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. | O CMOS | 1.8V or 3.3V | | |
| SDIO_B_CMD | K21 | SDIO B Command/Response. This signal is used for card initialization and for command transfers. During initialization mode | I/O CMOS | 1.8V or 3.3V | | |
| SDIO_B_D0 | L20 | SDIO B Data lines. These signals operate in push-pull mode. | I/O CMOS | 1.8V or 3.3V | | |
| SDIO_B_D1 | L21 | SDIO B Data lines. These signals operate in push-pull mode. | I/O CMOS | 1.8V or 3.3V | | |
| SDIO_B_D2 | M21 | SDIO B Data lines. These signals operate in push-pull mode. | I/O CMOS | 1.8V or 3.3V | | |
| SDIO_B_D3 | N20 | SDIO B Data lines. These signals operate in push-pull mode. | I/O CMOS | 1.8V or 3.3V | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| SDIO_B_D4 | N21 | SDIO B Data lines. These signals operate in push-pull mode. | I/O CMOS | 1.8V or 3.3V | | |
| SDIO_B_D5 | P20 | SDIO B Data lines. These signals operate in push-pull mode. | I/O CMOS | 1.8V or 3.3V | | |
| SDIO_B_D6 | P21 | SDIO B Data lines. These signals operate in push-pull mode. | I/O CMOS | 1.8V or 3.3V | | |
| SDIO_B_D7 | R21 | SDIO B Data lines. These signals operate in push-pull mode. | I/O CMOS | 1.8V or 3.3V | | |
| SDIO_B_CD# | T21 | SDIO B Card Detect. This signal indicates when a SDIO/MMC card is present. | I OD CMOS | 1.8V or 3.3V | PU 10k | |
| SDIO_B_WP | U20 | SDIO B Write Protect. This signal denotes the state of the write- protect tab on SD cards. | I OD CMOS | 1.8V or 3.3V | PU 10k | Tie to GND on carrier, if not used |
| SDIO_B_PWR_EN | U21 | SDIO B Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device. | O CMOS | 1.8V or 3.3V | | |
| SDIO_B_IOPWR | T20 | SDIO B Voltage. It is used to provide the IO Voltage Level | P | 1.8V or 3.3V | | Minimum current: 100mA |

## 4.3.8 SPI Interfaces

### 4.3.8.1. SPI A/B

| Contact Name | Contact Acronym | Functional Description | I/O Type | I/O Level (>Size-0) | PU / PD | Comments |
|---|---|---|---|---|---|---|
| SPI_A_SDI_(IO0) | U15 | SPI A Serial Data Input | IO CMOS | 1.8V | | Alternate use: QuadSPI IO0 |
| SPI_A_SDO_(IO1) | V15 | SPI A Serial Data Output | IO CMOS | 1.8V | | Alternate use: QuadSPI IO1 |
| SPI_A_/WP_(IO2) | W16 | SPI A Write Protect | IO CMOS | 1.8V | | Alternate use: QuadSPI IO2 |
| SPI_A_/HOLD_(IO3) | W15 | SPI A Suspends Serial Input | IO CMOS | 1.8V | | Alternate use: QuadSPI IO3 |
| SPI_A_CS0# | Y15 | SPI A Master Chip Select 0 | O CMOS | 1.8V | | |
| SPI_A_CS1# / GPIO_A_6 | K17 | SPI A Master Chip Select 1 | O CMOS | 1.8V | | |
| SPI_A_SCK | U16 | SPI A Serial Data Clock | O CMOS | 1.8V | | |
| SPI_B_SDI | Y22 | SPI B Serial Data Input | I CMOS | 1.8V | | |
| SPI_B_SDO | Y23 | SPI B Serial Data Output | O CMOS | 1.8V | | |
| SPI_B_CS0# | AA23 | SPI B Master Chip Select 0 | O CMOS | 1.8V | | |
| SPI_B_CS1# / GPIO_A_7 | L17 | SPI B Master Chip Select 1 | O CMOS | 1.8V | | |
| SPI_B_SCK | Y21 | SPI B Serial Data Clock | O CMOS | 1.8V | | |

### 4.3.9 GPIO

GPIO's are available, filling the 1st bank

| Contact Name | Contact Acronym | Functional Description | I/O Type | I/O Level (>Size-0) | PU / PD | Comments |
|---|---|---|---|---|---|---|
| GPIO_A_0 | D17 | General purpose I/O Contact A0 | I/O CMOS | 1.8V | | |
| GPIO_A_1 | E17 | General purpose I/O Contact A1 | I/O CMOS | 1.8V | | |
| GPIO_A_2 | F17 | General purpose I/O Contact A2 | I/O CMOS | 1.8V | | |
| GPIO_A_3 | G17 | General purpose I/O Contact A3 | I/O CMOS | 1.8V | | |
| GPIO_A_4 | H17 | General purpose I/O Contact A4 | I/O CMOS | 1.8V | | |
| GPIO_A_5 | J17 | General purpose I/O Contact A5 | I/O CMOS | 1.8V | | |
| GPIO_A_6 | K17 | General purpose I/O Contact A6 | I/O CMOS | 1.8V | | Dual function: SPI_A_CS1# |
| GPIO_A_7 | L17 | General purpose I/O Contact A7 | I/O CMOS | 1.8V | | Dual function: SPI_B_CS1# |

### 4.3.10 CAN Bus

| Contact Name | Contact Acronym | Functional Description | I/O Type | I/O Level (Size- 0 only, optional) | I/O Level (>Size-0) | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| CAN_A_TX | AC17 | CAN port A Transmit output | O CMOS | VCC_OUT_IO | 1.8V | | |
| CAN_A_RX | AB17 | CAN port A Receive input | I CMOS | VCC_OUT_IO | 1.8V | | |
| CAN_B_TX | AC19 | CAN port B Transmit output | O CMOS | VCC_OUT_IO | 1.8V | | |
| CAN_B_RX | AB19 | CAN port B Receive input | I CMOS | VCC_OUT_IO | 1.8V | | |

### 4.3.11 ADC

| Contact Name | Contact Acronym | Functional Description | I/O Type | I/O Level | PU / PD | Comments |
|---|---|---|---|---|---|---|
| ADC_0 | M18 | Analog Digital Converter 0 | Analog | 0V – 1.8V | | |
| ADC_1 | N18 | Analog Digital Converter 1 | Analog | 0V – 1.8V | | |

### 4.3.12 Power + Boot Select

| Contact Name | Contact Acronym | Functional Description | I/O Type | I/O Level | PU / PD | Comments |
|---|---|---|---|---|---|---|
| VCC_2_TEST[2] | M19 | Module power voltage testpoint | P | | | |
| VCC_3_TEST | Y16 | Module power voltage testpoint | P | | | |
| VCC_4_TEST | Y20 | Module power voltage testpoint | P | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| VCC_IN_5V | Y17 | Module power input voltage of 5V – Primary voltage rail for size S, M and L modules | P | | | Tolerance: 5V +-5% |
| VCC_IN_3V3 | Y19 | Module power input voltage of 3.3V – Primary voltage rail for 0 size modules | P | | | Tolerance: 3.3V +- 5% |
| V_BAT | AA18, AB18 | Module power input battery voltage | P | | | |
| GND | D18, E15, E21, F16, F20, J16, J20, L18, M16, M20, P18, R16, R20, V16, V20, Y18, AA14, AA17, AA19, AA22, AB15, AB21 | Module Signal and power return and GND reference | P | | | |
| SYS_RST# | U17 | Reset input from Carrier board. Carrier drives low to force a module reset, floats the line otherwise. | I OD CMOS | 1.8V | PU 10K | |
| CARRIER_PWR_EN | V17 | Carrier board circuits should not be powered up until the module asserts the CARRIER_PWR_EN signal | O CMOS | 1.8V | | |
| VCC_OUT_IO | U18 | Can provide IO voltage level for several interfaces to connect | P | 1.8V/3.3V | | Only applicable in size 0 – minimum current: 100mA;<br>All other sizes or feature not used: NC |
| RTC_PWR | W17 | Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier-based Lithium cell or Super Cap. | P | | | |
| BOOT_SEL0# | U19 | | I OD CMOS | 1.8V | PU 10k | The boot medium is the choice of the module vendor. |

| | | | | | | |
|---|---|---|---|---|---|---|
| BOOT_SEL1# | R18 | | I OD CMOS | 1.8V | PU 10k | The boot medium is the choice of the module vendor. |
| FORCE_RECOVERY# | T17 | If low on carrier board module enters recovery mode. | I OD CMOS | 1.8V | PU 10k | The recovery mode should be specified by module vendor. |
| Contact Name | Contact Acronym | Functional Description | I/O Type | I/O Level | PU / PD | Comments |
| VCC_5_TEST | Y3 | Module power voltage test point | P | | | |
| VCC_6_TEST | C5 | Module power voltage test point | P | | | |
| | | | | | | |
| VCC_IN_5V | Y8, Y9, Y10, Y11 | Module power input voltage of 5V | P | | | Tolerance:<br>5V +-5% |
| GND | A4, A7, A10, B2, B5, B8, B9, C11, D1, D5, D8, E2,<br>H2, H4, L2, L4, P2, P4, R1, U2, U4, V1, W3, Y2, AA1, AA4, AA7, AA8, AA10, AA11, AB3, AB6, AB9, AC4, AC7, AC10 | Module Signal and power return and GND reference | P | | | |
| PWR_BTN# | AA9 | Power-button input from Carrier board. Carrier to float the line in in-active state.<br>Active low, level sensitive. Should be de-bounced on the Module. | I OD CMOS | 1.8 to 5V | PU 10K | |
| Contact Name | Contact Acronym | Functional Description | I/O Type | I/O Level | PU / PD | Comments |

| | | | | | | |
|---|---|---|---|---|---|---|
| VCC_7_TEST | AA33 | Module power voltage testpoint | P | | | |
| VCC_8_TEST | B29 | Module power voltage testpoint | P | | | |
| | | | | | | |
| VCC_IN_5V | Y25, Y26, Y27, Y28 | Module power input voltage of 5V | P | | | Tolerance: 5V +-5% |
| GND | A26, A29, A32, B27, B28, B30, B33, | Module signal and power return and | P | | | |
| | C25, C32, C35, D28, D34, F33, F35, | GND reference | | | | |
| | G34, H32, J33, J35, K34, M35, N34, | | | | | |
| | T34, W34, AA25, AA26, AA27, AA28, | | | | | |
| | AA32, AB28, AB31, AB34, AC27, AC30, | | | | | |
| | AC33 | | | | | |
| Contact Name | Contact Acronym | Functional description | I/O Type | I/O Level | PU / PD | Comments |
| VCC_IN_5V | AE4, AF4, AG4, AH3, AH4, AJ3, AJ4, AK4 | Module power input voltage of 5V | P | | | Tolerance: 5V<br>-0.05 |

| | | | | | | |
|---|---|---|---|---|---|---|
| GND | AE2, AE34, AF35, AG3, AH2, AH34, AJ35, AK3, AL2, AL34, AM13, AM16, AM19, AM22, AM35, AN3, AN6, AN9, AN11, AN15, AN18, AN21, AN33, AP2, AP5, AP8, AP13, AP16, AP19, AP22, AP25, AP28, AP31, AP34, AR14, AR17, AR20, AR26, AR29, AR32 | Module signal, power return, and GND reference | P | | | |

# 5. Software Support

## 5.1. Early Access

The initial engineering versions of this product only supports Yocto

ALL software should use the standard NXP BSP release, with source code available on our GIT.**Deliverables**: Prebuilt runtime images will be available at launch for quick evaluation.

## 5.2. Yocto

All features will be supported on Yocto 64-bit BSP based on LTS kernel 5.4,

developed based on NXP Yocto upstream: https://github.com/Freescale/meta-freescale

**Deliverables**: Available on ADLINK GitHub Site (https://github.com/ADLINK/meta-adlink-nxp)

- Yocto meta layer with u-boot, kernel, root filesystem and middleware (MRAA/UPM library) recipes
- Yocto binary image for quick evaluation.
- A user guide to build BSP & deploy binary image

# 6. Mechanical

## 6.1. Module Dimensions

OSM L Size 45x45mm

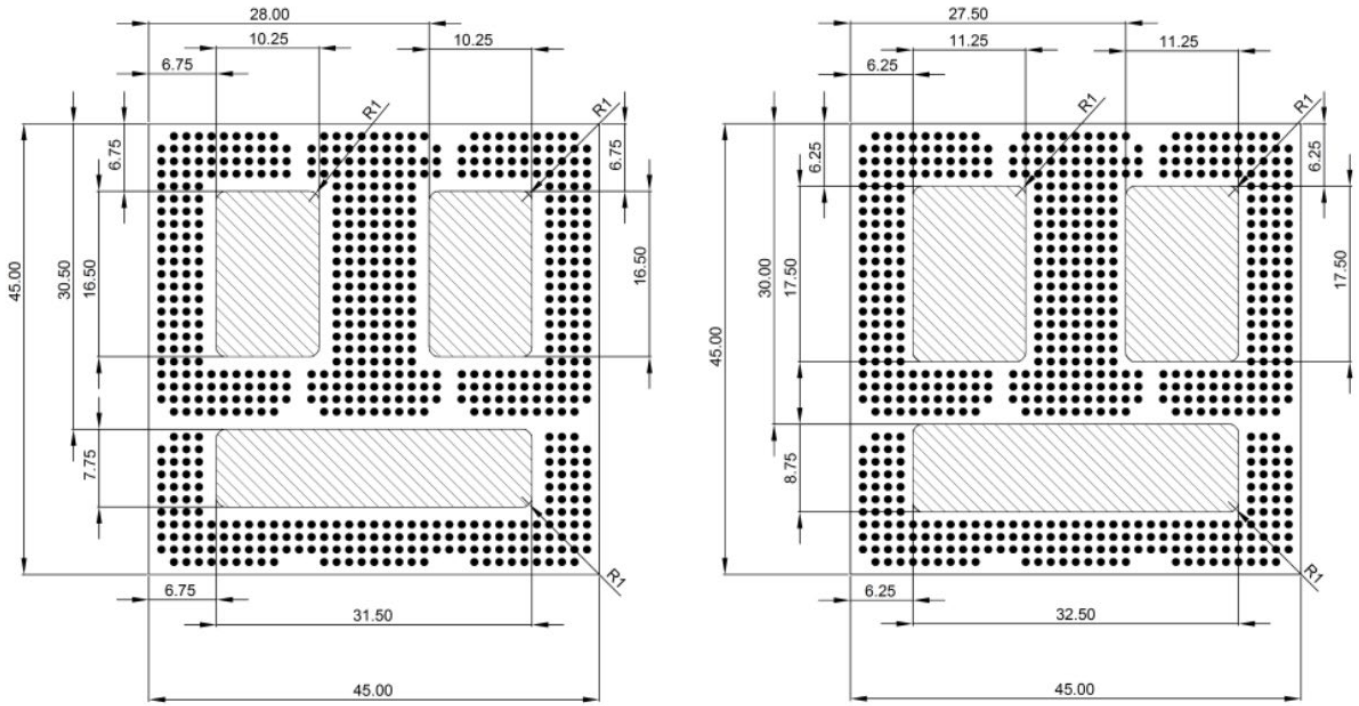


**Figure 4 – Placement area and Cut-out area – size L**

# 7. Thermal Solutions

## 7.1. Heatspreader : HTS

This isn't included in the module project, as it depends on the available space on the carrier. However, a standard heat solution is provided for the ADLINK carrier, which can be reused if needed.

## 7.2. Heatsink: THS

This isn't included in the module project, as it depends on the available space on the carrier. However, a standard heat solution is provided for the ADLINK carrier, which can be reused if needed.

## 7.3. DQA

All interfaces must undergo testing and validation. Since most of the PHYs are now situated on the carrier, the assembly shall be validated. Any additional hardware on future carriers will require validation on a case-by-case basis.