# OSM-MTK510

User's Guide

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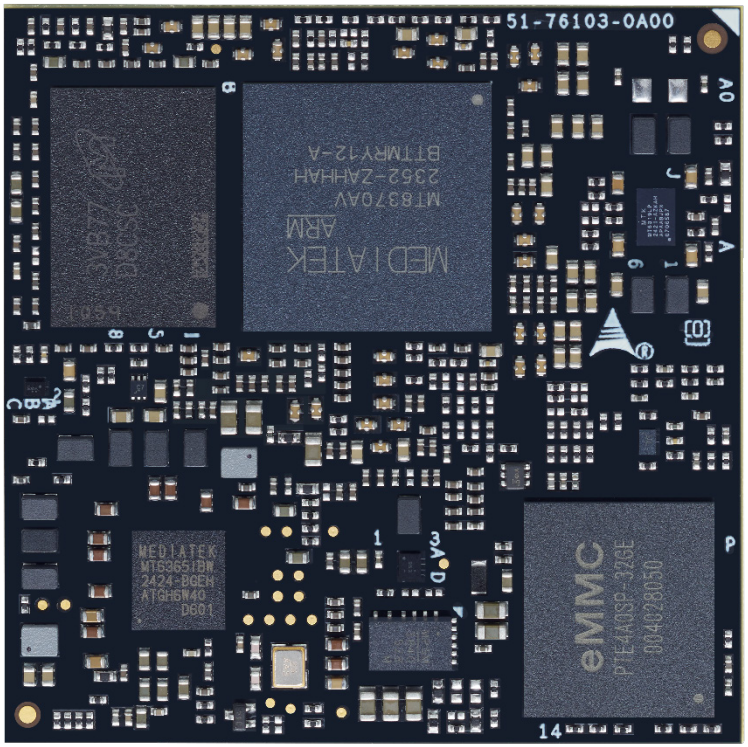


OPEN STANDARD MODULE ™


Revision: 1.1
Date: 2026-02-12
Part Number: 50M-76103-1010


ADLINK LEADING EDGE COMPUTING

# Revision History

| Revision | Description | Date | Author |
|---|---|---|---|
| 1.0 | Initial release | 2025-11-25 | AL |
| 1.1 | Specifications and block diagram updated | 2026-02-12 | AL |

# Preface

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## Safety Instructions

For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

Read these safety instructions carefully.

- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

## Conventions

The following conventions may be used throughout this manual, denoting special levels of information

**Note**: This information adds clarity or specifics to text and illustrations.

**Caution**: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

**Warning**: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

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# 1. Introduction

## 1.1 The OSM Form Factor

The OSM ("Open Standard Module") Open Standard Module™ specification facilitates the development, production, and distribution of embedded modules tailored for renowned MCU32, ARM, and x86 architectures. This standard is increasingly relevant for IoT applications, as it merges the benefits of modular embedded computing with the growing demands for cost efficiency, compactness, and versatile interfaces.

The modules serve as building blocks for portable and stationary embedded systems. They integrate the core CPU and support circuits, including DRAM, boot flash, power sequencing, and CPU power supplies. The modules are used with application-specific carrier boards to implement features such as audio CODECs, touch controllers, wireless devices, PHY, and more. The modular design not only promotes scalability and fast time to market but also ensures upgradability, all while maintaining low costs, low power consumption, and a compact physical size.

## 1.2 Brief

The OSM-MT510 is an OSM (Open Standard Module) size-L form factor for small-sized, low-cost embedded computer modules that are fully compliant with the SGET (Standardization Group for Embedded Technologies) OSM Specification Version 1.1.

OSM modules help combine the advantages of modular embedded computing with the increasing requirements for cost, space, and interfaces. The core of the OSM-MT510 is the MT8370 CPU, which integrates an ARM processor core, graphics, LPDDR4x memory controller, and I/O interfaces into a single system-on-chip solution. The OSM-MT510 also includes contemporary high-bandwidth interfaces such as PCI Express, USB 3.0/2.0, Gigabit Ethernet, CSI, I2S, HDMI, DP, eDP, DSI, and SDIO/eMMC.

SGeT STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

OSM module and carrier specifications are available online at: https://sget.org/standards/osm/

# 2. Specifications

## 2.1 Core System

**CPU**
2x ARM Cortex-A78 @2.0 GHz | 4x Cortex A55 @2.0 GHz
Ethos™ U-VP6 AI processing unit
ARM Cortex-A78 / A55 MP Core processors are high-performance and optimized for low power.

**Memory**
• LPDDR4-solder down memory, single chip
• 32-bit DRAM interface. Up to 8 GB

**L2 Cache**
64KB instruction L1 cache
64KB data cache
256KB L2 cache
Each core has its own cache

**Security**
• Arm TrustZone
• Security Boot (RSA4096)
• Crypto Engine
• RNG

## 2.2 Video

### 2.2.1 GPU

**GPU Core**
Mali G57 MC2

**Graphics Feature Support**
2x display video data processing pipelines, with the following support:
DP >4K @ 60H
eDP 1920 x 1440 @ 60H
HDMI 4K @ 60H
DSI FHD @60HZ

**Note**: DP/HDMI are BOM options.

### 2.2.2 Display Interfaces

**MIPI DSI**
1x MIPI DSI 4 lane Compliant to MIPI-DSI standard v1.2
Maximum resolution 1080p60 with 24-bit RGB

**HDMI/DP**
Maximum resolution up to 4K @60HZ

**eDP**

Maximum resolution 1920 x 1440 @ 60H

## 2.3 Camera

one 4-lane MIPI CSI2 camera input.

## 2.4 Audio

I2S to carrier

## 2.5 Wired Ethernet

**LAN**

Built in MAC 10/100/1000

Supports 10/100/1000-Mbps data transfer rates, both full-duplex and half-duplex

## 2.6 Extension busses

**USB**
1x USB 2.0, 1x USB 2.0 OTG, 1x USB 3.0

**UART**
4x UART interfaces (A: TX/RX/CTS/RTS; C & D: TX/RX; 1× console: TX/RX)

**SPI**
3x SPI

**I2S**
1x I2S interface supporting audio codec on carrier

**I2C**
6x I2C interfaces

- Support for 7-bit mode

- Software programmable clock frequency of 100 kbit/s in Standard-mode,

400 kbit/s in the Fast-mode or 1 Mbit/s in Fast-mode Plus

**GPIO**
19x GPIOs with interrupts

## 2.7 System Storage

**SDIO**
2x SDIO (4-bit) compatible with SD3.0

**eMMC**
32~ 256 GB (build option)

Compatible with eMMC specification 4.41, 4.51, 5.0 and 5.1

## 2.8 Power

| | |
|---|---|
| Power Modes: | ON / OFF / SUSPEND |
| *Power on / off behaviour same as x86* | *ATX (hold off boot until PWRBTN) / AT (always boot)* |
| Voltage Input: | 5.0V +/- 5% |
| Operating Temperatures | |
| Standard Operating Temperature: | 0°C to 60°C commercial grade BOM (memory, eMMC, SOC) |
| Extreme Rugged Operating Temperature: | -40°C + 85°C industrial grade BOM (memory, eMMC, SOC) |
| Derating for two different BOMs | |
| Environmental | |
| Humidity: | 5-90% RH operating, non-condensing<br>5-95% RH storage (and operating with conformal coating). |
| EMI: | EN55022 Class B inside an enclosure |
| Shock and Vibration: | HALT Testing, with test report that confirms Extended Operating Temp range during and after vibration.<br>Separate Shock test report to MIL-STD-202F, Method 213B, Table 213-I, Condition A.<br>IN ADDITION: When installed on baseboard shall operate under 18 sawtooth mechanical shocks (3 shocks in each direction) with a peak acceleration of 40g for a duration of 18 msec each and 75g for a duration of 6 msec each.<br><br>Capable of supporting Random Vibration: MIL-STD-202F, Method 214A, Table 214-I, Condition D.<br>If HALT testing shows equal or better performance, a separate vibration test report is not necessary. |
| MTBF : | 300,000 hrs (at 40°C), 100,000 hrs (at 85°C), |
| Two different BOM | 0°C-60°C<br>-40°C+85°C |

# 3. Block Diagram

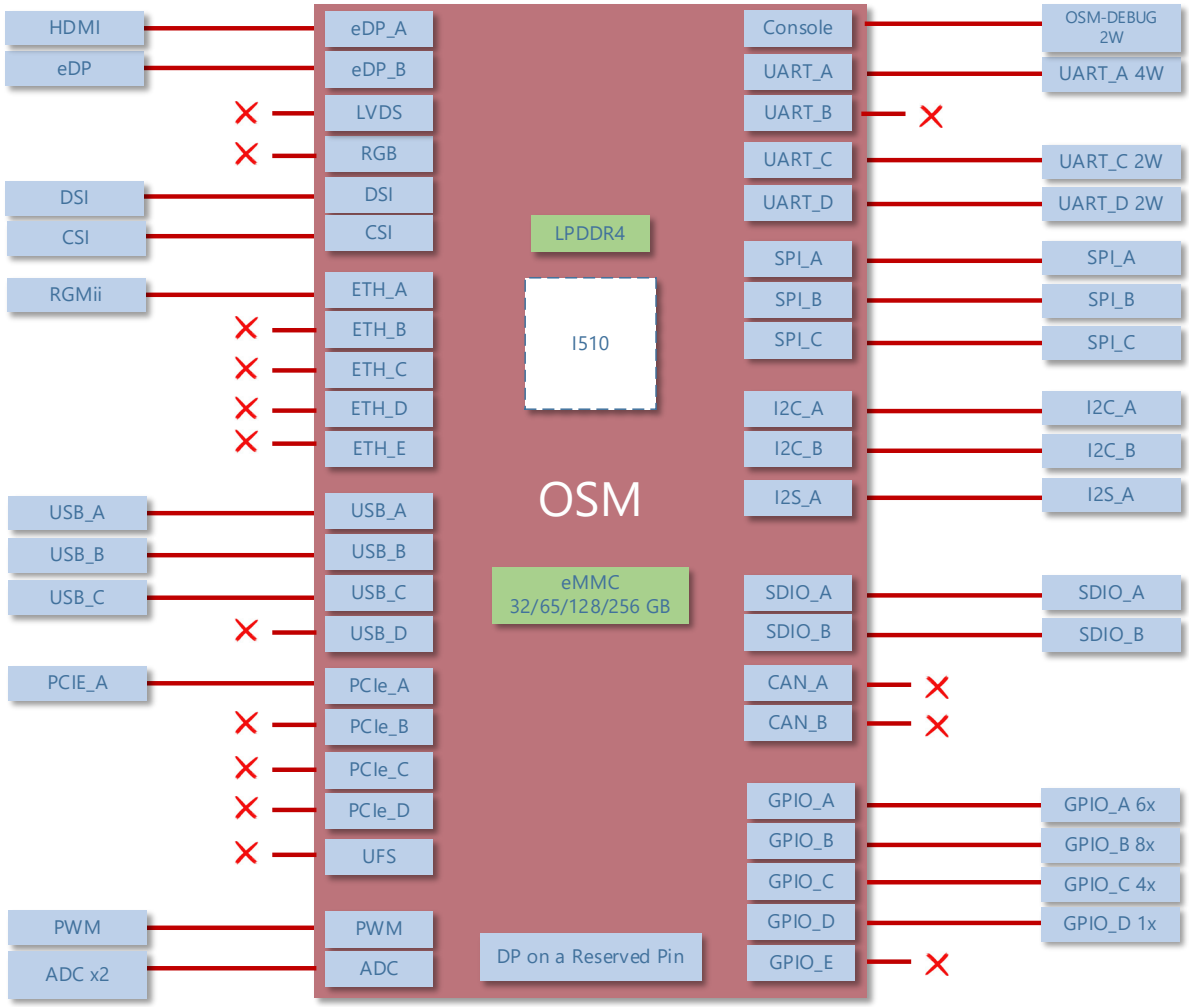


**Figure 1 – Module function diagram**

# 4. Pinout and Signal Descriptions

## 4.1 Pin Summary

The tables below are a list of all signals to the LGA pads following the OSM 1.2 specifications.

- Size-0 – "Zero": 30 mm x 15 mm
- Size-S – "Small": 30 mm x 30 mm
- Size-M – "Medium": 30 mm x 45 mm
- Size-L – "Large": 45 mm x 45 mm

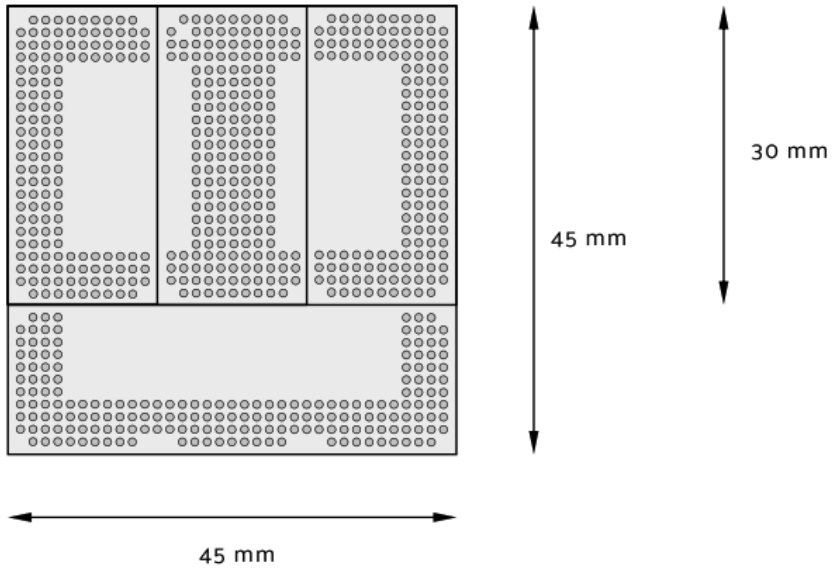


**Figure 2 – Module size grid**

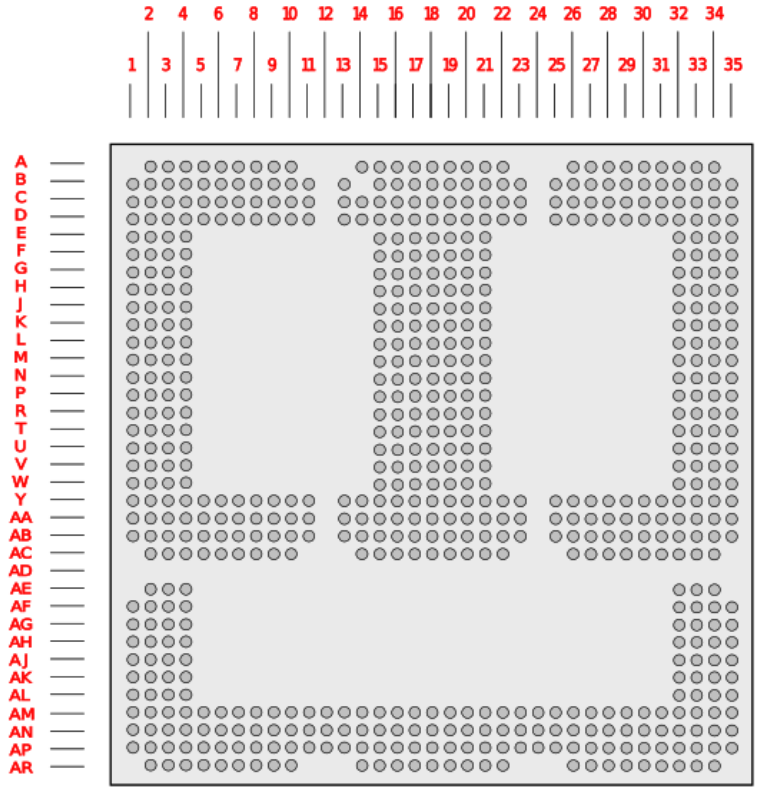


**Figure 21: Contact Grid (all sizes) (view from top, through the module)**

**Figure 3 – Module pinout grid**

## 4.2 Signal Terminology Descriptions

Meaning of the terms used for signal description tables. Signals described in the specification but not supported on the OSM-MTK510 are marked with strikethrough ~~STRIKETHROUGH~~.

| Term | Description |
|---|---|
| I | Input to the module |
| O | Output from the module |
| I/O | Bi-directional input/output |
| OD | Open drain |
| PU | PU (pull-up) resistor |
| PD | PD (pull-down) resistor |
| CMOS | Logic input or output |
| GBE MDI | Differential analogue signalling for gigabit media dependent interface |
| DP | Low voltage differential signal for DisplayPort interface |
| D-PHY | Low voltage differential signal for MIPI CSI-2 cameras and DSI displays |
| M-PHY | Low voltage differential signal for MIPI CSI-3 cameras |
| LVDS | Low voltage differential signal for LCD displays |
| PCIE | Low voltage differential signal for PCIe |
| SATA | Low voltage differential signal for SATA |
| TMDS HDMI | Transition minimized differential signal for HDMI displays |
| USB | DC coupled differential signalling for traditional (non-Superspeed) USB signals |
| USB SS | Differential signal for SuperSpeed USB signals |
| USB VBUS 5V | 5V tolerant input for USB VBUS detection |
| VDD_IN | Main power source from Carrier to module |
| 3.3V | 3.3V power domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e., both signals are high) |
| 1.8V | 1.8V power domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e., both signals are high) |
| 3.3Vsb | 3.3V standby power domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#) |
| 1.8Vsb | 1.8V standby power domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#) |
| Sleep | The module is in its lowest power state |
| Runtime | The module is full on. CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high) |
| Standby | The module is in standby state or higher |

## 4.3 Full Signal to Pad Table

| Contact Name | Contact Acronym | I/O Type | I/O Level | PU/PD | Net Name of Module OSM-MTK510 | Controller | Controller Pin Name | Description |
|---|---|---|---|---|---|---|---|---|
| GND | D18, E15, E21, F16, F20, J16, J20, L18, M16, M20, P18, R16, R20, V16, V20, Y18, AA14, AA17, AA19, AA22, AB15, AB21 | P | | | GND | | | Module signal and power return and GND reference |
| RESET_OUT# | T18 | O CMOS | VCC_OUT_IO | | OSM_nRST_OUT | Logic IC | | Reset output from the CPU to reset peripherals on the carrier. |
| RESET_IN# | U17 | I OD CMOS | VCC_OUT_IO | PU 10K | OSM_nRST_IN | Logic IC | | Reset input from the carrier board. The carrier drives the line low to force a module reset and leaves the line floating otherwise. |
| CARRIER_PWR_EN | V17 | O CMOS | VCC_OUT_IO | | CARRIER_PWR_EN | Logic IC | | The carrier board circuits should not be powered up until the module asserts the CARRIER_PWR_EN signal. |
| VCC_OUT_IO | U18 | P | 1.8V / 3.3V | | VIO18_PMU | MTK MT6365 | VIO18 | Can provide I/O voltage level for several interfaces to connect |
| RTC_PWR | W17 | P | | | VRTC28 | MTK MT6365 | L13 | Low current RTC circuit backup power – 3.0V nominal. May be sourced from a carrier based Lithium cell or Super Cap. |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| BOOT_SEL0# | U19 | I OD CMOS | VCC_OUT_IO | PU 10K | BOOT_SEL0_N | MOSFET | | |
| FORCE_RECOVERY# | T17 | I OD CMOS | VCC_OUT_IO | PU 10K | FORCE_RECOV# | MTK MT8370 | KPCOL0 | If low on the carrier board, the module enters recovery mode. |
| JTAG_TCK(SWCLK) | N17 | I CMOS | VCC_OUT_IO | | MT8370_JTCK | MTK MT8370 | JTCK | Test Clock |
| JTAG_TMS(SWDIO) | N19 | I CMOS | | | MT8370_JTMS | MTK MT8370 | JTMS | Test Mode Select |
| JTAG_TDI | P17 | I CMOS | | | MT8370_JTDI | MTK MT8370 | JTDI | Test Data Input |
| JTAG_TDO(SWO) | R17 | O CMOS | | | MT8370_JTDO | MTK MT8370 | JTDO | Test Data Output |
| JTAG_nTRST | R19 | I CMOS | | | MT8370_JTRST | MTK MT8370 | JTRST | Test Reset, Active Low |
| UART_A_RX | A14 | I CMOS | VCC_OUT_IO | | UART1_RXD | MTK MT8370 | UART1_RXD | Asynchronous serial data input port A |
| UART_A_TX | B13 | O CMOS | | | UART1_TXD | MTK MT8370 | UART1_TXD | Asynchronous serial data output port A |
| UART_A_RTS | C13 | O CMOS | | | UART1_RTS | MTK MT8370 | GPIO02 | Request to Send handshake line for port A |
| UART_A_CTS | C14 | I CMOS | | | UART1_CTS | MTK MT8370 | GPIO03 | Clear to Send handshake line for port A |
| UART_C_RX | A22 | I CMOS | VCC_OUT_IO | | UART2_RXD | MTK MT8370 | UART2_RXD | Asynchronous serial data input port C |
| UART_C_TX | B23 | O CMOS | | | UART2_TXD | MTK MT8370 | UART2_TXD | Asynchronous serial data output port C |
| UART_D_RX | C22 | I CMOS | VCC_OUT_IO | | UART3_RXD | MTK MT8370 | I2SO2_D3 | Asynchronous serial data input port D |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| UART_D_TX | C23 | O CMOS | | | UART3_TXD | MTK MT8370 | I2SO2_D2 | Asynchronous serial data output port D |
| UART_CON_RX | D22 | I CMOS | VCC_OUT_IO | | UART0_RXD | MTK MT8370 | UART0_RXD | Asynchronous serial data input port console |
| UART_CON_TX | D23 | O CMOS | | | UART0_TXD | MTK MT8370 | UART0_TXD | Asynchronous serial data output port console |
| ETH_A_(R)(G)MII_COL | F15 | I CMOS | 1.8V /2.5V / 3.3V | | GBE_COL_1V8 | MTK MT8370 | DPI_HSYNC | Collision detects (half speed only) port A |
| ETH_A_(S)(R)(G)MII_TXD0 | H15 | O CMOS | | | GBE_TXD0_1V8 | MTK MT8370 | DPI_D3 | Transmit data bit 0 (transmitted first) port A |
| ETH_A_(S)(R)(G)MII_TXD1 | G15 | O CMOS | | | GBE_TXD1_1V8 | MTK MT8370 | DPI_D2 | Transmit data bit 1 port A |
| ETH_A_(S)(R)(G)MII_TXD2 | H16 | O CMOS | | | GBE_TXD2_1V8 | MTK MT8370 | DPI_D1 | Transmit data bit 2 port A |
| ETH_A_(S)(R)(G)MII_TXD3 | G16 | O CMOS | | | GBE_TXD3_1V8 | MTK MT8370 | DPI_D0 | Transmit data bit 3 port A |
| ETH_A_(R)(G)MII_TX_EN(_ER) | K16 | O CMOS | | | GBE_TXEN_1V8 | MTK MT8370 | DPI_D11 | Transmit enable (Error) port A |
| ETH_A_(R)(G)MII_TX_CLK | J15 | I/O CMOS | | | GBE_TXC_1V8 | MTK MT8370 | DPI_D8 | Transmit clock port A |
| ETH_A_(S)(R)(G)MII_RXD0 | K15 | I CMOS | | | GBE_RXD0_1V8 | MTK MT8370 | DPI_D7 | Receive data bit 0 (received first) port A |
| ETH_A_(S)(R)(G)MII_RXD1 | L15 | I CMOS | | | GBE_RXD1_1V8 | MTK MT8370 | DPI_D6 | Receive data bit 1 port A |
| TH_A_(R)(G)MII_RXD2 | N15 | I CMOS | | | GBE_RXD2_1V8 | MTK MT8370 | DPI_D5 | Receive data bit 2 port A |
| ETH_A_(R)(G)MII_RXD3 | P15 | I CMOS | | | GBE_RXD3_1V8 | MTK MT8370 | DPI_D4 | Receive data bit 3 port A |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| ETH_A_(R)(G)MII_RX_ER | L16 | I CMOS | | | GBE_RXER_1V8 | MTK MT8370 | DPI_D15 | Receive error port A |
| ETH_A_(R)(G)MII_RX_DV(_ER) | M15 | I CMOS | | | GBE_RXDV_1V8 | MTK MT8370 | DPI_D10 | Receive data valid port A |
| ETH_A_(R)(G)MII_RX_CLK | R15 | I/O CMOS | | | GBE_RXC_1V8 | MTK MT8370 | DPI_D9 | Receive clock port A |
| ETH_MDIO | T15 | I/O CMOS | | | GBE_MDIO_1V8 | MTK MT8370 | DPI_D13 | Management bus data signal for Ethernet |
| ETH_MDC | T16 | O CMOS | | | GBE_MDC_1V8 | MTK MT8370 | DPI_D12 | Management bus clock signal for Ethernet |
| ETH_IOPWR | M17 | PO | | | VIO18_PMU | MTK MT6365 | VIO18 | ETH voltage. It is used to provide the I/O Voltage Level for all Ethernet interfaces. |
| GPIO_A_0 | D17 | I/O CMOS | VCC_OUT_IO | | GPIO_02 | MTK MT8370 | SPIM0_MOSI | General purpose I/O Contact A0 |
| GPIO_A_1 | E17 | | | | GPIO_04 | MTK MT8370 | SPIM0_MIO2 | General purpose I/O Contact A1 |
| GPIO_A_2 | F17 | | | | GPIO_05 | MTK MT8370 | SPIM0_MIO3 | General purpose I/O Contact A2 |
| GPIO_A_3 | G17 | | | | GPIO_03 | MTK MT8370 | SPIM0_MIO1 | General purpose I/O Contact A3 |
| GPIO_A_4 | H17 | | | | GBE_TXER_1V8 | MTK MT8370 | DPI_D14 | General purpose I/O Contact A4 |
| GPIO_A_5 | J17 | | | | GBE_INTR_1V8 | MTK MT8370 | DPI_D15 | General purpose I/O Contact A5 |
| GPIO_B_0 | D19 | | | | GPIO_12 | MTK MT8370 | GPIO12 | General purpose I/O Contact B0 |
| GPIO_B_1 | E19 | | | | GPIO_13 | MTK MT8370 | GPIO13 | General purpose I/O Contact B1 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| GPIO_B_2 | F19 | | | | GPIO_14 | MTK MT8370 | GPIO14 | General purpose I/O Contact B2 |
| GPIO_B_3 | G19 | | | | GPIO_15 | MTK MT8370 | GPIO15 | General purpose I/O Contact B3 |
| GPIO_B_4 | H19 | | | | GPIO_17 | MTK MT8370 | I2SIN_WS | General purpose I/O Contact B4 |
| GPIO_B_5 | J19 | | | | GPIO_08 | MTK MT8370 | CMMRST1 | General purpose I/O Contact B5 |
| GPIO_B_6 | K19 | | | | GPIO_06 | MTK MT8370 | CMMPDN1 | General purpose I/O Contact B6 |
| GPIO_B_7 | L19 | | | | GPIO_01 | MTK MT8370 | GPIO01 | General purpose I/O Contact B7 |
| SDIO_A_CMD | E20 | I/O CMOS | 1.8V / 3.3V | | MSDC1_CMD | MTK MT8370 | MSDC1_CMD | SDIO A Command/Response: This signal is used for card initialization and for command transfers. During initialization, this signal is open-drain. During command transfers, this signal is in push-pull mode. |
| SDIO_A_CLK | F21 | O CMOS | | | MSDC1_CLK | MTK MT8370 | MSDC1_CLK | SDIO A Clock: With each cycle of this signal, a one-bit transfer occurs on the command and each of the data line. |
| SDIO_A_D0 | G20 | I/O CMOS | | | MSDC1_DAT0 | MTK MT8370 | MSDC1_DAT0 | SDIO A Data lines: These signals operate in push-pull mode. |
| SDIO_A_D1 | G21 | I/O CMOS | | | MSDC1_DAT1 | MTK MT8370 | MSDC1_DAT1 | SDIO A Data lines: These signals operate in push-pull mode. |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| SDIO_A_D2 | H20 | I/O CMOS | | | MSDC1_DAT2 | MTK MT8370 | MSDC1_DAT2 | SDIO A Data lines: These signals operate in push-pull mode. |
| SDIO_A_D3 | H21 | I/O CMOS | | | MSDC1_DAT3 | MTK MT8370 | MSDC1_DAT3 | SDIO A Data lines: These signals operate in push-pull mode. |
| SDIO_A_CD# | J21 | I OD CMOS | | PU 10K | MSDC1_INSI | MTK MT8370 | GPIO06 | SDIO A Card Detect: This signal indicates when a SDIO/MMC card is present. |
| SDIO_A_WP | D20 | I OD CMOS | | PU 10K | MSDC1_WP | MTK MT8370 | GPIO05 | SDIO A Write Protect: This signal denotes the state of the write-protect tab on SD cards. |
| SDIO_A_PWR_EN | D21 | O CMOS | | | EXT_VMSDC1_EN | MTK MT8370 | GPIO04 | SDIO A Power Enabled: This signal is used to enable the power being supplied to a SD/MMC card device. |
| SDIO_A_IOPWR | C20 | PO | | | VSIM1_PMU | MTK MT6365 | VSIM1 | SDIO A Voltage: It is used to provide the I/O Voltage Level |
| SDIO_B_CLK | K20 | O CMOS | | | MSDC2_CLK | MTK MT8370 | MSDC2_CLK | SDIO B Clock: With each cycle of this signal, a one-bit transfer occurs on the command and each of the data line. |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| SDIO_B_CMD | K21 | I/O CMOS | | | MSDC2_CMD | MTK MT8370 | MSDC2_CMD | SDIO B Command/Response: This signal is used for card initialization and for command transfers. During initialization, this signal is open-drain. During the command transfers, this signal is in push-pull mode. |
| SDIO_B_D0 | L20 | I/O CMOS | | | MSDC2_DAT0 | MTK MT8370 | MSDC2_DAT0 | SDIO B Data lines: These signals operate in push-pull mode. |
| SDIO_B_D1 | L21 | I/O CMOS | | | MSDC2_DAT1 | MTK MT8370 | MSDC2_DAT1 | SDIO B Data lines: These signals operate in push-pull mode. |
| SDIO_B_D2 | M21 | I/O CMOS | | | MSDC2_DAT2 | MTK MT8370 | MSDC2_DAT2 | SDIO B Data lines: These signals operate in push-pull mode. |
| SDIO_B_D3 | N20 | I/O CMOS | | | MSDC2_DAT3 | MTK MT8370 | MSDC2_DAT3 | SDIO B Data lines: These signals operate in push-pull mode. |
| SDIO_B_IOPWR | T20 | PO | | | VIO18_PMU | MTK MT6365 | VIO18 | SDIO B Voltage: It is used to provide the I/O Voltage Level |
| PWM_0 | E18 | O CMOS | VCC_OUT_IO | | DSI0_DISP_PWM | MTK MT8370 | DISP_PWM0 | Pulse width modulation 0 |
| PWM_1 | F18 | O CMOS | | | OSM_PWM_1 | MTK MT8370 | CMMCLK1 | Pulse width modulation 1 |
| PWM_2 | G18 | O CMOS | | | OSM_PWM_2 | MTK MT8370 | CMMCLK2 | Pulse width modulation 2 |
| PWM_3 | H18 | O CMOS | | | OSM_PWM_3 | MTK MT8370 | GPIO09 | Pulse width modulation 3 |
| PWM_4 | J18 | O CMOS | | | OSM_PWM_4 | MTK MT8370 | GPIO10 | Pulse width modulation 4 |

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|---|---|---|---|---|---|---|---|---|
| ADC_0 | M18 | Analog | 0V – 1.8V | | AUXIN1_1V8 | MTK MT8370 | AUXIN1 | Analog Digital Converter 0 |
| ADC_1 | N18 | Analog | | | AUXIN2_1V8 | MTK MT8370 | AUXIN2 | Analog Digital Converter 1 |
| SPI_A_SDI_(IO0) | U15 | I/O CMOS | VCC_OUT_IO | | SPINOR_IO0 | MTK MT8370 | DMIC1_DAT_R | SPI A Serial Data Input |
| SPI_A_SDO_(IO1) | V15 | I/O CMOS | | | SPINOR_IO1 | MTK MT8370 | DMIC2_CLK | SPI A Serial Data Output |
| SPI_A_/WP_(IO2) | W16 | I/O CMOS | | | SPINOR_IO2 | MTK MT8370 | DMIC2_DAT | SPI A Write Protect |
| SPI_A_/HOLD_(IO3) | W15 | I/O CMOS | | | SPINOR_IO3 | MTK MT8370 | DMIC2_DAT_R | SPI A Suspends Serial Input |
| SPI_A_CS0# | Y15 | O CMOS | | | SPINOR_CS_N | MTK MT8370 | DMIC1_DAT | SPI A Master Chip Select 0 |
| SPI_A_SCK | U16 | O CMOS | | | SPINOR_CLK | MTK MT8370 | DMIC1_CLK | SPI A Serial Data Clock |
| SPI_B_SDI | Y22 | I CMOS | | | SPIM1_MOSI | MTK MT8370 | SPIM1_MOSI | SPI B Serial Data Input |
| SPI_B_SDO | Y23 | O CMOS | | | SPIM1_MISO | MTK MT8370 | SPIM1_MISO | SPI B Serial Data Output |
| SPI_B_CS0# | AA23 | O CMOS | | | SPIM1_CS_N | MTK MT8370 | SPIM1_CS | SPI B Master Chip Select 0 |
| SPI_B_SCK | Y21 | O CMOS | | | SPIM1_CLK | MTK MT8370 | SPIM1_CLK | SPI B Serial Data Clock |
| I2S_A_DATA_IN | V21 | I/O CMOS | VCC_OUT_IO | | I2S_IN_D0 | MTK MT8370 | I2SIN_D0 | I2S A Digital audio Input |
| I2S_A_DATA_OUT | W21 | | | | I2S_OUT_D0 | MTK MT8370 | I2SO2_D0 | I2S A Digital audio Output |
| I2S_B_DATA_IN | V19 | | | | | | | I2S B Digital audio Input |

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|---|---|---|---|---|---|---|---|---|
| I2S_B_DATA_OUT | W19 | | | | | | | I2S B Digital audio Output |
| I2S_MCLK | V18 | | | | I2S_IO_MCK | MTK MT8370 | I2SO2_MCK | Master clock output to I2S codec(s) |
| I2S_LRCLK | W18 | | | | I2S_IO_WS | MTK MT8370 | I2SO2_WS | I2S Left & Right synchronization clock |
| I2S_BITCLK | W20 | | | | I2S_IO_BCK | MTK MT8370 | I2SO2_BCK | I2S Digital audio clock |
| USB_A_D_N | AB13 | I/O USB | USB | | USB_DM_P0 | MTK MT8370 | USB_DM_P0 | USB differential data pairs for port A |
| USB_A_D_P | AC14 | I/O USB | USB | | USB_DP_P0 | MTK MT8370 | USB_DP_P0 | USB differential data pairs for port A |
| USB_A_ID | AB14 | I OD CMOS | VCC_OUT_IO | PU 10k | USB0_IDDIG | MTK MT8370 | USB0_IDDIG | Input Contact to announce OTG device insertion on USB 2.0 port |
| USB_A_OC# | AC15 | I OD CMOS | VCC_OUT_IO | PU 10k | USB0_OC_N | MTK MT8370 | KPCOL1 | USB over-current for port A |
| USB_A_VBUS | AB16 | I USB VBUS 5V | 5V | | USB0_VBUS_5V | MTK MT8370 | USB0_VBUS_VALID | USB port 0 port power detection |
| USB_A_EN | AC16 | O CMOS | VCC_OUT_IO | | USB0_DRV_VBUS | MTK MT8370 | USB0_DRV_VBUS | Power enables for USB VBUS voltage |
| USB_B_D_N | AB23 | I/O USB | USB | | USB_DM_P2 | MTK MT8370 | USB_DM_P2 | USB differential data pairs for port B |
| USB_B_D_P | AC22 | I/O USB | USB | | USB_DP_P2 | MTK MT8370 | USB_DP_P2 | USB differential data pairs for port B |
| USB_B_ID | AB22 | I OD CMOS | 1.8V | PU 10k | USB2_IDDIG | MTK MT8370 | USB2_IDDIG | Input Contact to announce OTG device insertion on th eUSB 2.0 port |

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|---|---|---|---|---|---|---|---|---|
| USB_B_OC# | AC21 | I OD CMOS | 1.8V | PU 10k | USB2_OC_N | MTK MT8370 | SPIM0_CLK | USB over-current for port B |
| USB_B_VBUS | AB20 | I USB VBUS 5V | 5V | | USB2_VBUS_5V | MTK MT8370 | USB2_VBUS_VALID | USB port 0 port power detection |
| USB_B_EN | AC20 | O CMOS | 1.8V | | USB2_DRV_VBUS | MTK MT8370 | USB2_DRV_VBUS | Power enable for USB VBUS voltage |
| I2C_A_SCL | AA15 | I/O OD CMOS | VCC_OUT_IO, Size-0 only 1.8V, >Size-0 | PU 2k2 | SCL0_A | MTK MT8370 | SCL0 | I2C Port A Clock Signal |
| I2C_A_SDA | AA16 | | | | SDA0_A | MTK MT8370 | SDA0 | I2C Port A Data Signal |
| I2C_B_SCL | AA20 | | | | SCL2_B | MTK MT8370 | SCL2 | I2C Port B Clock Signal |
| I2C_B_SDA | AA21 | | | | SDA2_B | MTK MT8370 | SDA2 | I2C Port B Data Signal |
| RESERVED | T19, Y13, Y14, AA13 | | | | | | | Reserved for future use |
| Vendor Defined | B22, C16, P16 | | | | | | | Defined by module manufacturer |
| GND | A4, A7, A10, B2, B5, B8, B9, C11, D1, D5, D8, E2, H2, H4, L2, L4, P2, P4, R1, U2, U4, V1, W3, Y2, AA1, AA4, AA7, AA8, AA10, AA11, AB3, AB6, AB9, AC4, AC7, AC10 | P | | | GND | | | Module signal and power return and GND reference |

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|---|---|---|---|---|---|---|---|---|
| PWR_BTN# | AA9 | I OD CMOS | 1.8 to 5V | PU 10K | PWR_KEY_N | MTK MT6365 | PWRKEY | Power-button input from the carrier board. The carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the module. |
| GPIO_C_0 | D3 | I/O CMOS | VCC_OUT_IO | | GPIO_00 | MTK MT8370 | GPIO00 | General purpose I/O Contact C0 |
| GPIO_C_1 | D4 | I/O CMOS | | | GPIO_11 | MTK MT8370 | GPIO11 | General purpose I/O Contact C1 |
| GPIO_C_2 | E3 | I/O CMOS | | | GPIO_09 | MTK MT8370 | DSI1_LCM_RST | General purpose I/O Contact C2 |
| GPIO_C_3 | E4 | I/O CMOS | | | GPIO_07 | MTK MT8370 | GPIO07 | General purpose I/O Contact C3 |
| GPIO_C_4 | F3 | I/O CMOS | | | DISP_VDD_EN | MTK MT8370 | I2SIN_D1 | General purpose I/O Contact C4 |
| GPIO_C_5 | F4 | I/O CMOS | | | DISP_BL_EN | MTK MT8370 | KPROW1 | General purpose I/O Contact C5 |
| DSI_DATA0_N | AB11 | O LVDS D-PHY | | | DSI0_D0N | MTK MT8370 | DSI0_D0N_T1A | DSI differential output (point to point) |
| DSI_DATA0_P | AB10 | O LVDS D-PHY | | | DSI0_D0P | MTK MT8370 | DSI0_D0P_T0C | DSI differential output (point to point) |
| DSI_DATA1_N | AC9 | O LVDS D-PHY | | | DSI0_D1N | MTK MT8370 | DSI0_D1N_T2B | DSI differential output (point to point) |
| DSI_DATA1_P | AC8 | O LVDS D-PHY | | | DSI0_D1P | MTK MT8370 | DSI0_D1P_T2A | DSI differential output (point to point) |
| DSI_DATA2_N | AC6 | O LVDS D-PHY | | | DSI0_D2N | MTK MT8370 | DSI0_D2N_T0B | DSI differential output (point to point) |
| DSI_DATA2_P | AC5 | O LVDS D-PHY | | | DSI0_D2P | MTK MT8370 | DSI0_D2P_T0A | DSI differential output (point to point) |

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|---|---|---|---|---|---|---|---|---|
| DSI_DATA3_N | AB5 | O LVDS D-PHY | | | DSI0_D3N | MTK MT8370 | DSI0_D3N | DSI differential output (point to point) |
| DSI_DATA3_P | AB4 | O LVDS D-PHY | | | DSI0_D3P | MTK MT8370 | DSI0_D3P_T2C | DSI differential output (point to point) |
| DSI_CLOCK_N | AB8 | O LVDS D-PHY | | | DSI0_CKN | MTK MT8370 | DSI0_CKN_T1C | DSI differential clock output (point to point) |
| DSI_CLOCK_P | AB7 | O LVDS D-PHY | | | DSI0_CKP | MTK MT8370 | DSI0_CKP_T1B | DSI differential clock output (point to point) |
| DSI_TE | AA3 | I CMOS | VCC_OUT_IO | | DSI0_TE | MTK MT8370 | DSI0_DSI_TE | DSI panel tearing effect signal |
| DISP_VDD_EN / GPIO_C_4 | F3 | O CMOS | VCC_OUT_IO | | DISP_VDD_EN | MTK MT8370 | I2SIN_D1 | Primary Display power enable, active high |
| DISP_BL_EN / GPIO_C_5 | F4 | O CMOS | VCC_OUT_IO | | DISP_BL_EN | MTK MT8370 | KPROW1 | Primary Display backlight enable, active high |
| CSI_DATA0_N | C1 | I LVDS D-PHY / I LVDS M-PHY | | | CSI0_DAT0_N | MTK MT8370 | CSI0A_L1N_T1A | CSI differential input (point to point) |
| CSI_DATA0_P | B1 | | | | CSI0_DAT0_P | MTK MT8370 | CSI0A_L1P_T0C | CSI differential input (point to point) |
| CSI_DATA1_N | A2 | | | | CSI0_DAT1_N | MTK MT8370 | CSI0B_L0N_T0B | CSI differential input (point to point) |
| CSI_DATA1_P | A3 | | | | CSI0_DAT1_P | MTK MT8370 | CSI0B_L0P_T0A | CSI differential input (point to point) |
| CSI_DATA2_N | A5 | | | | CSI0_DAT2_N | MTK MT8370 | CSI0A_L0N_T0A | CSI differential input (point to point) |
| CSI_DATA2_P | A6 | | | | CSI0_DAT2_P | MTK MT8370 | CSI0A_L0P_T0B | CSI differential input (point to point) |
| CSI_DATA3_N | B6 | | | | CSI0_DAT3_N | MTK MT8370 | CSI0B_L1N_T1A | CSI differential input (point to point) |

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|---|---|---|---|---|---|---|---|---|
| CSI_DATA3_P | B7 | | | | CSI0_DAT3_P | MTK MT8370 | CSI0B_L1P_T0C | CSI differential input (point to point) |
| CSI_CLOCK_N | B3 | I LVDS D-PHY | | | CSI0_CLK_N | MTK MT8370 | CSI0A_L2N_T1C | CSI differential clock input (point to point) |
| CSI_CLOCK_P | B4 | I LVDS D-PHY | | | CSI0_CLK_P | MTK MT8370 | CSI0A_L2P_T1B | CSI differential clock input (point to point) |
| CAM_MCK | C2 | O CMOS | VCC_OUT_IO | | CMMCLK0 | MTK MT8370 | CMMCLK0 | Master clock output |
| I2C_CAM_SDA / CSI_TX_N | C3 | I/O OD CMOS / O LVDS M-PHY | VCC_OUT_IO | PU 2k2 | SDA5_CAM | MTK MT8370 | SDA5 | I2C data for serial camera data support link or differential data lane |
| I2C_CAM_SCL / CSI_TX_P | C4 | I/O OD CMOS / O LVDS M-PHY | VCC_OUT_IO | PU 2k2 | SCL5_CAM | MTK MT8370 | SCL5 | I2C clock for serial camera data support link or differential data lane |
| CAM_PWR / GPIO_C_6 | G3 | O CMOS | VCC_OUT_IO | | CAM_PWR_EN | MTK MT8370 | CMMPDN0 | Camera 0 Power Enable, active high output. |
| CAM_RST# / GPIO_C_7 | G4 | O CMOS | VCC_OUT_IO | | CMMRST0_N | MTK MT8370 | CMMRST0 | Camera 0 reset, active low output |
| USB_C_D_N | D11 | I/O USB | USB | | USB_DM_P1 | MTK MT8370 | USB_DM_P1 | USB differential data pairs for port C |
| USB_C_D_P | D10 | I/O USB | USB | | USB_DP_P1 | MTK MT8370 | USB_DP_P1 | USB differential data pairs for port C |
| USB_C_ID | D9 | I OD CMOS | VCC_OUT_IO | PU 10K | USB1_IDDIG | MTK MT8370 | USB1_IDDIG | Input Contact to announce OTG device insertion on USB 2.0 port |
| USB_C_OC# | C8 | I OD CMOS | VCC_OUT_IO | PU 10K | USB1_OC_N | MTK MT8370 | KPROW0 | USB over-current for port C |

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|---|---|---|---|---|---|---|---|---|
| USB_C_VBUS | C9 | I USB VBUS 5V | 5V | | USB1_VBUS_5V | MTK MT8370 | USB1_VBUS_VALID | USB port 0 port power detection |
| USB_C_EN | C10 | O CMOS | VCC_OUT_IO | | USB1_DRV_VBUS | MTK MT8370 | USB1_DRV_VBUS | Power enable for USB VBUS voltage |
| USB_C_SSTX_N | A9 | O USB SS | USB SS | | SSUSB_TXN_P1 | MTK MT8370 | SSUSB_TXN | Transmit signal differential pairs for SuperSpeed on port C |
| USB_C_SSTX_P | A8 | O USB SS | USB SS | | SSUSB_TXP_P1 | MTK MT8370 | SSUSB_TXP | Transmit signal differential pairs for SuperSpeed on port C |
| USB_C_SSRX_N | B11 | I USB SS | USB SS | | SSUSB_RXN_P1 | MTK MT8370 | SSUSB_RXN | Receive signal differential pairs for SuperSpeed on port C |
| USB_C_SSRX_P | B10 | I USB SS | USB SS | | SSUSB_RXP_P1 | MTK MT8370 | SSUSB_RXP | Receive signal differential pairs for SuperSpeed on port C |
| PCIe_A_HSI0_P | AB1 | I LVDS PCIE | | | PCIEG2_L0_RXP | MTK MT8370 | PCIE_LN0_RXP | Differential PCIe link A receive data pair |
| PCIe_A_HSI0_N | AB2 | I LVDS PCIE | | | PCIEG2_L0_RXN | MTK MT8370 | PCIE_LN0_RXN | Differential PCIe link A receive data pair |
| PCIe_A_HSO0_P | AC2 | O LVDS PCIE | | | PCIEG2_L0_TXP | MTK MT8370 | PCIE_LN0_TXP | Differential PCIe link A transmit data pair |
| PCIe_A_HSO0_N | AC3 | O LVDS PCIE | | | PCIEG2_L0_TXN | MTK MT8370 | PCIE_LN0_TXN | Differential PCIe link A transmit data pair |
| PCIe_CLKREQ# | W2 | I OD CMOS | VCC_OUT_IO | PU 10k | PCIEG2_CLKREQ_N | MTK MT8370 | PCIE_CLKREQ | PCIe reference clock request |
| PCIe_A_PERST# | V21 | O CMOS | VCC_OUT_IO | | PCIEG2_PERESET_N | MTK MT8370 | PCIE_PERESET | PCIe Port A reset output |
| PCIe_REFCLK_P | W1 | O LVDS PCIE | | PD 49.9 (MTK request) | PCIEG2_CLK_P | MTK MT8370 | PCIE_CKP | Differential PCIe reference clock output |
| PCIe_REFCLK_N | Y1 | O LVDS PCIE | | PD 49.9 (MTK request) | PCIEG2_CLK_N | MTK MT8370 | PCIE_CKN | Differential PCIe reference clock output |

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| PCIe_WAKE# | T2 | I OD CMOS | VCC_OUT_IO | PU 10k | PCIEG2_WAKE_N | MTK MT8370 | PCIE_WAKE | PCIe wake up interrupt to host – common to PCIe links A, B, C, D |
| PCIe_SMDAT | U1 | I/O OD CMOS | VCC_OUT_IO | PU 2k2 | SDA3_PCIE | MTK MT8370 | SDA3 | System management I2C bus DATA |
| PCIe_SMCLK | T1 | O OD CMOS | VCC_OUT_IO | PU 2k2 | SCL3_PCIE | MTK MT8370 | SCL3 | System management I2C bus CLK |
| PCIe_SM_ALERT# | R2 | I OD CMOS | VCC_OUT_IO | PU 2k2 | PCIE_SM_ALERT_N | MTK MT8370 | SPIM0_CS | SMBus Alert# (interrupt) signal |
| DSI0_RST (Vendor Defined) | D6 | O | 1.8V | | DSI0_RST | MTK MT8370 | DSI0_LCM_RST | Defined by module manufacturer |
| VCC_IN_5V | Y25, Y26, Y27, Y28 | P | | | VCC_IN_5V | Buck IC | | Module power input voltage of 5V |
| GND | A26, A29, A32, B27, B28, B30, B33, C25, C32, C35, D28, D34, F33, F35, G34, H32, J33, J35, K34, M35, N34, T34, W34, AA25, AA26, AA27, AA28, AA32, AB28, AB31, AB34, AC27, AC30, AC33 | P | | | GND | | | Module signal and power return and GND reference |
| GPIO_D_0 | U32 | I/O CMOS | 1.8V | | GPIO_16 | MTK MT8370 | DSI1_DSI_TE | General purpose I/O Contact D0 |
| SPI_C_SDI | C29 | I CMOS | 1.8V | | SPIM2_MOSI | MTK MT8370 | SPIM2_MOSI | SPI C Serial Data Input |
| SPI_C_SDO | D30 | O CMOS | 1.8V | | SPIM2_MISO | MTK MT8370 | SPIM2_MISO | SPI C Serial Data Output |
| SPI_C_CS0# | C30 | O CMOS | 1.8V | | SPIM2_CS_N | MTK MT8370 | SPIM2_CS | SPI C Master Chip Select 0 |

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| SPI_C_SCK | D29 | O CMOS | 1.8V | | SPIM2_CLK | MTK MT8370 | SPIM2_CLK | SPI C Serial Data Clock |
| eDP_A_LANE0_P | A30 | O LVDS DP | | | HDMI_TX_CH0_P | MTK MT8370 | HDMITX21_CH0_P | Primary 4-lane eDP differential pair data lines |
| eDP_A_LANE0_N | A31 | O LVDS DP | | | HDMI_TX_CH0_M | MTK MT8370 | HDMITX21_CH0_M | Primary 4-lane eDP differential pair data lines |
| eDP_A_LANE1_P | B31 | O LVDS DP | | | HDMI_TX_CH1_P | MTK MT8370 | HDMITX21_CH1_P | Primary 4-lane eDP differential pair data lines |
| eDP_A_LANE1_N | B32 | O LVDS DP | | | HDMI_TX_CH1_M | MTK MT8370 | HDMITX21_CH1_M | Primary 4-lane eDP differential pair data lines |
| eDP_A_LANE2_P | A33 | O LVDS DP | | | HDMI_TX_CH2_P | MTK MT8370 | HDMITX21_CH2_P | Primary 4-lane eDP differential pair data lines |
| eDP_A_LANE2_N | A34 | O LVDS DP | | | HDMI_TX_CH2_M | MTK MT8370 | HDMITX21_CH2_M | Primary 4-lane eDP differential pair data lines |
| eDP_A_LANE3_P | B34 | O LVDS DP | | | HDMI_TX_CLK_P | MTK MT8370 | HDMITX21_CLK_P | Primary 4-lane eDP differential pair data lines |
| eDP_A_LANE3_N | B35 | O LVDS DP | | | HDMI_TX_CLK_M | MTK MT8370 | HDMITX21_CLK_M | Primary 4-lane eDP differential pair data lines |
| eDP_A_AUX_P | C33 | I/O LVDS DP | 1.8V (HDMI) | PD 100k PU 2k2 (HDMI) | HDMI_TX_SDA | MTK MT8370 | HDMITX_SDA | Primary bidirectional eDP channel used for link management and device control |
| eDP_A_AUX_N | C34 | I/O LVDS DP | 1.8V (HDMI) | PD 100k PU 2k2 (HDMI) | HDMI_TX_SCL | MTK MT8370 | HDMITX_SCL | Primary bidirectional eDP channel used for link management and device control |
| eDP_A_BL_HPD | D33 | I CMOS | VCC_OUT_IO | PD 1M | HDMI_TX_HPD | MTK MT8370 | HDMITX_HTPLG | Detection of Hot Plug / Unplug of primary eDP display and notification of the link layer. |

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| eDP_A_BL_EN | D31 | O CMOS | VCC_OUT_IO | | HDMI_TX_PWR_EN | MTK MT8370 | HDMITX_PWR5V | Primary eDP panel backlight enabled, active high |
| eDP_A_BL_PWM | C31 | O CMOS | VCC_OUT_IO | PU 4k7 (HDMI) | HDMI_TX_CEC | MTK MT8370 | HDMITX_CEC | Primary eDP panel brightness control through pulse width modulation |
| eDP_B_LANE0_P | D35 | O LVDS DP | | | EDP_L0_TXP | MTK MT8370 | EDP_LN0_TXP | Primary 4-lane eDP differential pair data lines |
| eDP_B_LANE0_N | E35 | O LVDS DP | | | EDP_L0_TXN | MTK MT8370 | EDP_LN0_TXN | Primary 4-lane eDP differential pair data lines |
| eDP_B_LANE1_P | E34 | O LVDS DP | | | EDP_L1_TXP | MTK MT8370 | EDP_LN1_TXP | Primary 4-lane eDP differential pair data lines |
| eDP_B_LANE1_N | F34 | O LVDS DP | | | EDP_L1_TXN | MTK MT8370 | EDP_LN1_TXN | Primary 4-lane eDP differential pair data lines |
| eDP_B_AUX_P | G33 | I/O LVDS DP | | PD 100k | EDP_AUX_P | MTK MT8370 | EDPAUXP | Secondary bidirectional eDP channel used for link management and device control |
| eDP_B_AUX_N | H33 | I/O LVDS DP | | PD 100k | EDP_AUX_N | MTK MT8370 | EDPAUXN | Secondary bidirectional eDP channel used for link management and device control |
| eDP_B_BL_HPD | G32 | I CMOS | VCC_OUT_IO | PD 1M | EDP_HPD | MTK MT8370 | GPIO17 | Detection of Hot Plug / Unplug of secondary eDP display and notification of the link layer. |
| eDP_B_BL_EN | E32 | O CMOS | VCC_OUT_IO | | EDP_BL_EN | MTK MT8370 | GPIO08 | Secondary eDP panel backlight enabled, active high |
| eDP_B_BL_PWM | E33 | O CMOS | VCC_OUT_IO | | EDP_BL_PWM | MTK MT8370 | DISP_PWM1 | Secondary eDP panel brightness control through pulse width modulation |

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|---|---|---|---|---|---|---|---|---|
| PCM_CLK (Vendor Defined) | Y29 | DIO | 1.8V | | PCM_CLK_1V8 | MTK MT8370 | PCM_CLK | Defined by module manufacturer (PCM clock) |
| PCM_SYNC (Vendor Defined) | Y30 | DIO | | | PCM_SYNC_1V8 | MTK MT8370 | PCM_SYNC | Defined by module manufacturer (PCM synchronization) |
| PCM_DO (Vendor Defined) | Y31 | DO | | | PCM_DO_1V8 | MTK MT8370 | PCM_DO | Defined by module manufacturer (PCM data output) |
| PCM_DI (Vendor Defined) | AA29 | DI | | | PCM_DI_1V8 | MTK MT8370 | PCM_DI | Defined by module manufacturer (PCM data input) |
| VCC_IN_5V | AE4, AF4, AG4, AH3, AH4, AJ3, AJ4, AK4 | P | | | VCC_IN_5V | Buck IC | | Module power input voltage of 5V |
| GND | AE2, AE34, AF35, AG3, AH2, AH34, AJ35, AK3, AL2, AL34, AM13, AM16, AM19, AM22, AM35, AN3, AN6, AN9, AN11, AN15, AN18, AN21, AN33, AP2, AP5, AP8, AP13, AP16, AP19, AP22, AP25, AP28, AP31, AP34, AR14, AR17, AR20, AR26, AR29, AR32 | P | | | GND | | | Module signal and power return and GND reference |
| RESERVED | AL3 | AIO | | | DPTX_L0_TXP | MTK MT8370 | DP_LN0_TXP | DPTX lane 0 (Positive) |
| RESERVED | AL4 | AIO | | | DPTX_L0_TXN | MTK MT8370 | DP_LN0_TXN | DPTX lane 0 (Negative) |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| RESERVED | AM3 | AIO | | | DPTX_L1_TXP | MTK MT8370 | DP_LN1_TXP | DPTX lane 1 (Positive) |
| RESERVED | AM4 | AIO | | | DPTX_L1_TXN | MTK MT8370 | DP_LN1_TXN | DPTX lane 1 (Negative) |
| RESERVED | AM5 | AIO | | | DPTX_L2_TXP | MTK MT8370 | DP_LN2_TXP | DPTX lane 2 (Positive) |
| RESERVED | AM6 | AIO | | | DPTX_L2_TXN | MTK MT8370 | DP_LN2_TXN | DPTX lane 2 (Negative) |
| RESERVED | AM7 | AIO | | | DPTX_L3_TXP | MTK MT8370 | DP_LN3_TXP | DPTX lane 3 (Positive) |
| RESERVED | AM8 | AIO | | | DPTX_L3_TXN | MTK MT8370 | DP_LN3_TXN | DPTX lane 3 (Negative) |
| RESERVED | AM9 | AIO | | PD 100k | DPTX_AUX_P | MTK MT8370 | DPAUXP | DPTX auxiliary channel (Positive) |
| RESERVED | AM10 | AIO | | PD 100k | DPTX_AUX_N | MTK MT8370 | DPAUXN | DPTX auxiliary channel (Negative) |
| RESERVED | AM23 | DI | | PD 1M | DPTX_HPD | MTK MT8370 | DPTX_HPD | DPTX hot plug detect |
| SCL4 (Vendor Defined) | AK32 | I/O OD CMOS | | PU 2k2 | SCL4 | MTK MT8370 | SCL4 | I2C4 Clock Signal |
| SDA4 (Vendor Defined) | AK33 | I/O OD CMOS | | PU 2k2 | SDA4 | MTK MT8370 | SDA4 | I2C4 Data Signal |
| SCL6 (Vendor Defined) | AL32 | I/O OD CMOS | | PU 2k2 | SCL6 | MTK MT8370 | SCL6 | I2C6 Clock Signal |
| SDA6 (Vendor Defined) | AL33 | I/O OD CMOS | | PU 2k2 | SDA6 | MTK MT8370 | SDA6 | I2C6 Data Signal |
| Vendor Defined | AM32 | AO | | | AU_LOLN | MTK MT6365 | AU_LOLN | Defined by the module manufacturer (Audio Lineout) |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Vendor Defined | AM33 | AO | | | AU_LOLP | MTK MT6365 | AU_LOLP | Defined by the module manufacturer (Audio Lineout) |

## 4.4 Signal Description by Function

### 4.4.1 DSIO

| Contact Name | Contact Acronym | I/O Type | I/O Level | PU/PD | Net Name of Module | Controller | Controller Pin Name | Description |
|---|---|---|---|---|---|---|---|---|
| DSI_DATA0_N | AB11 | O LVDS D-PHY | | | DSI0_D0N | MTK MT8370 | DSI0_D0N_T1A | DSI differential output (point to point) |
| DSI_DATA0_P | AB10 | O LVDS D-PHY | | | DSI0_D0P | MTK MT8370 | DSI0_D0P_T0C | DSI differential output (point to point) |
| DSI_DATA1_N | AC9 | O LVDS D-PHY | | | DSI0_D1N | MTK MT8370 | DSI0_D1N_T2B | DSI differential output (point to point) |
| DSI_DATA1_P | AC8 | O LVDS D-PHY | | | DSI0_D1P | MTK MT8370 | DSI0_D1P_T2A | DSI differential output (point to point) |
| DSI_DATA2_N | AC6 | O LVDS D-PHY | | | DSI0_D2N | MTK MT8370 | DSI0_D2N_T0B | DSI differential output (point to point) |
| DSI_DATA2_P | AC5 | O LVDS D-PHY | | | DSI0_D2P | MTK MT8370 | DSI0_D2P_T0A | DSI differential output (point to point) |
| DSI_DATA3_N | AB5 | O LVDS D-PHY | | | DSI0_D3N | MTK MT8370 | DSI0_D3N | DSI differential output (point to point) |
| DSI_DATA3_P | AB4 | O LVDS D-PHY | | | DSI0_D3P | MTK MT8370 | DSI0_D3P_T2C | DSI differential output (point to point) |
| DSI_CLOCK_N | AB8 | O LVDS D-PHY | | | DSI0_CKN | MTK MT8370 | DSI0_CKN_T1C | DSI differential clock output (point to point) |
| DSI_CLOCK_P | AB7 | O LVDS D-PHY | | | DSI0_CKP | MTK MT8370 | DSI0_CKP_T1B | DSI differential clock output (point to point) |
| DSI_TE | AA3 | I CMOS | VCC_OUT_IO | | DSI0_TE | MTK MT8370 | DSI0_DSI_TE | DSI panel tearing effect signal |
| DSI0_RST (Vendor Defined) | D6 | O | 1.8V | | DSI0_RST | MTK MT8370 | DSI0_LCM_RST | Defined by module manufacturer |

### 4.4.2 eDP A

| Contact Name | Contact Acronym | I/O Type | I/O Level | PU/PD | Net Name of Module | Controller | Controller Pin Name | Description |
|---|---|---|---|---|---|---|---|---|
| eDP_A_LANE0_P | A30 | O LVDS DP | | | HDMI_TX_CH0_P | MTK MT8370 | HDMITX21_CH0_P | Primary 4-lane eDP differential pair data lines |
| eDP_A_LANE0_N | A31 | O LVDS DP | | | HDMI_TX_CH0_M | MTK MT8370 | HDMITX21_CH0_M | Primary 4-lane eDP differential pair data lines |
| eDP_A_LANE1_P | B31 | O LVDS DP | | | HDMI_TX_CH1_P | MTK MT8370 | HDMITX21_CH1_P | Primary 4-lane eDP differential pair data lines |
| eDP_A_LANE1_N | B32 | O LVDS DP | | | HDMI_TX_CH1_M | MTK MT8370 | HDMITX21_CH1_M | Primary 4-lane eDP differential pair data lines |
| eDP_A_LANE2_P | A33 | O LVDS DP | | | HDMI_TX_CH2_P | MTK MT8370 | HDMITX21_CH2_P | Primary 4-lane eDP differential pair data lines |
| eDP_A_LANE2_N | A34 | O LVDS DP | | | HDMI_TX_CH2_M | MTK MT8370 | HDMITX21_CH2_M | Primary 4-lane eDP differential pair data lines |
| eDP_A_LANE3_P | B34 | O LVDS DP | | | HDMI_TX_CLK_P | MTK MT8370 | HDMITX21_CLK_P | Primary 4-lane eDP differential pair data lines |
| eDP_A_LANE3_N | B35 | O LVDS DP | | | HDMI_TX_CLK_M | MTK MT8370 | HDMITX21_CLK_M | Primary 4-lane eDP differential pair data lines |
| eDP_A_AUX_P | C33 | I/O LVDS DP | 1.8V (HDMI) | PD 100k<br>PU 2k2 (HDMI) | HDMI_TX_SDA | MTK MT8370 | HDMITX_SDA | Primary bidirectional eDP channel used for link management and device control |
| eDP_A_AUX_N | C34 | I/O LVDS DP | 1.8V (HDMI) | PD 100k<br>PU 2k2 (HDMI) | HDMI_TX_SCL | MTK MT8370 | HDMITX_SCL | Primary bidirectional eDP channel used for link management and device control |
| eDP_A_BL_HPD | D33 | I CMOS | VCC_OUT_IO | PD 1M | HDMI_TX_HPD | MTK MT8370 | HDMITX_HTPLG | Detection of Hot Plug / Unplug of primary eDP display and notification of the link layer. |
| eDP_A_BL_EN | D31 | O CMOS | VCC_OUT_IO | | HDMI_TX_PWR_EN | MTK MT8370 | HDMITX_PWR5V | Primary eDP panel backlight enabled, active high |
| eDP_A_BL_PWM | C31 | O CMOS | VCC_OUT_IO | PU 4k7 (HDMI) | HDMI_TX_CEC | MTK MT8370 | HDMITX_CEC | Primary eDP panel brightness control through pulse width modulation |

### 4.4.3 eDP B

| Contact Name | Contact Acronym | I/O Type | I/O Level | PU/PD | Net Name of Module | Controller | Controller Pin Name | Description |
|---|---|---|---|---|---|---|---|---|
| eDP_B_LANE0_P | D35 | O LVDS DP | | | EDP_L0_TXP | MTK MT8370 | EDP_LN0_TXP | Primary 4-lane eDP differential pair data lines |
| eDP_B_LANE0_N | E35 | O LVDS DP | | | EDP_L0_TXN | MTK MT8370 | EDP_LN0_TXN | Primary 4-lane eDP differential pair data lines |
| eDP_B_LANE1_P | E34 | O LVDS DP | | | EDP_L1_TXP | MTK MT8370 | EDP_LN1_TXP | Primary 4-lane eDP differential pair data lines |
| eDP_B_LANE1_N | F34 | O LVDS DP | | | EDP_L1_TXN | MTK MT8370 | EDP_LN1_TXN | Primary 4-lane eDP differential pair data lines |
| eDP_B_AUX_P | G33 | I/O LVDS DP | | PD 100k | EDP_AUX_P | MTK MT8370 | EDPAUXP | Secondary bidirectional eDP channel used for link management and device control |
| eDP_B_AUX_N | H33 | I/O LVDS DP | | PD 100k | EDP_AUX_N | MTK MT8370 | EDPAUXN | Secondary bidirectional eDP channel used for link management and device control |
| eDP_B_BL_HPD | G32 | I CMOS | VCC_OUT_IO | PD 1M | EDP_HPD | MTK MT8370 | GPIO17 | Detection of Hot Plug / Unplug of secondary eDP display and notification of the link layer. |
| eDP_B_BL_EN | E32 | O CMOS | VCC_OUT_IO | | EDP_BL_EN | MTK MT8370 | GPIO08 | Secondary eDP panel backlight enabled, active high |
| eDP_B_BL_PWM | E33 | O CMOS | VCC_OUT_IO | | EDP_BL_PWM | MTK MT8370 | DISP_PWM1 | Secondary eDP panel brightness control through pulse width modulation |

### 4.4.4 DP/HDMI

| Contact Name | Contact Acronym | I/O Type | I/O Level | PU/PD | Net Name of Module | Controller | Controller Pin Name | Description |
|---|---|---|---|---|---|---|---|---|
| RESERVED | AL3 | AIO | | | DPTX_L0_TXP | MTK MT8370 | DP_LN0_TXP | DPTX lane 0 (Positive) |
| RESERVED | AL4 | AIO | | | DPTX_L0_TXN | MTK MT8370 | DP_LN0_TXN | DPTX lane 0 (Negative) |
| RESERVED | AM3 | AIO | | | DPTX_L1_TXP | MTK MT8370 | DP_LN1_TXP | DPTX lane 1 (Positive) |
| RESERVED | AM4 | AIO | | | DPTX_L1_TXN | MTK MT8370 | DP_LN1_TXN | DPTX lane 1 (Negative) |
| RESERVED | AM5 | AIO | | | DPTX_L2_TXP | MTK MT8370 | DP_LN2_TXP | DPTX lane 2 (Positive) |
| RESERVED | AM6 | AIO | | | DPTX_L2_TXN | MTK MT8370 | DP_LN2_TXN | DPTX lane 2 (Negative) |
| RESERVED | AM7 | AIO | | | DPTX_L3_TXP | MTK MT8370 | DP_LN3_TXP | DPTX lane 3 (Positive) |
| RESERVED | AM8 | AIO | | | DPTX_L3_TXN | MTK MT8370 | DP_LN3_TXN | DPTX lane 3 (Negative) |
| RESERVED | AM9 | AIO | | PD 100k | DPTX_AUX_P | MTK MT8370 | DPAUXP | DPTX auxiliary channel (Positive) |
| RESERVED | AM10 | AIO | | PD 100k | DPTX_AUX_N | MTK MT8370 | DPAUXN | DPTX auxiliary channel (Negative) |
| RESERVED | AM23 | DI | | PD 1M | DPTX_HPD | MTK MT8370 | DPTX_HPD | DPTX hot plug detect |

### 4.4.5 MIPI Camera support

#### 4.4.5.1 CSI (4 lanes)

| Contact Name | Contact Acronym | I/O Type | I/O Level | PU/PD | Net Name of Module | Controller | Controller Pin Name | Description |
|---|---|---|---|---|---|---|---|---|
| CSI_DATA0_N | C1 | I LVDS D-PHY / I LVDS M-PHY | | | CSI0_DAT0_N | MTK MT8370 | CSI0A_L1N_T1A | CSI differential input (point to point) |
| CSI_DATA0_P | B1 | | | | CSI0_DAT0_P | MTK MT8370 | CSI0A_L1P_T0C | CSI differential input (point to point) |
| CSI_DATA1_N | A2 | | | | CSI0_DAT1_N | MTK MT8370 | CSI0B_L0N_T0B | CSI differential input (point to point) |
| CSI_DATA1_P | A3 | | | | CSI0_DAT1_P | MTK MT8370 | CSI0B_L0P_T0A | CSI differential input (point to point) |
| CSI_DATA2_N | A5 | | | | CSI0_DAT2_N | MTK MT8370 | CSI0A_L0N_T0A | CSI differential input (point to point) |
| CSI_DATA2_P | A6 | | | | CSI0_DAT2_P | MTK MT8370 | CSI0A_L0P_T0B | CSI differential input (point to point) |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| CSI_DATA3_N | B6 | | | | CSI0_DAT3_N | MTK MT8370 | CSI0B_L1N_T1A | CSI differential input (point to point) |
| CSI_DATA3_P | B7 | | | | CSI0_DAT3_P | MTK MT8370 | CSI0B_L1P_T0C | CSI differential input (point to point) |
| CSI_CLOCK_N | B3 | I LVDS D-PHY | | | CSI0_CLK_N | MTK MT8370 | CSI0A_L2N_T1C | CSI differential clock input (point to point) |
| CSI_CLOCK_P | B4 | I LVDS D-PHY | | | CSI0_CLK_P | MTK MT8370 | CSI0A_L2P_T1B | CSI differential clock input (point to point) |
| I2C_CAM_SDA / CSI_TX_N | C3 | I/O OD CMOS / O LVDS M-PHY | VCC_OUT_IO | PU 2k2 | SDA5_CAM | MTK MT8370 | SDA5 | I2C data for serial camera data support link or differential data lane |
| I2C_CAM_SCL / CSI_TX_P | C4 | I/O OD CMOS / O LVDS M-PHY | VCC_OUT_IO | PU 2k2 | SCL5_CAM | MTK MT8370 | SCL5 | I2C clock for serial camera data support link or differential data lane |

## 4.4.6 Audio Interfaces

### 4.4.6.1 I2S0

| Contact Name | Contact Acronym | I/O Type | I/O Level | PU/PD | Net Name of Module | Controller | Controller Pin Name | Description |
|---|---|---|---|---|---|---|---|---|
| I2S_A_DATA_IN | V21 | I/O CMOS | VCC_OUT_IO | | I2S_IN_D0 | MTK MT8370 | I2SIN_D0 | I2S A Digital audio Input |
| I2S_A_DATA_OUT | W21 | | | | I2S_OUT_D0 | MTK MT8370 | I2SO2_D0 | I2S A Digital audio Output |
| I2S_B_DATA_IN | V19 | | | | | | | I2S B Digital audio Input |
| I2S_B_DATA_OUT | W19 | | | | | | | I2S B Digital audio Output |
| I2S_MCLK | V18 | | | | I2S_IO_MCK | MTK MT8370 | I2SO2_MCK | Master clock output to I2S codec(s) |
| I2S_LRCLK | W18 | | | | I2S_IO_WS | MTK MT8370 | I2SO2_WS | I2S Left & Right synchronization clock |
| I2S_BITCLK | W20 | | | | I2S_IO_BCK | MTK MT8370 | I2SO2_BCK | I2S Digital audio clock |

### 4.4.7 USB Ports

| Contact Name | Contact Acronym | I/O Type | I/O Level | PU/PD | Net Name of Module | Controller | Controller Pin Name | Description |
|---|---|---|---|---|---|---|---|---|
| USB_A_D_N | AB13 | I/O USB | USB | | USB_DM_P0 | MTK MT8370 | USB_DM_P0 | USB differential data pairs for port A |
| USB_A_D_P | AC14 | I/O USB | USB | | USB_DP_P0 | MTK MT8370 | USB_DP_P0 | USB differential data pairs for port A |
| USB_A_ID | AB14 | I OD CMOS | VCC_OUT_IO | PU 10k | USB0_IDDIG | MTK MT8370 | USB0_IDDIG | Input Contact to announce OTG device insertion on USB 2.0 port |
| USB_A_OC# | AC15 | I OD CMOS | VCC_OUT_IO | PU 10k | USB0_OC_N | MTK MT8370 | KPCOL1 | USB over-current for port A |
| USB_A_VBUS | AB16 | I USB VBUS 5V | 5V | | USB0_VBUS_5V | MTK MT8370 | USB0_VBUS_VALID | USB port 0 port power detection |
| USB_A_EN | AC16 | O CMOS | VCC_OUT_IO | | USB0_DRV_VBUS | MTK MT8370 | USB0_DRV_VBUS | Power enable for USB VBUS voltage |
| USB_B_D_N | AB23 | I/O USB | USB | | USB_DM_P2 | MTK MT8370 | USB_DM_P2 | USB differential data pairs for port B |
| USB_B_D_P | AC22 | I/O USB | USB | | USB_DP_P2 | MTK MT8370 | USB_DP_P2 | USB differential data pairs for port B |
| USB_B_ID | AB22 | I OD CMOS | 1.8V | PU 10k | USB2_IDDIG | MTK MT8370 | USB2_IDDIG | Input Contact to announce OTG device insertion on USB 2.0 port |
| USB_B_OC# | AC21 | I OD CMOS | 1.8V | PU 10k | USB2_OC_N | MTK MT8370 | SPIM0_CLK | USB over-current for port B |
| USB_B_VBUS | AB20 | I USB VBUS 5V | 5V | | USB2_VBUS_5V | MTK MT8370 | USB2_VBUS_VALID | USB port 0 port power detection |
| USB_B_EN | AC20 | O CMOS | 1.8V | | USB2_DRV_VBUS | MTK MT8370 | USB2_DRV_VBUS | Power enabled for USB VBUS voltage |
| USB_C_D_N | D11 | I/O USB | USB | | USB_DM_P1 | MTK MT8370 | USB_DM_P1 | USB differential data pairs for port C |
| USB_C_D_P | D10 | I/O USB | USB | | USB_DP_P1 | MTK MT8370 | USB_DP_P1 | USB differential data pairs for port C |
| USB_C_ID | D9 | I OD CMOS | VCC_OUT_IO | PU 10K | USB1_IDDIG | MTK MT8370 | USB1_IDDIG | Input Contact to announce OTG device insertion on USB 2.0 port |
| USB_C_OC# | C8 | I OD CMOS | VCC_OUT_IO | PU 10K | USB1_OC_N | MTK MT8370 | KPROW0 | USB over-current for port C |
| USB_C_VBUS | C9 | I USB VBUS 5V | 5V | | USB1_VBUS_5V | MTK MT8370 | USB1_VBUS_VALID | USB port 0 port power detection |
| USB_C_EN | C10 | O CMOS | VCC_OUT_IO | | USB1_DRV_VBUS | MTK MT8370 | USB1_DRV_VBUS | Power enabled for USB VBUS voltage |
| USB_C_SSTX_N | A9 | O USB SS | USB SS | | SSUSB_TXN_P1 | MTK MT8370 | SSUSB_TXN | Transmit signal differential pairs for SuperSpeed on port C |
| USB_C_SSTX_P | A8 | O USB SS | USB SS | | SSUSB_TXP_P1 | MTK MT8370 | SSUSB_TXP | Transmit signal differential pairs for SuperSpeed on port C |
| USB_C_SSRX_N | B11 | I USB SS | USB SS | | SSUSB_RXN_P1 | MTK MT8370 | SSUSB_RXN | Receive signal differential pairs for SuperSpeed on port C |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| USB_C_SSRX_P | B10 | I USB SS | USB SS | | SSUSB_RXP_P1 | MTK MT8370 | SSUSB_RXP | Receive signal differential pairs for SuperSpeed on port C |

**Note**: 1. USB A and B have OTG 2. USB C carries SS signals

### 4.4.8 PCIe

| Contact Name | Contact Acronym | I/O Type | I/O Level | PU/PD | Net Name of Module | Controller | Controller Pin Name | Description |
|---|---|---|---|---|---|---|---|---|
| PCIe_A_HSI0_P | AB1 | I LVDS PCIE | | | PCIEG2_L0_RXP | MTK MT8370 | PCIE_LN0_RXP | Differential PCIe link A receive data pair |
| PCIe_A_HSI0_N | AB2 | I LVDS PCIE | | | PCIEG2_L0_RXN | MTK MT8370 | PCIE_LN0_RXN | Differential PCIe link A receive data pair |
| PCIe_A_HSO0_P | AC2 | O LVDS PCIE | | | PCIEG2_L0_TXP | MTK MT8370 | PCIE_LN0_TXP | Differential PCIe link A transmit data pair |
| PCIe_A_HSO0_N | AC3 | O LVDS PCIE | | | PCIEG2_L0_TXN | MTK MT8370 | PCIE_LN0_TXN | Differential PCIe link A transmit data pair |
| PCIe_CLKREQ# | W2 | I OD CMOS | VCC_OUT_IO | PU 10k | PCIEG2_CLKREQ_N | MTK MT8370 | PCIE_CLKREQ | PCIe reference clock request |
| PCIe_A_PERST# | V21 | O CMOS | VCC_OUT_IO | | PCIEG2_PERESET_N | MTK MT8370 | PCIE_PERESET | PCIe Port A reset output |
| PCIe_REFCLK_P | W1 | O LVDS PCIE | | PD 49.9 (MTK request) | PCIEG2_CLK_P | MTK MT8370 | PCIE_CKP | Differential PCIe reference clock output |
| PCIe_REFCLK_N | Y1 | O LVDS PCIE | | PD 49.9 (MTK request) | PCIEG2_CLK_N | MTK MT8370 | PCIE_CKN | Differential PCIe reference clock output |
| PCIe_WAKE# | T2 | I OD CMOS | VCC_OUT_IO | PU 10k | PCIEG2_WAKE_N | MTK MT8370 | PCIE_WAKE | PCIe wake up interrupt to host – common to PCIe links A, B, C, D |
| PCIe_SMDAT | U1 | I/O OD CMOS | VCC_OUT_IO | PU 2k2 | SDA3_PCIE | MTK MT8370 | SDA3 | System management I2C bus DATA |
| PCIe_SMCLK | T1 | O OD CMOS | VCC_OUT_IO | PU 2k2 | SCL3_PCIE | MTK MT8370 | SCL3 | System management I2C bus CLK |
| PCIe_SM_ALERT# | R2 | I OD CMOS | VCC_OUT_IO | PU 2k2 | PCIE_SM_ALERT_N | MTK MT8370 | SPIM0_CS | SMBus Alert# (interrupt) signal |

### 4.4.9 LAN Port

| Contact Name | Contact Acronym | I/O Type | I/O Level | PU/PD | Net Name of Module | Controller | Controller Pin Name | Description |
|---|---|---|---|---|---|---|---|---|
| ETH_A_(R)(G)MII_COL | F15 | I CMOS | 1.8V /2.5V / 3.3V | | GBE_COL_1V8 | MTK MT8370 | DPI_HSYNC | Collision detects (half speed only) port A |
| ETH_A_(S)(R)(G)MII_TXD0 | H15 | O CMOS | 1.8V /2.5V / 3.3V | | GBE_TXD0_1V8 | MTK MT8370 | DPI_D3 | Transmit data bit 0 (transmitted first) port A |
| ETH_A_(S)(R)(G)MII_TXD1 | G15 | O CMOS | 1.8V /2.5V / 3.3V | | GBE_TXD1_1V8 | MTK MT8370 | DPI_D2 | Transmit data bit 1 port A |
| ETH_A_(S)(R)(G)MII_TXD2 | H16 | O CMOS | 1.8V /2.5V / 3.3V | | GBE_TXD2_1V8 | MTK MT8370 | DPI_D1 | Transmit data bit 2 port A |
| ETH_A_(S)(R)(G)MII_TXD3 | G16 | O CMOS | 1.8V /2.5V / 3.3V | | GBE_TXD3_1V8 | MTK MT8370 | DPI_D0 | Transmit data bit 3 port A |
| ETH_A_(R)(G)MII_TX_EN(_ER) | K16 | O CMOS | 1.8V /2.5V / 3.3V | | GBE_TXEN_1V8 | MTK MT8370 | DPI_D11 | Transmit enable (Error) port A |
| ETH_A_(R)(G)MII_TX_CLK | J15 | I/O CMOS | 1.8V /2.5V / 3.3V | | GBE_TXC_1V8 | MTK MT8370 | DPI_D8 | Transmit clock port A |
| ETH_A_(S)(R)(G)MII_RXD0 | K15 | I CMOS | 1.8V /2.5V / 3.3V | | GBE_RXD0_1V8 | MTK MT8370 | DPI_D7 | Receive data bit 0 (received first) port A |
| ETH_A_(S)(R)(G)MII_RXD1 | L15 | I CMOS | 1.8V /2.5V / 3.3V | | GBE_RXD1_1V8 | MTK MT8370 | DPI_D6 | Receive data bit 1 port A |
| ETH_A_(R)(G)MII_RXD3 | P15 | I CMOS | 1.8V /2.5V / 3.3V | | GBE_RXD3_1V8 | MTK MT8370 | DPI_D4 | Receive data bit 3 port A |
| ETH_A_(R)(G)MII_RX_ER | L16 | I CMOS | 1.8V /2.5V / 3.3V | | GBE_RXER_1V8 | MTK MT8370 | DPI_D15 | Receive error port A |
| ETH_A_(R)(G)MII_RX_DV(_ER) | M15 | I CMOS | 1.8V /2.5V / 3.3V | | GBE_RXDV_1V8 | MTK MT8370 | DPI_D10 | Receive data valid port A |
| ETH_A_(R)(G)MII_RX_CLK | R15 | I/O CMOS | 1.8V /2.5V / 3.3V | | GBE_RXC_1V8 | MTK MT8370 | DPI_D9 | Receive clock port A |
| ETH_MDIO | T15 | I/O CMOS | 1.8V /2.5V / 3.3V | | GBE_MDIO_1V8 | MTK MT8370 | DPI_D13 | Management bus data signal for Ethernet |
| ETH_MDC | T16 | O CMOS | 1.8V /2.5V / 3.3V | | GBE_MDC_1V8 | MTK MT8370 | DPI_D12 | Management bus clock signal for Ethernet |
| ETH_IOPWR | M17 | PO | 1.8V /2.5V / 3.3V | | VIO18_PMU | MTK MT6365 | VIO18 | ETH voltage. It is used to provide the I/O Voltage Level for all Ethernet interfaces. |

### 4.4.10 SDIO

| Contact Name | Contact Acronym | I/O Type | I/O Level | PU/PD | Net Name of Module | Controller | Controller Pin Name | Description |
|---|---|---|---|---|---|---|---|---|
| SDIO_A_CMD | E20 | I/O CMOS | 1.8V / 3.3V | | MSDC1_CMD | MTK MT8370 | MSDC1_CMD | SDIO A Command/Response: This signal is used for card initialization and for command transfers. During initialization, this signal is open-drain. During command transfers, this signal is in push-pull mode. |
| SDIO_A_CLK | F21 | O CMOS | 1.8V / 3.3V | | MSDC1_CLK | MTK MT8370 | MSDC1_CLK | SDIO A Clock: With each cycle of this signal, a one-bit transfer occurs on the command and each of the data line. |
| SDIO_A_D0 | G20 | I/O CMOS | 1.8V / 3.3V | | MSDC1_DAT0 | MTK MT8370 | MSDC1_DAT0 | SDIO A Data lines: These signals operate in push-pull mode. |
| SDIO_A_D1 | G21 | I/O CMOS | 1.8V / 3.3V | | MSDC1_DAT1 | MTK MT8370 | MSDC1_DAT1 | SDIO A Data lines: These signals operate in push-pull mode. |
| SDIO_A_D2 | H20 | I/O CMOS | 1.8V / 3.3V | | MSDC1_DAT2 | MTK MT8370 | MSDC1_DAT2 | SDIO A Data lines: These signals operate in push-pull mode. |
| SDIO_A_D3 | H21 | I/O CMOS | 1.8V / 3.3V | | MSDC1_DAT3 | MTK MT8370 | MSDC1_DAT3 | SDIO A Data lines: These signals operate in push-pull mode. |
| SDIO_A_CD# | J21 | I OD CMOS | 1.8V / 3.3V | PU 10K | MSDC1_INSI | MTK MT8370 | GPIO06 | SDIO A Card Detect: This signal indicates when a SDIO/MMC card is present. |
| SDIO_A_WP | D20 | I OD CMOS | 1.8V / 3.3V | PU 10K | MSDC1_WP | MTK MT8370 | GPIO05 | SDIO A Write Protect: This signal denotes the state of the write-protect tab on SD cards. |
| SDIO_A_PWR_EN | D21 | O CMOS | 1.8V / 3.3V | | EXT_VMSDC1_EN | MTK MT8370 | GPIO04 | SDIO A Power Enable: This signal is used to enable the power being supplied to a SD/MMC card device. |
| SDIO_A_IOPWR | C20 | PO | 1.8V / 3.3V | | VSIM1_PMU | MTK MT6365 | VSIM1 | SDIO A Voltage: It is used to provide the IO Voltage Level |
| SDIO_B_CLK | K20 | O CMOS | 1.8V / 3.3V | | MSDC2_CLK | MTK MT8370 | MSDC2_CLK | SDIO B Clock: With each cycle of this signal, a one-bit transfer occurs on the command and each of the data line. |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| SDIO_B_CMD | K21 | I/O CMOS | 1.8V / 3.3V | | MSDC2_CMD | MTK MT8370 | MSDC2_CMD | SDIO B Command/Response: This signal is used for card initialization and for command transfers. During initialization, this signal is open-drain. During command transfers, this signal is in push-pull mode. |
| SDIO_B_D0 | L20 | I/O CMOS | 1.8V / 3.3V | | MSDC2_DAT0 | MTK MT8370 | MSDC2_DAT0 | SDIO B Data lines: These signals operate in push-pull mode. |
| SDIO_B_D1 | L21 | I/O CMOS | 1.8V / 3.3V | | MSDC2_DAT1 | MTK MT8370 | MSDC2_DAT1 | SDIO B Data lines: These signals operate in push-pull mode. |
| SDIO_B_D2 | M21 | I/O CMOS | 1.8V / 3.3V | | MSDC2_DAT2 | MTK MT8370 | MSDC2_DAT2 | SDIO B Data lines: These signals operate in push-pull mode. |
| SDIO_B_D3 | N20 | I/O CMOS | 1.8V / 3.3V | | MSDC2_DAT3 | MTK MT8370 | MSDC2_DAT3 | SDIO B Data lines: These signals operate in push-pull mode. |
| SDIO_B_IOPWR | T20 | PO | 1.8V / 3.3V | | VIO18_PMU | MTK MT6365 | VIO18 | SDIO B Voltage: It is used to provide the I/O Voltage Level |

The carrier SDIO card ***may*** be selected as the boot device.

## 4.4.11 SPI Interfaces

### 4.4.11.1 SPI A/B/C

| Contact Name | Contact Acronym | I/O Type | I/O Level | PU/PD | Net Name of Module | Controller | Controller Pin Name | Description |
|---|---|---|---|---|---|---|---|---|
| SPI_A_SDI_(IO0) | U15 | I/O CMOS | VCC_OUT_IO | | SPINOR_IO0 | MTK MT8370 | DMIC1_DAT_R | SPI A Serial Data Input |
| SPI_A_SDO_(IO1) | V15 | I/O CMOS | VCC_OUT_IO | | SPINOR_IO1 | MTK MT8370 | DMIC2_CLK | SPI A Serial Data Output |
| SPI_A_/WP_(IO2) | W16 | I/O CMOS | VCC_OUT_IO | | SPINOR_IO2 | MTK MT8370 | DMIC2_DAT | SPI A Write Protect |
| SPI_A_/HOLD_(IO3) | W15 | I/O CMOS | VCC_OUT_IO | | SPINOR_IO3 | MTK MT8370 | DMIC2_DAT_R | SPI A Suspends Serial Input |
| SPI_A_CS0# | Y15 | O CMOS | VCC_OUT_IO | | SPINOR_CS_N | MTK MT8370 | DMIC1_DAT | SPI A Master Chip Select 0 |
| SPI_A_SCK | U16 | O CMOS | VCC_OUT_IO | | SPINOR_CLK | MTK MT8370 | DMIC1_CLK | SPI A Serial Data Clock |
| SPI_B_SDI | Y22 | I CMOS | VCC_OUT_IO | | SPIM1_MOSI | MTK MT8370 | SPIM1_MOSI | SPI B Serial Data Input |
| SPI_B_SDO | Y23 | O CMOS | VCC_OUT_IO | | SPIM1_MISO | MTK MT8370 | SPIM1_MISO | SPI B Serial Data Output |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| SPI_B_CS0# | AA23 | O CMOS | VCC_OUT_IO | | SPIM1_CS_N | MTK MT8370 | SPIM1_CS | SPI B Master Chip Select 0 |
| SPI_B_SCK | Y21 | O CMOS | VCC_OUT_IO | | SPIM1_CLK | MTK MT8370 | SPIM1_CLK | SPI B Serial Data Clock |
| SPI_C_SDI | C29 | I CMOS | 1.8V | | SPIM2_MOSI | MTK MT8370 | SPIM2_MOSI | SPI C Serial Data Input |
| SPI_C_SDO | D30 | O CMOS | 1.8V | | SPIM2_MISO | MTK MT8370 | SPIM2_MISO | SPI C Serial Data Output |
| SPI_C_CS0# | C30 | O CMOS | 1.8V | | SPIM2_CS_N | MTK MT8370 | SPIM2_CS | SPI C Master Chip Select 0 |
| SPI_C_SCK | D29 | O CMOS | 1.8V | | SPIM2_CLK | MTK MT8370 | SPIM2_CLK | SPI C Serial Data Clock |

### 4.4.11.2 I2C

| Contact Name | Contact Acronym | I/O Type | I/O Level | PU/PD | Net Name of Module | Controller | Controller Pin Name | Description |
|---|---|---|---|---|---|---|---|---|
| I2C_A_SCL | AA15 | I/O OD CMOS | VCC_OUT_IO, Size-0 only 1.8V, >Size-0 | PU 2k2 | SCL0_A | MTK MT8370 | SCL0 | I2C Port A Clock Signal |
| I2C_A_SDA | AA16 | | | | SDA0_A | MTK MT8370 | SDA0 | I2C Port A Data Signal |
| I2C_B_SCL | AA20 | | | | SCL2_B | MTK MT8370 | SCL2 | I2C Port B Clock Signal |
| I2C_B_SDA | AA21 | | | | SDA2_B | MTK MT8370 | SDA2 | I2C Port B Data Signal |
| I2C_CAM_SDA / CSI_TX_N | C3 | I/O OD CMOS / O LVDS M-PHY | VCC_OUT_IO | PU 2k2 | SDA5_CAM | MTK MT8370 | SDA5 | I2C data for serial camera data support link or differential data lane |
| I2C_CAM_SCL / CSI_TX_P | C4 | I/O OD CMOS / O LVDS M-PHY | VCC_OUT_IO | PU 2k2 | SCL5_CAM | MTK MT8370 | SCL5 | I2C clock for serial camera data support link or differential data lane |
| SCL4 (Vendor Definied) | AK32 | I/O OD CMOS | | PU 2k2 | SCL4 | MTK MT8370 | SCL4 | I2C4 Clock Signal |
| SDA4 (Vendor Definied) | AK32 | I/O OD CMOS | | PU 2k2 | SDA4 | MTK MT8370 | SDA4 | I2C4 Data Signal |
| SCL6 (Vendor Definied) | AK32 | I/O OD CMOS | | PU 2k2 | SCL6 | MTK MT8370 | SCL6 | I2C6 Clock Signal |
| SDA6 (Vendor Definied) | AK32 | I/O OD CMOS | | PU 2k2 | SDA6 | MTK MT8370 | SDA6 | I2C6 Data Signal |
| PCIe_SMDAT | U1 | I/O OD CMOS | VCC_OUT_IO | PU 2k2 | SDA3_PCIE | MTK MT8370 | SDA3 | System management I2C bus DATA |
| PCIe_SMCLK | T1 | O OD CMOS | VCC_OUT_IO | PU 2k2 | SCL3_PCIE | MTK MT8370 | SCL3 | System management I2C bus CLK |

**Note**: MIPI-CSI 2.0 mode uses I2C_CAM_SDA /MIPI-CSI 3.0 mode uses CSI_TX_N

MIPI-CSI 2.0 mode uses I2C_CAM_SCL /MIPI-CSI 3.0 mode uses CSI_TX_P

### 4.4.12 GPIO

| Contact Name | Contact Acronym | I/O Type | I/O Level | PU/PD | Net Name of Module | Controller | Controller Pin Name | Description |
|---|---|---|---|---|---|---|---|---|
| GPIO_A_0 | D17 | I/O CMOS | VCC_OUT_IO | | GPIO_02 | MTK MT8370 | SPIM0_MOSI | General purpose I/O Contact A0 |
| GPIO_A_1 | E17 | I/O CMOS | VCC_OUT_IO | | GPIO_04 | MTK MT8370 | SPIM0_MIO2 | General purpose I/O Contact A1 |
| GPIO_A_2 | F17 | I/O CMOS | VCC_OUT_IO | | GPIO_05 | MTK MT8370 | SPIM0_MIO3 | General purpose I/O Contact A2 |
| GPIO_A_3 | G17 | I/O CMOS | VCC_OUT_IO | | GPIO_03 | MTK MT8370 | SPIM0_MIO1 | General purpose I/O Contact A3 |
| GPIO_A_4 | H17 | I/O CMOS | VCC_OUT_IO | | GBE_TXER_1V8 | MTK MT8370 | DPI_D14 | General purpose I/O Contact A4 |
| GPIO_A_5 | J17 | I/O CMOS | VCC_OUT_IO | | GBE_INTR_1V8 | MTK MT8370 | DPI_D15 | General purpose I/O Contact A5 |
| GPIO_B_0 | D19 | I/O CMOS | VCC_OUT_IO | | GPIO_12 | MTK MT8370 | GPIO12 | General purpose I/O Contact B0 |
| GPIO_B_1 | E19 | I/O CMOS | VCC_OUT_IO | | GPIO_13 | MTK MT8370 | GPIO13 | General purpose I/O Contact B1 |
| GPIO_B_2 | F19 | I/O CMOS | VCC_OUT_IO | | GPIO_14 | MTK MT8370 | GPIO14 | General purpose I/O Contact B2 |
| GPIO_B_3 | G19 | I/O CMOS | VCC_OUT_IO | | GPIO_15 | MTK MT8370 | GPIO15 | General purpose I/O Contact B3 |
| GPIO_B_4 | H19 | I/O CMOS | VCC_OUT_IO | | GPIO_17 | MTK MT8370 | I2SIN_WS | General purpose I/O Contact B4 |
| GPIO_B_5 | J19 | I/O CMOS | VCC_OUT_IO | | GPIO_08 | MTK MT8370 | CMMRST1 | General purpose I/O Contact B5 |
| GPIO_B_6 | K19 | I/O CMOS | VCC_OUT_IO | | GPIO_06 | MTK MT8370 | CMMPDN1 | General purpose I/O Contact B6 |
| GPIO_B_7 | L19 | I/O CMOS | VCC_OUT_IO | | GPIO_01 | MTK MT8370 | GPIO01 | General purpose I/O Contact B7 |
| GPIO_C_0 | D3 | I/O CMOS | VCC_OUT_IO | | GPIO_00 | MTK MT8370 | GPIO00 | General purpose I/O Contact C0 |
| GPIO_C_1 | D4 | I/O CMOS | VCC_OUT_IO | | GPIO_11 | MTK MT8370 | GPIO11 | General purpose I/O Contact C1 |
| GPIO_C_2 | E3 | I/O CMOS | VCC_OUT_IO | | GPIO_09 | MTK MT8370 | DSI1_LCM_RST | General purpose I/O Contact C2 |
| GPIO_C_3 | E4 | I/O CMOS | VCC_OUT_IO | | GPIO_07 | MTK MT8370 | GPIO07 | General purpose I/O Contact C3 |
| GPIO_C_4 | F3 | I/O CMOS | VCC_OUT_IO | | DISP_VDD_EN | MTK MT8370 | I2SIN_D1 | Dual function: DISP_VDD_EN |
| GPIO_C_5 | F4 | I/O CMOS | VCC_OUT_IO | | DISP_BL_EN | MTK MT8370 | KPROW1 | Dual function: DISP_BL_EN |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| GPIO_D_0 | U32 | I/O CMOS | 1.8V | | GPIO_16 | MTK MT8370 | DSI1_DSI_TE | General purpose I/O Contact D0 |

## 4.4.13 Power

| Contact Name | Contact Acronym | I/O Type | I/O Level | PU/PD | Net Name of Module | Controller | Controller Pin Name | Description |
|---|---|---|---|---|---|---|---|---|
| VCC_OUT_IO | U18 | P | 1.8V / 3.3V | | VIO18_PMU | MTK MT6365 | VIO18 | Can provide IO voltage level for several interfaces to connect |
| VCC_IN_5V | Y25, Y26, Y27, Y28 | P | | | VCC_IN_5V | Buck IC | | Module power input voltage of 5V |
| VCC_IN_5V | AE4, AF4, AG4, AH3, AH4, AJ3, AJ4, AK4 | P | | | VCC_IN_5V | Buck IC | | Module power input voltage of 5V |

| Contact Name | Contact Acronym | I/O Type | I/O Level | PU/PD | Net Name of Module | Controller | Controller Pin Name | Description |
|---|---|---|---|---|---|---|---|---|
| GND | D18, E15, E21, F16, F20, J16, J20, L18, M16, M20, P18, R16, R20, V16, V20, Y18, AA14, AA17, AA19, AA22, AB15, AB21 | P | | | GND | | | Module Signal and power return and GND reference |
| GND | A4, A7, A10, B2, B5, B8, B9, C11, D1, D5, D8, E2, H2, H4, L2, L4, P2, P4, R1, U2, U4, V1, W3, Y2, AA1, AA4, AA7, AA8, AA10, AA11, AB3, AB6, AB9, AC4, AC7, AC10 | P | | | GND | | | Module Signal and power return and GND reference |
| GND | A26, A29, A32, B27, B28, B30, B33, C25, C32, C35, D28, D34, F33, F35, G34, H32, J33, J35, K34, M35, N34, T34, W34, AA25, AA26, AA27, AA28, AA32, AB28, AB31, AB34, AC27, AC30, AC33 | P | | | GND | | | Module Signal and power return and GND reference |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| GND | AE2, AE34, AF35, AG3, AH2, AH34, AJ35, AK3, AL2, AL34, AM13, AM16, AM19, AM22, AM35, AN3, AN6, AN9, AN11, AN15, AN18, AN21, AN33, AP2, AP5, AP8, AP13, AP16, AP19, AP22, AP25, AP28, AP31, AP34, AR14, AR17, AR20, AR26, AR29, AR32 | P | | | GND | | | Module Signal and power return and GND reference |

# 5. Software Support

## 5.1 Yocto

Yocto is the main OS supplied for this product, this is based upon the MediaTek Genio releases

MediaTek Releases > https://mediatek.gitlab.io/aiot/doc/aiot-dev-guide/master/

ADLINK Releases > https://github.com/ADLINK/meta-adlink-mtk

## 5.2 Canonical Ubuntu

Ubuntu will be supported in a later stage on this platform, based upon the official Canonical/MediaTek releases

https://ubuntu.com/download/mediatek-genio

# 6. Mechanical

## 6.1 Module Dimensions

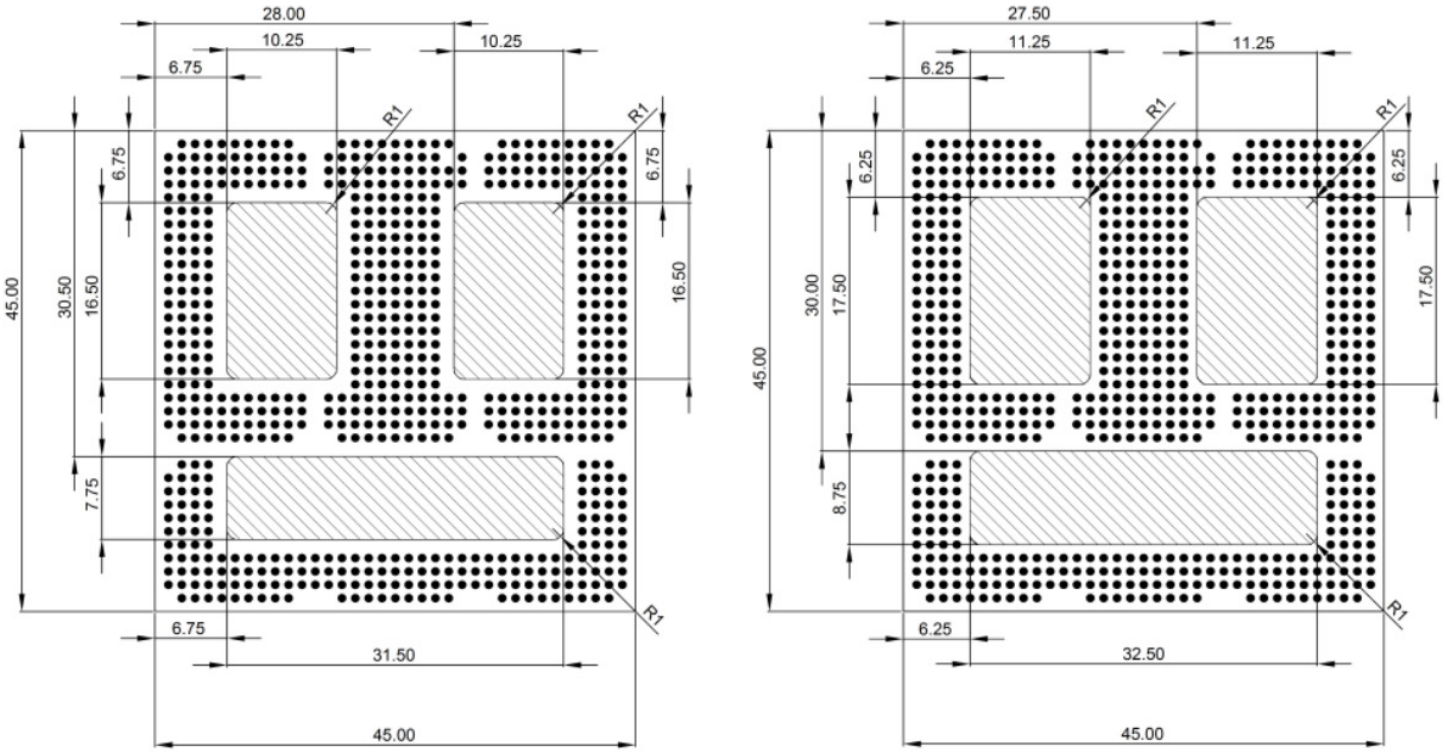


**Figure 16: Placement Area (left) and Cut-Out Area (right) - Size L (view from bottom)**

**Figure 4 – Mechanical dimensions**

# 7. Thermal Solutions

## 7.1 Heatspreader: HTS

To define on the carrier, follow the carrier mounting points for off-the-shelf designs.

## 7.2 Heatsink: THS

To define on the carrier, follow the carrier mounting points for off-the-shelf designs.