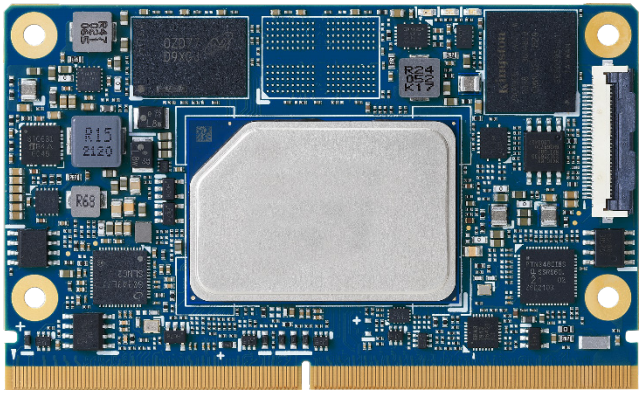
LEC-EL

User's Guide



SMARC module

Revision:	Rev. 1.5
Date:	2025-11-05
Part Number:	50M-72513-1050

ADLINK LEADING EDGE COMPUTING

Revision History

Revision	Description	Date	Author
1.0	Initial release	2023-05-09	CC
1.1	BIOS info added	2023-10-13	CC
1.2	Specifications updated	2025-02-12	AL
1.3	Specifications updated	2025-04-07	AL
1.4	Pinout and signal descriptions updated	2025-05-08	AL
1.5	Specifications updated	2025-11-05	AL

Preface

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Safety Instructions

For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

Read these safety instructions carefully.

- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

Conventions

The following conventions may be used throughout this manual, denoting special levels of information

Note: This information adds clarity or specifics to text and illustrations.

Caution: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

Warning: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

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Ask an Expert: https://www.adlinktech.com/en/Askanexpert

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1. Introduction

1.1 LEC-EL

ADLINK LEC-EL is a SMARC module based on Intel Atom® x6000 series (e.g., x6425E, x6414RE) processors (formerly Elkhart Lake) with integrated Intel® UHD graphics and high-speed interfaces. It supports up to 16GB LPDDR4 memory and is available with rugged operating temperature range and low power envelope, making it ideal for mission-critical fanless edge computing applications that require safety and reliability at all times.

1.2 The SMARC Form Factor

The SMARC ("Smart Mobility ARChitecture") is a versatile small form factor Computer on Module definition targeting applications that require low power and high performance at low costs. Typically, under 6W, the modules often utilize ARM and other alternative low-power option CPUs, and are used in many familiar handheld devices, such as tablet computers and smart phones.

Two module sizes are defined in SMARC: 82 mm x 50 mm and 82 mm x 80 mm.

The module PCBs have 314 edge fingers that mate with a low-profile 314 pin 0.5 mm pitch right angle connector (the connector is sometimes identified as a 321-pin connector, with 7 pins used by the key).

SMARC modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE and a single channel LVDS display transmitter are concentrated on the module. Modules are used with application-specific carrier boards that implement other features such as audio codecs, touch controllers, wireless devices, etc.

The modular approach allows scalability, faster time to market and upgradability while still maintaining low costs, low power, and small physical size.

SGeT STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

SMARC module and carrier specifications are available online at: https://www.sget.org/standards/smarc.html

2. Specifications

2.1 Core System

SoC

6th Gen Intel® Atom® series (formerly Elkhart Lake)

- x6211E
- x6413E
- x6425E
- x6200FE
- x6414RE
- x6425RE

Standard embedded and industrial grade parts

L2 Cache

1.5 MB I2 Cache, 4MB LLC Cache

Memory

2/4/8/16 GB LPDDR4 at 4266 MT/s memory down type with IBECC

2.2 Video

LEC-EL standard display supports 4K capable HDMI 2.0a, 4K DP++ and single/dual channel 24-bit LVDS

Note : The LVDS output is derived from an eDP to LVDS bridge. As build option, the bridge can be removed.

GPU Core:

Intel Gen11LP UHD Graphics

HDMI

HDMI 2.0a supporting up to 4K (4096 x 2160 at 60Hz)

LVDS

LVDS single/dual channel 24-bit at max. 1920x 1200 over eDP to LVDS bridge

MIPI DSI (option)

DSI 4 lanes at max. 1080p@60fps display output (build option multiplexed with LVDS signal)

2.3 Audio

HDA audio interface (used by default)

Note: Audio codec is located on carrier.

2.4 Dual Ethernet

Primary LAN (GbE0) GPY

SoC-embedded RGMII Ethernet controller with optional IEEE-1588 PTP (Precision Time Protocol)

Supports 2.5Gb data transfer rates, both full-duplex and half-duplex

Secondary LAN (GbE1) GPY

SoC-embedded RGMII Ethernet controller with optional IEEE-1588 PTP (Precision Time Protocol)

Supports 2.5Gb data transfer rates, both full-duplex and half-duplex

2.5 Extension busses

PCIe

4x PCI Express Gen3 x1 interfaces (configurable to one x4, two x2 or one x2 + two x1 or four x1)

USB

2x USB 3.1, 6x USB 2.0, no OTG support

UART

4x UART interface SER0, 2(Tx/Rx/CTS/RTS) and SER1, SER3 (Tx/Rx)

7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none)

Note : SER0 and SER1 can be used as legacy ports while SER2 and SER3 will require additional drivers. Only SER2 and SER3 support 4Mbps. For SER0 and SER1, please contact your ADLINK representative.

CAN bus

2x CAN2.0B only or mixed CAN2.0B and CAN FB mode, data bit rate up to 8 Mbps, only supported on Linux

SPI

1x SPI, 1x eSPI

SPI0: FSPI interface for BIOS and TPM)

SPI1: eSPI interface for flash device

HDA / I2S

1x High-Definition Audio (HDA) as default or 1x I2S on I2S2 port

I2C

4x I2C interfaces

Supports 7-bit and 10-bit address modes

Software programmable clock frequency:

- 100 kbit/s in Standard-mode
- 400 kbit/s in Fast-mode
- 1 Mbit/s in Fast-mode Plus

GPIO

14x GPIO with interrupt (GPIO4 used as HAD_RST# by default)

2.6 System Storage

SDIO

1x SDIO (4-bit) compatible up to version 3.0.

eMMC

Soldered on module 8, 16, 32, 64, 128 GB (build option) either standard or at -40 to 85°C temperature range

Compatible with eMMC specification 4.51 and higher

2.7 Board Controller

BMC lite for power sequence

SEMA BMC Error Code

Exception Code	Error Code
0	NOERROR
2	NO_VIN
3	NO_SDM_RESIN_N
4	NO_SDM_RESIN_N

2.8 SEMA® Board Management Controller

Voltage/current monitoring, boot configuration, logistics, forensic information, flat panel control, watchdog timer

2.9 Debug Header

30-pin multipurpose flat cable connector for use with optional DB-30 debug module

Provides JTAG, BMC access; UART, power test points; diagnostic LEDs, Power, Reset, Boot configuration

2.10 BIOS

Single BIOS chip, UEFI BIOS

2.11 Power

Supply Voltage

5V +/- 5%

Power Sequencing

VDD_IN is the first power domain to be turned on by the carrier circuit during power-up. Other circuit components on the carrier, which are galvanically coupled to the module, shall not be supplied to avoid feedback. From the moment VDD_IN is stable — recognizable by VIN_PWR_BAD# de-asserted — the module takes over control of the power sequencing. As soon as the module reaches the next system state standby, CARRIER_PWR_ON signals the carrier to switch on all its standby voltages. No feedback is provided to allow the carrier to signal Power OK to the modules power state machine. When the state Runtime is reached, the module de-asserts CARRIER_STBY#. The carrier then switches on the remaining rails.

2.12 Mechanical and Environmental

Form Factor

SGET SMARC Specifications v2.1.1

Dimension

SMARC small size module, 82mm x 50mm

Operating Temperature

Standard: 0°C to 60°C

Rugged: -40°C to 85°C (optional)

Humidity

5-90% RH operating, non-condensing

5-95% RH storage (and operating with conformal coating)

Shock and Vibration

IEC 60068-2-64 and IEC-60068-2-27, MIL-STD-202 F, Method 213B, Table 213-I,

Condition A and Method 214A, Table 214-I, Condition D

3. Block Diagram

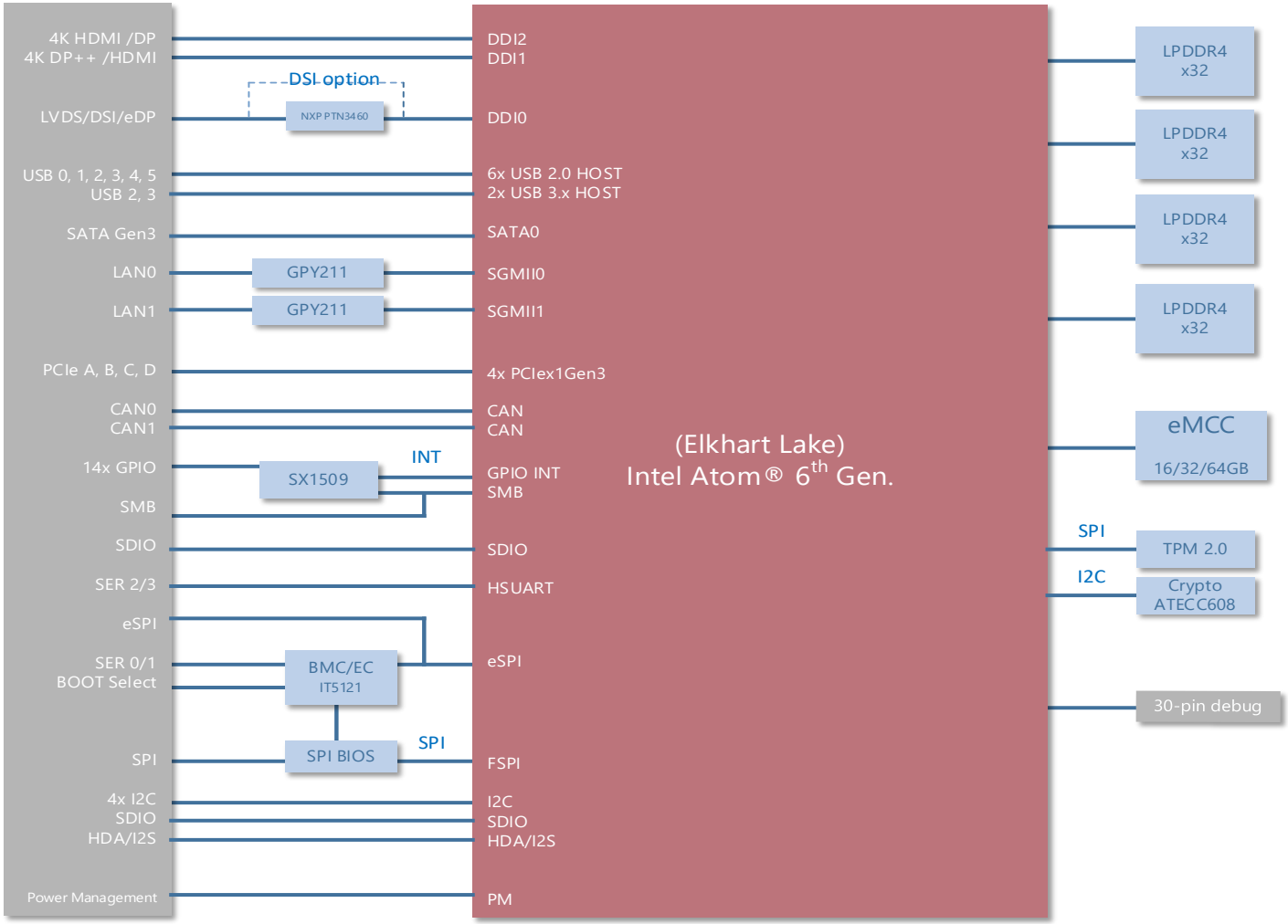


Figure 1 – Module function diagram

4. Pinout and Signal Descriptions

4.1 Pin Summary

The below tables are a list of all signal pins on the MXM 3 connector in the standard specification of SMARC 2.1.

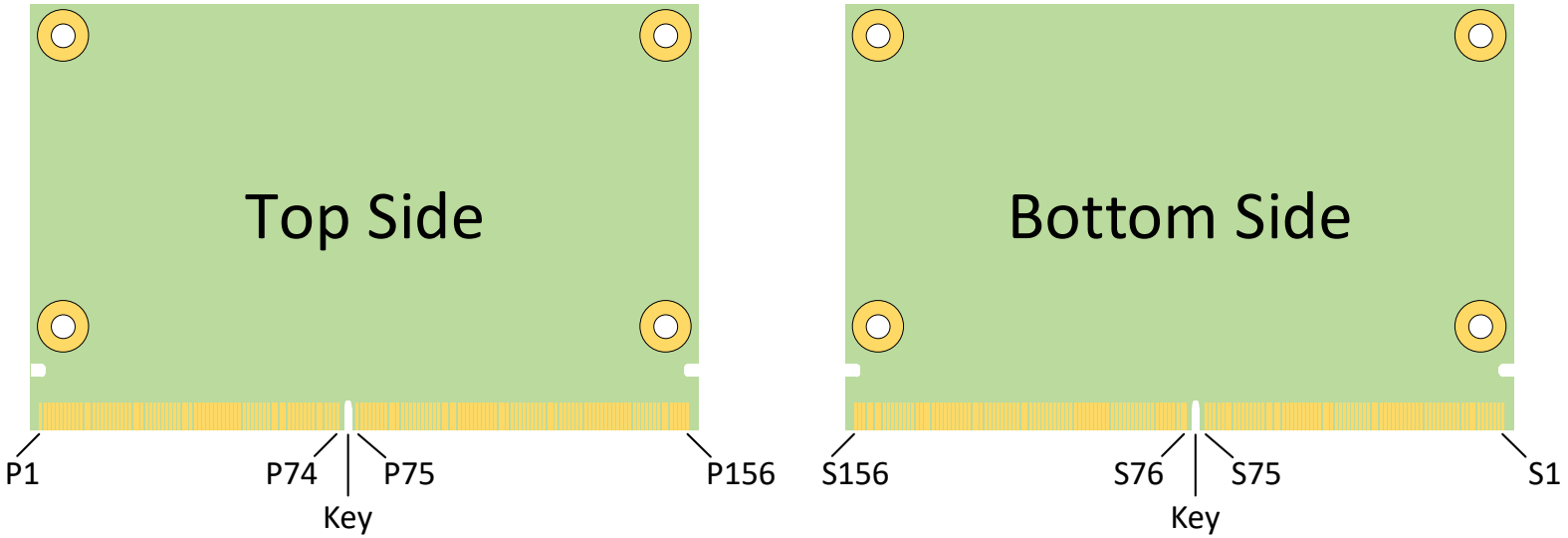


Figure 2 – Module top/botom side pin numbering

4.2 Signal Terminology Descriptions

Meaning of the terms used for signal description tables. Signals described in the specification but not supported on the LEC-EL are marked with strikethrough ~~STRIKETHROUGH~~

Term	Description
I	Input to the module
O	Output from the module
O OD	Open drain output from the module
I OD	Open drain input to the module, with mandatory PU (pull up) on module
OD	Open drain
I/O	Bi-directional Input/Output
PU	PU (pull-up) resistor on module
PD	PD (pull-down) resistor on module
VDD_IN	Main power source from carrier to module
CMOS	Logic input or output
GBE MDI	Differential analog signaling for Gigabit Media Dependent Interface
LVDS DP	Low Voltage Differential Signal for DisplayPort interface
LVDS D-PHY	Low Voltage Differential Signal for MIPI CSI-2 cameras and DSI displays
LVDS M-PHY	Low Voltage Differential Signal for MIPI CSI-3 cameras
LVDS LCD	Low Voltage Differential Signal for LCD displays
LVDS PCIE	Low Voltage Differential Signal for PCIe
LVDS SATA	Low Voltage Differential Signal for SATA
TMDS HDMI	Transition Minimized Differential Signal for HDMI displays
USB	DC coupled differential signaling for traditional (non-Superspeed) USB signals
USB SS	Differential signal for SuperSpeed USB signals
USB VBUS 5V	5V tolerant input for USB VBUS detection
3.3V	3.3V Power Domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
1.8V	1.8V Power Domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
3.3Vsb	3.3V Power Domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)
1.8Vsb	1.8V Power Domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)

4.3 Signal Description by function

4.3.1 The First Display Interface

The first display interface is a group of 30-pins that is split into a channel 0 and channel 1. The SMARC specification allows support for dual channel LVDS ports, 2 separate single channel LVDS ports, 2 MIPI DSI ports of 4 lanes each or 2 eDP ports 4 lanes each. A mix of different display type such as DSI and eDP is also permitted. Below tables show which display ports are supported on this particular module

Pin #	LVDS Name	MIPI DSI Name	eDP Name
S125 S126 S128 S129 S131 S132 S137 S138	LVDS0_0+ LVDS0_0- LVDS0_1+ LVDS0_1 - LVDS0_2+ LVDS0_2- LVDS0_3+ LVDS0_3-	DSI0_D0+ DSI0_D0- DSI0_D1+ DSI0_D1- DSI0_D2+ DSI0_D2- DSI0_D3+ DSI0_D3-	eDP0_TX0+ eDP0_TX0- eDP0_TX1+ eDP0_TX1- eDP0_TX2+ eDP0_TX2- eDP0_TX3+ eDP0_TX3-
S134 S135	LVDS0_CK+ LVDS0_CK-	DSI0_CLK+ DSI0_CLK-	eDP0_AUX+ eDP0_AUX-
S133	LCD0_VDD_EN	LCD0_VDD_EN	LCD0_VDD_EN
S127	LCD0_BKLT_EN	LCD0_BKLT_EN	LCD0_BKLT_EN
S141	LCD0_BKLT_PWM	LCD0_BKLT_PWM	LCD0_BKLT_PWM
S144		DSI0_TE	eDP0_HPD

Pin #	LVDS Name	MIPI DSI Name	eDP Name
S111 S112 S114 S115 S117 S118 S120 S121	LVDS1_0+ LVDS1_0- LVDS1_1+ LVDS1_1 - LVDS1_2+ LVDS1_2- LVDS1_3+ LVDS1_3-	~~DSI1_D0+~~ ~~DSI1_D0-~~ ~~DSI1_D1+~~ ~~DSI1_D1-~~ ~~DSI1_D2+~~ ~~DSI1_D2-~~ ~~DSI1_D3+~~ ~~DSI1_D3-~~	eDP1_TX0+ eDP1_TX0- eDP1_TX1+ eDP1_TX1- eDP1_TX2+ eDP1_TX2- eDP1_TX3+ eDP1_TX3-
S108 S109	LVDS1_CK+ LVDS1_CK-	~~DSI1_CLK+~~ ~~DSI1_CLK-~~	eDP1_AUX+ eDP1_AUX-
S116	LCD1_VDD_EN	~~LCD1_VDD_EN~~	LCD1_VDD_EN
S107	LCD1_BKLT_EN	~~LCD1_BKLT_EN~~	LCD1_BKLT_EN
S122	LCD1_BKLT_PWM	~~LCD1_BKLT_PWM~~	LCD1_BKLT_PWM
S113		~~DSI1_TE~~	eDP1_HPD

S139	I2C_LCD_CK	~~I2C_LCD_CK~~	I2C_LCD_CK
S140	I2C_LCD_DAT	~~I2C_LCD_DAT~~	I2C_LCD_DAT

Note :

1. LVDS0/LVDS1 are standard supported through a eDP to LVDS bridge on the module
2. eDP or DSI can be used by build option, disabling the LVDS0/LVDS1 ports.

4.3.1.1 LVDS0/LVDS1 mode

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
LVDS0_0+ LVDS0_0- LVDS0_1+ LVDS0_1 - LVDS0_2+ LVDS0_2- LVDS0_3+ LVDS0_3-	S125 S126 S128 S129 S131 S132 S137 S138	Primary LVDS Channel Differential Pair Data Lines	O LVDS		Runtime		100 ohm differential termination across the differential pairs at the endpoint of the signal path, usually on the display assembly.
LVDS0_CK+ LVDS0_CK-	S134 S135	Primary LVDS Channel Differential Pair Clock Lines	O LVDS		Runtime		100 ohm differential termination across the differential pair at the endpoint of the signal path, usually on the display assembly.
LCD0_VDD_EN	S133	Primary LVDS Channel Power Enable	O CMOS	1.8V	Runtime		Active high
LCD0_BKLT_EN	S127	Primary LVDS Channel Backlight Enable	O CMOS	1.8V	Runtime		Active high
LCD0_BKLT_PWM	S141	Primary LVDS Channel Brightness Control	O CMOS	1.8V	Runtime		Through pulse width modulation (PWM)
LVDS1_0+ LVDS1_0- LVDS1_1+ LVDS1_1 - LVDS1_2+ LVDS1_2- LVDS1_3+ LVDS1_3-	S111 S112 S114 S115 S117 S118 S120 S121	Secondary LVDS Channel Differential Pair Data Lines	O LVDS		Runtime		100 ohm differential termination across the differential pairs at the endpoint of the signal path, usually on the display assembly.
LVDS1_CK+ LVDS1_CK-	S108 S109	Secondary LVDS Channel Differential Pair Clock Lines	O LVDS		Runtime		100 ohm differential termination across the differential pair at the endpoint of the signal path, usually on the display assembly.

~~LCD1_VDD_EN~~	~~S116~~	~~Secondary LVDS Channel Power Enable~~	~~O CMOS~~	~~1.8V~~	~~Runtime~~	-	~~Active high Only in use, when two separate LVDS ports are supported, please check Module user manual~~
~~LCD1_BKLT_EN~~	~~S107~~	~~Secondary LVDS Channel Backlight Enable~~	~~O CMOS~~	~~1.8V~~	~~Runtime~~	-	~~Active high Only in use, when two separate LVDS ports are supported, please check Module user manual~~
~~LCD1_BKLT_PWM~~	~~S122~~	~~Secondary LVDS Channel Brightness Control~~	~~O CMOS~~	~~1.8V~~	~~Runtime~~	-	~~Through pulse width modulation (PWM) only in use, when two separate LVDS ports are supported, please check Module user manual~~

I2C_LCD_DAT	S140	DDC data line used for flat panel detection and control	I/O OD CMOS	1.8V	Runtime	PU 2k2	Possible conflict if two LVDS panels are used
I2C_LCD_CK	S139	DDC clock line used for flat panel detection and control	O OD CMOS	1.8V	Runtime	PU 2k2	Possible conflict if two LVDS panels are used

4.3.1.2 eDP mode (build option)

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
eDP0_TX0+ eDP0_TX0- eDP0_TX1+ eDP0_TX1- eDP0_TX2+ eDP0_TX2- eDP0_TX3+ eDP0_TX3-	S125 S126 S128 S129 S131 S132 S137 S138	Primary 4-Lane eDP Differential Pair Data Lines	O DP		Runtime		AC coupled off Module 100 nF DC blocking capacitors ***shall*** be placed on the Carrier.
eDP0_AUX+ eDP0_AUX-	S134 S135	Primary Bidirectional Channel used for Link Management and Device Control	I/O DP		Runtime		AC coupled off Module
LCD0_VDD_EN	S133	Primary Panel Power Enable	O CMOS	1.8V	Runtime		Active high
LCD0_BKLT_EN	S127	Primary Panel Backlight Enable	O CMOS	1.8V	Runtime		Active high

LCD0_BKLT_PWM	S141	Primary Panel Brightness Control	O CMOS	1.8V	Runtime		Through pulse width modulation (PWM)
eDP0_HPD	S144	Detection of Hot Plug / Unplug of Primary eDP Display and Notification of the Link Layer	I CMOS	1.8V	Runtime	PD 1M	Module must tolerate high level in stand-by mode

4.3.2 Second Display Interface

Pin #	HDMI signal names	DP++ signal names
P92 P93 P95 P96 P98 P99	HDMI_D2+ HDMI_D2- HDMI_D1+ HDMI_D1- HDMI_D0+ HDMI_D0-	DP1_LANE0+ DP1_LANE0- DP1_LANE1+ DP1_LANE1- DP1_LANE2+ DP1_LANE2-
P101 P102	HDMI_CK+ HDMI_CK-	DP1_LANE3+ DP1_LANE3-
S105	HDMI_CTRL_CK	DP1_AUX+
S106	HDMI_CTRL_DAT	DP1_AUX-
P104	HDMI_HPD	DP1_HPD

4.3.2.1 HDMI

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
HDMI_D2+ HDMI_D2- HDMI_D1+ HDMI_D1- HDMI_D0+ HDMI_D0-	P92 P93 P95 P96 P98 P99	HDMI port, differential pair data lines	O TMDS HDMI		Runtime		AC coupled off module
HDMI_CK+ HDMI_CK-	P101 P102	HDMI port, differential pair clock lines	O TMDS HDMI		Runtime		AC coupled off module
HDMI_CTRL_CK	P105	I2C_CLK line dedicated to HDMI	O OD COMS	1.8V	Runtime	PU 100K	Level shifter FET and 5V PU resistor ***shall*** be placed between the Module and the HDMI connector. Stronger pull-up is demanded to the carrier board. The pull-ups may be part of an integrated HDMI ESD protection and control-line level shift device, such as the Texas Instruments TPD12S016. If discrete Carrier pull-ups are used, the value depends on the individual carrier board implementation.
HDMI_CTRL_DAT	P106	I2C_DAT line dedicated to HDMI	I/O OD COMS	1.8V	Runtime	PU 100K	Level shifter FET and 5V PU resistor ***shall*** be placed between the Module and the HDMI connector. Stronger pull-up is demanded to the carrier board. The pull-ups may be part of an integrated HDMI ESD protection and control-line level shift device, such as the Texas Instruments TPD12S016. If discrete Carrier pull-ups are used, the value depends on the individual carrier board implementation.
HDMI_HPD	P104	HDMI Hot plug active high detection signal that serves as an interrupt request	I CMOS	1.8V	runtime	PD 1M	Module must tolerate high level in stand-by mode

4.3.3 MIPI Camera support

4.3.3.1 MIPI CSI0

This design does not support CSI

4.3.4 HDA (Audio)

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
HDA_SYNC / I2S2_LRCK	S50	High Definition Audio Sample synchronization clock to codec	I/O CMOS	1.8V / 1.5V	Runtime		SMARC HDA Audio signalling supports 1.5V or 1.8V. Please check with your module vendor if 1.5V or 1.8V is supported and use an audio codec that is capable to support the regarding I/O voltage. This specification ignores the discrepancy between the 1.5V and 1.8V signalling, as the chance of damage in mismatched systems is negligible. The SMARC HD Audio pins are shared with the I2S2 pins, which are defined to be 1.8V only.
HDA_SDO / I2S2_SDOUT	S51	High Definition Audio data out to codec	O CMOS	1.8V / 1.5V	Runtime		
HDA_SDI / I2S2_SDIN	S52	High Definition Audio data in from codec	I/O CMOS	1.8V / 1.5V	Runtime		
HDA_CK / I2S2_CK	S53	High Definition Audio clock to codec	O CMOS	1.8V / 1.5V	Runtime		
HDA_RST# / GPIO4	P112	High Definition Audio reset output to codec, low active.	O CMOS	1.8V / 1.5V	Runtime		

Note: Support for I2S1 signalling pins has been removed during update to SMARC 2.0 specification

4.3.5 USB ports

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
USB0+ USB0-	P60 P61	USB differential data pairs for port 0	I/O USB	USB	Standby		
USB0_EN_OC#	P62	USB over-current sense for port 0	I/O OD CMOS	3.3Vsb / 3.3V	Standby	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
~~USB0_VBUS_DET~~	~~P63~~	~~USB port 0 host power detection, when this port is used as a device.~~	~~I USB VBUS 5V~~	~~USB VBUS 5V~~	~~Standby~~		Can be connected to a USB client port VBUS pin
~~USB0_OTG_ID~~	~~P64~~	~~Input pin to announce OTG device insertion on USB 2.0 port~~	~~I CMOS~~	~~3.3Vsb / 3.3V~~	~~Standby~~		
USB1+ USB1-	P65 P66	USB differential data pairs for port 1	I/O USB	USB	Standby		
USB1_EN_OC#	P67	USB over-current sense for port 1	I/O OD CMOS	3.3Vsb / 3.3V	Standby	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB2+ USB2-	P69 P70	USB differential data pairs for port 2	I/O USB	USB	Standby		
USB2_SSRX+ USB2_SSRX-	S74 S75	Receive signal differential pairs for SuperSpeed on port 2	I USB SS	USB SS	Standby		Coupling caps for RX pairs are on the USB Device
USB2_SSTX+ USB2_SSTX-	S71 S72	Transmit signal differential pairs for SuperSpeed on port 2	O USB SS	USB SS	Standby		Coupling caps for TX pairs are on the Module
USB2_EN_OC#	P71	USB over-current sense for port 2	I/O OD CMOS	3.3Vsb / 3.3V	Standby	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB3+ USB3-	S68 S69	USB differential data pairs for port 3	I/O USB	USB	Standby		
USB3_SSRX+ USB3_SSRX-	S65 S66	Receive signal differential pairs for SuperSpeed on port 3	I USB SS	USB SS	Standby		Coupling caps for RX pairs are on the USB Device

USB3_SSTX+ USB3_SSTX-	S62 S63	Transmit signal differential pairs for SuperSpeed on port 3	O USB SS	USB SS	Standby		Coupling caps for TX pairs are on the Module
USB3_EN_OC#	P74	USB over-current sense for port 3	I/O OD CMOS	3.3Vsb / 3.3V	Standby	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
~~USB3_VBUS_DET~~	~~S37~~	~~USB port 3 host power detection, when this port is used as a device.~~	~~I USB VBUS 5V~~	~~USB VBUS 5V~~	~~Standby~~		
~~USB3_OTG_ID~~	~~S104~~	~~Input pin to announce OTG device insertion on USB 3.0 port~~	~~I CMOS~~	~~3.3Vsb / 3.3V~~	~~Standby~~		
USB4+ USB4-	S35 S36	USB differential data pairs for port 4	I/O USB	USB	Standby		
USB4_EN_OC#	P76	USB over-current sense for port 4	I/O OD CMOS	3.3Vsb / 3.3V	Standby	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB5+ USB5-	S59 S60	USB differential data pairs for port 5	I/O USB	USB	Standby		
USB5_EN_OC#	S55	USB over-current sense for port 5	I/O OD CMOS	3.3Vsb / 3.3V	Standby	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.

Note: All USB connected straight from SoC , no support for OTG

4.3.6 PCIe Ports

The module supports 4x PCIe Gen 3.0 ports

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
PCIE_A_TX+ PCIE_A_TX-	P89 P90	Differential PCIe link A transmit data pair	O LVDS PCIE		Runtime		Series AC coupled on module
PCIE_A_RX+ PCIE_A_RX-	P86 P87	Differential PCIe link A receive data pair	I LVDS PCIE		Runtime		Series AC coupled off module
PCIE_A_REFCK+ PCIE_A_REFCK-	P83 P84	Differential PCIe Link A reference clock output	O LVDS PCIE		Runtime		
PCIE_A_RST#	P75	PCIe Port A reset output	O CMOS	3.3V	Runtime		
PCIE_A_CKREQ#	P78	PCIe Port A clock request	I OD CMOS	3.3V	Runtime		Can be used for power saving mode on PCIe - Pulled up or terminated on Module
PCIE_B_TX+ PCIE_B_TX-	S90 S91	Differential PCIe link B transmit data pair	O LVDS PCIE		Runtime		Series AC coupled on module
PCIE_B_RX+ PCIE_B_RX-	S87 S88	Differential PCIe link B receive data pair	I LVDS PCIE		Runtime		Series AC coupled off module
PCIE_B_REFCK+ PCIE_B_REFCK-	S84 S85	Differential PCIe Link B reference clock output	O LVDS PCIE		Runtime		
PCIE_B_RST#	S76	PCIe Port B reset output	O CMOS	3.3V	Runtime		
PCIE_B_CKREQ#	P77	PCIe Port B clock request	I OD CMOS	3.3V	Runtime		Can be used for power saving mode on PCIe - Pulled up or terminated on Module
PCIE_C_TX+ PCIE_C_TX-	S81 S82	Differential PCIe link C transmit data pair	O LVDS PCIE		Runtime		Series AC coupled on module
PCIE_C_RX+ PCIE_C_RX-	S78 S79	Differential PCIe link C receive data pair	I LVDS PCIE		Runtime		Series AC coupled off module
PCIE_C_REFCK+ PCIE_C_REFCK-	P80 P81	Differential PCIe Link C reference clock output	O LVDS PCIE		Runtime		

PCIE_C_RST#	S77	PCIe Port C reset output	O CMOS	3.3V	Runtime		
PCIE_D_TX+ PCIE_D_TX-	S29 S30	Differential PCIe link D transmit data pair	O LVDS PCIE		Runtime		Series AC coupled on module
PCIE_D_RX+ PCIE_D_RX-	S32 S33	Differential PCIe link D receive data pair	I LVDS PCIE		Runtime		Series AC coupled off module
PCIE_WAKE#	S146	PCIe wake up interrupt to host – common to PCIe links A, B, C, D	I OD CMOS	3.3V	Standby	PU 10k	

4.3.7 SATA Gen 3 Ports

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SATA0_TX+ SATA0_TX-	P48 P49	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Runtime		Series AC coupled on Module 10 nF
SATA0_RX+ SATA0_RX-	P51 P52	Serial ATA channel 0, Receive Input differential pair.	I SATA		Runtime		Series AC coupled on Module 10 nF
SATA_ACT#	S54	SATA activity indicator	O OD CMOS	3.3V	Runtime		Shall be able to sink 24mA or more Carrier LED current

4.3.8 LAN ports

4.3.8.1 First LAN port

The first LAN port is derived from the SoC's RGMII interface

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	P30 P29 P27 P26 P24 P23 P20 P19	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations	I/IO GBE MDI		Standby		Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000 100 10 MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-
GBE0_LINK100#	P21	Link Speed Indication LED for GBE0 10/100Mbps	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current [1]
GBE0_LINK1000#	P22	Link Speed Indication LED for GBE0 1000Mbps	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current [1]
GBE0_LINK_ACT#	P25	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current [1]
GBE0_CTREF	P28	Center-Tap reference voltage for Carrier board Ethernet magnetic (if required by the Module GBE PHY)	Analog	0 to 3.3V max	Standby		
GBE0_SDP	P6	IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol)	IO CMOS	3.3V	Standby		

4.3.8.2 Second LAN port

The second LAN port is derived from the SOCs RGMII interface

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GBE1_MDI0+ GBE1_MDI0- GBE1_MDI1+ GBE1_MDI1- GBE1_MDI2+ GBE1_MDI2- GBE1_MDI3+ GBE1_MDI3-	S17 S18 S20 S21 S23 S24 S26 S27	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations	I/O GBE MDI		Standby		Gigabit Ethernet Controller 1: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000 100 10 MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-
GBE1_LINK100#	S19	Link Speed Indication LED for GBE1 10/100Mbps	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current [1]
GBE1_LINK1000#	S22	Link Speed Indication LED for GBE1 1000Mbps	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current [1]
GBE1_LINK_ACT#	S31	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current [1]
GBE1_CTREF	S28	Center-Tap reference voltage for Carrier board Ethernet magnetic (if required by the Module GBE PHY)	Analog	0 to 3.3V max	Standby		
GBE1_SDP	P5	IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol)	IO CMOS	3.3V	Standby		

Note:
1. Both LAN interfaces use a GPY 2.5Gb Ethernet PHY, there is also a 1Gb pin-compatible part.
2. LAN LEDs are inactive when the LAN transfer rate is 2.5Gb.

4.3.9 SDIO

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SDIO_D0 SDIO_D1 SDIO_D2 SDIO_D3	P39 P40 P41 P42	SDIO Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
SDIO_WP	P33	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I OD CMOS	3.3V	Runtime	PU 10k	Pulled up on module
SDIO_CMD	P34	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
SDIO_CD#	P35	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	I OD CMOS	3.3V	Runtime	PU 10k	Pulled up on module
SDIO_CK	P36	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	O CMOS	1.8V or 3.3V	Runtime		
SDIO_PWR_EN	P37	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	O CMOS	3.3V	Runtime		should be driven low in STB Mode by the module

4.3.10 SPI & ESPI

4.3.11 SPI0

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SPI0_CS0#	P43	SPI0 Master Chip Select 0	O CMOS	1.8V	Standby		This signal can be used to select carrier SPI as boot device
SPI0_CS1#	P31	SPI0 Master Chip Select 1	O CMOS	1.8V	Standby		
SPI0_CK	P44	SPI0 Clock	O CMOS	1.8V	Standby		
SPI0_DIN	P45	SPI0 Master input / Slave output	I CMOS	1.8V	Standby		also referred to as MISO
SPI0_DO	P46	SPI0 Master output / Slave input	O CMOS	1.8V	Standby		also referred to as MOSI

~~SPI1_CS0#~~	~~P54~~	~~SPI1 Master Chip Select 0~~	~~O CMOS~~	~~1.8V~~	~~Standby~~	-	See ESPI
~~SPI1_CS1#~~	~~P55~~	~~SPI1 Master Chip Select 1~~	~~O CMOS~~	~~1.8V~~	~~Standby~~	-	See ESPI
~~SPI1_CK~~	~~P56~~	~~SPI1 Clock~~	~~O CMOS~~	~~1.8V~~	~~Standby~~	-	See ESPI
~~SPI1_DIN~~	~~P57~~	~~SPI1 Master input / Slave output~~	~~I CMOS~~	~~1.8V~~	~~Standby~~	-	See ESPI
~~SPI1_DO~~	~~P58~~	~~SPI1 Master output / Slave input~~	~~O CMOS~~	~~1.8V~~	~~Standby~~	-	See ESPI

Note: SPI bus only supports FSPI mode on LEC-EL.

4.3.12 ESPI

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
ESPI_CS0#	P54	ESPI1 Master Chip Select 0	O CMOS	1.8V	Standby		
ESPI_CS1#	P55	ESPI1 Master Chip Select 1	O CMOS	1.8V	Standby		
ESPI_CK	P56	ESPI Master Clock output	O CMOS	1.8V	Standby		
ESPI_RESET#	S58	ESPI Reset	O CMOS	1.8V	Standby		Reset the eSPI interface for both master and slaves. eSPI Reset# is typically driven from eSPI master to eSPI slaves
ESPI_ALERT0# ESPI_ALERT1#	S43 S44	ESPI ALERT	I OD CMOS	1.8V	Standby		This pin is used by eSPI slave to request service from eSPI.master.Alert# is an open-drain output from the slave. This pin is optional for Single Master-Single Slave configuration where I/O[1] can be used to signal the Alert event.
ESPI_IO_0 ESPI_IO_1 ESPI_IO_2 ESPI_IO_3	P58 P57 S56 S57	ESPI Master Data Input / Output.	I/O CMOS	1.8V	Standby		ESPI_IO_0 can also be used as SPI1_DO (MOSI) ESPI_IO_1 can also be used as SPI1_DIN (MISO) In Single I/O mode, ESPI_IO_0 is the eSPI master output / eSPI slave input (MOSI) whereas ESPI_IO_1 is the SPI master input / eSPI slave output (MISO).

4.4 General Purpose I2C

The SMARC specification supports a total of 6 different I2C busses on its pinout. Most of these busses are designated for specific functions such as I2C for camera management, I2C for EDID on HDMI, LVDS panels or I2C for PMIC. Only one I2C bus is marked as General purpose

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
I2C_GP_DAT	S49	General purpose I2C data signal	I/O OD CMOS	1.8V	Runtime	PU 2k2	
I2C_GP_CK	S48	General purpose I2C clock signal	O OD CMOS	1.8V	Runtime	PU 2k2	

Most of the other I2C busses are described in their designated function tables as opposed to a combined list.

Below is an overview of all I2C busses and where to find them.

Name	Pin #	Description	Where to find
I2C_LCD_DAT	S140	DDC data line used for flat panel detection and control	LVDS / DSI / eDP tables
I2C_LCD_CK	S139	DDC clock line used for flat panel detection and control	LVDS / DSI / eDP tables
HDMI_CTRL_CK	P105	I2C_CLK line dedicated to HDMI	HDMI table
HDMI_CTRL_DAT	P106	I2C_DAT line dedicated to HDMI	HDMI table
~~I2C_CAM0_DAT~~	~~S7~~	~~I2C data for serial camera data support link~~	~~MIPI CSI table~~
~~I2C_CAM0_CK~~	~~S5~~	~~I2C clock for serial camera data support link~~	~~MIPI CSI table~~
~~I2C_CAM1_DAT~~	~~S2~~	~~I2C data for serial camera data support link~~	~~MIPI CSI table~~
~~I2C_CAM1_CK~~	~~S1~~	~~I2C clock for serial camera data support link~~	~~MIPI CSI table~~
I2C_PM_DAT	P122	Power management I2C bus DATA (SMBus for x86)	Power and System Management
I2C_PM_CK	P121	Power management I2C bus CLK (SMBus for x86)	Power and System Management

4.4.1 GPIO

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GPIO0 / ~~CAM0_PWR#~~	P108	General purpose I/O pin 0.	I/O CMOS	1.8V	Runtime	PU 470K on the Module.	Default use is GPIO0, alternative use is Camera 0 Power Enable - active low, through DTS
GPIO1 / ~~CAM1_PWR#~~	P109	General purpose I/O pin 1.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	Default use is is GPIO1 alternative use is Camera 1 Power Enable - active low, through DTS
GPIO2 / CAM0_RST#	P110	General purpose I/O pin 2.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	Default use is GPIO2, alternative use is Camera 0 Reset - active low, through DTS
GPIO3 / ~~CAM1_RST#~~	P111	General purpose I/O pin 3.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	Default use is GPIO3, alternative use is Camera 1 Reset - active low, through DTS
~~GPIO4~~ / HDA_RST#	P112	General purpose I/O pin 4.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	GPIO 4 support requires BOM change
GPIO5 / ~~PWM_OUT~~	P113	General purpose I/O pin 5.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO6	P114	General purpose I/O pin 6.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO7	P115	General purpose I/O pin 7.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO8	P116	General purpose I/O pin 8.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO9	P117	General purpose I/O pin 9.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO10	P118	General purpose I/O pin 10.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO11	P119	General purpose I/O pin 11.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO12	S142	General purpose I/O pin 12	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO13	S123	General purpose I/O pin 13	I/O CMOS	1.8V	Runtime	PU 470K on the Module	

4.4.2 UART

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SER0_TX	P129	Asynchronous serial data output port 0	O CMOS	1.8V	Runtime		
SER0_RX	P130	Asynchronous serial data input port 0	I CMOS	1.8V	Runtime		
SER0_RTS#	P131	"Request to Send" handshake line for port 0	O CMOS	1.8V	Runtime		
SER0_CTS#	P132	"Clear to Send" handshake line for port 0	I CMOS	1.8V	Runtime		
SER1_TX	P134	Asynchronous serial data output port 1	O CMOS	1.8V	Runtime		
SER1_RX	P135	Asynchronous serial data input port 1	I CMOS	1.8V	Runtime		
SER2_TX	P136	Asynchronous serial data output port 2	O CMOS	1.8V	Runtime		-
SER2_RX	P137	Asynchronous serial data input port 2	I CMOS	1.8V	Runtime		-
SER2_RTS#	P138	"Request to Send" handshake line for port 2	O CMOS	1.8V	Runtime		-
SER2_CTS#	P139	"Clear to Send" handshake line for port 2	I CMOS	1.8V	Runtime		-
SER3_TX	P140	Asynchronous serial data output port 3	O CMOS	1.8V	Runtime		
SER3_RX	P141	Asynchronous serial data input port 3	I CMOS	1.8V	Runtime		

4.4.3 CAN bus

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CAN0_TX	P143	CAN port 0 Transmit output	O CMOS	1.8V	Runtime		Only supported on Linux
CAN0_RX	P144	CAN port 0 Receive input	I CMOS	1.8V	Runtime		Only supported on Linux
CAN1_TX	P145	CAN port 1 Transmit output	O CMOS	1.8V	Runtime		Only supported on Linux
CAN1_RX	P146	CAN port1 Receive input	I CMOS	1.8V	Runtime		Only supported on Linux

4.4.4 Miscellaneous

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
TEST#	S157	Held low by Carrier to invoke Module vendor specific test function(s).	I CMOS	1.8V	Runtime	PU on Module. Driven by OD on Carrier	Module must implement PU but actual value is depended on particular module design. Carrier Board should leave this pin floating for normal operation
WDT_TIME_OUT#	S145	Watch-Dog-Timer Output, low active.	O CMOS	1.8V	Runtime		Driven only during runtime

4.4.5 Power and System Management

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
BATLOW#	S156	Battery low indication to Module. Carrier to float the line in inactive state.	I OD CMOS	1.8V	Runtime	PU 10K	Driven by OD on Carrier. Pulled up on module.
CARRIER_PWR_ON	S154	Carrier board circuits (apart from power management and power path circuits) should not be powered up until the Module asserts the CARRIER_PWR_ON signal.	O CMOS	1.8Vsb / 1.8V	-		1.8Vsb is only used for signaling, not a power source to the module
CARRIER_STBY#	S153	The Module shall drive this signal low when the system is in a standby power state.	O CMOS	1.8Vsb / 1.8V	-		
CHARGER_PRSNT#	S152	Held low by Carrier if DC input for battery charger is present.	I OD CMOS	1.8V	Runtime	PU 4.7K	Driven by OD on Carrier. Pulled up on module.
CHARGING#	S151	Held low by Carrier during battery charging. Carrier to float the line when charge is complete.	I OD CMOS	1.8V	Runtime	PU 4.7K	Driven by OD on Carrier. Pulled up on module.
VIN_PWR_BAD#	S150	Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) shall not be enabled while this signal is held low by the Carrier.	I OD CMOS	1.8V	Runtime	PU 2.2K	Driven by OD on Carrier Module must implement PU but actual value is depended on particular module design.
SLEEP#	S149	Sleep indicator from Carrier board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module.	I OD CMOS	1.8V	Runtime	PU 4.7K	Driven by OD on Carrier. Pulled up on module.
LID#	S148	Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module.	I OD CMOS	1.8V	Runtime	PU 4.7K	Driven by OD on Carrier. Pulled up on module.
POWER_BTN#	P128	Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module.	I OD CMOS	1.8V	Runtime	PU 4.7K	Driven by OD on Carrier. Pulled up on module.
RESET_OUT#	P126	General purpose reset output to Carrier board.	O CMOS	1.8V	Runtime		

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
RESET_IN#	P127	Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise.	I OD CMOS	1.8V	Runtime	PU 4.7K	Driven by OD on Carrier. Pulled up on module.
I2C_PM_DAT	P122	Power management I2C bus DATA	I/O OD CMOS	1.8V	Runtime	PU 2k2	On x86 systems these serve as SMB DATA. Pulled up on module.
I2C_PM_CK	P121	Power management I2C bus CLK	O OD CMOS	1.8V	Runtime	PU 2k2	On x86 systems these serve as SMB CLK. Pulled up on module.
SMB_ALERT_1V8#	P1	SMBus Alert# (interrupt) signal	I OD CMOS	1.8V	Runtime	PU 2k2	only used on x86 design

4.4.6 Boot Select

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
BOOT_SEL0# BOOT_SEL1# BOOT_SEL2#	P123 P124 P125	Input straps determine the Module boot	I OD CMOS	1.8Vsb	Standby	PU 4.7K	Driven by OD on Carrier. Pulled up on module. Supports MODE 7 (default) and MODE 3.
~~FORCE_RECOV#~~	S155		~~I OD CMOS~~	~~1.8Vsb~~	~~Standby~~	~~PU 10K~~ -	~~Driven by OD on Carrier.~~ ~~Pulled up on module.~~ ~~Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based Force Recovery functions, then a low on the Module FORCE_RECOV# pin may invoke the SOC native Force Recovery mode – such as over a Serial Port. For x86 systems this signal may be used to load BIOS defaults. Pulled up on Module. Driven by OD part on Carrier.~~

4.4.7 Power

Name	Pin #	Description	I/O Type	Power Rail / Tolerance	PU / PD	Comments
VDD_IN	P147, P148, P149, P150, P151, P152, P153, P154, P155, P156	Module power input voltage 4.75 min to 5.25V max	P	4.75 to 5.25V		
GND	P2, P9, P12, P15, P18, P32, P38, P47, P50, P53, P59, P68, P79, P82, P85, P88, P91, P94, P97, P100, P103, P120, P133, P142, S3, S10, S16, S25, S34, S47, S61, S64, S67, S70, S73, S80, S83, S86, S89, S92, S101, S110, S119, S124, S130, S136, S143, S158	Module signal and power return, and GND reference	P	Ground		
VDD_RTC	S147	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based Lithium cell or Super Cap.	P	[2 to 3.25] / 3.25V		

4.5 SMARC pin to controller mapping

Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	I/O Mux default	Power Rail
P1	SMB_ALERT_1V8#	-	-	-			_	-
P2	GND	-	-	-	-	-	_	-
~~P3~~	~~CSI1_CK+~~	~~In~~	~~-~~	~~LVDS D-PHY~~		~~MIPI_CSI2_CLK_P~~	_	~~CSI_P2_VDDHA~~
~~P4~~	~~CSI1_CK-~~	~~In~~	~~-~~	~~LVDS D-PHY~~		~~MIPI_CSI2_CLK_N~~	_	~~CSI_P2_VDDHA~~
P5	GBE1_SDP	Out	-	GPIO/3.3V		SPD0		
P6	GBE0_SDP	Out	-	GPIO/3.3V		CLK_OUT		
P7	~~CSI1_RX0+~~	~~In~~	~~-~~	~~LVDS D-PHY~~		~~MIPI_CSI2_D0_P~~	_	~~CSI_P2_VDDHA~~
P8	~~CSI1_RX0-~~	~~In~~	~~-~~	~~LVDS D-PHY~~		~~MIPI_CSI2_D0_N~~	_	~~CSI_P2_VDDHA~~
P9	GND	-	-	-	-	-		
P10	~~CSI1_RX1+~~	~~In~~	~~-~~	~~LVDS D-PHY~~		~~MIPI_CSI2_D1_P~~	_	~~CSI_P2_VDDHA~~
P11	~~CSI1_RX1-~~	~~In~~	~~-~~	~~LVDS D-PHY~~		~~MIPI_CSI2_D1_N~~	_	~~CSI_P2_VDDHA~~
P12	GND	-	-	-	-	-		
P13	~~CSI1_RX2+~~	~~In~~	~~-~~	~~LVDS D-PHY~~		~~MIPI_CSI2_D2_P~~	_	~~CSI_P2_VDDHA~~
P14	~~CSI1_RX2-~~	~~In~~	~~-~~	~~LVDS D-PHY~~		~~MIPI_CSI2_D2_N~~	_	~~CSI_P2_VDDHA~~
P15	GND	-	-	-	-	-		
P16	~~CSI1_RX3+~~	~~In~~	~~-~~	~~LVDS D-PHY~~		~~MIPI_CSI2_D3_P~~	_	~~CSI_P2_VDDHA~~
P17	~~CSI1_RX3-~~	~~In~~	~~-~~	~~LVDS D-PHY~~		~~MIPI_CSI2_D3_N~~	_	~~CSI_P2_VDDHA~~
P18	GND	-	-	-	-	-	_	-
P19	GBE0_MDI3-	Bi-Dir	-	GBE MDI	GPY	TD_M_D	_	VDDIO
P20	GBE0_MDI3+	Bi-Dir	-	GBE MDI	GPY	TD_P_D	_	VDDIO
P21	GBE0_LINK100#	Out/OD	-	GPIO / 3.3V	GPY	LED_1	_	VDDIO
P22	GBE0_LINK1000#	Out/OD	-	GPIO / 3.3V	GPY	LED_2	_	VDDIO
P23	GBE0_MDI2-	Bi-Dir	-	GBE MDI	GPY	TD_M_C	_	VDDIO
P24	GBE0_MDI2+	Bi-Dir	-	GBE MDI	GPY	TD_P_C	_	VDDIO
P25	GBE0_LINK_ACT#	Out/OD	-	GPIO / 3.3V	GPY	LED_0	_	VDDIO
P26	GBE0_MDI1-	Bi-Dir	-	GBE MDI	GPY	TD_M_B	_	VDDIO
P27	GBE0_MDI1+	Bi-Dir	-	GBE MDI	GPY	TD_P_B	_	VDDIO
P28	GBE0_CTREF	PWR	-	-	-	-	_	-

Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	I/O Mux default	Power Rail
P29	GBE0_MDI0-	Bi-Dir	-	GBE MDI	GPY	TD_M_A	_	VDDIO
P30	GBE0_MDI0+	Bi-Dir	-	GBE MDI	GPY	TD_P_A	_	VDDIO
P31	SPI0_CS1#	-	-	-	N.C.	N.C.	_	-
P32	GND	-	-	-	-	-	_	-
P33	SDIO_WP	In	-	SD2 / 3.3V	EL x6000	SD2_WP	ALT0	NVCC_SD2
P34	SDIO_CMD	Bi-Dir	-	SD2 / 3.3V	EL x6000	SD2_CMD	ALT0	NVCC_SD2
P35	SDIO_CD#	In	-	SD2 / 3.3V	EL x6000	SD2_CD	ALT0	NVCC_SD2
P36	SDIO_CK	Out	-	SD2 / 3.3V	EL x6000	SD2_CLK	ALT0	NVCC_SD2
P37	SDIO_PWR_EN	Out	-	GPIO / 3.3V	EL x6000	GPIO1_IO12	ALT0	NVCC_GPIO1
P38	GND	-	-	-	-	-		
P39	SDIO_D0	Bi-Dir	-	SD2 / 3.3V	EL x6000	SD2_DATA0	ALT0	NVCC_SD2
P40	SDIO_D1	Bi-Dir	-	SD2 / 3.3V	EL x6000	SD2_DATA1	ALT0	NVCC_SD2
P41	SDIO_D2	Bi-Dir	-	SD2 / 3.3V	EL x6000	SD2_DATA2	ALT0	NVCC_SD2
P42	SDIO_D3	Bi-Dir	-	SD2 / 3.3V	EL x6000	SD2_DATA3	ALT0	NVCC_SD2
P43	SPI0_CS0#	Out	-	SPI / 1.8V	EL x6000	ECSPI2_SS0	ALT0	NVCC_ECSPI
P44	SPI0_CK	Out	-	SPI / 1.8V	EL x6000	ECSPI2_SCLK	ALT0	NVCC_ECSPI
P45	SPI0_DIN	In	-	SPI / 1.8V	EL x6000	ECSPI2_MISO	ALT0	NVCC_ECSPI
P46	SPI0_DO	Out	-	SPI / 1.8V	EL x6000	ECSPI2_MOSI	ALT0	NVCC_ECSPI
P47	GND	-	-	-	-	-	_	-
P48	SATA_TX+	out	-	-	EL x6000	N.C.	_	-
P49	SATA_TX-	out	-	-	EL x6000	N.C.	_	-
P50	GND	-	-	-	-	-	_	-
P51	SATA_RX+	In	-	-	EL x6000	N.C.	_	-
P52	SATA_RX-	In	-	-	EL x6000	N.C.	_	-
P53	GND	-	-	-	-	-	_	-
P54	ESPI_CS0# / SPI1_CS0#	Out	-	SPI / 1.8V	EL x6000	ECSPI1_SS0	ALT0	NVCC_ECSPI
P55	ESPI_CS1# / SPI1_CS1#	-	-	-	EL x6000	N.C.	_	-
P56	ESPI_CK / SPI1_CK	Out	-	SPI / 1.8V	EL x6000	ECSPI1_SCLK	ALT0	NVCC_ECSPI
P57	ESPI_IO_1 / SPI1_DIN	In	-	SPI / 1.8V	EL x6000	ECSPI1_MISO	ALT0	NVCC_ECSPI
P58	ESPI_IO_0 / SPI1_DO	Out	-	SPI / 1.8V	EL x6000	ECSPI1_MOSI	ALT0	NVCC_ECSPI

Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	I/O Mux default	Power Rail
P59	GND	-	-	-	-	-		
P60	USB0+	Bi-Dir	-	USB	EL x6000	USB1_DP		USB1_VDD33
P61	USB0-	Bi-Dir	-	USB	EL x6000	USB1_DN		USB1_VDD33
P62	USB0_EN_OC#	In	PU-10K	GPIO / 3.3V	EL x6000	GPIO1_IO13	ALT0	NVCC_GPIO1
~~P63~~	~~USB0_VBUS_DET~~	~~PWR~~	~~-~~	~~USB~~	~~EL x6000~~	~~USB1_VBUS~~	~~-~~	~~USB1_VDD33~~
~~P64~~	~~USB0_OTG_ID~~	~~In~~	~~-~~	~~USB~~	~~EL x6000~~	~~USB1_ID~~	~~-~~	~~USB1_VDD33~~
P65	USB1+	Bi-Dir	-	USB	EL x6000	DS3_DP	-	AVDD33
P66	USB1-	Bi-Dir	-	USB	EL x6000	DS3_DM	-	AVDD33
P67	USB1_EN_OC#	In	-	GPIO / 3.3V	EL x6000	DS3_OVRCURR	-	AVDD33
P68	GND	-	-	-	-	-		
P69	USB2+	Bi-Dir	-	PHY	EL x6000	DS2_DP	-	AVDD33
P70	USB2-	Bi-Dir	-	PHY	EL x6000	DS2_DM	-	AVDD33
P71	USB2_EN_OC#	In	-	GPIO / 3.3V	EL x6000	DS2_OVRCURR	-	AVDD33
P72	RSVD	-	-	-	N.C.	N.C.		
P73	RSVD	-	-	-	N.C.	N.C.		
P74	USB3_EN_OC#	In	-	GPIO / 3.3V	EL x6000	DS1_OVRCURR	-	AVDD33
P75	PCIE_A_RST#	Out	-	GPIO / 3.3V	EL x6000	SAI1_TXC	ALT5	NVCC_SAI1
P76	USB4_EN_OC#	In	-	GPIO / 3.3V	EL x6000	DS4_OVRCURR	-	AVDD33
P77	PCIE_B_CKREQ#	-	-	-	EL x6000	PCIE_B_CKREQ#	-	-
P78	PCIE_A_CKREQ#	-	-	-	EL x6000	PCIE_A_CKREQ#	-	-
P79	GND	-	-	-	-	-	-	-
P80	PCIE_C_REFCK+	Out	-	-	EL x6000	N.C.	-	-
P81	PCIE_C_REFCK-	Out	-	-	EL x6000	N.C.	-	-
P82	GND	-	-	-	-	-	-	-
P83	PCIE_A_REFCK+	Out	Serial-0.1uF	PCIe	EL x6000	DIF3	-	VDDDIG1p8
P84	PCIE_A_REFCK-	Out	Serial-0.1uF	PCIe	EL x6000	DIF3\	-	VDDDIG1p8
P85	GND	-	-		-	-	-	-
P86	PCIE_A_RX+	In	Serial-0.1uF	PCIe	EL x6000	PCIE2_RXN_P	-	PCIE2_VPH
P87	PCIE_A_RX-	In	Serial-0.1uF	PCIe	EL x6000	PCIE2_RXN_N	-	PCIE2_VPH

Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	I/O Mux default	Power Rail
P88	GND	-	-	-	-	-	_	-
P89	PCIE_A_TX+	Out	Serial-0.1uF	PCIe	EL x6000	PCIE2_TXN_P	_	PCIE2_VPH
P90	PCIE_A_TX-	Out	Serial-0.1uF	PCIe	EL x6000	PCIE2_TXN_N	_	PCIE2_VPH
P91	GND	-	-	-	-	-		
P92	HDMI_D2+ / DP1_LANE0+	Out	-	HDMI	EL x6000	HDMI_TX_P_LN_2	_	HDMI_AVDDIO
P93	HDMI_D2- / DP1_LANE0-	Out	-	HDMI	EL x6000	HDMI_TX_N_LN_2	_	HDMI_AVDDIO
P94	GND	-	-	-	-	-	_	-
P95	HDMI_D1+ / DP1_LANE1+	Out	-	HDMI	EL x6000	HDMI_TX_P_LN_1		HDMI_AVDDIO
P96	HDMI_D1- / DP1_LANE1-	Out	-	HDMI	EL x6000	HDMI_TX_N_LN_1		HDMI_AVDDIO
P97	GND	-	-	-	-	-	_	-
P98	HDMI_D0+ / DP1_LANE2+	Out	-	HDMI	EL x6000	HDMI_TX_P_LN_0	_	HDMI_AVDDIO
P99	HDMI_D0- / DP1_LANE2-	Out	-	HDMI	EL x6000	HDMI_TX_N_LN_0	_	HDMI_AVDDIO
P100	GND	-	-	-	-	-	_	-
P101	HDMI_CK+ / DP1_LANE3+	Out	-	HDMI	EL x6000	HDMI_TX_P_LN_3	_	HDMI_AVDDIO
P102	HDMI_CK- / DP1_LANE3-	Out	-	HDMI	EL x6000	HDMI_TX_N_LN_3	`	HDMI_AVDDIO
P103	GND	-	-	-	-	-	_	-
P104	HDMI_HPD / DP1_HPD	In		HDMI	EL x6000	HDMI_HPD	_	HDMI_AVDDIO
P105	HDMI_CTRL_CK / DP1_AUX+	Out	PU-2.2K / PD-100K	HDMI	EL x6000	HDMI_DDC_SCL(H) HDMI_AUXP(L)	-	HDMI_AVDDIO
P106	HDMI_CTRL_DAT / DP1_AUX-	Bi-Dir	PU-2.2K / PD-100K	HDMI	EL x6000	HDMI_DDC_SDA(H) HDMI_AUXN(L)	-	HDMI_AVDDIO
P107	DP1_AUX_SEL	Out	PD-1M	HDMI	EL x6000	-	_	-
P108	GPIO0 / ~~CAM0_PWR#~~	Out	PU-470K	GPIO / 1.8V	EL x6000	GPIO1_IO03	ALT0	NVCC_GPIO1
P109	GPIO1 / ~~CAM1_PWR#~~	Out	PU-470K	GPIO / 1.8V	EL x6000	GPIO1_IO05	ALT0	NVCC_GPIO1
P110	GPIO2 / ~~CAM0_RST#~~	Out	PU-470K	GPIO / 1.8V	EL x6000	GPIO1_IO06	ALT0	NVCC_GPIO1
P111	GPIO3 / ~~CAM1_RST#~~	Out	PU-470K	GPIO / 1.8V	EL x6000	GPIO1_IO06	ALT0	NVCC_GPIO1
P112	~~GPIO4~~ / HDA_RST#	Out	PU-470K	GPIO / 1.8V	SX1509	P0_4	_	VDD_1V8
P113	GPIO5 / ~~PWM_OUT~~	Out	PU-470K	GPIO / 1.8V	SX1509	P0_5	_	VDD_1V8
P114	GPIO6 / ~~TACHIN~~	In	PU-470K	GPIO / 1.8V	SX1509	P0_6	_	VDD_1V8

Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	I/O Mux default	Power Rail
P115	GPIO7	In	PU-470K	GPIO / 1.8V	SX1509	P0_7	_	VDD_1V8
P116	GPIO8	In	PU-470K	GPIO / 1.8V	SX1509	P1_0	_	VDD_1V8
P117	GPIO9	In	PU-470K	GPIO / 1.8V	SX1509	P1_1	_	VDD_1V8
P118	GPIO10	In	PU-470K	GPIO / 1.8V	SX1509	P1_2	_	VDD_1V8
P119	GPIO11	In	PU-470K	GPIO / 1.8V	SX1509	P1_3	_	VDD_1V8
P120	GND	-	-	-	-	-		
P121	I2C_PM_CK	Out	PU-2k2	I2C2	EL x6000	I2C2_SCL	ALT0	NVCC_I2C
P122	I2C_PM_DAT	Bi-Dir	PU-2k2	I2C2	EL x6000	I2C2_SDA	ALT0	NVCC_I2C
P123	BOOT_SEL0#	In	PU-4k7	GPIO / 1.8V	BMC	PB0	_	+1V8SMC
P124	BOOT_SEL1#	In	PU-4k7	GPIO / 1.8V	BMC	PB1	_	+1V8SMC
P125	BOOT_SEL2#	In	PU-4k7	GPIO / 1.8V	BMC	PB2	_	+1V8SMC
P126	RESET_OUT#	Out	-	GPIO / 1.8V	BMC	PB15	_	+1V8SMC
P127	RESET_IN#	In	PU-4K7	GPIO / 1.8V	BMC	PB14	_	+1V8SMC
P128	POWER_BTN#	In	PU-4K7	GPIO / 1.8V	BMC	PB4	_	+1V8SMC
P129	SER0_TX	Out	-	UART / 1.8V	EL x6000	UART2_TXD	ALT0	NVCC_UART
P130	SER0_RX	In	-	UART / 1.8V	EL x6000	UART2_RXD	ALT0	NVCC_UART
P131	SER0_RTS#	In	-	UART / 1.8V	EL x6000	UART4_TXD	ALT1	NVCC_UART
P132	SER0_CTS#	Out	-	UART / 1.8V	EL x6000	UART4_RXD	ALT1	NVCC_UART
P133	GND	-	-	-	-	-	_	-
P134	SER1_TX	Out	-	UART / 1.8V	EL x6000	UART1_TXD	ALT0	NVCC_UART
P135	SER1_RX	In	-	UART / 1.8V	EL x6000	UART1_RXD	ALT0	NVCC_UART
P136	SER2_TX	-	-	-	N.C.	N.C.	_	-
P137	SER2_RX	-	-	-	N.C.	N.C.	_	-
P138	SER2_RTS#	-	-	-	N.C.	N.C.	_	-
P139	SER2_CTS#	-	-	-	N.C.	N.C.	_	-
P140	SER3_TX	Out	-	UART / 1.8V	EL x6000	UART3_TXD	ALT0	NVCC_UART
P141	SER3_RX	In	-	UART / 1.8V	EL x6000	UART3_RXD	ALT0	NVCC_UART
P142	GND	-	-	-	-	-	_	-
P143	CAN0_TX	Out	-	CAN	EL x6000	TXCAN	_	VDD_1V8
P144	CAN0_RX	In	-	CAN	EL x6000	RXCAN	_	VDD_1V8

Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	I/O Mux default	Power Rail
P145	CAN1_TX	-	-	-	EL x6000	TXCAN		
P146	CAN1_RX	-	-	-	EL x6000	RXCAN		
P147	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V
P148	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V
P149	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V
P150	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V
P151	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V
P152	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V
P153	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V
P154	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V
P155	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V
P156	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V

Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	I/O Mux default	Power Rail
~~S1~~	~~CSI1_TX+ / I2C_CAM1_CK~~	~~In~~	~~PU-2k2~~	~~I2C3~~	~~EL x6000~~	~~I2C3_SCL~~	~~ALT0~~	~~NVCC_I2C~~
~~S2~~	~~CSI1_TX- / I2C_CAM1_DAT~~	~~In~~	~~PU-2k2~~	~~I2C3~~	~~EL x6000~~	~~I2C3_SDA~~	~~ALT0~~	~~NVCC_I2C~~
S3	GND	-	-	-	-	-	_	-
~~S4~~	~~RSVD~~	~~In~~	~~-~~	~~-~~	~~N.C.~~	~~N.C.~~	~~_~~	~~-~~
~~S5~~	~~CSI0_TX- / I2C_CAM0_CK~~	~~Out~~	~~PU-2k2~~	~~I2C4~~	~~EL x6000~~	~~I2C4_SCL~~	~~ALT0~~	~~NVCC_I2C~~
~~S6~~	~~CAM_MCK~~	~~Out~~	~~-~~	~~GPIO / 1.8V~~	~~EL x6000~~	~~GPIO1_IO15~~	~~ALT5~~	~~NVCC_GPIO1~~
~~S7~~	~~CSI0_TX+ / I2C_CAM0_DAT~~	~~Bi-Dir~~	~~PU-2k2~~	~~I2C4~~	~~EL x6000~~	~~I2C4_SDA~~	~~ALT0~~	~~NVCC_I2C~~
~~S8~~	~~CSI0_CK+~~	~~In~~	~~-~~	~~MIPI-CSI~~	~~EL x6000~~	~~MIPI_CSI1_CLK_P~~	~~_~~	~~MIPI_CSI1_VDDHA~~
~~S9~~	~~CSI0_CK-~~	~~In~~	~~-~~	~~MIPI-CSI~~	~~EL x6000~~	~~MIPI_CSI1_CLK_N~~	~~_~~	~~MIPI_CSI1_VDDHA~~
S10	GND	-	-	-	-	-	_	-
~~S11~~	~~CSI0_RX0+~~	~~In~~	~~-~~	~~MIPI-CSI~~	~~EL x6000~~	~~MIPI_CSI1_D0_P~~	~~_~~	~~MIPI_CSI1_VDDHA~~
~~S12~~	~~CSI0_RX0-~~	~~In~~	~~-~~	~~MIPI-CSI~~	~~EL x6000~~	~~MIPI_CSI1_D0_N~~	~~_~~	~~MIPI_CSI1_VDDHA~~
S13	GND	-	-	-	-	-	_	-
~~S14~~	~~CSI0_RX1+~~	~~In~~	~~-~~	~~MIPI-CSI~~	~~EL x6000~~	~~MIPI_CSI1_D1_P~~	~~_~~	~~MIPI_CSI1_VDDHA~~
~~S15~~	~~CSI0_RX1-~~	~~In~~	~~-~~	~~MIPI-CSI~~	~~EL x6000~~	~~MIPI_CSI1_D1_N~~	~~_~~	~~MIPI_CSI1_VDDHA~~

Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	I/O Mux default	Power Rail
S16	GND	-	-	-	-	-	_	-
S17	GBE1_MDI0+	Bi-Dir	-	GBE MDI	GPY	MDI_PLUS[0]	_	-
S18	GBE1_MDI0-	Bi-Dir	-	GBE MDI	GPY	MDI_MINUS[0]	_	-
S19	GBE1_LINK100#	Out	-	GPIO / 3.3V	GPY	LED0	_	-
S20	GBE1_MDI1+	Bi-Dir	-	GBE MDI	GPY	MDI_PLUS[1]	_	-
S21	GBE1_MDI1-	Bi-Dir	-	GBE MDI	GPY	MDI_MINUS[1]	_	-
S22	GBE1_LINK1000#	Out	-	GPIO / 3.3V	GPY	LED2	_	-
S23	GBE1_MDI2+	Bi-Dir	-	GBE MDI	GPY	MDI_PLUS[2]	_	-
S24	GBE1_MDI2-	Bi-Dir	-	GBE MDI	GPY	MDI_MINUS[2]	_	-
S25	GND	-	-	-	-	-	_	-
S26	GBE1_MDI3+	Bi-Dir	-	GBE MDI	GPY	MDI_PLUS[3]	_	-
S27	GBE1_MDI3-	Bi-Dir	-	GBE MDI	GPY	MDI_MINUS[3]	_	-
S28	GBE1_CTREF	-	-	-	N.C.	N.C.	_	-
S29	PCIE_D_TX+ / SERDES_1_TX+	-	-	-	PCIE_D	PCIE_D	_	-
S30	PCIE_D_TX- / SERDES_1_TX-	-	-	-	PCIE_D	PCIE_D	_	-
S31	GBE1_LINK_ACT#	Out	-	GPIO / 3.3V	GPY	LED1	_	-
S32	PCIE_D_RX+ / SERDES_1_RX+	-	-	-	PCIE_D	PCIE_D	_	-
S33	PCIE_D_RX- / SERDES_1_RX-	-	-	-	PCIE_D	PCIE_D	_	-
S34	GND	-	-	-	-	-		
S35	USB4+	Bi-Dir	-	USB	EL x6000	DS4_DP	_	-
S36	USB4-	Bi-Dir	-	USB	EL x6000	DS4_DM	_	-
S37	USB3_VBUS_DET	-	-	-	N.C.	N.C.	_	-
S38	AUDIO_MCK	Out	-	SAI / 1.8V	EL x6000	SAI2_MCLK	ALT0	NVCC_SAI2
S39	I2S0_LRCK	Bi-Dir	-	SAI / 1.8V	EL x6000	SAI2_TXFS	ALT0	NVCC_SAI2
S40	I2S0_SDOUT	Out	-	SAI / 1.8V	EL x6000	SAI2_TXD0	ALT0	NVCC_SAI2
S41	I2S0_SDIN	In	-	SAI / 1.8V	EL x6000	SAI2_RXD0	ALT0	NVCC_SAI2
S42	I2S0_CK	Bi-Dir	-	SAI / 1.8V	EL x6000	SAI2_TXC	ALT0	NVCC_SAI2
S43	ESPI_ALERT0#	In	-	SAI / 1.8V	EL x6000	SAI1_RXFS	ALT5	NVCC_SAI1
S44	ESPI_ALERT1#	-	-	-	N.C.	N.C.		

Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	I/O Mux default	Power Rail
~~S45~~	~~MDIO_CLK~~	~~-~~	~~-~~	~~-~~	~~N.C.~~	~~N.C.~~		
~~S46~~	~~MDIO_DAT~~	~~-~~	~~-~~	~~-~~	~~N.C.~~	~~N.C.~~		
S47	GND	-	-	-	-	-		
S48	I2C_GP_CK	Out	PU-2.2K	I2C3	EL x6000	I2C3_SCL	ALT0	NVCC_I2C
S49	I2C_GP_DAT	Bi-Dir	PU-2.2K	I2C3	EL x6000	I2C3_SDA	ALT0	NVCC_I2C
S50	HDA_SYNC / I2S2_LRCK	-	-	SAI / 1.8V	EL x6000	SAI3_TXFS	ALT0	NVCC_SAI3
S51	HDA_SDO / I2S2_SDOUT	-	-	SAI / 1.8V	EL x6000	SAI3_TXD	ALT0	NVCC_SAI3
S52	HDA_SDI / I2S2_SDIN	-	-	SAI / 1.8V	EL x6000	SAI3_RXD	ALT0	NVCC_SAI3
S53	HDA_CK / I2S2_CK	-	-	SAI / 1.8V	EL x6000	SAI3_TXC	ALT0	NVCC_SAI3
S54	SATA_ACT#	-	-	-	EL x6000	N.C.	_	-
S55	USB5_EN_OC#	-	-	-	EL x6000	N.C.	_	-
S56	ESPI_IO_2	-	-	-	N.C.	N.C.	_	-
S57	ESPI_IO_3	-	-	-	N.C.	N.C.	_	-
S58	ESPI_RESET#	Out	-	GPIO / 1.8V	BMC	PB15	_	+1V8SMC
S59	USB5+	-	-	-	N.C.	N.C.	_	-
S60	USB5-	-	-	-	N.C.	N.C.	_	-
S61	GND	-	-	-	-	-	_	-
S62	USB3_SSTX+	Out	Serial-0.1uF	USB	EL x6000	DS1_TXP	_	-
S63	USB3_SSTX-	Out	Serial-0.1uF	USB	EL x6000	DS1_TXM	_	-
S64	GND	-	-	-	-	-	_	-
S65	USB3_SSRX+	In	-	USB	EL x6000	DS1_RXP	_	-
S66	USB3_SSRX-	In	-	USB	EL x6000	DS1_RXM	_	-
S67	GND	-	-	-	-	-	_	-
S68	USB3+	Bi-Dir	-	USB	EL x6000	DS1_DP	_	-
S69	USB3-	Bi-Dir	-	USB	EL x6000	DS1_DM	_	-
S70	GND	-	-	-	-	-	_	-
S71	USB2_SSTX+	Out	Serial-0.1uF	USB	EL x6000	DS2_TXP	_	-
S72	USB2_SSTX-	Out	Serial-0.1uF	USB	EL x6000	DS2_TXM	_	-
S73	GND	-	-	-	-	-	_	-

Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	I/O Mux default	Power Rail
S74	USB2_SSRX+	In	-	USB	EL x6000	DS2_RXP	_	-
S75	USB2_SSRX-	In	-	USB	EL x6000	DS2_RXM	_	-
S76	PCIE_B_RST#	Out	-	GPIO / 3.3V	EL x6000	NAND_ALE	ALT5	NVCC_NAND
S77	PCIE_C_RST#	-	-	-	EL x6000	N.C.	_	-
S78	PCIE_C_RX+ / SERDES_2_RX+	-	-	-	EL x6000	N.C.	_	-
S79	PCIE_C_RX- / SERDES_2_RX-	-	-	-	EL x6000	N.C.	_	-
S80	GND	-	-	-	-	-	_	-
S81	PCIE_C_TX+ / SERDES_2_TX+	-	-	-	EL x6000	N.C.	_	-
S82	PCIE_C_TX- / SERDES_2_TX-	-	-	-	EL x6000	N.C.	_	-
S83	GND	-	-	-	-	-	_	-
S84	PCIE_B_REFCK+	Out	Serial-0.1uF	PCIe	EL x6000	DIF1	_	VDDDIG1p8
S85	PCIE_B_REFCK-	Out	Serial-0.1uF	PCIe	EL x6000	DIF1\	_	VDDDIG1p8
S86	GND	-	-	-	-	-	_	-
S87	PCIE_B_RX+	In	Serial-0.1uF	PCIe	EL x6000	PCIE1_RXN_P	_	PCIE1_VPH
S88	PCIE_B_RX-	In	Serial-0.1uF	PCIe	EL x6000	PCIE1_RXN_N	_	PCIE1_VPH
S89	GND	-	-	-	-	-	_	-
S90	PCIE_B_TX+	Out	Serial-0.1uF	PCIe	EL x6000	PCIE1_TXN_P	_	PCIE1_VPH
S91	PCIE_B_TX-	Out	Serial-0.1uF	PCIe	EL x6000	PCIE1_TXN_N	_	PCIE1_VPH
S92	GND	-	-	-	-	-	_	-
S93	DP0_LANE0+	-	-	-	DDI1	DDI1	_	-
S94	DP0_LANE0-	-	-	-	DDI1	DDI1	_	-
S95	DP0_AUX_SEL	-	-	-	DDI1	DDI1	_	-
S96	DP0_LANE1+	-	-	-	DDI1	DDI1	_	-
S97	DP0_LANE1-	-	-	-	DDI1	DDI1	_	-
S98	DP0_HPD	-	-	-	DDI1	DDI1	_	-
S99	DP0_LANE2+	-	-	-	DDI1	DDI1	_	-
S100	DP0_LANE2-	-	-	-	-	-	_	-
S101	GND	-	-	-	-	-	_	-
S102	DP0_LANE3+	-	-	-	N.C.	N.C.	_	-
S103	DP0_LANE3-	-	-	-	N.C.	N.C.	_	-

Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	I/O Mux default	Power Rail
~~S104~~	~~USB3_OTG_ID~~	~~-~~	~~-~~	~~-~~	~~N.C.~~	~~N.C.~~	~~-~~	~~-~~
S105	DP0_AUX+	-	-	-	N.C.	N.C.	-	-
S106	DP0_AUX-	-	-	-	N.C.	N.C.	-	-
~~S107~~	~~LCD1_BKLT_EN~~	~~-~~	~~-~~	~~-~~	~~N.C.~~	~~N.C.~~	~~-~~	~~-~~
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	Out	Serial-0R	LVDS	PTN3460	B_CLKP	-	-
S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	Out	Serial-0R	LVDS	PTN3460	B_CLKN	-	-
S110	GND	-	-	-			-	-
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	Out	Serial-0R	LVDS	PTN3460	B_Y0P	-	-
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	Out	Serial-0R	LVDS	PTN3460	B_Y0N	-	-
~~S113~~	~~eDP1_HPD / DSI1_TE~~	~~-~~	~~-~~	~~-~~	~~N.C.~~	~~N.C.~~	~~-~~	~~-~~
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	Out	Serial-0R	LVDS	PTN3460	B_Y1P	-	-
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	Out	Serial-0R	LVDS	PTN3460	B_Y1N	-	-
~~S116~~	~~LCD1_VDD_EN~~	~~-~~	~~-~~	~~-~~	~~N.C.~~	~~N.C.~~	~~-~~	~~-~~
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	Out	Serial-0R	LVDS	PTN3460	B_Y2P	-	-
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	Out	Serial-0R	LVDS	PTN3460	B_Y2N	-	-
S119	GND	-	-	-	-	-	-	-
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	Out	Serial-0R	LVDS	PTN3460	B_Y3P	-	-
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	Out	Serial-0R	LVDS	PTN3460	B_Y3N	-	-
~~S122~~	~~LCD1_BKLT_PWM~~	~~-~~	~~-~~	~~-~~	~~N.C.~~	~~N.C.~~	~~-~~	~~-~~
S123	GPIO13	-	-	-	N.C.	N.C.	-	-
S124	GND	-	-	-	-	-	-	-
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	Out	Serial-0R	LVDS	PTN3460	A_Y0P	-	-

Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	I/O Mux default	Power Rail
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	Out	Serial-0R	LVDS	PTN3460	A_Y0N	-	-
S127	LCD0_BKLT_EN	Out	-	GPIO / 1.8V	EL x6000	GPIO1_IO00	-	-
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	Out	Serial-0R	LVDS	PTN3460	A_Y1P	-	-
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	Out	Serial-0R	LVDS	PTN3460	A_Y1N	-	-
S130	GND	-	-	-	-	-	-	-
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	Out	Serial-0R	LVDS	PTN3460	A_Y2P	-	-
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	Out	Serial-0R	LVDS	PTN3460	A_Y2N	-	-
S133	LCD0_VDD_EN	Out	-	GPIO/1.8V	EL x6000	GPIO1_IO04	-	-
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	Out	Serial-0R	LVDS	PTN3460	A_CLKP	-	-
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	Out	Serial-0R	LVDS	PTN3460	A_CLKN	-	-
S136	GND	-	-	-	-	-	-	-
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	Out	Serial-0R	LVDS	PTN3460	A_Y3P	-	-
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	Out	Serial-0R	LVDS	PTN3460	A_Y3N	-	-
S139	I2C_LCD_CK	Out	PU-2.2K	I2C4	EL x6000	I2C4_SCL	ALT0	NVCC_I2C
S140	I2C_LCD_DAT	Bi-Dir	PU-2.2K	I2C4	EL x6000	I2C4_SCL	ALT0	NVCC_I2C
S141	LCD0_BKLT_PWM	Out	-	GPIO / 1.8V	EL x6000	GPIO1_IO01	ALT1	NVCC_GPIO1
S142	GPIO12	In	PU-10K	GPIO / 1.8V	BMC	PC14	-	-
S143	GND	-	-	-	-	-	-	-
S144	eDP0_HPD / DSI0_TE	-	-	-	N.C.	N.C.	-	-
S145	WDT_TIME_OUT#	Out	-	GPIO / 1.8V	BMC	PD2	-	+1V8SMC
S146	PCIE_WAKE#	In	-	GPIO / 3.3V	EL x6000	SAI1_TXFS	ALT5	NVCC_SAI1
S147	VDD_RTC	PWR	-	PWR	-	-	-	-
S148	LID#	In	PU-4.7K	GPIO / 1.8V	EL x6000	SAI5_MCLK	ALT5	NVCC_SAI5

Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	I/O Mux default	Power Rail
S149	SLEEP#	In	PU-4.7K	GPIO / 1.8V	EL x6000	SAI5_RXFS	ALT5	NVCC_SAI5
S150	VIN_PWR_BAD#	In	PU-10K	GPIO / 1.8V	BMC	PB7	-	+1V8SMC
S151	CHARGING#	Out	PU-68K	GPIO / 1.8V	EL x6000	SAI5_RXC	ALT5	NVCC_SAI5
S152	CHARGER_PRSNT#	Out	PU-100K	GPIO / 1.8V	EL x6000	SAI5_RXD0	ALT5	NVCC_SAI5
S153	CARRIER_STBY#	Out	-	GPIO / 1.8V	BMC	PB5	-	+1V8SMC

5. Additional Features

This chapter describes connectors, LEDs, switches and additional items located on the module and not necessarily included in the PICMG standard specification. The locations of these items are as below:

5.1 Module Feature Locations

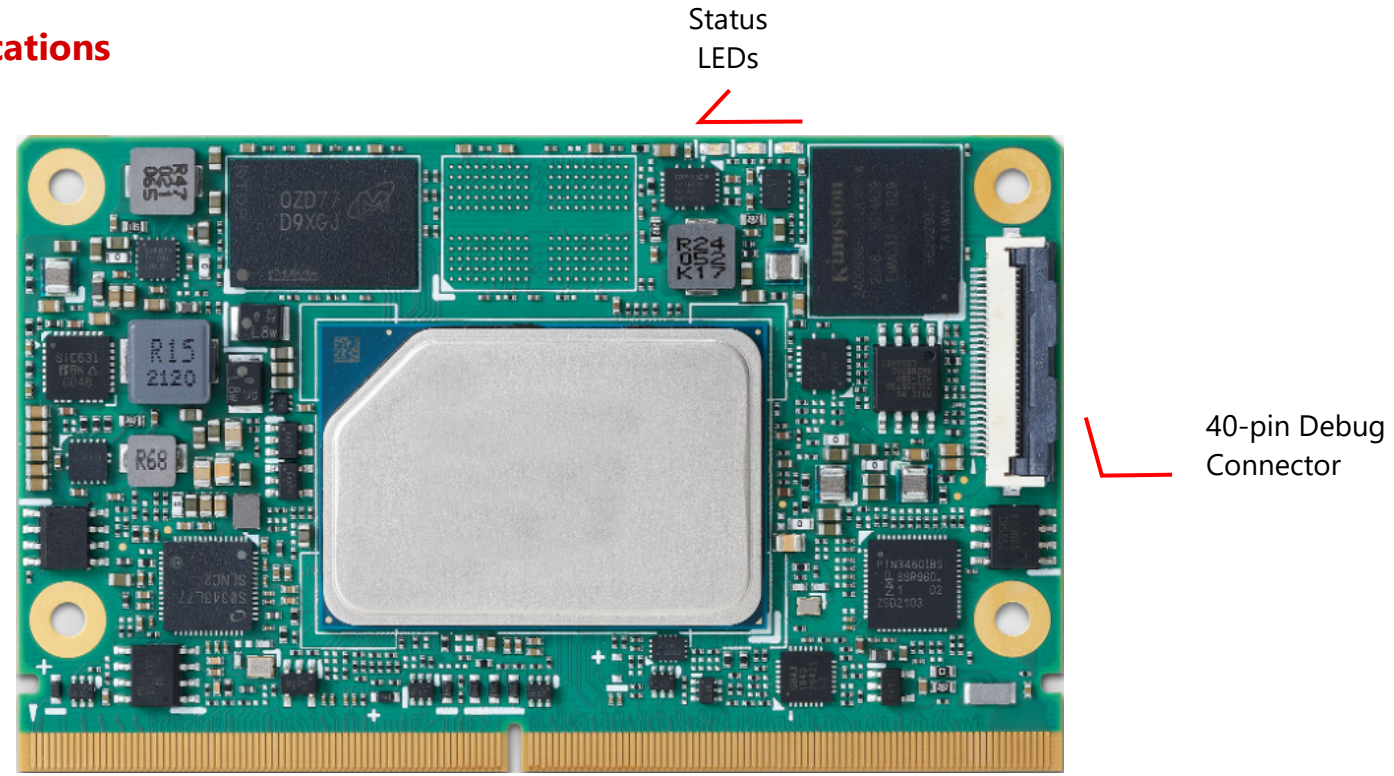
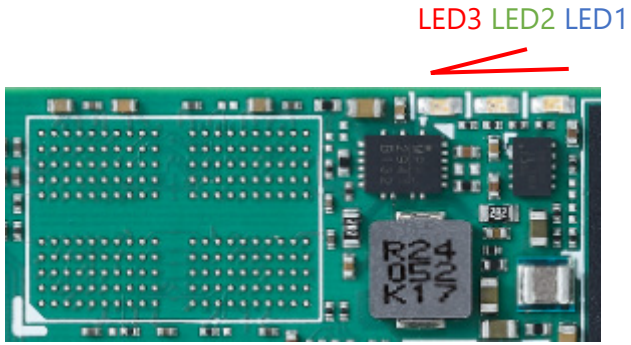


Figure 3 – Module feature locations (top side)

5.2 Status LEDs

Status LED's are mounted on the module to facilitate easier maintenance.



Name	Color	Connection	Function
LED1	Blue	BMC/EC output	Power Sequence Status Code (BMC) Power Changes, RESET (see Exception Codes below)
LED2	Green	Power Source	S0 LED ON S3/S4/S5 LED OFF ECO mode LED OFF
LED3	Red	Watchdog (WD)	Module power up WD LED = LED OFF Watchdog counting WD LED = Keep Last State Watchdog timed out WD LED = LED ON Watchdog RESET WD LED = LED ON Rebooted after WD RESET WD LED = LED ON Rebooted after PWRBTN WD LED = LED OFF Rebooted after RESET BTN WD LED = LED OFF Note: only a RESET not initiated by the BMC can clear the WD LED (user action)

5.2.1 Exception Codes

Exception Code	Error Message
0	NOERROR
3	NO_SLP_S5
4	NO_SLP_S4
5	NO_SLP_S3
6	BIOS_FAIL
8	RESETIN_FAIL
9	NO_CB_PWROK
10	CRITICAL_TEMP
11	POWER_FAIL
12	VOLTAGE_FAIL
13	RSMRST_FAIL
14	NO_VDDQ_PG
16	NO_VCORE_PG
17	NO_SYS_GD
19	NO_V3P3A
21	NO_PWRSRC_GD

6. System Resources

6.1 System Memory Map

Memory Range	Target	Dependency / Comments
000E 0000h-000E FFFFh	SPI	Bit6 in BIOS Decode Enable register is set
0000F 0000h-0000F FFFFh	SPI	Bit7 in BIOS Decode Enable register is set
FECX X000h-FECX X040h	IO(x) APIC inside PCH	XX controlled via APIC Range Select(ASEL) field and APIC Enable IOAC.AE bit.
FEC1 0000h-FEC1 7FFFh	PCI Express* Port 1	PCI Express Root Port 1 I/OxAPIC Enable(PAE) set
FEC1 8000h-FEC1 FFFFh	PCI Express* Port 2	PCI Express Root Port 2 I/OxAPIC Enable(PAE) set
FEC2 0000h-FEC2 7FFFh	PCI Express* Port 3	PCI Express Root Port 3 I/OxAPIC Enable(PAE) set
FEC2 8000h-FEC2 FFFFh	PCI Express* Port 4	PCI Express Root Port 4 I/OxAPIC Enable(PAE) set
FEC3 8000h-FEC3 FFFFh	PCI Express* Port 5	PCI Express Root Port 5 I/OxAPIC Enable(PAE) set
FEC3 8000h-FEC3 FFFFh	PCI Express* Port 6	PCI Express Root Port 6 I/OxAPIC Enable(PAE) set
FEC4 0000h-FEC4 7FFFh	PCI Express* Port 7	PCI Express* Root Port 7 I/OxAPIC Enable(PAE) set
FEF0 0000h-FEFF FFFFh	SPI	uCode Patch Region Enable UCPR.UPRE is set
FEC0 0000h-FFC7 FFFFh FF80 0000h-FF87 FFFFh	SPI	Bit 8 in BIOS Decode Enable register is set
FFC8 0000h-FFCF FFFFh FF88 0000h-FF8F	SPI	Bit 9 in BIOS Decode Enable register is set
FED0 0000h-FFD7 FFFFh FF90 0000h-FF97 FFFFh	SPI	Bit 10 in BIOS Decode Enable register is set
FFD8 0000h-FFDF FFFFh FF98 0000h-FF9F FFFFh	SPI	Bit11 in BIOS Decode Enable register is set
FFE0 0000h-FFE7 FFFFh FFA0 0000h-FFA7 FFFFh	SPI	Bit 12 in BIOS Decode Enable register is set
FFE8 0000h-FFEF FFFFh FFA8 0000h-FFAF FFFFh	SPI	Bit 13 in BIOS Decode Enable register is set
FFF0 0000h-FFF7 FFFFh FFB0 0000h-FFB7 FFFFh	SPI	Bit 14 in BIOS Decode Enable register is set
FFFC 0000h-FFFFh	SPI	Always Enabled.
FFF8 0000h-FFFB FFFFh	SPI	Always enabled.

FFB8 0000h-FFBF FFFFh		
FF70 0000h-FF7F FFFFh FF30 0000h-FF3F FFFFh	SPI	Bit 3 in BIOS Decode Enable register is set
FF60 0000h-FF6F FFFFh FF20 0000h-FF2F FFFFh	SPI	Bit 2 in BIOS Decode Enable register is set
FF50 0000h-FF5F FFFFh FF10 0000h-FF1F FFFFh	SPI(	Bit 1 in BIOS Decode Enable register is set
FF40 0000h-FF4F FFFFh FF00 0000h-FF0F FFFFh	SPI	Bit 0 in BIOS Decode Enable register is set
FED0 X000h-FED0 X3FFh	HPET	BIOS determines "fixed" location which is one of four 1KB ranges where X(in the first column) is 0h,1h,2h,or 3h.
FED4 0000h-FED4 7FFFh	SPI or CSE(set by strap)	TPM nad Trusted Mobile KBC
FED4 C000h-FED4 FFFFh	PCH Internal(PSE Error Handler)	Always Enable
FED5 0000h-FED5 FFFFh	CSE	Always Enable
FED6 0000h-FED6 1FFFh	XHCI	NOT positively decoded in PCH(OPI/PSF)
FED7 0000h-FED7 4FFFh	Internal Device	Security feature related
64Kb(MBAR) anywhere in 64-bit address range	XHCI	Enable via standard PCI mechanism(D20:F0)
2MB(BAR)&4Kb(BAR1) anywhere in 64-bit address range	USB eXtensible Device Controller Interface(xDCI)	Enable via standard PCI mechanism(D20:F1)
16kB(HDAxBA),4kB(SPCxBA) &1MB(ADSPxBA) anywhere in 64-bit address range	Converged Audio, Video Speech(cAVS) Controller	Enable via standard PCI mechanism(D20:F3)
64 KB anywhere in 4 GB range	eSPI	LPC Generic Memory Range.Enable via setting bit[0] of the LPC Generic Memory Range Register(D31:F0:offset98h).
32B(SMBBAR) anywhere in 64-bit address range	SM Bus	Enable via standard PCI mechanism(D31:F4)
2 KB anywhere above 64 KB to 4 GB range	SATA Controller(AHCI)	Enable via standard PCI mechanism(D23:F0)
Memory Base/Limit anywhere in 4 GB range	PCI Express Root Ports1-7	Enable via standard PCI mechanism(D28:F[0:6])
Pre-fetchable Memory Base/Limit anywhere in 64-bit address range	PCI Express Root Ports1-7	Enable via standard PCI mechanism(D28:F[0:6])
16B(HECIx_MMIO_BAR) anywhere in 64-bit address range	HECI #0,#1,#2,#4	Enable via standard PCI mechanism(D22:F[0:1,4:5])

16 MB(SBREG_BAR) anywhere in 64-bit address range	P2SB	Enable via standard PCI mechanism(D31:F1)
4kB(BAR & BAR1) anywhere in 64-bit address range	Intel(R) Serial I/O Controllers	Enable via standard PCI mechanism(D30:F[0:3,D25:F[0:2],D21:F[0:3],D18:F0,D16:F[1:0])
4kB(BAR & BAR1) anywhere in 64-bit address range	Embedded Multi Media Card(eMMC) Controller	Enable via standard PCI mechanism(D26:F0)
4kB(BAR & BAR1) anywhere in 64-bit address range	Secure Digital (SD) & Secure Digital I/O Controller	Enable via standard PCI mechanism(D26:F1)
4kB(BAR & BAR1) anywhere in 64-bit address range	Universal Flash Storage(UFS) Controller	Enable via standard PCI mechanism(D18:F[5,7])

6.2 Fixed I/O Address Range Map

Hex Range	Device
020-021	Interrupt Controller
024-025	Interrupt Controller
028-029	Interrupt Controller
02C-02D	Interrupt Controller
02E-02F	Super I/O
030-031	
034-035	
038-039	Interrupt Controller
03C-03D	Interrupt Controller
040	Timer/Counter
042-043	Timer/Counter
04E-04F	Microcontroller
050	Timer/Counter
052-053	Timer/Counter
060	Keyboard Controller
061	NMI Controller
062	Microcontroller
063	NMI Controller
064	Keyboard Controller
065	NMI Controller
066	Microcontroller
067	NMI Controller

Hex Range	Device
070	RTC Controller
071	RTC Controller
072	RTC Controller
073	RTC Controller
074	RTC Controller
075	RTC Controller
076-077	RTC Controller
080	eSPI or PCIe
084-086	eSPI or PCIe
088	eSPI or PCIe
08C-08E	eSPI or PCIe
090	eSPI
092	Reset Generator
094-096	eSPI
098	eSPI
09C-09E	eSPI
0A0-0A1 0A4-0A5 0A8-0A9 0AC-0AD	Interrupt Controller
0B0-0B1	Interrupt Controller
0B2-0B3	Power Management
0B4-0B5 0B8-0B9 0BC-0BD	Interrupt Controller
200-207	Gameport Low
208-20F	Gameport High
4D0-4D1	Interrupt Controller
CF9	Reset Generator

6.3 Variable I/O Address Range Map

Hex Range	Device
Anywhere in 64 K I/O Space	ACPI
Anywhere in 64 K I/O Space	SMBus
Anywhere in 64 KB I/O Space	TCO
3 ranges in 64 KB I/O Space	Parallel Port
8 ranges in 64 KB I/O Space	Serial Port1
8 ranges in 64 KB I/O Space	Serial Port2
2 ranges in 64 KB I/O Space	Serial Port3
Anywhere in 64 K I/O Space	Floppy Disk Controller
Anywhere in 64 KB I/O Space	LPC Generic 1
Anywhere in 64 KB I/O Space	LPC Generic 2
Anywhere in 64 KB I/O Space	LPC Generic 3
Anywhere in 64 KB I/O Space	LPC Generic 4
Anywhere in 64 KB I/O Space	Serial ATA Index/Data Pair
Anywhere in 64 KB I/O Space	PCI Express Root Ports

6.4 PCI Configuration Space Map

Bus Number	Device Number	Function Number	Description
00h	31h	00h	Enhanced Serial Peripheral Interface(eSPI) Controller
00h	31h	01h	Primary to Sideband Bridge(P2SB)
00h	31h	02h	Power Management Controller(PMC)
00h	31h	03h	Converged Audio,Video,Speech(cAVS) Controller
00h	31h	04h	System Management Bus(SMBus) Controller
00h	31h	05h	Serial Peripheral Interface(SPI) Controller for Flash & TPM
00h	31h	07h	Intel(R) Trace Hub
00h	30h	00h	Intel(R) Serial I/O:Universal Asynchronous Receiver/Transmitter(UART) Controller #0
00h	30h	01h	Intel(R) Serial I/O:UART Controller #1
00h	30h	02h	Intel(R) Serial I/O:Serial Peripheral Interface(SPI) Controller #0
00h	30h	03h	Intel(R) Serial I/O:SPI Controller #1

Bus Number	Device Number	Function Number	Description
00h	30h	04h	Gigabit Ethernet TSN Controller
00h	30h	06h	High Precision Event Timer(HPET)
00h	30h	07h	I/O Advanced Programmable Interrupt Controller(IOAPIC)
00h	29h	00h	Intel(R) Programmable Services Engine(Intel(R) PSE):Local Host to PSE(LH2OSE) IPC
00h	29h	01h	Intel(R) Programmable Services Engine(Intel(R) PSE):Gigabit Ethernet TSN Controller #0(RGMII:1 Gb Mode)
00h	29h	01h	Intel(R) PSE:Gigabit Ethernet TSN Controller #0(SGMII:1 Gb Mode)
00h	29h	01h	Intel(R) PSE:Gigabit Ethernet TSN Controller #0(SGMII:2.5 Gb Mode)
00h	29h	02h	Intel(R) PSE:Gigabit Ethernet Time Sensitive Networking(TSN) Controller #1(RGMII:1 Gb Mode)
00h	29h	02h	Intel(R) PSE:Gigabit Ethernet TSN Controller #1(SGMII:1 Gb Mode)
00h	29h	02h	ntel(R) PSE:Gigabit Ethernet TSN Controller #1(SGMII:2.5 Gb Mode)
00h	29h	03h	Intel(R) PSE:Direct Memory Access (DMA) Controller #0
00h	29h	04h	Intel(R) PSE:DMA Controller #1
00h	29h	05h	Intel(R) PSE:DMA Controller #2
00h	29h	06h	Intel(R) PSE:Pulse Width Modulation(PWM) Controller
00h	29h	07h	Intel(R) PSE:Analog to Digital Converter(ADC)
00h	28h	00h	PCI Express*(PCIe*) Root Port #0(PCIe 0,Single VC)
00h	28h	01h	PCIe* Root Port #1(PCIe 0,Single VC)
00h	28h	02h	PCIe* Root Port #2(PCIe 0,Single VC)
00h	28h	03h	PCIe* Root Port #3(PCIe 0,Single VC)
00h	28h	04h	PCIe* Root Port #4(PCIe 0,Multi VC)
00h	28h	05h	PCIe* Root Port #5(PCIe 0, Multi VC)
00h	28h	06h	PCIe* Root Port #6(PCIe 0, Multi VC)
00h	27h	00h	Intel(R) PSE:Inter-Integrated Circuit(I2C) Controller #0
00h	27h	01h	Intel(R) PSE:I2C Controller #1
00h	27h	02h	Intel(R) PSE:I2C Controller #2
00h	27h	03h	Intel(R) PSE:I2C Controller #3
00h	27h	04h	Intel(R) PSE:I2C Controller #4
00h	27h	05h	Intel(R) PSE:I2C Controller #5
00h	27h	06h	Intel(R) PSE:I2C Controller #6

Bus Number	Device Number	Function Number	Description
00h	26h	00h	Embedded Multi Media Card(eMMC) Controller
00h	26h	01h	Secure Digital (SD) & Secure Digital I/O Controller
00h	26h	03h	Intel(R) Safely Island(Intel(R) SI) Controller
00h	25h	00h	Intel(R) Serial I/O:Inter-Integrated Circuit(I2C) Controller #4
00h	25h	01h	Intel(R) Serial I/O I2C Controller #5
00h	25h	02h	Intel(R) Serial I/O:Universal Asynchronous Receiver/Transmitter(UART) Controller #2
00h	24h	00h	Intel(R) Programmable Services Engine(Intel(R) PSE):I2C Controller #7
00h	24h	01h	Intel(R) PSE:Controller Area Network (CAN) Controller #0
00h	24h	02h	Intel(R) PSE:CAN Controller #1
00h	24h	03h	Intel(R) PSE:Quadrature Encoder Peripheral,(QEP) Controller #0
00h	24h	04h	Intel(R) PSE:QEP Controller #1
00h	24h	05h	Intel(R) PSE: QEP Controller #2
00h	24h	06h	Intel(R) PSE: QEP Controller #3
00h	22h	00h	Intel(R)
00h	22h	01h	Intel(R) CSE:HECI #1
00h	22h	04h	Intel(R) CSE:HECI #2
00h	22h	05h	Intel(R) CSE:HECI #3
00h	21h	00h	Intel(R) Serial I/O:Inter-Integrated Circuit(I2C) Controller #0
00h	21h	01h	
00h	21h	02h	Intel(R) Serial I/O:I2C Controller #1
00h	21h	03h	Intel(R) Serial I/O:I2C Controller #2
00h	21h	07h	Intel(R) Serial I/O:I2C Controller #3
00h	19h	00h	Intel(R) PSE:Serial Peripheral Interface(SPI) Controller #0
00h	19h	01h	Intel(R) PSE:SPI Controller #1
00h	19h	02h	Intel(R) PSE:SPI Controller #2
00h	19h	03h	Intel(R) PSE:SPI Controller #3
00h	19h	04h	Intel(R) PSE:General Pupose Input Output(GPIO) Controller #0
00h	19h	05h	Intel(R) PSE:General Pupose Input Output(GPIO) Controller #1
00h	18h	00h	Intel(R) Serial I/O:SPI Controller #2

Bus Number	Device Number	Function Number	Description
00h	18h	03h	Intel(R) Converged Security Engine(Intel(R) CSE):UMA Access
00h	18h	04h	Intel(R) CSE:Intel(R) PTT DMA Controller
00h	18h	05h	Universal Flash Storage(UFS) Controller #0
00h	18h	07h	UFS Controller #1
00h	17h	00h	Intel(R) PSE:Universal Asynchronous Receiver/Transmitter(UART) Controller#0
00h	17h	01h	Intel(R) PSE:UART Controller #1
00h	17h	02h	Intel(R) PSE:UART Controller #2
00h	17h	03h	Intel(R) PSE:UART Controller #3
00h	17h	04h	Intel(R) PSE:UART Controller #4
00h	17h	05h	Intel(R) PSE:UART Controller #5
00h	17h	06h	Intel(R) PSE:Inter-Integrated Circuit Sound(I2S) Controller #0
00h	17h	07h	Intel(R) PSE:I2S Controller #1
00h	16h	00h	Intel(R) Serial I/O:Inter-Integrated Circuit(I2C) Controller #6
00h	16h	01h	Intel(R) Serial I/O:I2C Controller #7
00h	16h	05h	Integrated Error Handler(IEH)

6.5 PCI Interrupt Routing Map

INT Line	xHCI Controller	SATA Controller	SMBus Controller
Int0	INTA:16	INTA:16	INTA:16
Int1	INTB:17		
Int2	INTC:18		
Int3	INTD:19		

INT Line	PCIe Port 1	PCIe Port 2	PCIe Port 3	PCIe Port 4	PCIe Port 5	PCIe Port 6	PCIe Port 7
Int0	INTA:16	INTB:17	INTC:18	INTD:19	INTA:16	INTB:17	INTC:18
Int1	INTB:17	INTC:18	INTD:19	INTA:16	INTB:17	INTC:18	INTD:19
Int2	INTC:18	INTD:19	INTA:16	INTB:17	INTC:18	INTD:19	INTA:16
Int3	INTD:19	INTA:16	INTB:17	INTC:18	INTD:19	INTA:16	INTB:17

6.6 SMBus Address Table

Device	Address
PTN3460	C0h

7. BIOS Configurations

This section presents the six primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. The subsections in this section describe the submenus and setting options for each menu item. The default setting options are presented in bold, and the function of each setting is described in the right hand column of the respective table.

Main	Advanced	Chipset	Security	Boot	Save & Exit
BIOS Information System Information Board Information System Date and Time Access Level	CPU Configuration Power & Performance Graphics Configuration Power Management System Management Thermal Management Watchdog Timer Super IO Configuration Miscellaneous USB Configuration Serial Port Console Redirection Network Stack Configuration Trusted Computing	System Agent (SA) Configuration PCH-IO Configuration	Setup Administrator Password User Password Secure Boot	Boot Configuration FIXED BOOT ORDER Priorities UEFI USB Key Drive BBS Priorities	Save Change and Exit Discard Changes and Exit Save Changes and Reset Discard Changes and Reset Save Options Boot Override

7.1 Main

7.1.1 Main > BIOS Information

Feature	Options	Description
BIOS Vendor	Info only	American Megatrends
BIOS Version	Info only	ADLINK BIOS version
Build Date	Info only	ADLINK BIOS Build Date
MRC Version	Info only	Display MRC Version
GOP Version	Info only	Display GOP Version
ME FW Version	Info only	Display ME FW Version
BIOS Boot Source	Info only	Display BIOS Boot Source

7.1.2 Main > System Information

Feature	Options	Description
Project Name	Info only	Display Project Name.
CPU Board version	Info only	Display CPU Board Version.
CPU Board String	Info only	Display CPU Board String.
CPU Frequency	Info only	Display CPU Frequency.
Total Memory	Info only	Display Installed Memory Size.
Memory Frequency	Info only	Display Memory Frequency.
PCH SKU	Info only	Display PCH SKU Version

7.1.3 Main > Board Information

Feature	Options	Description
Board Information	Info only	
Serial Number	Info only	Display SEMA serial Number.
Manufacturing Date	Info only	Display SEMA manufacturing date.
Last Repair Date	Info only	Display SEMA last repair date.
MAC ID	Info only	Display SEMA MAC ID.
Runtime Statistics	Info only	
Total Runtime	Info only	The returned value specifies the total time in minutes the system is running in S0 state.
Current Runtime	Info only	The returned value specifies the time in seconds the system is running in S0 state. This counter is cleared when the system is removed from the external power supply.
Power Cycles	Info only	The returned value specifies the number of times the external power supply has been shut down
Boot Cycles	Info only	The Boot counter is increased after a HW- or SW-Reset or after a successful power-up.
Boot Reason	Info only	The boot reason is the event which causes the reboot of the system.

7.1.4 Main > System Date/Time

Feature	Options	Description
System Date	Info only	
System Time	Info only	

7.1.5 Main > Access Level

Feature	Options	Description
Access Level	Info only	

7.2 Advanced

7.2.1 Advanced > CPU Configuration

Feature	Options	Description
CPU Configuration	Info only	
Type	Info only	Socket Specific CPU Information.
ID	Info only	Display Microcode Patch.
Speed	Info only	Display Max CPU speed.
Stepping	Info only	Display Min CPU stepping.
L1 Data Cache	Info only	Display cache info.
L1 Instruction Cache	Info only	Display cache info.
L2 Cache	Info only	Display cache info.
L3 Cache	Info only	Display cache info.
L4 Cache	Info only	Display cache info.
VMX	Info only	Display VMX support info.
SMX/TXT	Info only	Display SMX/TXT support info.
Intel Virtualization Technology	Disabled **Enabled**	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.
Active Processor Cores	**ALL**	Number of cores to enable in each processor package.

Feature	Options	Description
	1 2 3	

7.2.2 Advanced > Power & Performance

Feature	Options	Description
CPU – Power Management Control	Submenu	CPU- Power Management Control Options
GT – Power Management Control	Submenu	GT- Power Management Control

7.2.2.1 Advanced > Power & Performance > CPU – Power Management

Feature	Options	Description
CPU – Power Management Control	Info only	
P0 Fused Max Core Ratio	Info only	
P1 Fused Max Core Ratio	Info only	
P2 Fused Max Core Ratio	Info only	
P3 Fused Max Core Ratio	Info only	
Boot performance mode	Max Battery **Max Non-Turbo Performance** Turbo Performance	Select the performance state that the BIOS will set starting from reset vector.
Intel(R) SpeedStep(tm)	Disabled **Enabled**	Allows more than two frequency ranges to be supported

Feature	Options	Description
Race To Halt (RTH)	Disabled **Enabled**	Enable/Disable Race To Halt features. RTH will dynamically increase CPU frequency in order to enter pkg C-State faster to reduce overall power. (RTH is controlled through MSR 1FC bit 20)
Intel(R) Speed Shift Technology	Disabled **Enabled**	Enable/Disable Intel(R) Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states.
HwP Autonomous EPP Grouping	Disabled **Enabled**	Enable EPP grouping (default bit 29 = 0, command 0x11) Autonomous will request the same values for all cores with same EPP. Disable EPP grouping (BIT 29 = 1, command 0x11) Autonomous will not necessarily request same values for all cores with same EPP.
EPB override over PECI	**Disabled** Enabled	Enable/Disable EPB override over PECI. Enable by sending pcode command 0x2b, subcommand 0x3 to1. This will allow OOB EPB PECI override control
HwP Fast MSR Support	Disabled **Enabled**	Enable/Disable HwP Fast MSR Support for IA32_HwP_REQUEST MSR.
HDC Control	Disabled **Enabled**	This option allows HDC configuration. Disabled: Disable HDC Enabled: Can be enabled by OS if OS native support is available.
View/Configure Turbo Options	Submenu	View/Configure Turbo Options
CPU VR Settings	Submenu	CPU VR Settings
Platform PL1 Enable	**Disabled** Enabled	Enable/Disable Platform Power Limit 1 programming. If this option is enabled, it activates the PL1 value to be used by the processor to limit the average power of given time window.
Platform PL2 Enable	**Disabled** Enabled	
Power Limit 4 override	**Disabled** Enabled	Enable/Disable Power Limit 4 override. If this option is disabled, BIOS will leave the default values for Power Limit 4.
C states	Disabled **Enabled**	Enable/Disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.
Enhanced C-states	Disabled **Enabled**	Enable/DISABLE C1E. When enabled, CPU will switch to minimum speed when all cores enter C-State.
C-State Auto Demotion	Disabled	Configure C-State Auto Demotion

Feature	Options	Description
	C1	
C-State Un-demotion	Disabled **C1**	Configure C-State Un-demotion
Package C-State Demotion	Disabled **Enabled**	Package C-State Demotion
Package C-State Un-demotion	Disabled **Enabled**	Package C-State Un-demotion
CState Pre-Wake	Disabled **Enabled**	Disable – Sets bit 30 of POWER_CTL MSR(0x1FC) to 1 to disable the Cstate Pre-Wake
IO MWAIT Redirection	**Disabled** Enabled	When set, will map IO_read instructions sent to IO registers PMG_IO_BASE_ADDRBASE+offset to MWAIT(offset)
Package C State Limit	C0/C1 C2 C3 C6 C7 C7S C8 C9 C10 Cpu Default **Auto**	Maximum Package C State Limit Setting. Cpu Default: Leaves to Factory default value. Auto: Initializes to deepest available Package C State Limit.
C6/C7 Short Latency Control(MSR 0x60B)	Info only	
Time Unit	1 ns 32ns **1024ns**	Unit of measurement for IRTL value – bits [12:10]

Feature	Options	Description
	32768 ns 1048576 ns 33554432 ns	
Latency	**0**-1023	Interrupt Response Time Limit value- bits [9:0], Enter 0-1023
C6/C7 Long Latency Control(MSR 0x60C)	Info only	
Time Unit	1 ns 32ns **1024ns** 32768 ns 1048576 ns 33554432 ns	Unit of measurement for IRTL value – bits [12:10]
Latency	**0**-1023	Interrupt Response Time Limit value- bits [9:0], Enter 0-1023
C8 Latency Control(MSR 0x633)		
Time Unit	1 ns 32ns **1024ns** 32768 ns 1048576 ns 33554432 ns	Unit of measurement for IRTL value – bits [12:10]
Latency	**0**-1023	Interrupt Response Time Limit value- bits [9:0], Enter 0-1023
C9 Latency Control(MSR 0x634)		
Time Unit	1 ns 32ns **1024ns** 32768 ns 1048576 ns 33554432 ns	Unit of measurement for IRTL value – bits [12:10]

Feature	Options	Description
Latency	**0**-1023	Interrupt Response Time Limit value- bits [9:0], Enter 0-1023
C10 Latency Control(MSR 0x635)		
Time Unit	1 ns 32ns **1024ns** 32768 ns 1048576 ns 33554432 ns	Unit of measurement for IRTL value – bits [12:10]
Latency	**0**-1023	Interrupt Response Time Limit value- bits [9:0], Enter 0-1023
Thermal Monitor	Disabled Enabled	Enable/Disable Thermal Monitor
Interrupt Redirection mode Selection	Fixed Priority Round robin Hash Vector No Change	Interrupt Redirection Mode Select for Logical Interrupts
Timed MWAIT	**Disabled** Enabled	Enable/Disable Timed MWAIT Support
Custom P-state Table	Submenu	
EC Turbo Control Mode	**Disabled** Enabled	Enable/Disable EC Turbo Control mode
Energy Performance Gain	**Disabled** Enabled	Enable/Disable Energy Performance Gain.
EPG DIMM Idd3N	26	Active standby current (Idd3N) in milliamps from datasheet. Must be calculated on a per DIMM basis.
EPG DIMM Idd3P	11	Active power-down current(Idd3P) in milliamps from datasheet. Must be calculated on a per DIMM basis.
Power Limit 3 Settings	Submenu	
CPU Lock Configuration	Submenu	CPU Lock Configuration

7.3.2.1.1 Advanced > Thermal Management > CPU – Power Management > View/Configure Turbo Options

Feature	Options	Description
Current Turbo Settings	Info only	
Max Turbo Power Limit	Info only	
Min Turbo Power Limit	Info only	
Package TDP Limit	Info only	
Power Limit 1	Info only	
Power Limit 2	Info only	
1-core Turbo Ratio	Info only	
2-core Turbo Ratio	Info only	
3-core Turbo Ratio	Info only	
4-core Turbo Ratio	Info only	
Energy Efficient P-state	Disabled **Enabled**	Enable/Disable Energy Efficient P-state feature. When set to 0, will disable access to ENERGY_PERFORMANCE_BIAS MSR and CPUID Function 6 ECX[3] will read 0 indicating no support for Energy Efficient policy setting. When set to 1 will enable access to ENERGY_PERFORMANCE_BIAS MSR
Package Power Limit MSR Lock	**Disabled** Enabled	Enable/Disable locking of Package Power Limit settings. When enabled, PACKAGE_POWER_LIMIT MSR will be locked and a reset will be required to unlock the register.
Power Limit 1 Override	**Disabled** Enabled	Enable/Disable Power Limit 1 override. If this option is disabled, BIOS will program the default values for Power Limit 1 and Power Limit 1 Time Window.
Power Limit 2 Override	Disabled **Enabled**	Enable/Disable Power Limit 2 override. If this option is disabled, BIOS will program the default values for Power Limit 2.
Power Limit 2	0	Power Limit 2 value in milli-watts. BIOS will round to the nearest 1/8W when programming. If the value is 0, BIOS will program this value as 1.25*TDP. For 12.50W, enter 12500. Processor applies control policies such that the package power does not exceed this limit.
1-Core Ratio Limit Override	19	1-Core Ratio Limit with range 0 to 83. The Minimum range may vary between Processors. This 1-Core Ratio Limit Must be greater than or equal to 2-Core Ratio Limit, 3-Core Ratio Limit, 4-Core Ratio Limit.

Feature	Options	Description
2-Core Ratio Limit Override	19	2-Core Ratio Limit with range 0 to 83. The Minimum range may vary between Processors. This 2-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit.
3-Core Ratio Limit Override	19	3-Core Ratio Limit with range 0 to 83. The Minimum range may vary between Processors. This 3-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit.
4-Core Ratio Limit Override	19	4-Core Ratio Limit with range 0 to 83. The Minimum range may vary between Processors. This 4-Core Ratio Limit Must be Less than or equal to 1-Core Ratio Limit.
Energy Efficient Turbo	Disabled **Enabled**	Enable/Disable Energy Efficient Turbo Feature. This feature will opportunistically lower the turbo frequency to increase efficiency. Recommended only to disable in overclocking situations where turbo frequency must remain constant. Otherwise, leave enabled.

7.3.2.1.2 Advanced > Thermal Management > CPU – Power Management > CPU VR Settings

Feature	Options	Description
CPU VR Settings	Info only	
PSYS Slope	0	
PSYS Offset	0	
PSYS PMax Power	**+** -	
Acoustic Noise Settings	Submenu	Configure Acoustic Noise Settings for IA, GT and SA domains
VccIn VR Settings	Submenu	VccIn VR Settings
RFI Settings	Submenu	RFI Settings

7.3.2.1.3 Advanced > Thermal Management > CPU – Power Management > Custom P-state Table

Feature	Options	Description
Custom P-state Table	Info only	
Number of P states	0	Sets the number of custom P-states. At least 2 states must be present.

7.3.2.1.4 Advanced > Thermal Management > CPU – Power Management > CPU Lock Configuration

Feature	Options	Description
CFG Lock	Disabled **Enabled**	Configure MSR 0xE2[15], CFG Lock bit
Overclocking Lock	**Disabled** Enabled	Enable/Disable Overclocking Lock (BIT 20) in FLEX_RATIO(194) MSR

7.2.2.2 Advanced > Power & Performance > GT – Power Management Control

Feature	Options	Description
GT – Power Management Control	Info only	
RC6(Render Standby)	Disabled **Enabled**	
Maximum GT frequency	Default Max Frequency 100Mhz 150Mhz 200Mhz 250Mhz 300Mhz 350Mhz 400Mhz	Maximum GT frequency limited by the user. Choose between 400MHz (RPN) and 400MHz (RP0). Value beyond the range will be clipped to min/max supported by SKU

Feature	Options	Description
	450Mhz 500Mhz 550Mhz 600Mhz 650Mhz 700Mhz 750Mhz 800Mhz 850Mhz 900Mhz 950Mhz 1000Mhz 1050Mhz 1100Mhz 1150Mhz 1200Mhz	
Disable Turbo GT frequency	Enabled **Disabled**	Enabled: Disables Turbo GT frequency. Disabled: GT frequency is not limited

7.2.3 Advanced > Graphics Configuration

Feature	Options	Description
Nxp configuration	Info Only	
Data format and Color Depth	VESA 24 bpp JEIDA 24 bpp **JEIDA/vesa 18 bpp**	Data format and Color Depth select
LVDS Output Mode	Dual LVDS bus **Single LVDS bus**	Single/Dual mode select
DE Polarity	**Active High** Active Low	DE Polarity select
Vsync Polarity	**Active High** Active Low	Vsync Polarity select
Hsync Polarity	**Active High** Active Low	Hsync Polarity select
Spreading depth	**No Spreading** 0.5% 1.0% 1.5% 2.0% 2.5%	Clock frequency center spreading depth.
Integrated Display Configuration	Info only	
eDP/LVDS	**Disabled** Enabled	Enable/Disable eDP/LVDS
LFP Panel Type	**VBIOS Default** 640x480 800x600 1024x768 1280x1024	Select LFP panel used by Internal Graphics Device by selecting the appropriate setup item.

Feature	Options	Description
	1400x1050 LVDS1 1400x1050 LVDS2 1600x1200 1366x768 1680x1050 1920x1200 1440x900 1600x900 1024x768 1280x800 1920x1080 2048x1536	
LVDS Backlight Mode	**EC Mode** GTT Mode	Select LVDS Backlight control function.
LVDS Backlight	Submenu	
DDI port 1	No Device Display Port HDMI **DisplayPort With HDMI/DVI Compatible**	DDI port 1 function choose to Display Port or HDMI
DDI port 2	No Device Display Port HDMI **DisplayPort With HDMI/DVI Compatible**	DDI port 2 function choose to Display Port or HDMI

7.2.3.1 Advanced > Graphics Configuration > LVDS Backlight

Feature	Options	Description
LVDS Backlight	Info Only	
LVDS Backlight Brightness	0-**255**	A change takes effect immediately. The value range starts by 0 and ends by 255.

7.2.4 Advanced > AMI Graphic Output Protocol Policy

Feature	Options	Description
Intel (R) Graphics Controller	Info Only	
Intel (R) GOP Driver	Info Only	
Output Select	DP1[ACTIVE Current]	Output Interface

7.2.5 Advanced > Power Management

Feature	Options	Description
Power Management	Info Only	
Enable ACPI Auto Configuration	**Disabled** Enabled	Enables or Disables BIOS ACPI Auto Configuration
Enable Hibernation	Disabled **Enabled**	Enables or Disables System ability to Hibernate (OS/S4 Sleep State), This option may not be effective with some operating systems.
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
LID Function	**Disabled** Enabled	Enable/Disable LID Function.
ECO Mode	**Disabled**	Reduces the power consumption of the system, but after a shut down, you have to wait at least 5 seconds before

Feature	Options	Description
	Enabled	you can restart the system.
Power-Up Mode	**Turn On** Remain Off Last State	Turn on: The machine starts automatically when the power supply is turned on. Remain Off: To start the machine the power button has to be pressed. Last State: The machine will power up to last power state.
Power Consumption	**Submenu**	Power Consumption.

7.2.6 Advanced > System Management

Feature	Options	Description
System Management	Info Only	
Version	Info Only	Display SEMA Module Version.
SEMA Firmware	Info Only	Display SEMA Firmware Version.
SEMA Flags	Submenu	Display SEMA Flags
SEMA Features	Info	Display SEMA Supported Features

7.2.6.1 Advanced > System Management > SEMA Flags

Feature	Options	Description
SEMA Flags	Info Only	
BIOS Select	Info Only	
ATX/AT-Mode	Info Only	

7.2.7 Advanced > Thermal Management

Feature	Options	Description
Thermal Management	Info Only	
Critical Trip Point	**Disabled** 80 C 90 C 95 C	The value is the temperature threshold of the Critical Trip Point.
Passive Cooling Trip Point	**Disabled** 70 C 80 C 90 C 100 C	The value is the temperature threshold of the Passive Cooling Trip Point.
Active Cooling Trip Point	40 C 50 C 60 C 70 C **Refer to BMC**	This value is the temperature threshold of the active cooling trip point.
Watchdog ACPI Event Shutdown	**Disabled** Enabled	Watchdog ACPI Event Shutdown Enabled/Disabled
Temperature and Fan Speed	Submenu	

7.2.7.1 Advanced > Thermal Management > Temperatures

Feature	Options	Description
Temperatures	Info Only	
CPU Temperature	Info Only	
Current	Info Only	Display Current CPU Temperature
Startup	Info Only	Display Startup Board Temperature
Min	Info Only	Display Min Board Temperature
Max	Info Only	Display Max Board Temperature
Board Temperatures	Info Only	
Current	Info Only	Display Current Board Temperature
Startup	Info Only	Display Startup Board Temperature
Min	Info Only	Display Min Board Temperature
Max	Info Only	Display Max Board Temperature

7.2.8 Advanced > Watchdog Timer

Feature	Options	Description
Watchdog Timer	Info only	
Power-Up Watchdog	**Disabled** Enabled	The Power Up Watchdog resets the system after a certain amount of time after power up. Pressing F12 during start up disables the Power Up Watchdog
Timeout	**65535**	Here you can enter the time the Power Up Watchdog should wait until it resets the system. The value range starts by 24 and ends by 65535

7.2.9 Advanced > Super IO Configuration

Feature	Options	Description
Super IO Configuration	Info only	
IT5121E Super IO Configuration	Submenu	System Super IO Chip Parameters.

7.2.9.1 Advanced > Super IO Configuration > IT5121E Super IO Configuration

Feature	Options	Description
IT5121E Super IO Configuration	Info only	
Serial Port 1/2 Configuration	Submenu	Set Parameters of Serial Port 1/2
Serial Port 1/2 Configuration	Info only	
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	Info Only	Display IO / IRQ information of COM Port.
Change Settings	**Auto** IO=3F8h/2F8h; IRQ=4; IO=3F8h; IRQ=3,4,5,6,7,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for Super IO Device.
Change Settings	**Normal** High Speed	Select an optimal settings for Super IO Device

7.2.10 Advanced > Serial Console Redirection

Feature	Options	Description
COM1	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange

Feature	Options	Description
		data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.
COM2	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.
COM3	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.
COM4	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.
Legacy Console Redirection	Info only	
Legacy Console Redirection Settings	Submenu	Legacy Console Redirection Settings

7.2.10.1 Advanced > Serial Console Redirection > Console Redirection Settings (if COM1 enabled)

Feature	Options	Description
COM1	Info only	
Console Redirection Settings	Info only	
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
VT-UTF8 Combo Key Support	**Enabled** Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Recorder Mode	**Disabled**	With this mode enabled only text will be sent.

Feature	Options	Description
	Enabled	This is to capture Terminal data.
Resolution 100x31	Enabled **Disabled**	On Legacy OS, the Number of Rows and Columns supported redirection
Legacy OS Redirection Resolution	**80x24** 80x25	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** Intel Linux XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	**Always Enable** BootLoader	When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.

7.2.10.2 Advanced > Serial Console Redirection > Console Redirection Settings (if COM2 enabled)

Feature	Options	Description
COM2	Info only	
Console Redirection Settings	Info only	
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.

Feature	Options	Description
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
VT-UTF8 Combo Key Support	**Enabled** Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With this mode enabled only text will be sent. This is to capture Terminal data.
Resolution 100x31	Enabled **Disabled**	On Legacy OS, the Number of Rows and Columns supported redirection
Legacy OS Redirection Resolution	**80x24** 80x25	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** Intel Linux XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	**Always Enable** BootLoader	When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.

7.2.10.3 Advanced > Serial Console Redirection > Console Redirection Settings (if COM3 enabled)

Feature	Options	Description
COM3	Info only	
Console Redirection Settings	Info only	
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
VT-UTF8 Combo Key Support	**Enabled** Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Recorder Mode	**Disabled**	With this mode enabled only text will be sent.

Feature	Options	Description
	Enabled	This is to capture Terminal data.
Resolution 100x31	Enabled **Disabled**	On Legacy OS, the Number of Rows and Columns supported redirection
Legacy OS Redirection Resolution	**80x24** 80x25	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** Intel Linux XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	**Always Enable** BootLoader	When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.

7.2.10.4 Advanced > Serial Console Redirection > Console Redirection Settings (if COM4 enabled)

Feature	Options	Description
COM4	Info only	
Console Redirection Settings	Info only	
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.

Feature	Options	Description
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
VT-UTF8 Combo Key Support	**Enabled** Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With this mode enabled only text will be sent. This is to capture Terminal data.
Resolution 100x31	Enabled **Disabled**	On Legacy OS, the Number of Rows and Columns supported redirection
Legacy OS Redirection Resolution	**80x24** 80x25	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** Intel Linux XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	**Always Enable** BootLoader	When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.

7.2.10.5 Advanced > Serial Console Redirection >Legacy Console Redirection Settings

Feature	Options	Description
Legacy Serial Redirection Port	**COM1** COM2 COM3 COM4	Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages

7.2.11 Advanced > Miscellaneous

Feature	Options	Description
Miscellaneous	Info Only	
Power Supply Unit	Emulate AT Mode **ATX Mode**	Select Emulation AT or ATX function. If this option set to [Emulation AT], BIOS will report no suspend functions (S3 & S4) to ACPI OS. In windows XP, it will make OS show shutdown message during system shutdown. ATX: OS will turn off system power when shutdown.
I2C Speed Control	**100 kbps** 400 kbps	I2C Speed Control
Smart Battery Function	**Disabled** Enabled Auto	Enable/Disable Smart Battery function. Auto: disable Smart Battery function if charger IC not be detected.
WOL From S5	**ON** OFF	This Config to control power on/off LAN in S5 State by SEMA (EC).

7.2.12 Advanced > USB Configuration

Feature	Options	Description
USB Configuration	Info Only	
USB Module Version	Info Only	Display USB Module Version
USB Controllers:	Info Only	Display USB Controllers is XHCI or EHCI.
USB Devices:	Info Only	Display attachment USB devices.
Legacy USB Support	**Enabled** Disabled Auto	Enables Legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications.
XHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	Disabled **Enabled**	Enable / Disable USB Mass Storage Driver Support.
USB hardware delays and time-outs:	Info Only	
USB transfer rime-out	1 sec 5sec 10sec **20 sec**	The time-out value for Control, Bulk, and Interrupt transfers.
Device reset time-out	10 sec **20 sec** 30 sec 40 sec	USB mass storage device Start Unit command time-out.
Device power-up delay	**Auto** Manual	Maximum time the device will take before it properly reports itself to the Hot Controller. 'Auto' uses default value: for a Root po\rt it is 100 ms, for a Hub port the delay is taken form Hub descriptor.

7.2.13 Advanced > Network Stack Configuration

Feature	Options	Description
Network Stack	**Disable** Enable	Enable / Disable UEFI Network Stack.

7.2.14 Advanced > Trusted Computing

Feature	Options	Description
TPM20 Device Found	Info Only	
Security Device Support	**Disable** Enable	Enables or Disable BIOS support for security device. OS will not show Security Device. TCG EFI protocol and available.

7.3 Chipset

7.3.1 Chipset > System Agent (SA) Configuration

Feature	Options	Description
Memory Configuration	Submenu	Memory Configuration Parameters
Graphics Configuration	Submenu	Graphics Configuration
VT-D	Disabled **Enabled**	VT-d capability
GNA Device	Disabled **Enabled**	Enable/Disable SA GNA Device.
Above 4GB MMIO BIOS assignment	Disabled **Enabled**	Enable/Disable above 4GB MemoryMappedIO BIOS assignment. This is enabled automatically when Aperture Size is set to 2048MB.

7.3.1.1 Chipset > System Agent (SA) Configuration > Memory Configuration

Feature	Options	Description
Memory Configuration	Info Only	
Memory RC Version	Info Only	
Memory Data Rate	Info Only	
Memory Timings (tCL-tRCD-tRP-tRAS)	Info Only	
Channel 0 Slot 0	Info Only	
Channel 1 Slot 0	Info Only	
Size	Info Only	
Number of Ranks	Info Only	

Feature	Options	Description
Manufacturer	Info Only	
Maximum Memory Frequency	Auto 1067 1200 1333 1400 ..... **4267**	Maximum Memory Frequency in Mhz. Must divide by 133 or 100 according to the refclk. In Gear2 must divide by 266 or 200. Lowest Gear2 speed is 2133
HOB Buffer Size	Auto 1B 1KB Max (assuming 63KB total HOB size)	Size to set HOB Buffer
Max TOLUD	Dynamioc 1 GB 1.25 GB 3.5GB	Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller
SA GV	Disabled Fixed Low Fixed Mid Fixed High **Enabled**	System Agent Geyserville. Can disable, fix to a specific point, or enable frequency switching.
In-Band ECC	**Enabled** Disabled	Enable/Disable In-Band ECC.
In-Band ECC Operation Mode	0 1 **2**	0: Functional Mode protects requests based on the address range, 1: Makes all requests non protected and ignore range checks, 2:Makes all requests protected and ignore range checks
In-Band ECC Error Injection	Enabled	By enabling this Error Injection Enabling feature, the user acknowledges the security risks. Enabling Error

Feature	Options	Description
	Disabled	Injection allows attackers who have access to the Host Operating System to inject IBECC errors that can cause unintended memory corruption and enable the leak of security data in the BIOS stolen memory regions
Memory Remap	**Enabled** Disabled	Enable/Disable Memory Remap above 4GB
Memory Test on Warm Boot	Disabled **Enabled**	Enable Or Disable Base Memory Test Run on Warm Boot

7.3.1.2 Chipset > System Agent (SA) Configuration > Graphics Configuration

Feature	Options	Description
Graphics Configuration	Info Only	
Primary Display	**Auto** IGFX PEG PCIe	Select which of IGFX/PEG/PCIe Graphics device should be Primary Display Or select HG for Hybrid Gfx.
External Gfx Card Primary Display Configuration	Submenu	External Gfx Card Primary Display Configuration
Internal Graphics	**Auto** Disabled Enabled	Keep IGFX enabled based on the setup options.
GTT Size	2MB 4MB **8MB**	Select the GTT Size
Aperture Size	128MB **256MB** 512MB 1024MB 2048MB	Select the Aperture Size
DVMT Pre-Allocated	0M 32M 46M 96M 128M **60M**	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
DVMT Total Gfx Mem	128 **256**	Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.

Feature	Options	Description
	MAX	
Intel Graphics Pei Display Peim	Enabled **Disabled**	Enable/Disable Pei (Early) Display

7.4.1.2.1 Chipset > System Agent (SA) Configuration > Graphics Configuration > External Gfx Card Primary Display Configuration

Feature	Options	Description
External Gfx Card Primary Display Configuration	Info Only	
Primary PCIE	**Auto**	Select Auto/PCIE1/PCIE2/PCIE3/PCIE4/PCIE5/PCIE6/PCIE7 of D28:F0/F1/F2/F3/F4/F5/F6/F7, PCIE8/PCIE9/PCIE10/PCIE11/PCIE12/PCIE13/PCIE14/PCIE15 of D29:F0/F1/F2/F3/F4/F5/F6/F7, PCIE16/PCIE17/PCIE18/PCIE19 of D27:F0/F1/F2/F3, Graphics device should be Primary PCIE.

7.3.2 Chipset > PCH-IO Configuration

Feature	Options	Description
PCH-IO Configuration	Info Only	Memory Configuration Parameters
PCI Express Configuration	Submenu	PCI Express Configuration setting
SATA Configuration	Submenu	SATA Device Options Settings
USB Configuration	Submenu	USB Configuration settings
Security Configuration	Submenu	Security Configuration setting
HD Audio Configuration	Submenu	HD Audio Subsystem Configuration Settings
SCS Configuration	Submenu	Storage and Communication Subsystem (SCS) Configuration
PSE Configuration	Submenu	Programmable Service Engine (PSE) Configuration

Feature	Options	Description
TSN GBE Configuration	Submenu	Time Sensitive Network GBE Configuration
Enhance Port 80h LPC Decoding	Disabled **Enabled**	Support the word/dword decoding of port 80h behind LPC
Enable TCO Timer	**Disabled** Enabled	Enable/Disable TCO timer. When disabled, it disables PCH ACPI timer, stops TCO timer, and ACPI WDAT table will not be published.
PCIe Pll SSC	**Auto**	Pcie Pll SSC percentage.AUTO - Keep hw default, no BIOS override. Range is 0.0%-2.0%.
SPD Write Disable	**TRUE** FALSE	Enable/Disable setting SPD Write Disable. For security recommendations, SPD write disable bit must be set.

7.3.2.1 Chipset > PCH-IO Configuration > PCIE Express Configuration

Feature	Options	Description
PCI Express Configuration	Info Only	
DMI Link ASPM Control	**Disabled** L0s L1 L0sL1 Auto	The control of Active State Power Management of the DMI Link.
PCIE Ports 1-4 Configuration	**4x1 Port** 1x2 2x1 Port 2x2 Port 1x4 Port	To configure PCI-E Port 1-4 of PCH.[4X1]:Port 1-4 (x1) and Port 8 (x1) / [1x2 2x1]:Port 1 (x2), Port 2 (disabled), Ports 3 and Port 4 (x1) / [2x2]:Port 1-2 (x2) and Port 3-4 (x2) / [1x4]:Port 1 (x4), Ports 2-4 (disabled)
Port8xh Decode	**Disabled** Enabled	
Peer Memory Write Enable	**Disabled** Enabled	

Feature	Options	Description
Compliance Test Mode	**Disabled** Enabled	
PCH PCI Express Clock Gating	**Platform-POR** Enabled Disabled	
PCIe function swap	Disabled **Enabled**	
PCIe EQ settings	Submenu	
PCI Express Root Port 1/2/3/4/5/6/7	Submenu	
PCIE clocks	Submenu	

7.4.2.1.1 Chipset > PCH-IO Configuration > PCI Express Configuration > PCIe EQ Settings

Feature	Options	Description
PCIe EQ override	**Disabled** Enabled	Choose your own PCIe EQ settings, only for users who have a thorough understanding of equalization process

7.4.2.1.2 Chipset > PCH-IO Configuration > PCI Express Configuration > PCI Express Root Port 1/2/3/4/5/6/7/

Feature	Options	Description
PCI Express Root Port 1/2/3/4/5/6/7/	Disabled **Enabled**	Control the PCI Express Root Port.
Connection Type	Build-in **Slot**	Built-In: a built-in device is connected to this rootport. SlotImplemented bit will be clear. Slot: this rootport connects to user-accessible slot. SlotImplemented bit will be set.
ASPM	**Disabled**	Set the ASPM Level:

Feature	Options	Description
	L0s L1 L0sL1 Auto	Force L0s – Force all links to L0s State Auto – BIOS auto configure DISABLE – Disables ASPM
L1 Substates	Disabled L1.1 L1.1 & L1.2	PCI Express L1 Substates settings.
ACS	Disabled **Enabled**	Enable/Disable Access Control Services Extended Capability
PTM	**Disabled** Enabled	Enable/Disable Precision Time Measurement
DPC	Disabled **Enabled**	Enable/Disable Downstream Port Containment
EDPC	Disabled **Enabled**	Enable/Disable Rootport extensions for Downstream Port Containment
URR	**Disabled** Enabled	PCI Express Unsupported Request Reporting Enable/Disable.
FER	**Disabled** Enabled	PCI Express Device Fatal Error Reporting Enable/Disable.
NFER	**Disabled** Enabled	PCI Express Device Non-Fatal Error Reporting Enable/Disable.
CER	**Disabled** Enabled	PCI Express Device Correctable Error Reporting Enable/Disable.
SEFE	**Disabled** Enabled	Root PCI Express System Error on Fatal Error Enable/Disable.
SENFE	**Disabled** Enabled	Root PCI Express System Error on Non-Fatal Error Enable/Disable.

Feature	Options	Description
SECE	**Disabled** Enabled	Root PCI Express System Error on Correctable Error Enable/Disable.
PME SCI	Disabled **Enabled**	PCI Express PME SCI Enable/Disable.
Hot Plug	**Disabled** Enabled	PCI Express Hot Plug Enable/Disable.
Advanced Error Reporting	Disabled **Enabled**	Advanced Error Reporting Enable/Disable.
PCIe Speed	**Auto** Gen1 Gen2 Gen3	Configure PCIe Speed
Transmitter Halt Swing	**Disabled** Enabled	Transmitter Half Swing Enable/Disable.
Detect Timeout	0	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.
Extra Bus Reserved	0	Extra Bus Reserved (0-7) for bridges behind this Root Bridge.
Reserved Memory	10	Reserved Memory for this Root Bridge (1-20) MB
Reserved I/O	4	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.
PCH PCIe LTR Configuration	Info Only	
LTR	Disabled **Enabled**	PCH PCIE Latency Reporting Enable/Disable
Snoop Latency Override	Disabled Manual **Auto**	Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.

Feature	Options	Description
Non Snoop Latency Override	Disabled Manual **Auto**	Non Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manual enter override values. Auto (default): Maintain default bios flow.
Force LTR Override	**Disabled** Enabled	Force LTR Override for PCH PCIE.
LTR Lock	**Disabled** Enabled	PCIE LTR Configuration Lock
Extra options	Submenu	

7.4.2.1.2.1 Chipset > PCH-IO Configuration > PCI Express Configuration > PCI Express Root Port 1/2/3/4/5/6/7/ > Extra Options

Feature	Options	Description
Detect Non-Compliance Device/	**Disabled** Enabled	Detect Non-Compliance PCI Express Device. If enable, it will take more time at POST time.
Prefetchable Memory	**10**	Prefetchable Memory Range for this Root Bridge.
Reserved Memory Alignment	**1**	Reserved Memory Alignment (0 - 31 bits)
Prefetchable Memory Alignment	**1**	Prefetchable Memory Alignment (0 - 31 bits)

7.4.2.1.3 Chipset > PCH-IO Configuration > PCI Express Configuration > PCIe Clocks

Feature	Options	Description
Clock0 assignment	**Platform-POR** Enabled Disabled	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.

Feature	Options	Description
ClkReq for Clock0	**Platform-POR** Disabled	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock1 assignment	**Platform-POR** Enabled Disabled	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock1	**Platform-POR** Disabled	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock2 assignment	**Platform-POR** Enabled Disabled	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock2	**Platform-POR** Disabled	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock3 assignment	**Platform-POR** Enabled Disabled	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock3	**Platform-POR** Disabled	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock4 assignment	**Platform-POR** Enabled Disabled	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock4	**Platform-POR** Disabled	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock5 assignment	**Platform-POR** Enabled Disabled	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock5	**Platform-POR** Disabled	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.

7.3.2.2 Chipset > PCH-IO Configuration > SATA Configuration

Feature	Options	Description
SATA Configuration	Info Only	
SATA Controller	Submenu	PCI Express Configuration setting
SATA Mode Selection	AHCI	Determines how SATA controller(s) operate.
SATA Controller Speed	Default Gen1 **Gen2** Gen3	Indicates the maximum speed the SATA controller can support.
SATA Ports Multiplier	Enabled **Disabled**	Ports Multiplier Enable/Disable
SATA Test Mode	Enabled **Disabled**	Test Mode Enable/Disable (Loop Back).
Software Feature Mask Configuration	Submenu	RST Legacy OROM/RST UEFI driver will refer to the SWFM configuration to enable/disable the storage features.
Aggressive LPM Support	Disabled **Enabled**	Enable PCH to aggressively enter link power state.
Serial ATA Port x	Info Only	
Software Preserve	Info Only	
Port0	Disabled **Enabled**	Enable or Disable SATA Port
Hot Plug	**Disabled** Enabled	Designates this port as Hot Pluggable.
Configured as eSATA	Info Only	
External	**Disabled** Enabled	Marks this port as external.

Feature	Options	Description
Spin Up Device	**Disabled** Enabled	If enabled for any of ports Staggerred Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	**Hard Disk Drive** Solid State Drive	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive
Topology	**Unknown** ISATA Direct Connect Flex M2	Identify the SATA Topology if it is Default or ISATA or Flex or DirectConnect or M2
SATA Portx DevSlp	**Disabled** Enabled	Enable/Disable SATA Port 0 DevSlp. For DevSlp to work, both hard drive and SATA port need to support DevSlp function, otherwise an unexpected behavior might happen. Please check board design before enabling it.
SATA Portx RxPolarity	**Disabled** Enabled	Enable/Disable SATA Port 0 RxPolarity. Default should disable, please check board design before enable it.
DITO Configuration	**Disabled** Enabled	Enable/Disable DITO Configuration
DITO value	Info Only	
DM Value	Info Only	

7.4.2.2.1 Chipset > PCH-IO Configuration > SATA Configuration > Software Feature Mask Configuration

Feature	Options	Description
Software Feature Mask Configuration	Info Only	
HDD Unlock	Disabled **Enabled**	If enabled, indicates that the HDD password unlock in the OS is enabled.
LED Locate	Disabled	If enabled, indicates that the LED/SGPIO hardware is attached and ping to locate feature is enabled on the OS.

Feature	Options	Description
	Enabled	

7.3.2.3 Chipset > PCH-IO Configuration > USB Configuration

Feature	Options	Description
USB Configuration	Info Only	
XHCI Compliance Mode	**Disabled** Enabled	Option to enable Compliance Mode. Default is to disable Compliance Mode. Change to enabled for Compliance Mode testing.
xDCI Support	**Disabled** Enabled	Enable/Disable xDCI (USB OTG Device).
USB2 PHY Sus Well Power Gating	GEN1 **GEN2**	Select 'Enabled' to enable SUS Well PG for USB2 PHY. This option has no effect on PCH-H
USB3 Link Speed Selection	Disabled **Enabled**	This option is to select USB3 Link Speed GEN1 or GEN2
USB PD0 Programming	Disabled **Enabled**	Select 'Enabled' if Port Disable Override functionality is used.
USB Overcurrent	Disabled **Enabled**	Select 'Disabled' for pin-based debug. If pin-based debug is enabled but USB overcurrent is not disabled, USB DbC does not work.
USB Overcurrent Lock	Disabled **Enabled**	Select 'Enabled' if Overcurrent functionality is used. Enabling this will make xHCI controller consume the Overcurrent mapping data
USB Port Disable Override	**Disabled** Select Per-Pin	Selectively Enable/Disable the corresponding USB port from reporting a Device Connection to the controller.
USB Device/HOST Mode Override	**Disabled** Select Per-Pin	Selectively Enable/Disable the corresponding USB 2.0 and USB 3.0 port device mode
USB UCSI ACPI device	**Disabled** Enabled	Enable/Disable USB UCSI ACPI device

7.3.2.4 Chipset > PCH-IO Configuration > Security Configuration

Feature	Options	Description
Security Configuration	Info Only	
RTC Memory Lock	Disabled **Enabled**	Enable will lock bytes 38h-3Fh in the lower/upper 128-byte bank of RTC RAM
BIOS Lock	**Disabled** Enabled	Enable/Disable the PCH BIOS Lock Enable feature. Required to be enabled to ensure SMM protection of flash.
Force unlock on all GPIO pads	**Disabled** Enabled	If Enabled BIOS will force all GPIO pads to be in unlocked state

7.3.2.5 Chipset > PCH-IO Configuration > HD Audio Configuration

Feature	Options	Description
HD Audio Subsystem Configuration Settings	Info Only	
HD Audio	Disabled **Enabled**	Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HDA will be unconditionally enabled.

7.3.2.6 Chipset > PCH-IO Configuration > SCS Configuration

Feature	Options	Description
eMMC 5.1 Controller	Disabled **Enabled**	Enable or Disable SCS eMMC 5.1 Controller
eMMC 5.1 HS400 Mode	Disabled **Enabled**	Enable or Disable SCS eMMC 5.1 HS400 Mode
Enable HS400 software tuning	**Disabled** Enabled	Software tuning should improve eMMC HS400 stability at the expense of boot time
Driver Strength	33 0hm **40 0hm** 50 0hm	Sets I/O driver strength
SDCard 3.0 Controller	Disabled **Enabled**	Enable or Disable SCS SDHC 3.0 Controller

7.3.2.7 Chipset > PCH-IO Configuration > PSE Configuration

Feature	Options	Description
PSE Controller	Disabled **Enabled**	Enables/Disables Programmable Service Engine (PSE) Device
PSE DashBoard Configuration	Info Only	
LOG OUTPUT CHANNEL	3	Determine the PSE log output channel
LOG PUTPUT OFFSET	0	Determine the PSE log output region offset in memory
LOT OUTPUT SIZE	0	Determine the PSE log output region size limitation in memory
Shell	**Disabled** Enabled	Enable/Disable PSE Shell
Eclite	**Disabled**	Enable/Disable PSE Eclite Service

Feature	Options	Description
	Enabled	
OOB	Disabled **Enabled**	Enable/Disable PSE OOB Service
WOL	Disabled **Enabled**	Enable/Disable PSE GBE WoL
PSE Debug (JTAGSWD) Enable	**Disabled** Enabled	PSE JTAG/SWD Debug enable. Set to enable. Unset to disable
PSE JTAG/SWD PIN MUX	**Disabled** Enabled	Enable/Disable PSE Jtag Pin Mux. Grayed out if Sci Pin Mux is enabled
PSE Add-In-Card	**Disabled** Enabled	Enable/Disable PSE Add-In-Card
PSE IP Ownership and GPIO Mux Assignment Configuration	Info Only	
UART1/SER3	None PSE owned with pin muxed **Host owned with pin muxed**	To assign this device to host owned, you must enable PSE UART0 to host owned because UART0 is the function 0 of this device.\nUART0 has no pin conflict. UART1 has pin conflict with TGPIO.\nUART2 is default enabled for PSE logging purpose.\nUART3 has pin conflict with GBE0-1, PWM and TGPIO. UART4 has no pin conflict.\nUART5 has pin conflict with GBE1.\nIf it is grayed out, check the above options.The same pin cannot be assigned to multiple IP.
UART1/SER3 ACPI UART SubDevice	Disabled **Enabled**	Enable/Disable ACPI Uart Subdevice for Windows. Disable for Linux
UART1/SER3 ACPI UART Baudrate	**9600** 19200 38400 57600 115200	Select default Baudrate
Uart4/SER2	None PSE owned with pin muxed **Host owned with pin**	To assign this device to host owned, you must enable PSE UART0 to host owned because UART0 is the function 0 of this device.\nUART0 has no pin conflict. UART1 has pin conflict with TGPIO.\nUART2 is default enabled for PSE logging purpose.\nUART3 has pin conflict with GBE0-1, PWM and TGPIO. UART4 has no pin conflict.\nUART5 has pin conflict with GBE1.\nIf it is grayed out, check the above options. The same pin cannot be assigned to multiple

Feature	Options	Description
	muxed	IP.
UART4/SER2 ACPI UART SubDevice	Disabled **Enabled**	Enable/Disable ACPI Uart Subdevice for Windows. Disable for Linux
UART4/SER2 ACPI UART Baudrate	**9600** 19200 38400 57600 115200	Select default Baudrate
I2C5	None PSE owned with pin muxed **Host owned with pin muxed**	To assign this device to host owned, you must enable PSE I2C0 to host owned because I2C0 is the function 0 of this device.\nI2C1 has pin conflict with TGPIO8-9\nI2C2 has no pin conflict.I2C3 has pin conflict with TGPIO18-19.I2C4 has no pin conflict.I2C5 has pin conflict with PWM.\nI2C6 has no pin conflict.I2C7 has no pin conflict If it is greyed out, check the above options. The same pin cannot be assigned to multiple IP.
I2C7	None PSE owned with pin muxed **Host owned with pin muxed**	If I2C7 is not set to host owned, all PSE CAN and QEP devices could not be set to host owned too due to sharing same function.I2C7 can't assign Host own if UCSI ACPI device enabled
CAN0	**None** PSE owned with pin muxed Host owned with pin muxed	To assign this device to host owned, you must enable PSE I2C7 to host owned because I2C7 is the function 0 of this device.CAN0 has pin conflict with I2S0 and TGPIO 16-17.\nCAN1 has pin conflict with I2S0 and TGPIO14-15.If it is greyed out, check the above options. The same pin cannot be assigned to multiple IP.
CAN1	**None** PSE owned with pin muxed Host owned with pin muxed	To assign this device to host owned, you must enable PSE I2C7 to host owned because I2C7 is the function 0 of this device.CAN0 has pin conflict with I2S0 and TGPIO 16-17.\nCAN1 has pin conflict with I2S0 and TGPIO14-15.If it is greyed out, check the above options. The same pin cannot be assigned to multiple IP.
GBE0	None PSE owned with pin muxed	Select ownership for GBE

Feature	Options	Description
	Host owned with pin muxed	
PSE GBE0 DLL Overrid	**Disabled** Enabled	Enable/Disable PSE GBE0 DLL.To Enable this GBE1 must be Enabled
GBE1	None PSE owned with pin muxed **Host owned with pin muxed**	Select ownership for GBE
PSE GBE1 DLL Overrid	**Disabled** Enabled	Enable/Disable PSE GBE1 DLL.To Enable this GBE1 must be Enabled
GPIO/TGPIO 0	None **PSE owned with pin muxed** Host owned with pin muxed	Owner of GPIO/TGPIO 0 Controller (PSE or HOST owned).
GPIO/TGPIO 0 MUX SELECTION	LOWER MID TOP **All pins are GPIO**	Choose Top, Mid, Lower or All mux for GPIO/TGPIO 1 Controller Instance.
GPIO/TGPIO 0 Pin Selection	Submenu	Enable individual GPIO/TGPIO pin
GPIO/TGPIO 1	None **PSE owned with pin muxed** Host owned with pin muxed	Owner of GPIO/TGPIO 1 Controller(PSE or HOST owned).
GPIO/TGPIO 1 MUX SELECTION	LOWER MID TOP **All pins are GPIO**	Choose Top, Mid, Lower or All mux for GPIO/TGPIO 1 Controller Instance.

Feature	Options	Description
GPIO/TGPIO 1 Pin SELECTION	Submenu	Enable individual GPIO/TGPIO pin
PSE Interrupt Assignment Configuration	Info Only	
I2S0	**Disabled** Enabled	Checked = Interrupt set to SB mode. Default unchecked is MSI mode.
I2S1	**Disabled** Enabled	Checked = Interrupt set to SB mode. Default unchecked is MSI mode.
UART1/SER3	**Disabled** Enabled	Checked = Interrupt set to SB mode. Default unchecked is MSI mode.
UART4/SER2	**Disabled** Enabled	Checked = Interrupt set to SB mode. Default unchecked is MSI mode.
I2C5	**Disabled** Enabled	Checked = Interrupt set to SB mode. Default unchecked is MSI mode.
LH2PSE	**Disabled** Enabled	Checked = Interrupt set to SB mode. Default unchecked is MSI mode.
CAN0	**Disabled** Enabled	Checked = Interrupt set to SB mode. Default unchecked is MSI mode.
CAN1	**Disabled** Enabled	Checked = Interrupt set to SB mode. Default unchecked is MSI mode.

7.3.2.8 Chipset > PCH-IO Configuration > TSN GBE Configuration

Feature	Options	Description
PSE TSN GBE 0 Multi-Vc	Enabled **Disabled**	Enable/Disable TSN Multi Virtual Channels. TSN GBE must be host owned.
PSE TSN GBE 0 SGMII Support	Enabled **Disabled**	Enable/Disable Modphy support for SGMII mode for PSE TSN GBE 0. Ports in SGMII mode with the same PLL common lane must use the same link speed. UFS will need to be disabled as this TSN port uses the same PLL

Feature	Options	Description
		common lane. Please make sure IFWI has proper straps set for SGMII. Make sure Flex IO Lane Assignment is not NONE.
PSE TSN GBE 0 Link Speed	RefClk 24Mhz 2.5Gbps RefClk 24Mhz 1Gbps RefClk 38.4Mhz 2.5Gbps **RefClk 38.4Mhz 1Gbps**	PSE TSN GBE 0 Link Speed configuration.
Flex IO Lane Assignment:	Info Only	
PSE TSN GBE1 Multi-Vc	**Enabled** Disabled	Enable/Disable TSN Multi Virtual Channels. TSN GBE must be host owned.
PSE TSN GBE1 SGMII Support	**Enabled** Disabled	Enable/Disable Modphy support for SGMII mode for PSE TSN GBE 1. Ports in SGMII mode with the same PLL common lane must use the same link Speed. SATA or UFS may need to be disabled if TSN port is using the same PLL common lane. Please make sure IFWI has proper straps set for SGMII. Make sure Flex IO Lane Assignment is not NONE.
PSE TSN GBE 1 Link Speed	RefClk 24Mhz 2.5Gbps RefClk 24Mhz 1Gbps RefClk 38.4Mhz 2.5Gbps **RefClk 38.4Mhz 1Gbps**	PSE TSN GBE 1 Link Speed configuration.
Flex IO Lane Assignment:	Info Only	
PLL Common Lane 1	Info Only	

7.4 Security

7.4.1 Security > Password Description

Feature	Options	Description
Password Description	Info only	
Setup Administrator Password	Enter Password	Set Setup Administrator Password
User Password	Enter Password	Set User Password
Secure Boot	Submenu	Customizable Secure Boot settings.
System Mode	Info only	
Secure Boot	Info only	
Secure Boot Control	**Disabled** Enabled	Secure Boot activated when Platform Key(PK) is enrolled, System mode is User / Deployed, and CSM function is disabled

7.5 Boot

7.5.1 Boot > Boot Configuration

Feature	Options	Description
Boot Configuration	Info only	
Setup Prompt Timeout	**1**	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
Bootup NumLock State	**On** Off	Select the keyboard Number state.
Quiet Boot	Disabled **Enabled**	Select the keyboard NumLock state.
Fast Boot	**Disabled** Enabled	Enable or Disable FastBoot features. Most probes are skipped to reduce time cost during boot.
New Boot Option Policy	**Default** Place First Place Last	Controls the placement of newly detected UEFI boot option.
Boot Mode select	LEGACY **UEFI**	Select boot mode LEGACY/UEFI

7.5.2 Boot > Fixed Boot Order Priorities

Feature	Options	Description
Boot Option #1	Hardware	Set the system boot order.
Boot Option #2	CD/DVD	Set the system boot order.
Boot Option #3	USB Hard Disk	Set the system boot order.
Boot Option #4	USB CD/DVD	Set the system boot order.
Boot Option #5	USB Key	Set the system boot order.
Boot Option #6	USB Floppy	Set the system boot order.
Boot Option #7	USB Lan	Set the system boot order.
Boot Option #8	Network	Set the system boot order.

7.6 Save & Exit

Feature	Options	Description
Save Changes and Exit		Exit system setup after saving the changes.
Discard Changes and Exit		Exit system setup without saving any changes.
Save Change and Reset		Reset the system after saving the changes.
Discard Changes and Reset		Reset system setup without saving any changes.
Save Options	Info only	
Save Changes		Save Changes done so far to any of the setup options.
Save as User Defaults		Save the changes done so far as User Defaults.
Restore User Defaults		Restore the User Defaults to all the setup options.
Boot Override	Info only	

8. BIOS Checkpoints, Beep Codes

A status code is a data value used to provide diagnostic information about the boot process. Progress codes are status codes that signify successful progression to a following initialization step. Error codes signify error conditions encountered in the process of system initialization. Aptio 5.x core can be configured to send status codes to a variety of sources. The two most commonly used types of status codes are checkpoint codes and beep codes. Checkpoint codes are byte length data values. Checkpoints are typically output to I/O port 80h, but Aptio 5.x core can be configured to send checkpoints to a variety of sources. Aptio 5.x core outputs checkpoints throughout the boot process to indicate the task the system is currently executing. Checkpoints are very useful in aiding software developers or technicians in debugging problems that occur during the pre-boot process on production hardware. Beep code is a series of short sound signals. Beep codes are typically error codes that do not occur during normal boot process.

Note: Beep codes are not the only sounds generated during the boot process. Some firmware components may use sounds to notify user about other events such as detection of a hot-pluggable device. These sounds are typically generated using a frequency that is different from the frequency of the beep codes

Aptio 5.x core follows the firmware model described by the UEFI Platform Initialization Specification (PI). The PI Specification refers the following "boot phases", which may apply to various checkpoint and beep code descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization
- Driver Execution Environment (DXE) – main hardware initialization
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, ...)

Viewing Checkpoints

Checkpoints generated by Aptio firmware can be viewed using a PCI checkpoint card, also referred to as a "POST Card" or "POST Diagnostic Card". These PCI add-in cards show the value of I/O port 80h on a LED display. Checkpoint cards are available through a variety of computer mail-order outlets.

Newer systems feature support for AMI Debug Rx, a USB connected alternative to the PCI POST Card. AMI Debug Rx is a low-cost debug tool built around the debug port feature common to today's USB 2.0 EHCI controllers. AMI Debug Rx is designed as replacement for the PCI POST Checkpoint Card as newer systems omit PCI expansion slots. Along with checkpoints, AMI Debug Rx has several features specifically designed for BIOS developers.

8.1 Status Code Ranges

Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

8.2 Standard Status Codes

8.2.1 SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization

SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

8.2.2 SEC Phase > SEC Beep Codes

None.

8.2.3 SEC Phase > PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information

Status Code	Description
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed

Status Code	Description
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes

Status Code	Description
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

8.2.4 SEC Phase > PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

8.2.5 SEC Phase > DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started

Status Code	Description
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization

Status Code	Description
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)

Status Code	Description
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM

Status Code	Description
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

8.2.6 SEC Phase > DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

8.2.7 SEC Phase > ACPI/ASL Checkpoint

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

8.3 OEM-reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

9. Software Support

9.1.1 Yocto

Yocto is available on ADlink Github > https://github.com/ADLINK/meta-adlink-x86-64bit

9.1.2 Ubuntu

Ubuntu is supported from kernel 5.15 and up

9.1.3 Windows

Windows 10 is supported

10. Mechanical

PCB dimension: 82 x 50 x 1.2 mm, 12 layer PCB

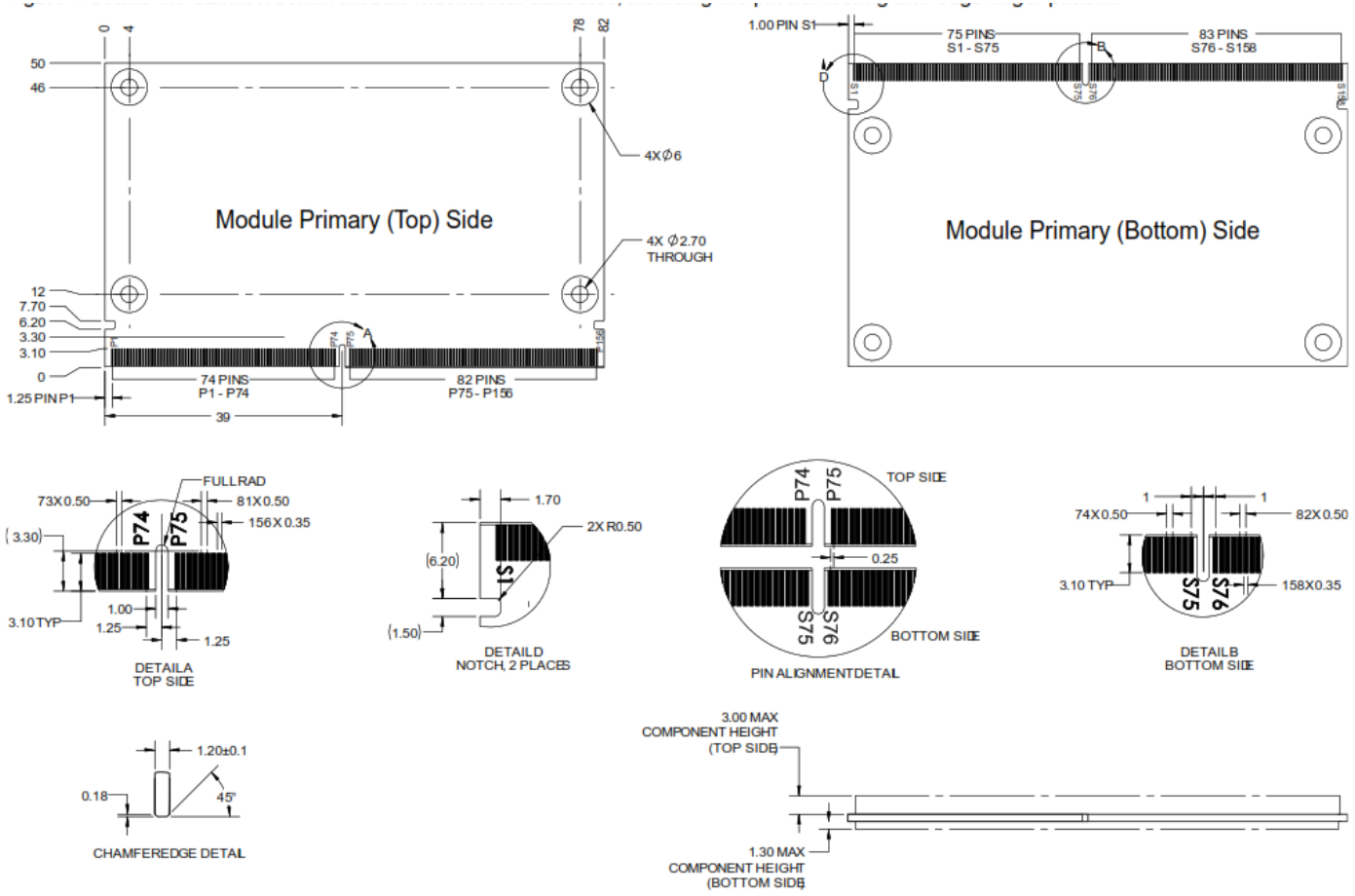
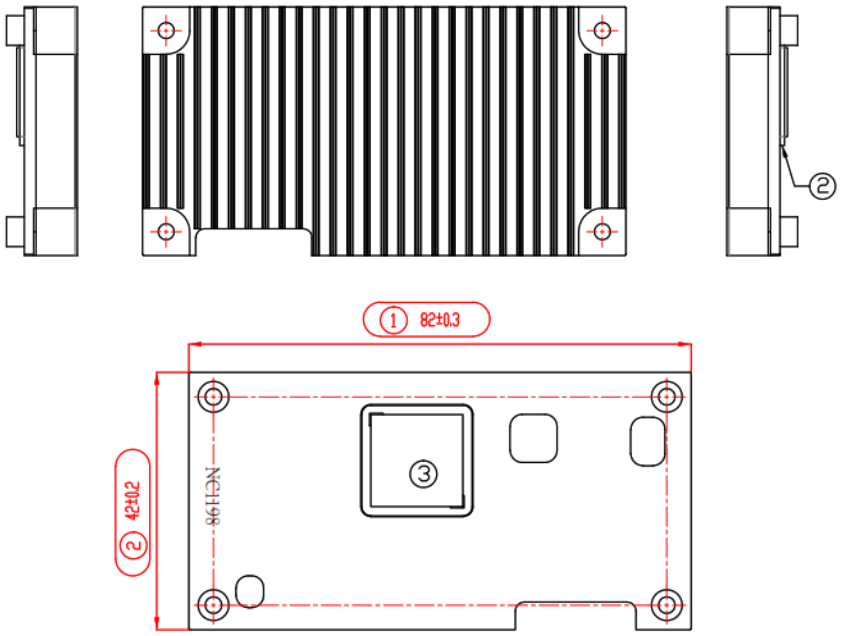


Figure 4: Mechanical dimensions

11. Thermal Solutions

For optimal performance, LEC-EL has to be cooled by a passive heatsink / heat-spreader optionally available for ordering



HTS-sEL	Heatspreader for LEC-EL
THS-sEL	Low profile heatsink for LEC-EL

Figure 5: Thermal solutions