# LEC-IMX8M

User's Guide

01/12/2021

SMARC module

ADLINK Leading EDGE COMPUTING

# Preface

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## Safety Instructions

For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

## Conventions

The following conventions may be used throughout this manual, denoting special levels of information

**Note**: This information adds clarity or specifics to text and illustrations.

**Caution**: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

**Warning**: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

## Revision History

| Revision | Description | Date dd/mm/yyyy | Author |
|---|---|---|---|
| 0.6 | Preliminary engineering version | 06/09/2019 | JB |
| 0.8 | Preliminary engineering version updated | 05/04/2020 | HP |
| 0.9 | Preliminary engineering version updated | 30/07/2020 | HP |
| 1.0 | Release version | 12/01/2021 | HP |
| | | | |

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# Introduction

## 1.1 The SMARC Formfactor

The SMARC ("Smart Mobility ARChitecture") is a versatile small form factor computer on Module definition targeting applications that require low power, low costs, and high performance. The Modules will typically use ARM SOCs similar or the same as those used in many familiar devices such as tablet computers and smart phones. Alternative low power SOCs and CPUs, such as tablet oriented X86 devices and other RISC CPUs may be used as well. The Module power envelope is typically under 6W.

Two Module sizes are defined: 82 mm x 50 mm and 82 mm x 80 mm.

The Module PCBs have 314 edge fingers that mate with a low profile 314 pin 0.5 mm pitch right angle connector (the connector is sometimes identified as a 321 pin connector, but 7 pins are lost to the key).

The Modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE and a single channel LVDS display transmitter are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

SGeT STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

SMARC module and carrier specifications are available online at: https://www.sget.org/standards/smarc.html

# 2. Specifications

## 2.1 Core System

**SoC**

NXP iMX 8M Series

- i.MX8M Quad: 4 x Cortex-A53 at 1.3 - 1.5GHz, 1 x Cortex-M4, GPU, VPU Decode
- i.MX8M QuadLite: 4 x Cortex-A53 at 1.3 - 1.5GHz, 1 x Cortex-M4, GPU
- i.MX8M Dual: 2 x Cortex-A53 at 1.3 - 1.5GHz, 1 x Cortex-M4, GPU, VPU Decode
  available either as industrial (-40°C to +85°C) or commercial (0°C to +70°C) type"

**L2 Cache**

32 KB I-cache 32 KB D-cache (A53) & 16 KB I-cache16 KB D-cache (M4)

**Memory**

1 / 2 / 4 GB DDR3L memory down

**IoT security**

CryptoAuthentication™ Device, Microchip ATECC608A

- Cryptographic co-processor with secure hardware-based key storage
- Protected storage for up to 16 Keys, certificates or data
- ECDH: FIPS SP800-56A Elliptic Curve Diffie-Hellman
- NIST standard P256 elliptic curve support
- SHA-256 & HMAC hash including off-chip context save/restore
- AES-128: encrypt/decrypt, galois field multiply for GCM

## 2.2 Video

LEC-iMX8M standard display support is consisting of 4K capable HDMI 2.0a and single/dual channel 24-bit LVDS.

The LVDS output is derived from an DSI to LVDS bridge. As build option the bridge can be removed and the module can output 4-lane DSI.

**GPU Core:**

Vivante GC7000Lite 2D/3D

**GPU/VPU Feature Support**

- GPU : 4 shaders, OpenGL ES 3.1, OpenCL 1.2, OpenGL 3.0, OpenVG and Vulkan
  Up to 4kp60 UHD resolutions.
- VPU : HEVC/H.265, H.264, VP9 Decoder 1080p60 MPEG-2, MPEG-4p2, VC-1, VP8, RV9, AVS, MJPEG, H.263 Decoder
- (no VPU support for iMX 8M Quad Lite version)

**HDMI**

HDMI 2.0a supporting resolution up to 4K (4096 x 2160 at 60 Hz)

**LVDS**

LVDS single/dual channel 24-bit at max. 2048x1024

**optional MIPI DSI**

DSI 4 lanes at max. 1080p@60fps display output (build option multiplexed with LVDS signal)

**Camera support**

- Compatible with the MIPI Alliance Interface specification v2.1

- Two MIPI-CSI2 camera inputs, one 4-lane and one 2-lane

## 2.3 Audio

Supports i2S audio codec interface , audio ADC and DAC (located on carrier)

## 2.4 Dual Ethernet

**Primary LAN**

SOC embedded GbE Ethernet Controller with IEEE-1588 PTP (Precision Time Protocol) and AVB (Audio Video Bridging) support

Supports 10/100/1000-Mbps data transfer rates, both full-duplex and half-duplex "

**Optional Secondary LAN**

Intel i210 GbE controller with IEEE-1588 PTP (Precision Time Protocol) support (build option over PCIe )

Supports 10/100/1000-Mbps data transfer rates, both full-duplex and half-duplex

## 2.5 Extension busses

**PCIe**

Two PCI Express GEN2 x1 interfaces

**USB**

2x USB 3.0/2.0, 2x USB 2.0 and , 1x USB2.0 OTG

**UART**

three UART interface SER0 (Tx/Rx/CTS/RTS) and SER1, SER3 (Tx/Rx)

7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none)

Programmable baud rates up to 4 Mbps.

**CAN bus**

supporting CAN2.0B only or mixed CAN2.0B and CAN FB mode, data bit rate up to 8 Mbps via SPI to CAN controller

**SPI**

1 x SPI, optional 2 x SPI (SPI0 occupied by SPI-to-CAN controller can be freed up by build option)

**I2S**

2x I2S interfaces with audio resolution from 16-bits to 32-bits and sample rate up to 192KHz (see Audio Codec support)

**I2C**

Four I2C interfaces

- Support for 7-bit and 10-bit address mode

- Software programmable clock frequency of 100 kbit/s in Standard-mode,

400 kbit/s in the Fast-mode or 1 Mbit/s in Fast-mode Plus

**GPIO**

12x GPIO with interrupt

## 2.6 System Storage

**SDIO**

1x SDIO (4-bit) compatible up to version 3.0.

**eMMC**

soldered on module 16, 32 or 64 GB (build option) either standard or -40+85C temp range

Compatible with eMMC specification 4.41, 4.51 and 5.0

## 2.7 SEMA® Board Management Controller

Voltage/current monitoring, boot configuration, logistics and forensic

information, flat panel control, watchdog timer

## 2.8 Debug Header

30-pin multipurpose flat cable connector for use with optional DB-30 debug module Provides JTAG, BMC access; UART, power test points; diagnostic LEDs, Power, Reset, Boot configuration

## 2.9 Boot Modes

eMMC and SD-Card boot modes are supported

## 2.10 Power

**Supply Voltage**

4.75 V – 5.25 V

**Rise Time**

TBD

## 2.11 Mechanical and Environmental

**Form Factor**

SGET SMARC Specifications v2.1

**Dimension**

SMARC small size module, 82mm x 50mm

**Operating Temperature**

Standard: 0°C to +60°C

Rugged: -40°C to +85°C (optional)

**Humidity**

5-90% RH operating, non-condensing

5-95% RH storage (and operating with conformal coating)

**Shock and Vibration**

IEC 60068-2-64 and IEC-60068-2-27, MIL-STD-202 F, Method 213B, Table 213-I,

Condition A and Method 214A, Table 214-I, Condition D

# 3. Block Diagram

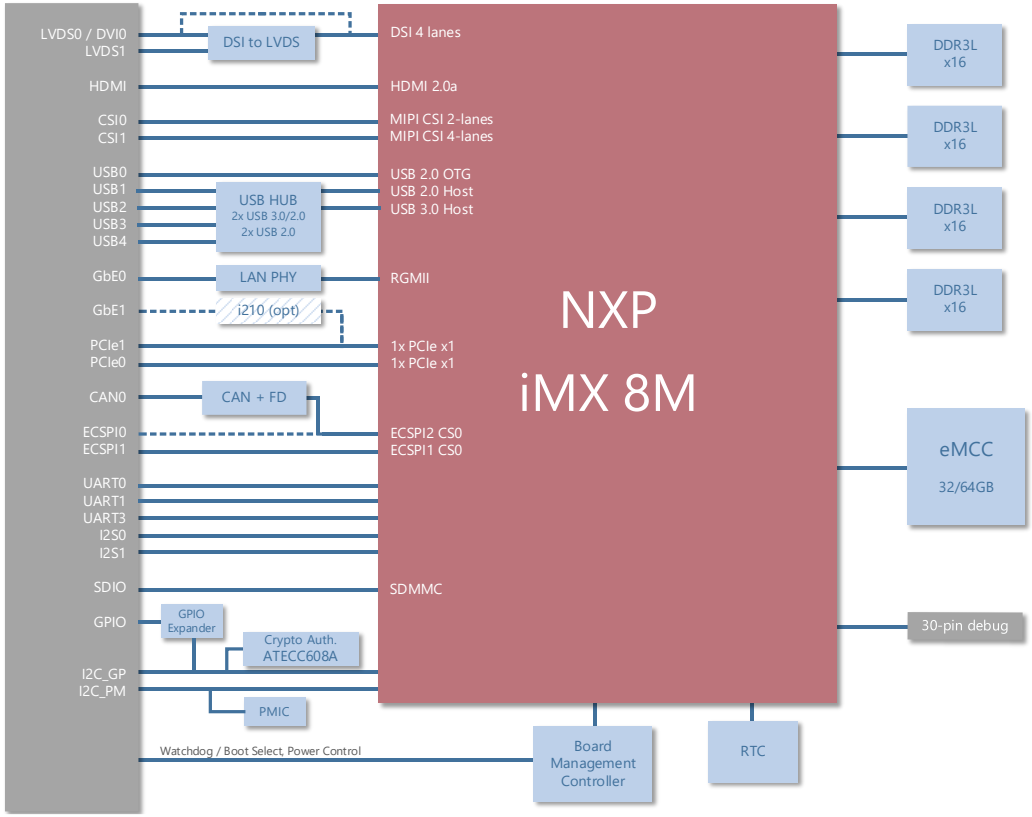



**Figure 1 – Module function diagram**

# 4. Pinout and Signal Descriptions

## 4.1 Pin Summary

The below table is a comprehensible list of all signal pins on the MXM 3 connector in the standard specification SMARC 2.1.

Those signals not supported on LEC-iMX8M are strikethrough ~~STRIKETHROUGH~~

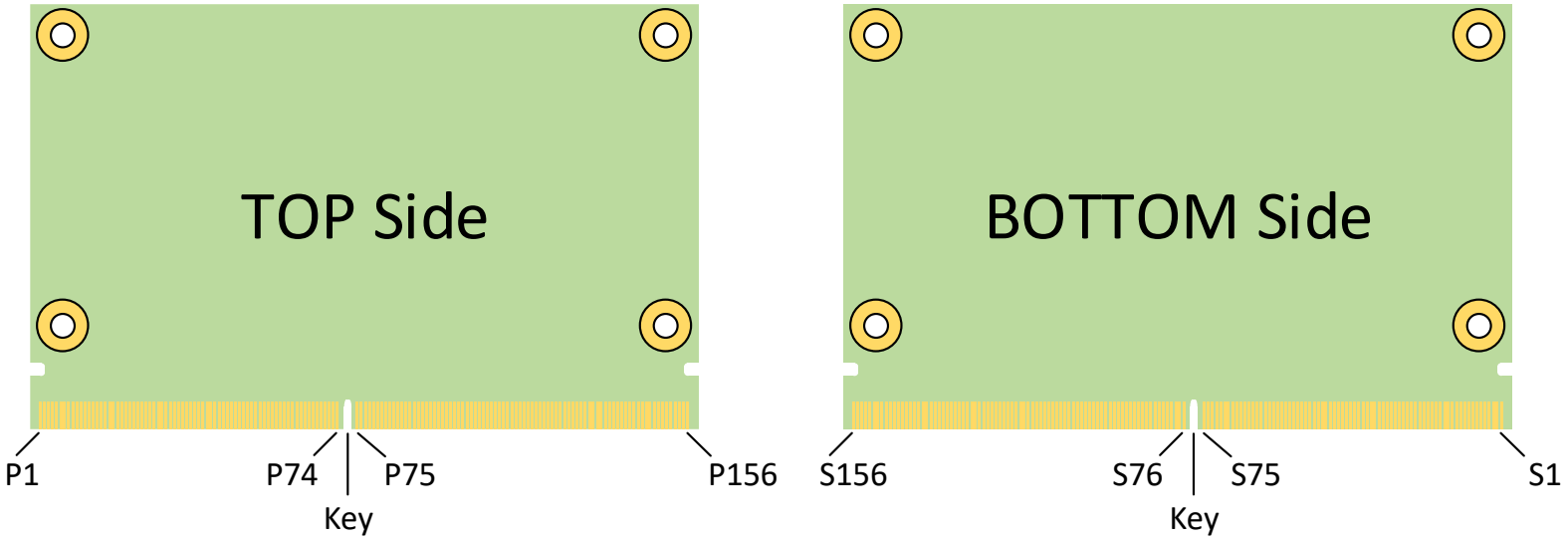


**Figure 2 – Module top/botom side pin numbering**

| P-Pin | Primary (Top) Side |
|---|---|
| | |
| P1 | ~~SMB_ALERT_1V8#~~ |
| P2 | GND |
| P3 | CSI1_CK+ |
| P4 | CSI1_CK- |
| P5 | ~~GBE1_SDP~~ note 1 |
| P6 | GBE0_SDP |
| P7 | CSI1_RX0+ |
| P8 | CSI1_RX0- |
| P9 | GND |
| P10 | CSI1_RX1+ |
| P11 | CSI1_RX1- |
| P12 | GND |
| P13 | CSI1_RX2+ |
| P14 | CSI1_RX2- |
| P15 | GND |
| P16 | CSI1_RX3+ |
| P17 | CSI1_RX3- |
| P18 | GND |
| P19 | GBE0_MDI3- |
| P20 | GBE0_MDI3+ |
| P21 | GBE0_LINK100# |
| P22 | GBE0_LINK1000# |
| P23 | GBE0_MDI2- |
| P24 | GBE0_MDI2+ |
| P25 | GBE0_LINK_ACT# |
| P26 | GBE0_MDI1- |
| P27 | GBE0_MDI1+ |
| P28 | ~~GBE0_CTREF~~ |
| P29 | GBE0_MDI0- |
| P30 | GBE0_MDI0+ |
| P31 | ~~SPI0_CS1#~~ note 2 |

| S-Pin | Secondary (Bottom) Side |
|---|---|
| S1 | ~~CSI1_TX+~~ / I2C_CAM1_CK |
| S2 | ~~CSI1_TX-~~ / I2C_CAM1_DAT |
| S3 | GND |
| S4 | RSVD |
| S5 | ~~CSI0_TX-~~ / I2C_CAM0_CK |
| S6 | CAM_MCK |
| S7 | ~~CSI0_TX+~~ / I2C_CAM0_DAT |
| S8 | CSI0_CK+ |
| S9 | CSI0_CK- |
| S10 | GND |
| S11 | CSI0_RX0+ |
| S12 | CSI0_RX0- |
| S13 | GND |
| S14 | CSI0_RX1+ |
| S15 | CSI0_RX1- |
| S16 | GND |
| S17 | ~~GBE1_MDI0+~~ note 1 |
| S18 | ~~GBE1_MDI0-~~ note 1 |
| S19 | ~~GBE1_LINK100#~~ note 1 |
| S20 | ~~GBE1_MDI1+~~ note 1 |
| S21 | ~~GBE1_MDI1-~~ note 1 |
| S22 | ~~GBE1_LINK1000#~~ note 1 |
| S23 | ~~GBE1_MDI2+~~ note 1 |
| S24 | ~~GBE1_MDI2-~~ note 1 |
| S25 | GND |
| S26 | ~~GBE1_MDI3+~~ note 1 |
| S27 | ~~GBE1_MDI3-~~ note 1 |
| S28 | ~~GBE1_CTREF~~ note 1 |
| S29 | ~~PCIE_D_TX+ / SERDES_1_TX+~~ |
| S30 | ~~PCIE_D_TX- / SERDES_1_TX-~~ |
| S31 | ~~GBE1_LINK_ACT#~~ note 1 |
| S32 | ~~PCIE_D_RX+ / SERDES_1_RX+~~ |

| P-Pin | Primary (Top) Side |
|---|---|
| P32 | GND |
| P33 | SDIO_WP |
| P34 | SDIO_CMD |
| P35 | SDIO_CD# |
| P36 | SDIO_CK |
| P37 | SDIO_PWR_EN |
| P38 | GND |
| P39 | SDIO_D0 |
| P40 | SDIO_D1 |
| P41 | SDIO_D2 |
| P42 | SDIO_D3 |
| P43 | ~~SPI0_CS0#~~ note 2 |
| P44 | ~~SPI0_CK~~ note 2 |
| P45 | ~~SPI0_DIN~~ note 2 |
| P46 | ~~SPI0_DO~~ note 2 |
| P47 | GND |
| P48 | ~~SATA_TX+~~ |
| P49 | ~~SATA_TX-~~ |
| P50 | GND |
| P51 | ~~SATA_RX+~~ |
| P52 | ~~SATA_RX-~~ |
| P53 | GND |
| P54 | ESPI_CS0# / SPI1_CS0# |
| P55 | ~~ESPI_CS1#~~ / SPI1_CS1# |
| P56 | ESPI_CK / SPI1_CK |
| P57 | ESPI_IO_1 / SPI1_DIN |
| P58 | ESPI_IO_0 / SPI1_DO |
| P59 | GND |
| P60 | USB0+ |
| P61 | USB0- |
| P62 | USB0_EN_OC# |
| P63 | USB0_VBUS_DET |

| S-Pin | Secondary (Bottom) Side |
|---|---|
| S33 | ~~PCIE_D_RX-~~ / SERDES_1_RX- |
| S34 | GND |
| S35 | USB4+ |
| S36 | USB4- |
| S37 | ~~USB3_VBUS_DET~~ |
| S38 | AUDIO_MCK |
| S39 | I2S0_LRCK |
| S40 | I2S0_SDOUT |
| S41 | I2S0_SDIN |
| S42 | I2S0_CK |
| S43 | ESPI_ALERT0# |
| S44 | ~~ESPI_ALERT1#~~ |
| S45 | ~~MDIO_CLK~~ |
| S46 | ~~MDIO_DAT~~ |
| S47 | GND |
| S48 | I2C_GP_CK |
| S49 | I2C_GP_DAT |
| S50 | ~~HDA_SYNC~~ / I2S2_LRCK |
| S51 | ~~HDA_SDO~~ / I2S2_SDOUT |
| S52 | ~~HDA_SDI~~ / I2S2_SDIN |
| S53 | ~~HDA_CK~~ / I2S2_CK |
| S54 | ~~SATA_ACT#~~ |
| S55 | ~~USB5_EN_OC#~~ |
| S56 | ~~ESPI_IO_2~~ |
| S57 | ~~ESPI_IO_3~~ |
| S58 | ESPI_RESET# |
| S59 | ~~USB5+~~ |
| S60 | ~~USB5-~~ |
| S61 | GND |
| S62 | USB3_SSTX+ |
| S63 | USB3_SSTX- |
| S64 | GND |

| P-Pin | Primary (Top) Side |
|---|---|
| P64 | USB0_OTG_ID |
| P65 | USB1+ |
| P66 | USB1- |
| P67 | USB1_EN_OC# |
| P68 | GND |
| P69 | USB2+ |
| P70 | USB2- |
| P71 | USB2_EN_OC# |
| P72 | RSVD |
| P73 | RSVD |
| P74 | USB3_EN_OC# |
| | |
| | Key |
| | |
| P75 | PCIE_A_RST# |
| P76 | USB4_EN_OC# |
| P77 | ~~PCIE_B_CKREQ#~~ |
| P78 | ~~PCIE_A_CKREQ#~~ |
| P79 | GND |
| P80 | ~~PCIE_C_REFCK+~~ |
| P81 | ~~PCIE_C_REFCK-~~ |
| P82 | GND |
| P83 | PCIE_A_REFCK+ |
| P84 | PCIE_A_REFCK- |
| P85 | GND |
| P86 | PCIE_A_RX+ |
| P87 | PCIE_A_RX- |
| P88 | GND |
| P89 | PCIE_A_TX+ |
| P90 | PCIE_A_TX- |
| P91 | GND |
| P92 | HDMI_D2+ / ~~DP1_LANE0+~~ |
| P93 | HDMI_D2- / ~~DP1_LANE0-~~ |
| P94 | GND |
| P95 | HDMI_D1+ / ~~DP1_LANE1+~~ |

| S-Pin | Secondary (Bottom) Side |
|---|---|
| S65 | USB3_SSRX+ |
| S66 | USB3_SSRX- |
| S67 | GND |
| S68 | USB3+ |
| S69 | USB3- |
| S70 | GND |
| S71 | USB2_SSTX+ |
| S72 | USB2_SSTX- |
| S73 | GND |
| S74 | USB2_SSRX+ |
| S75 | USB2_SSRX- |
| | |
| | Key |
| | |
| S76 | PCIE_B_RST# |
| S77 | ~~PCIE_C_RST#~~ |
| S78 | ~~PCIE_C_RX+ / SERDES_2_RX+~~ |
| S79 | ~~PCIE_C_RX- / SERDES_2_RX-~~ |
| S80 | GND |
| S81 | ~~PCIE_C_TX+ / SERDES_2_TX+~~ |
| S82 | ~~PCIE_C_TX- / SERDES_2_TX-~~ |
| S83 | GND |
| S84 | PCIE_B_REFCK+ |
| S85 | PCIE_B_REFCK- |
| S86 | GND |
| S87 | PCIE_B_RX+ |
| S88 | PCIE_B_RX- |
| S89 | GND |
| S90 | PCIE_B_TX+ |
| S91 | PCIE_B_TX- |
| S92 | GND |
| S93 | ~~DP0_LANE0+~~ |
| S94 | ~~DP0_LANE0-~~ |
| S95 | ~~DP0_AUX_SEL~~ |
| S96 | ~~DP0_LANE1+~~ |

| P-Pin | Primary (Top) Side |
|---|---|
| P96 | HDMI_D1- / ~~DP1_LANE1-~~ |
| P97 | GND |
| P98 | HDMI_D0+ / ~~DP1_LANE2+~~ |
| P99 | HDMI_D0- / ~~DP1_LANE2-~~ |
| P100 | GND |
| P101 | HDMI_CK+ / ~~DP1_LANE3+~~ |
| P102 | HDMI_CK- / ~~DP1_LANE3-~~ |
| P103 | GND |
| P104 | HDMI_HPD / ~~DP1_HPD~~ |
| P105 | HDMI_CTRL_CK / ~~DP1_AUX+~~ |
| P106 | HDMI_CTRL_DAT / ~~DP1_AUX-~~ |
| P107 | ~~DP1_AUX_SEL~~ |
| P108 | GPIO0 / CAM0_PWR# |
| P109 | GPIO1 / CAM1_PWR# |
| P110 | GPIO2 / CAM0_RST# |
| P111 | GPIO3 / CAM1_RST# |
| P112 | GPIO4 / ~~HDA_RST#~~ |
| P113 | GPIO5 / ~~PWM_OUT~~ |
| P114 | GPIO6 / ~~TACHIN~~ |
| P115 | GPIO7 |
| P116 | GPIO8 |
| P117 | GPIO9 |
| P118 | GPIO10 |
| P119 | GPIO11 |
| P120 | GND |
| P121 | I2C_PM_CK |
| P122 | I2C_PM_DAT |
| P123 | BOOT_SEL0# |
| P124 | BOOT_SEL1# |
| P125 | BOOT_SEL2# |
| P126 | RESET_OUT# |
| P127 | RESET_IN# |
| P128 | POWER_BTN# |
| P129 | SER0_TX |
| P130 | SER0_RX |

| S-Pin | Secondary (Bottom) Side |
|---|---|
| S97 | ~~DP0_LANE1-~~ |
| S98 | ~~DP0_HPD~~ |
| S99 | ~~DP0_LANE2+~~ |
| S100 | ~~DP0_LANE2-~~ |
| S101 | GND |
| S102 | ~~DP0_LANE3+~~ |
| S103 | ~~DP0_LANE3-~~ |
| S104 | USB3_OTG_ID |
| S105 | ~~DP0_AUX+~~ |
| S106 | ~~DP0_AUX-~~ |
| S107 | ~~LCD1_BKLT_EN~~ |
| S108 | LVDS1_CK+/~~eDP1_AUX+/ DSI1_CLK+~~ |
| S109 | LVDS1_CK- / ~~eDP1_AUX- / DSI1_CLK-~~ |
| S110 | GND |
| S111 | LVDS1_0+ / ~~eDP1_TX0+ / DSI1_D0+~~ |
| S112 | LVDS1_0- / ~~eDP1_TX0- / DSI1_D0-~~ |
| S113 | eDP1_HPD / ~~DSI1_TE~~ |
| S114 | LVDS1_1+ / ~~eDP1_TX1+ / DSI1_D1+~~ |
| S115 | LVDS1_1- / ~~eDP1_TX1- / DSI1_D1-~~ |
| S116 | LCD1_VDD_EN |
| S117 | LVDS1_2+ / ~~eDP1_TX2+ / DSI1_D2+~~ |
| S118 | LVDS1_2- / ~~eDP1_TX2- / DSI1_D2-~~ |
| S119 | GND |
| S120 | LVDS1_3+ / ~~eDP1_TX3+ / DSI1_D3+~~ |
| S121 | LVDS1_3- / ~~eDP1_TX3- / DSI1_D3-~~ |
| S122 | ~~LCD1_BKLT_PWM~~ |
| S123 | ~~GPIO13~~ |
| S124 | GND |
| S125 | LVDS0_0+ / ~~eDP0_TX0+~~ / DSI0_D0+ |
| S126 | LVDS0_0- / ~~eDP0_TX0-~~ / DSI0_D0- |
| S127 | LCD0_BKLT_EN |
| S128 | LVDS0_1+ / ~~eDP0_TX1+~~ / DSI0_D1+ |
| S129 | LVDS0_1- / ~~eDP0_TX1-~~ / DSI0_D1- |
| S130 | GND |
| S131 | LVDS0_2+/~~eDP0_TX2+~~/ DSI0_D2+ |

| P-Pin | Primary (Top) Side |
|---|---|
| P131 | SER0_RTS# |
| P132 | SER0_CTS# |
| P133 | GND |
| P134 | SER1_TX |
| P135 | SER1_RX |
| P136 | ~~SER2_TX~~ |
| P137 | ~~SER2_RX~~ |
| P138 | ~~SER2_RTS#~~ |
| P139 | ~~SER2_CTS#~~ |
| P140 | SER3_TX |
| P141 | SER3_RX |
| P142 | GND |
| P143 | CAN0_TX |
| P144 | CAN0_RX |

| S-Pin | Secondary (Bottom) Side |
|---|---|
| S132 | LVDS0_2- / ~~eDP0_TX2-~~ / DSI0_D2- |
| S133 | LCD0_VDD_EN |
| S134 | LVDS0_CK+/~~eDP0_AUX~~/ DSI0_CLK+ |
| S135 | LVDS0_CK-/~~eDP0_AUX-~~/ DSI0_CLK- |
| S136 | GND |
| S137 | LVDS0_3+ / ~~eDP0_TX3+~~ / DSI0_D3+ |
| S138 | LVDS0_3- / ~~eDP0_TX3-~~ / DSI0_D3- |
| S139 | I2C_LCD_CK |
| S140 | I2C_LCD_DAT |
| S141 | LCD0_BKLT_PWM |
| S142 | ~~GPIO12~~ |
| S143 | GND |
| S144 | ~~eDP0_HPD~~ / ~~DSI0_TE~~ |
| S145 | WDT_TIME_OUT# |

| P-Pin | Primary (Top) Side |
|---|---|
| P145 | ~~CAN1_TX~~ |
| P146 | ~~CAN1_RX~~ |
| P147 | VDD_IN |
| P148 | VDD_IN |
| P149 | VDD_IN |
| P150 | VDD_IN |
| P151 | VDD_IN |
| P152 | VDD_IN |
| P153 | VDD_IN |
| P154 | VDD_IN |
| P155 | VDD_IN |
| P156 | VDD_IN |
| | |
| | |

| S-Pin | Secondary (Bottom) Side |
|---|---|
| S146 | PCIE_WAKE# |
| S147 | ~~VDD_RTC~~ |
| S148 | LID# |
| S149 | SLEEP# |
| S150 | VIN_PWR_BAD# |
| S151 | CHARGING# |
| S152 | CHARGER_PRSNT# |
| S153 | CARRIER_STBY# |
| S154 | CARRIER_PWR_ON |
| S155 | FORCE_RECOV# |
| S156 | BATLOW# |
| S157 | TEST# |
| S158 | GND |
| | |

**Note 1**: Secondary LAN (GBE1) is available as a build option, it will occupy the PCIE_B port

**Note 2**: SPI0 is occupied by CAN+FD controller, SPI0 can be freed up by build option losing CAN+FD function, only CS0 available

**Note 3**: DSI0 is occupied by a DSI to LVDS0/1 bridge, DSI0 can be freed up by build option losing LVDS function

## 4.2 Signal Terminology Descriptions

Meaning of the terms used for signal description tables

| Term | Description |
|---|---|
| I | Input to the module |
| O | Output from the module |
| O OD | Open drain output from the module |
| I OD | Open drain input to the module, with mandatory PU (pull up) on module |
| OD | Open drain |
| I/O | Bi-directional Input/Output |
| PU | PU (pull-up) resistor on module |
| PD | PD (pull-down) resistor on module |
| VDD_IN | Main power source from carrier to module |
| CMOS | Logic input or output |
| GBE MDI | Differential analog signaling for Gigabit Media Dependent Interface |
| LVDS DP | Low Voltage Differential Signal for DisplayPort interface |
| LVDS D-PHY | Low Voltage Differential Signal for MIPI CSI-2 cameras and DSI displays |
| LVDS M-PHY | Low Voltage Differential Signal for MIPI CSI-3 cameras |
| LVDS LCD | Low Voltage Differential Signal for LCD displays |
| LVDS PCIE | Low Voltage Differential Signal for PCIe |
| LVDS SATA | Low Voltage Differential Signal for SATA |
| TMDS HDMI | Transition Minimized Differential Signal for HDMI displays |
| USB | DC coupled differential signaling for traditional (non-Superspeed) USB signals |
| USB SS | Differential signal for SuperSpeed USB signals |
| USB VBUS 5V | 5V tolerant input for USB VBUS detection |
| 3.3V | 3.3V Power Domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high) |
| 1.8V | 1.8V Power Domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high) |
| 3.3Vsb | 3.3V Power Domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#) |
| 1.8Vsb | 1.8V Power Domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#) |

## 4.3 Signal Description by function

### 4.3.1 The First Display Interface

The first display interface is a group of 30-pins that is split into a channel 0 and channel 1. The SMARC specification allows to support either dual channel LVDS ports, 2 separate single channel LVDS ports, 2 MIPI DSI ports of 4 lanes each or 2 eDP ports 4 lanes each. A mix of different display type such as DSI and eDP is also permitted. Below tables show which display ports are supported on this particular module

| Pin # | LVDS Name | MIPI DSI Name | eDP Name |
|---|---|---|---|
| S125 | LVDS0_0+ | DSI0_D0+ | ~~eDP0_TX0+~~ |
| S126 | LVDS0_0- | DSI0_D0- | ~~eDP0_TX0-~~ |
| S128 | LVDS0_1+ | DSI0_D1+ | ~~eDP0_TX1+~~ |
| S129 | LVDS0_1 - | DSI0_D1- | ~~eDP0_TX1-~~ |
| S131 | LVDS0_2+ | DSI0_D2+ | ~~eDP0_TX2+~~ |
| S132 | LVDS0_2- | DSI0_D2- | ~~eDP0_TX2-~~ |
| S137 | LVDS0_3+ | DSI0_D3+ | ~~eDP0_TX3+~~ |
| S138 | LVDS0_3- | DSI0_D3- | ~~eDP0_TX3-~~ |
| S134 | LVDS0_CK+ | DSI0_CLK+ | ~~eDP0_AUX+~~ |
| S135 | LVDS0_CK- | DSI0_CLK- | ~~eDP0_AUX-~~ |
| S133 | LCD0_VDD_EN | LCD0_VDD_EN | ~~LCD0_VDD_EN~~ |
| S127 | LCD0_BKLT_EN | LCD0_BKLT_EN | ~~LCD0_BKLT_EN~~ |
| S141 | LCD0_BKLT_PWM | LCD0_BKLT_PWM | ~~LCD0_BKLT_PWM~~ |
| S144 | | DSI0_TE | ~~eDP0_HPD~~ |
| S139 | I2C_LCD_CK | I2C_LCD_CK | ~~I2C_LCD_CK~~ |
| S140 | I2C_LCD_DAT | I2C_LCD_DAT | ~~I2C_LCD_DAT~~ |

| Pin # | LVDS Name | MIPI DSI Name | eDP Name |
|---|---|---|---|
| S111 | LVDS1_0+ | ~~DSI1_D0+~~ | ~~eDP1_TX0+~~ |
| S112 | LVDS1_0- | ~~DSI1_D0-~~ | ~~eDP1_TX0-~~ |
| S114 | LVDS1_1+ | ~~DSI1_D1+~~ | ~~eDP1_TX1+~~ |
| S115 | LVDS1_1 - | ~~DSI1_D1-~~ | ~~eDP1_TX1-~~ |
| S117 | LVDS1_2+ | ~~DSI1_D2+~~ | ~~eDP1_TX2+~~ |
| S118 | LVDS1_2- | ~~DSI1_D2-~~ | ~~eDP1_TX2-~~ |
| S120 | LVDS1_3+ | ~~DSI1_D3+~~ | ~~eDP1_TX3+~~ |
| S121 | LVDS1_3- | ~~DSI1_D3-~~ | ~~eDP1_TX3-~~ |
| S108 | LVDS1_CK+ | ~~DSI1_CLK+~~ | ~~eDP1_AUX+~~ |
| S109 | LVDS1_CK- | ~~DSI1_CLK-~~ | ~~eDP1_AUX-~~ |
| S116 | ~~LCD1_VDD_EN~~ | ~~LCD1_VDD_EN~~ | ~~LCD1_VDD_EN~~ |
| S107 | ~~LCD1_BKLT_EN~~ | ~~LCD1_BKLT_EN~~ | ~~LCD1_BKLT_EN~~ |
| S122 | ~~LCD1_BKLT_PWM~~ | ~~LCD1_BKLT_PWM~~ | ~~LCD1_BKLT_PWM~~ |
| S113 | | ~~DSI1_TE~~ | ~~eDP1_HPD~~ |

**Note** : LVDS0/LVDS1 are standard supported through a DSI to LVDS bridge on the module

**Note** : DSI0 can be freed up by build option, disabling the LVDS0/LVDS1 ports

#### 4.3.1.1 LVDS0/LVDS1 mode

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| LVDS0_0+<br>LVDS0_0-<br>LVDS0_1+<br>LVDS0_1 -<br>LVDS0_2+<br>LVDS0_2-<br>LVDS0_3+<br>LVDS0_3- | S125<br>S126<br>S128<br>S129<br>S131<br>S132<br>S137<br>S138 | Primary LVDS channel differential pair data lines | O LVDS LCD | | Runtime | | |
| LVDS0_CK+<br>LVDS0_CK- | S134<br>S135 | Primary LVDS channel differential pair clock lines | O LVDS LCD | | Runtime | | |
| LCD0_VDD_EN | S133 | Primary LVDS channel power enable, active high | O CMOS | 1.8V | Runtime | | |
| LCD0_BKLT_EN | S127 | Primary LVDS channel backlight enable, active high | O CMOS | 1.8V | Runtime | | |
| LCD0_BKLT_PWM | S141 | Primary LVDS channel brightness control through pulse width modulation (PWM) | O CMOS | 1.8V | Runtime | | |
| LVDS1_0+<br>LVDS1_0-<br>LVDS1_1+<br>LVDS1_1 -<br>LVDS1_2+<br>LVDS1_2-<br>LVDS1_3+<br>LVDS1_3- | S111<br>S112<br>S114<br>S115<br>S117<br>S118<br>S120<br>S121 | Secondary LVDS channel differential pair data lines | O LVDS LCD | | Runtime | | |
| LVDS1_CK+<br>LVDS1_CK- | S108<br>S109 | Secondary LVDS channel differential pair clock lines. | O LVDS LCD | | Runtime | | |
| LCD1_VDD_EN | S116 | Secondary panel power enable, active high | O CMOS | 1.8V | Runtime | | |
| LCD1_BKLT_EN | S107 | Secondary panel backlight enable, active high | O CMOS | 1.8V | Runtime | | |
| LCD1_BKLT_PWM | S122 | Secondary panel brightness control through pulse width modulation (PWM) | O CMOS | 1.8V | Runtime | | |

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| I2C_LCD_DAT | S140 | DDC data line used for flat panel detection and control | I/O OD CMOS | 1.8V | Runtime | PU 2k2 | |
| I2C_LCD_CK | S139 | DDC clock line used for flat panel detection and control | O OD CMOS | 1.8V | Runtime | PU 2k2 | |

#### 4.3.1.2 DSI mode (build option)

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| DSI0_D0+<br>DSI0_D0-<br>DSI0_D1+<br>DSI0_D1-<br>DSI0_D2+<br>DSI0_D2-<br>DSI0_D3+<br>DSI0_D3- | S125<br>S126<br>S128<br>S129<br>S131<br>S132<br>S137<br>S138 | Primary DSI panel differential pair data lines | O LVDS D-PHY | | Runtime | | Build option |
| DSI0_CLK+<br>DSI0_CLK- | S134<br>S135 | Primary DSI panel differential pair clock lines. | O LVDS D-PHY | | Runtime | | Build option |
| LCD0_VDD_EN | S133 | Primary panel power enable, active high | O CMOS | 1.8V | Runtime | | |
| LCD0_BKLT_EN | S127 | Primary panel backlight enable, active high | O CMOS | 1.8V | Runtime | | |
| LCD0_BKLT_PWM | S141 | Primary panel brightness control through pulse width modulation (PWM) | O CMOS | 1.8V | Runtime | | |
| DSI0_TE | S144 | Primary DSI panel tearing effect sigal | I CMOS | 1.8V | Runtime | | |
| I2C_LCD_DAT | S140 | DDC data line used for flat panel detection and control | I/O OD CMOS | 1.8V | Runtime | PU 2k2 | |
| I2C_LCD_CK | S139 | DDC clock line used for flat panel detection and control | O OD CMOS | 1.8V | Runtime | PU 2k2 | |

### 4.3.2 Second & Third Display Interface

| Pin # | HDMI signal names | DP++ signal names |
|---|---|---|
| P92 | HDMI_D2+ | ~~DP1_LANE0+~~ |
| P93 | HDMI_D2- | ~~DP1_LANE0-~~ |
| P95 | HDMI_D1+ | ~~DP1_LANE1+~~ |
| P96 | HDMI_D1- | ~~DP1_LANE1-~~ |
| P98 | HDMI_D0+ | ~~DP1_LANE2+~~ |
| P99 | HDMI_D0- | ~~DP1_LANE2-~~ |
| P101 | HDMI_CK+ | ~~DP1_LANE3+~~ |
| P102 | HDMI_CK- | ~~DP1_LANE3-~~ |
| S105 | HDMI_CTRL_CK | ~~DP1_AUX+~~ |
| S106 | HDMI_CTRL_DAT | ~~DP1_AUX-~~ |
| P104 | HDMI_HPD | ~~DP1_HPD~~ |
| P107 | - | ~~DP1_AUX_SEL~~ |

| Pin # | DP++ signal names |
|---|---|
| P92 | ~~DP0_LANE0+~~ |
| P93 | ~~DP0_LANE0-~~ |
| P95 | ~~DP0_LANE1+~~ |
| P96 | ~~DP0_LANE1-~~ |
| P98 | ~~DP0_LANE2+~~ |
| P99 | ~~DP0_LANE2-~~ |
| P101 | ~~DP0_LANE3+~~ |
| P102 | ~~DP0_LANE3-~~ |
| S105 | ~~DP0_AUX+~~ |
| S106 | ~~DP0_AUX-~~ |
| P104 | ~~DP0_HPD~~ |
| P107 | ~~DP0_AUX_SEL~~ |

**Note**: DisplayPort is not supported on both second and third display interface

#### 4.3.2.1 HDMI

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| HDMI_D2+<br>HDMI_D2-<br>HDMI_D1+<br>HDMI_D1-<br>HDMI_D0+<br>HDMI_D0- | P92<br>P93<br>P95<br>P96<br>P98<br>P99 | HDMI port, differential pair data lines | O TMDS HDMI | | Runtime | | AC coupled off module |
| HDMI_CK+<br>HDMI_CK- | P101<br>P102 | HDMI port, differential pair clock lines | O TMDS HDMI | | Runtime | | AC coupled off module |
| HDMI_CTRL_CK | P105 | I2C_CLK line dedicated to HDMI | O OD COMS | 1.8V | Runtime | PU 2.2 | Level shifter FET and 5V PU resistor shall be placed between the module and the HDMI connector. |
| HDMI_CTRL_DAT | P106 | I2C_DAT line dedicated to HDMI | I/O OD COMS | 1.8V | Runtime | PU 2.2K | Level shifter FET and 5V PU resistor shall be placed between the module and the HDMI connector. |
| HDMI_HPD | P104 | HDMI Hot plug active high detection signal that serves as an interrupt request | I CMOS | 1.8V | Standby | | Module must tolerate high level in stand-by mode |

### 4.3.3 MIPI Camera support

#### 4.3.3.1 MIPI CSI0

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| CSI0_RX0+<br>CSI0_RX0-<br>CSI0_RX1+<br><br>CSI0_RX1- | S11<br>S12<br>S14<br>S15 | CSI0 differential input (point to point) | I LVDS D-PHY / I LVDS M-PHY | | Runtime | | |
| CSI0_CK+<br>CSI0_CK- | S8<br>S9 | CSI0 differential clock intput (point to point) | I LVDS D-PHY | | Runtime | | |
| I2C_CAM0_DAT / ~~CSI0_TX-~~ | S7 | I2C data for serial camera data support link or differential data lane | I/O OD CMOS / O LVDS M-PHY | 1.8V | Runtime | PU 2.2K | MIPI-CSI 2.0 uses I2C_CAM0_DAT<br>MIPI-CSI 3.0 uses CSI0_TX- |
| I2C_CAM0_CK / ~~CSI0_TX+~~ | S5 | I2C clock for serial camera data support link or differential data lane | O OD CMOS / O LVDS M-PHY | 1.8V | Runtime | PU 2.2K | MIPI-CSI 2.0 uses I2C_CAM0_CK<br>MIPI-CSI 3.0 uses CSI0_TX+ |
| CAM0_PWR# / GPIO0 | P108 | Camera 0 Power Enable, active low output. | O CMOS | 1.8V | Runtime | | |
| CAM0_RST# / GPIO2 | P110 | Camera 0 reset, active low output | O CMOS | 1.8V | Runtime | | |
| CAM_MCK | S6 | Master clock output | O CMOS | 1.8V | Runtime | | This signal is used by both CSI0 and CSI1 |

#### 4.3.3.2 MIPI CSI1 (Camera)

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| CSI1_RX0+<br>CSI1_RX0-<br>CSI1_RX1+<br>CSI1_RX1-<br>CSI1_RX2+<br>CSI1_RX2-<br>CSI1_RX3+<br>CSI1_RX3- | P7<br>P8<br>P10<br>P11<br>P13<br>P14<br>P16<br>P17 | CSI1 differential input (point to point) | I LVDS D-PHY / I LVDS M-PHY | | Runtime | | |
| CSI1_CK+<br>CSI1_CK- | P3<br>P4 | CSI1 differential clock input (point to point) | I LVDS D-PHY | | Runtime | | |
| I2C_CAM1_DAT / ~~CSI1_TX-~~ | S2 | I2C data for serial camera data support link or differential data lane | I/O OD CMOS / O LVDS M-PHY | 1.8V | Runtime | PU 2.2K | MIPI-CSI 2.0 mode uses I2C_CAM1_DAT<br>MIPI-CSI 3.0 mode uses CSI1_TX- |
| I2C_CAM1_CK / ~~CSI1_TX+~~ | S1 | I2C clock for serial camera data support link or differential data lane | O OD CMOS / O LVDS M-PHY | 1.8V | Runtime | PU 2.2K | MIPI-CSI 2.0 mode uses I2C_CAM1_CK<br>MIPI-CSI 3.0 mode uses CSI1_TX+ |
| CAM1_PWR# / GPIO1 | P109 | Camera 0 Power Enable, active low output. | O CMOS | 1.8V | Runtime | | CAM1_PWR# is default, GPIO1 can be enabled through DVT |
| CAM1_RST# / GPIO3 | P111 | Camera 0 reset, active low output | O CMOS | 1.8V | Runtime | | CAM1_PWR# is default, GPIO3 can be enabled through DVT |
| CAM_MCK | S6 | Master clock output | O CMOS | 1.8V | Runtime | | This signal is used by both CSI0 and CSI1 |

### 4.3.4 I2S (audio)

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| I2S0_LRCK | S39 | I2S0 Left & Right synchronization clock | I/O CMOS | 1.8V | Runtime | | Module Output if CPU acts in Master Mode<br>Module Input if CPU acts in Slave Mode |
| I2S0_SDOUT | S40 | I2S0 Digital audio Output | O CMOS | 1.8V | Runtime | | |
| I2S0_SDIN | S41 | I2S0 Digital audio Input | I CMOS | 1.8V | Runtime | | |
| I2S0_CK | S42 | I2S0 Digital audio clock | I/O CMOS | 1.8V | Runtime | | Module Output if CPU acts in Master Mode<br>Module Input if CPU acts in Slave Mode |
| I2S2_LRCK | S50 | I2S2 Left & Right synchronization clock | I/O CMOS | 1.8V | Runtime | | Module Output if CPU acts in Master Mode<br>Module Input if CPU acts in Slave Mode |
| I2S2_SDOUT | S51 | I2S2 Digital audio Output | O CMOS | 1.8V | Runtime | | |
| I2S2_SDIN | S52 | I2S2 Digital audio Input | I CMOS | 1.8V | Runtime | | |
| I2S2_CK | S53 | I2S2 Digital audio clock | I/O CMOS | 1.8V | Runtime | | Module Output if CPU acts in Master Mode<br>Module Input if CPU acts in Slave Mode |
| AUDIO_MCK | S38 | Master clock output to I2S codec(s) | O CMOS | 1.8V | Runtime | | |

**Note**: support for I2S1 signalling pins has been removed during update to SMARC 2.0 specification

### 4.3.5 USB ports

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| USB0+<br>USB0- | P60<br>P61 | USB differential data pairs for port 0 | I/O<br>USB | USB | Runtime | | From SOC |
| USB0_EN_OC# | P62 | USB over-current sense for port 0 | I/O OD<br>CMOS | 3.3Vsb / 3.3V | Runtime | PU 10k | Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation. |
| USB0_VBUS_DET | P63 | USB port 0 host power detection, when this port is used as a device. | I USB<br>VBUS 5V | USB VBUS 5V | Runtime | | Can be connected to a USB client port VBUS pin |
| USB0_OTG_ID | P64 | Input pin to announce OTG device insertion on USB 2.0 port | I<br>CMOS | 3.3Vsb / 3.3V | Runtime | | |
| USB1+<br>USB1- | P65<br>P66 | USB differential data pairs for port 1 | I/O<br>USB | USB | Runtime | | From USB HUB |
| USB1_EN_OC# | P67 | USB over-current sense for port 1 | I/O OD<br>CMOS | 3.3Vsb / 3.3V | Runtime | PU 10k | Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation. |
| USB2+<br>USB2- | P69<br>P70 | USB differential data pairs for port 2 | I/O<br>USB | USB | Runtime | | From USB HUB |
| USB2_SSRX+<br>USB2_SSRX- | S74<br>S75 | Receive signal differential pairs for SuperSpeed on port 2 | I<br>USB SS | USB SS | Runtime | - | |
| USB2_SSTX+<br>USB2_SSTX- | S71<br>S72 | Transmit signal differential pairs for SuperSpeed on port 2 | O<br>USB SS | USB SS | Runtime | - | |
| USB2_EN_OC# | P71 | USB over-current sense for port 2 | I/O OD<br>CMOS | 3.3Vsb / 3.3V | Runtime | PU 10k | Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation. |
| USB3+<br>USB3- | S68<br>S69 | USB differential data pairs for port 3 | I/O<br>USB | USB | Runtime | | From USB HUB |
| USB3_SSRX+<br>USB3_SSRX- | S65<br>S66 | Receive signal differential pairs for SuperSpeed on port 3 | I<br>USB SS | USB SS | Runtime | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| USB3_SSTX+<br>USB3_SSTX- | S62<br>S63 | Transmit signal differential pairs for SuperSpeed on port 3 | O<br>USB SS | USB SS | Runtime | | |
| USB3_EN_OC# | P74 | USB over-current sense for port 3 | I/O OD<br>CMOS | 3.3Vsb / 3.3V | Runtime | PU 10k | Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation. |
| ~~USB3_VBUS_DET~~ | ~~S37~~ | ~~USB port 3 host power detection, when this port is used as a device.~~ | ~~I<br>USB VBUS 5V~~ | ~~USB VBUS 5V~~ | ~~Runtime~~ | - | - |
| ~~USB3_OTG_ID~~ | ~~S104~~ | ~~Input pin to announce OTG device insertion on USB 3.0 port~~ | ~~I<br>CMOS~~ | ~~3.3Vsb / 3.3V~~ | ~~Runtime~~ | - | - |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| USB4+<br>USB4- | S35<br>S36 | USB differential data pairs for port 4 | I/O<br>USB | USB | Runtime | | |
| USB4_EN_OC# | P76 | USB over-current sense for port 4 | I/O OD<br>CMOS | 3.3Vsb / 3.3V | Runtime | PU 10k | Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation. |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ~~USB5+<br>USB5-~~ | ~~S59<br>S60~~ | ~~USB differential data pairs for port 5~~ | ~~I/O<br>USB~~ | ~~USB~~ | ~~Standby~~ | - | |
| ~~USB5_EN_OC#~~ | ~~S55~~ | ~~USB over-current sense for port 5~~ | ~~I/O OD<br>CMOS~~ | ~~3.3Vsb / 3.3V~~ | ~~Standby~~ | ~~PU 10k~~ | ~~Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.~~ |

**Note**: USB0 is directly connected to the SOC, USB1/2/3/4 have shared bandwidth through a HUB, USB5 is not supported

### 4.3.6 PCIe Ports

The module supports two PCIe Gen 2.1 ports (PCIE_A and PCIE_B).

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| PCIE_A_TX+<br>PCIE_A_TX- | P89<br>P90 | Differential PCIe link A transmit data pair | O LVDS PCIE | | Runtime | | Series AC coupled on module |
| PCIE_A_RX+<br>PCIE_A_RX- | P86<br>P87 | Differential PCIe link A receive data pair | I LVDS PCIE | | Runtime | | Series AC coupled off module |
| PCIE_A_REFCK+<br>PCIE_A_REFCK- | P83<br>P84 | Differential PCIe Link A reference clock output | O LVDS PCIE | | Runtime | | |
| PCIE_A_RST# | P75 | PCIe Port A reset output | O CMOS | 3.3V | Runtime | | |
| ~~PCIE_A_CKREQ#~~ | ~~P78~~ | ~~PCIe Port A clock request~~ | ~~I OD CMOS~~ | ~~3.3V~~ | ~~Runtime~~ | - | No need for this signal because module provides onboard PCIe clock |
| PCIE_B_TX+<br>PCIE_B_TX- | S90<br>S91 | Differential PCIe link B transmit data pair | O LVDS PCIE | | Runtime | | Series AC coupled on module |
| PCIE_B_RX+<br>PCIE_B_RX- | S87<br>S88 | Differential PCIe link B receive data pair | I LVDS PCIE | | Runtime | | Series AC coupled off module |
| PCIE_B_REFCK+<br>PCIE_B_REFCK- | S84<br>S85 | Differential PCIe Link B reference clock output | O LVDS PCIE | | Runtime | | |
| PCIE_B_RST# | S76 | PCIe Port B reset output | O CMOS | 3.3V | Runtime | | |
| ~~PCIE_B_CKREQ#~~ | ~~P77~~ | ~~PCIe Port B clock request~~ | ~~I OD CMOS~~ | ~~3.3V~~ | ~~Runtime~~ | | No need for this signal because module provides onboard PCIe clock |
| ~~PCIE_C_TX+<br>PCIE_C_TX-~~ | ~~S81<br>S82~~ | ~~Differential PCIe link C transmit data pair~~ | ~~O LVDS PCIE~~ | - | ~~Runtime~~ | - | ~~Series AC coupled on module~~ |
| ~~PCIE_C_RX+<br>PCIE_C_RX-~~ | ~~S78<br>S79~~ | ~~Differential PCIe link C receive data pair~~ | ~~I LVDS PCIE~~ | - | ~~Runtime~~ | - | ~~Series AC coupled off module~~ |
| ~~PCIE_C_REFCK+<br>PCIE_C_REFCK-~~ | ~~P80<br>P81~~ | ~~Differential PCIe Link C reference clock output~~ | ~~O LVDS PCIE~~ | - | ~~Runtime~~ | - | - |
| ~~PCIE_C_RST#~~ | ~~S77~~ | ~~PCIe Port C reset output~~ | ~~O CMOS~~ | ~~3.3V~~ | ~~Runtime~~ | - | - |

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| ~~PCIE_D_TX+~~<br>~~PCIE_D_TX-~~ | ~~S29~~<br>~~S30~~ | ~~Differential PCIe link D transmit data pair~~ | ~~O LVDS PCIE~~ | - | ~~Runtime~~ | - | ~~Series AC coupled on module~~ |
| ~~PCIE_D_RX+~~<br>~~PCIE_D_RX-~~ | ~~S32~~<br>~~S33~~ | ~~Differential PCIe link D receive data pair~~ | ~~I LVDS PCIE~~ | - | ~~Runtime~~ | - | ~~Series AC coupled off module~~ |
| PCIE_WAKE# | S146 | PCIe wake up interrupt to host – common to PCIe links A, B, C, D | I OD CMOS | 3.3V | Runtime | PU 10k | |

**Note**: Module provides PCIe clock generators for PCIE_A and PCIE_B so no external clock source on the carrier is needed

**Note**: Second LAN is a build option and will occupy PCIe_B port

### 4.3.7 SATA Ports

This design does not support SATA ports

## 4.3.8 LAN ports

### 4.3.8.1 First LAN port

The first LAN port is derived from the SOCs RGMII interface

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| GBE0_MDI0+<br>GBE0_MDI0-<br>GBE0_MDI1+<br>GBE0_MDI1-<br>GBE0_MDI2+<br>GBE0_MDI2-<br>GBE0_MDI3+<br>GBE0_MDI3- | P30<br>P29<br>P27<br>P26<br>P24<br>P23<br>P20<br>P19 | Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following:<br>1000 / 100 / 10<br>MDI[0]+/- B1_DA+/- TX+/- TX+/-<br>MDI[1]+/- B1_DB+/- RX+/- RX+/-<br>MDI[2]+/- B1_DC+/-<br>MDI[3]+/- B1_DD+/- | GBE MDI | | Runtime | | Twisted pair signals for external transformer. |
| GBE0_LINK100# | P21 | Link Speed Indication LED for GBE 0 100Mbps | O OD CMOS | 3.3V | Runtime | | Shall be able to sink 24mA or more Carrier LED current |
| GBE0_LINK1000# | P22 | Link Speed Indication LED for GBE 0 1000Mbps | O OD CMOS | 3.3V | Runtime | | Shall be able to sink 24mA or more Carrier LED current |
| GBE0_LINK_ACT# | P25 | Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity | O OD CMOS | 3.3V | Runtime | | Shall be able to sink 24mA or more Carrier LED current |
| ~~GBE0_CTREF~~ | ~~P28~~ | ~~Center-Tap reference voltage for Carrier board Ethernet magnetic (if required by the Module GBE PHY)~~ | ~~Analog~~ | ~~0 to 3.3V max~~ | Runtime | - | - |
| GBE0_SDP | P6 | IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol) | IO CMOS | 3.3V | Runtime | | |

#### 4.3.8.2 Second LAN port (optional)

Second LAN port is available as build option and is derived from an Intel i210 controller connected to the PCIE_B port.

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| GBE1_MDI0+<br>GBE1_MDI0-<br>GBE1_MDI1+<br>GBE1_MDI1-<br>GBE1_MDI2+<br>GBE1_MDI2-<br>GBE1_MDI3+<br>GBE1_MDI3- | S17<br>S18<br>S20<br>S21<br>S23<br>S24<br>S26<br>S27 | Gigabit Ethernet Controller 1: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following:<br>1000 100 10<br>MDI[0]+/- B1_DA+/- TX+/- TX+/-<br>MDI[1]+/- B1_DB+/- RX+/- RX+/-<br>MDI[2]+/- B1_DC+/-<br>MDI[3]+/- B1_DD+/- | GBE MDI | | Runtime | | Twisted pair signals for external transformer. |
| GBE1_LINK100# | S19 | Link Speed Indication LED for GBE 1 100Mbps | O OD CMOS | 3.3V | Runtime | | Shall be able to sink 24mA or more Carrier LED current |
| GBE1_LINK1000# | S22 | Link Speed Indication LED for GBE 1 1000Mbps | O OD CMOS | 3.3V | Runtime | | Shall be able to sink 24mA or more Carrier LED current |
| GBE1_LINK_ACT# | S31 | Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity | O OD CMOS | 3.3V | Runtime | | Shall be able to sink 24mA or more Carrier LED current |
| ~~GBE1_CTREF~~ | ~~S28~~ | ~~Center-Tap reference voltage for Carrier board Ethernet magnetic `(if required by the Module GBE PHY)`~~ | ~~Analog~~ | ~~0 to 3.3V max~~ | ~~Runtime~~ | | |
| GBE1_SDP | P5 | IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol) | IO CMOS | 3.3V | Runtime | | |

### 4.3.9 SDIO

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| SDIO_D0<br>SDIO_D1<br>SDIO_D2<br>SDIO_D3 | P39<br>P40<br>P41<br>P42 | SDIO Data lines. These signals operate in push-pull mode. | I/O CMOS | 1.8V or 3.3V | Runtime | | SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly |
| SDIO_WP | P33 | SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards. | I OD CMOS | 3.3V | Runtime | PU 10k | Pulled up on module |
| SDIO_CMD | P34 | SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode. | I/O CMOS | 1.8V or 3.3V | Runtime | | SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly |
| SDIO_CD# | P35 | SDIO Card Detect.<br>This signal indicates when a SDIO/MMC card is present. | I OD CMOS | 3.3V | Runtime | PU 10k | Pulled up on module |
| SDIO_CK | P36 | SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. | O CMOS | 1.8V or 3.3V | Runtime | | |
| SDIO_PWR_EN | P37 | SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device. | O CMOS | 3.3V | Runtime | | should be driven low in STB Mode by the module |

### 4.3.10 SPI & ESPI

### 4.3.11 SPI0

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| SPI0_CS0# | P43 | SPI0 Master Chip Select 0 | O CMOS | 1.8V | Standby | | This signal can be used to select carrier SPI as boot device |
| ~~SPI0_CS1#~~ | P31 | ~~SPI0 Master Chip Select 1~~ | ~~O CMOS~~ | ~~1.8V~~ | ~~Standby~~ | | |
| SPI0_CK | P44 | SPI0 Clock | O CMOS | 1.8V | Standby | | |
| SPI0_DIN | P45 | SPI0 Master input / Slave output | I CMOS | 1.8V | Standby | | also referred to as MISO |
| SPI0_DO | P46 | SPI0 Master output / Slave input | O CMOS | 1.8V | Standby | | also referred to as MOSI |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ~~SPI1_CS0#~~ | ~~P54~~ | ~~SPI1 Master Chip Select 0~~ | ~~O CMOS~~ | ~~1.8V~~ | ~~Standby~~ | - | See ESPI |
| ~~SPI1_CS1#~~ | ~~P55~~ | ~~SPI1 Master Chip Select 1~~ | ~~O CMOS~~ | ~~1.8V~~ | ~~Standby~~ | - | See ESPI |
| ~~SPI1_CK~~ | ~~P56~~ | ~~SPI1 Clock~~ | ~~O CMOS~~ | ~~1.8V~~ | ~~Standby~~ | - | See ESPI |
| ~~SPI1_DIN~~ | ~~P57~~ | ~~SPI1 Master input / Slave output~~ | ~~I CMOS~~ | ~~1.8V~~ | ~~Standby~~ | - | See ESPI |
| ~~SPI1_DO~~ | ~~P58~~ | ~~SPI1 Master output / Slave input~~ | ~~O CMOS~~ | ~~1.8V~~ | ~~Standby~~ | - | See ESPI |

**Note**: SPI0 is free to use on the carrier but support only one device through CS0

SPI1 supports a CAN bus controller on the module through CS0, that leaves CS1 free for a device on the carrier

### 4.3.12 ESPI

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| ESPI_CS0# | P54 | ESPI1 Master Chip Select 0 | O CMOS | 1.8V | Standby | | |
| ~~ESPI_CS1#~~ | P55 | ESPI1 Master Chip Select 1 | O CMOS | 1.8V | Standby | | |
| ESPI_CK | P56 | ESPI Master Clock output | O CMOS | 1.8V | Standby | | |
| ESPI_RESET# | S58 | ESPI Reset | O CMOS | 1.8V | Standby | | Reset the eSPI interface for both master and slaves.<br><br>eSPI Reset# is typically driven from eSPI master to eSPI slaves |
| ESPI_ALERT0#<br>~~ESPI_ALERT1#~~ | S43<br>S44 | ESPI ALERT | I OD CMOS | 1.8V | Standby | | This pin is used by eSPI slave to request service from eSPI.master.Alert# is an open-drain output from the slave.<br>This pin is optional for Single Master-Single Slave configuration where I/O[1] can be used to signal the Alert event. |
| ESPI_IO_0<br>ESPI_IO_1<br>~~ESPI_IO_2~~<br>~~ESPI_IO_3~~ | P58<br>P57<br>~~S56~~<br>~~S57~~ | ESPI Master Data Input / Output. | I/O CMOS | 1.8V | Standby | | ESPI_IO_0 can also be used as SPI1_DO (MOSI)<br>ESPI_IO_1 can also be used as SPI1_DIN (MISO)<br><br>In Single I/O mode, ESPI_IO_0 is the eSPI master output / eSPI slave input (MOSI) whereas ESPI_IO_1 is the SPI master input / eSPI slave output (MISO). |

**Note**: On NXP i.MX8M parts ECSPI is used (Enhanced Configurable Serial Peripheral Interface)

## 4.4 General Purpose I2C

The SMARC specification supports a total of 6 different I2C busses on its pinout. Most of these busses are designated for specific functions such as I2C for camera management, I2C for EDID on HDMI, LVDS panels or I2C for PMIC. Just one I2C bus is marked as General purpose

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| I2C_GP_DAT | S49 | General purpose I2C data signal | I/O OD CMOS | 1.8V | Runtime | PU 2k2 | |
| I2C_GP_CK | S48 | General purpose I2C clock signal | O OD CMOS | 1.8V | Runtime | PU 2k2 | |

Most of the other I2C busses are described in their designated function tables rather than in a single big list.

Below is an overview of all I2C busses and where to find them.

| Name | Pin # | Description | Where to find |
|---|---|---|---|
| I2C_LCD_DAT | S140 | DDC data line used for flat panel detection and control | LVDS / DSI / eDP tables |
| I2C_LCD_CK | S139 | DDC clock line used for flat panel detection and control | LVDS / DSI / eDP tables |
| HDMI_CTRL_CK | P105 | I2C_CLK line dedicated to HDMI | HDMI table |
| HDMI_CTRL_DAT | P106 | I2C_DAT line dedicated to HDMI | HDMI table |
| I2C_CAM0_DAT | S7 | I2C data for serial camera data support link | MIPI CSI table |
| I2C_CAM0_CK | S5 | I2C clock for serial camera data support link | MIPI CSI table |
| I2C_CAM1_DAT | S2 | I2C data for serial camera data support link | MIPI CSI table |
| I2C_CAM1_CK | S1 | I2C clock for serial camera data support link | MIPI CSI table |
| I2C_PM_DAT | P122 | Power management I2C bus DATA (SMBus for x86) | Power and System Management |
| I2C_PM_CK | P121 | Power management I2C bus CLK (SMBus for x86) | Power and System Management |

### 4.4.1 GPIO

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| GPIO0 / CAM0_PWR# | P108 | General purpose I/O pin 0. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module. | Default use is GPIO0, alternative use is Camera 0 Power Enable - active low, through DTS |
| GPIO1 / CAM1_PWR# | P109 | General purpose I/O pin 1. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | Default use is is GPIO1 alternative use is Camera 1 Power Enable - active low, through DTS |
| GPIO2 / CAM0_RST# | P110 | General purpose I/O pin 2. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | Default use is GPIO2, alternative use is Camera 0 Reset - active low, through DTS |
| GPIO3 / CAM1_RST# | P111 | General purpose I/O pin 3. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | Default use is GPIO3, alternative use is Camera 1 Reset - active low, through DTS |
| GPIO4 / ~~HDA_RST#~~ | P112 | General purpose I/O pin 4. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | |
| GPIO5 / ~~PWM_OUT~~ | P113 | General purpose I/O pin 5. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | |
| GPIO6 | P114 | General purpose I/O pin 6. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | |
| GPIO7 | P115 | General purpose I/O pin 7. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | |
| GPIO8 | P116 | General purpose I/O pin 8. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | |
| GPIO9 | P117 | General purpose I/O pin 9. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | |
| GPIO10 | P118 | General purpose I/O pin 10. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | |
| GPIO11 | P119 | General purpose I/O pin 11. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | |
| ~~GPIO12~~ | ~~S142~~ | ~~General purpose I/O pin 12~~ | ~~I/O CMOS~~ | ~~1.8V~~ | ~~Runtime~~ | ~~PU 470K on the Module~~ | |
| ~~GPIO13~~ | ~~S123~~ | ~~General purpose I/O pin 13~~ | ~~I/O CMOS~~ | ~~1.8V~~ | ~~Runtime~~ | ~~PU 470K on the Module~~ | |

### 4.4.2 UART

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| SER0_TX | P129 | Asynchronous serial data output port 0 | O CMOS | 1.8V | Runtime | | |
| SER0_RX | P130 | Asynchronous serial data input port 0 | I CMOS | 1.8V | Runtime | | |
| SER0_RTS# | P131 | "Request to Send" handshake line for port 0 | O CMOS | 1.8V | Runtime | | |
| SER0_CTS# | P132 | "Clear to Send" handshake line for port 0 | I CMOS | 1.8V | Runtime | | |
| SER1_TX | P134 | Asynchronous serial data output port 1 | O CMOS | 1.8V | Runtime | | |
| SER1_RX | P135 | Asynchronous serial data input port 1 | I CMOS | 1.8V | Runtime | | |
| ~~SER2_TX~~ | ~~P136~~ | ~~Asynchronous serial data output port 2~~ | ~~O CMOS~~ | ~~1.8V~~ | ~~Runtime~~ | - | - |
| ~~SER2_RX~~ | ~~P137~~ | ~~Asynchronous serial data input port 2~~ | ~~I CMOS~~ | ~~1.8V~~ | ~~Runtime~~ | - | - |
| ~~SER2_RTS#~~ | ~~P138~~ | ~~"Request to Send" handshake line for port 2~~ | ~~O CMOS~~ | ~~1.8V~~ | ~~Runtime~~ | - | - |
| ~~SER2_CTS#~~ | ~~P139~~ | ~~"Clear to Send" handshake line for port 2~~ | ~~I CMOS~~ | ~~1.8V~~ | ~~Runtime~~ | - | - |
| SER3_TX | P140 | Asynchronous serial data output port 3 | O CMOS | 1.8V | Runtime | | |
| SER3_RX | P141 | Asynchronous serial data input port 3 | I CMOS | 1.8V | Runtime | | |

### 4.4.3 CAN bus

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| CAN0_TX | P143 | CAN port 0 Transmit output | O CMOS | 1.8V | Runtime | | |
| CAN0_RX | P144 | CAN port 0 Receive input | I CMOS | 1.8V | Runtime | | |
| ~~CAN1_TX~~ | P145 | ~~CAN port 1 Transmit output~~ | ~~O CMOS~~ | ~~1.8V~~ | ~~Runtime~~ | | |
| ~~CAN1_RX~~ | P146 | ~~CAN port1 Receive input~~ | ~~I CMOS~~ | ~~1.8V~~ | ~~Runtime~~ | | |

### 4.4.4 Miscellaneous

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| TEST# | S157 | Held low by Carrier to invoke Module vendor specific test function(s). | I CMOS | 1.8V | Runtime | PU on Module. Driven by OD on Carrier | Module must implement PU but actual value is depended on particular module design. Carrier Board should leave this pin floating for normal operation |
| WDT_TIME_OUT# | S145 | Watch-Dog-Timer Output, low active. | O CMOS | 1.8V | Runtime | | Driven only during runtime |

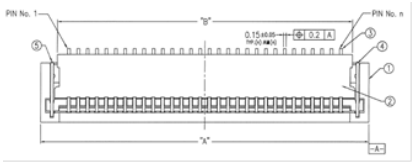
### 4.4.5 Power and System Management

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| BATLOW# | S156 | Battery low indication to Module. Carrier to float the line in inactive state. | I OD CMOS | 1.8V | Runtime | PU 10K | Driven by OD on Carrier.<br>Pulled up on module. |
| CARRIER_PWR_ON | S154 | Carrier board circuits (apart from power management and power path circuits) should not be powered up until the Module asserts the CARRIER_PWR_ON signal. | O CMOS | 1.8Vsb / 1.8V | - | | 1.8Vsb is only used for signaling, not a power source to the module |
| CARRIER_STBY# | S153 | The Module shall drive this signal low when the system is in a standby power state. | O CMOS | 1.8Vsb / 1.8V | - | | |
| CHARGER_PRSNT# | S152 | Held low by Carrier if DC input for battery charger is present. | I OD CMOS | 1.8V | Runtime | PU 4.7K | Driven by OD on Carrier.<br>Pulled up on module. |
| CHARGING# | S151 | Held low by Carrier during battery charging. Carrier to float the line when charge is complete. | I OD CMOS | 1.8V | Runtime | PU 4.7K | Driven by OD on Carrier.<br>Pulled up on module. |
| VIN_PWR_BAD# | S150 | Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) shall not be enabled while this signal is held low by the Carrier. | I OD CMOS | 1.8V | Runtime | PU 2.2K | Driven by OD on Carrier<br>Module must implement PU but actual value is depended on particular module design. |
| SLEEP# | S149 | Sleep indicator from Carrier board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state.Active low, level sensitive. Should be de-bounced on the Module. | I OD CMOS | 1.8V | Runtime | PU 4.7K | Driven by OD on Carrier.<br>Pulled up on module. |
| LID# | S148 | Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module. | I OD CMOS | 1.8V | Runtime | PU 4.7K | Driven by OD on Carrier.<br>Pulled up on module. |
| POWER_BTN# | P128 | Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module. | I OD CMOS | 1.8V | Runtime | PU 4.7K | Driven by OD on Carrier.<br>Pulled up on module. |
| RESET_OUT# | P126 | General purpose reset output to Carrier board. | O CMOS | 1.8V | Runtime | | |

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| RESET_IN# | P127 | Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise. | I OD CMOS | 1.8V | Runtime | PU 4.7K | Driven by OD on Carrier. Pulled up on module. |
| I2C_PM_DAT | P122 | Power management I2C bus DATA | I/O OD CMOS | 1.8V | Runtime | PU 2k2 | On x86 systems these serve as SMB DATA. Pulled up on module. |
| I2C_PM_CK | P121 | Power management I2C bus CLK | O OD CMOS | 1.8V | Runtime | PU 2k2 | On x86 systems these serve as SMB CLK. Pulled up on module. |
| ~~SMB_ALERT_1V8#~~ | P1 | ~~SMBus Alert# (interrupt) signal~~ | ~~I OD CMOS~~ | ~~1.8V~~ | ~~Runtime~~ | ~~PU 2k2~~ | ~~only used on x86 design~~ |

### 4.4.6 DB30 Multipurpose Connector

- **FPC Connector type :** HIROSE,FH12-30S-0.5SH(55)



DB30 connector brings out the following type of signals

**SPI0 bus**

**JTAG to SOC**

**Boot Select strap pins**

**BMC programming interface**

**Serial port**

### 4.4.7 Boot Select

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| BOOT_SEL0#<br>BOOT_SEL1#<br>BOOT_SEL2# | P123<br>P124<br>P125 | Input straps determine the Module boot | I OD CMOS | 1.8Vsb | Standby | PU 4.7K | Driven by OD on Carrier.<br>Pulled up on module.<br><br>Only booting from EMMc and SDcard is supported |
| ~~FORCE_RECOV#~~ | S155 | | ~~I OD CMOS~~ | ~~1.8Vsb~~ | ~~Standby~~ | ~~PU 10K~~<br>- | ~~Driven by OD on Carrier.~~<br>~~Pulled up on module.~~<br><br>~~Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based Force Recovery functions, then a low on the Module FORCE_RECOV# pin may invoke the SOC native Force Recovery mode – such as over a Serial Port. For x86 systems this signal may be used to load BIOS defaults. Pulled up on Module. Driven by OD part on Carrier.~~ |

### 4.4.8 Power

| Name | Pin # | Description | I/O Type | Power Rail / Tolerance | PU / PD | Comments |
|---|---|---|---|---|---|---|
| VDD_IN | P147, P148, P149, P150, P151, P152, P153, P154, P155, P156 | Module power input voltage 4.75 min to 5.25V max | P Not defined within Signal Terminolgy Descriptions. Should we define a specific rail? | 3 to 5.25V / 5V | | |
| GND | P2, P9, P12, P15, P18, P32, P38, P47, P50, P53, P59, P68, P79, P82, P85, P88, P91, P94, P97, P100, P103, P120, P133, P142, S3, S10, S16, S25, S34, S47, S61, S64, S67, S70, S73, S80, S83, S86, S89, S92, S101, S110, S119, S124, S130, S136, S143, S158 | Module signal and power return, and GND reference | P Not defined within Signal Terminolgy Descriptions. Should we define a specific rail? | Ground | | |
| ~~VDD_RTC~~ | ~~S147~~ | ~~Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based Lithium cell or Super Cap.~~ | ~~P Not defined within Signal Terminolgy Descriptions. Should we define a specific rail?~~ | [2 to 3.25] / 3.25V | | |

## 4.5 SMARC pin to controller mapping

| Pin | SMARC Signal Name | Module Direction | Module Termination | Type/Tolerance | Controller | Controller Pin Name | I/O Mux default | Power Rail |
|---|---|---|---|---|---|---|---|---|
| P1 | SMB_ALERT_1V8# | - | - | - | N.C. | N.C. | _ | - |
| P2 | GND | - | - | - | - | - | _ | - |
| P3 | CSI1_CK+ | In | - | LVDS D-PHY | i.MX8M | MIPI_CSI2_CLK_P | _ | MIPI_VDDHA |
| P4 | CSI1_CK- | In | - | LVDS D-PHY | i.MX8M | MIPI_CSI2_CLK_N | _ | MIPI_VDDHA |
| P5 | GBE1_SDP | Out | - | GPIO/3.3V | I210 | SPD0 | | |
| P6 | GBE0_SDP | Out | - | GPIO/3.3V | DP83867 | CLK_OUT | | |
| P7 | CSI1_RX0+ | In | - | LVDS D-PHY | i.MX8M | MIPI_CSI2_D0_P | _ | MIPI_VDDHA |
| P8 | CSI1_RX0- | In | - | LVDS D-PHY | i.MX8M | MIPI_CSI2_D0_N | _ | MIPI_VDDHA |
| P9 | GND | - | - | - | - | - | | |
| P10 | CSI1_RX1+ | In | - | LVDS D-PHY | i.MX8M | MIPI_CSI2_D1_P | _ | MIPI_VDDHA |
| P11 | CSI1_RX1- | In | - | LVDS D-PHY | i.MX8M | MIPI_CSI2_D1_N | _ | MIPI_VDDHA |
| P12 | GND | - | - | - | - | - | | |
| P13 | CSI1_RX2+ | In | - | LVDS D-PHY | i.MX8M | MIPI_CSI2_D2_P | _ | MIPI_VDDHA |
| P14 | CSI1_RX2- | In | - | LVDS D-PHY | i.MX8M | MIPI_CSI2_D2_N | _ | MIPI_VDDHA |
| P15 | GND | - | - | - | - | - | | |
| P16 | CSI1_RX3+ | In | - | LVDS D-PHY | i.MX8M | MIPI_CSI2_D3_P | _ | MIPI_VDDHA |
| P17 | CSI1_RX3- | In | - | LVDS D-PHY | i.MX8M | MIPI_CSI2_D3_N | _ | MIPI_VDDHA |
| P18 | GND | - | - | - | - | - | _ | - |
| P19 | GBE0_MDI3- | Bi-Dir | - | GBE MDI | DP83867 | TD_M_D | _ | VDDIO |
| P20 | GBE0_MDI3+ | Bi-Dir | - | GBE MDI | DP83867 | TD_P_D | _ | VDDIO |
| P21 | GBE0_LINK100# | Out/OD | - | GPIO / 3.3V | DP83867 | LED_1 | _ | VDDIO |
| P22 | GBE0_LINK1000# | Out/OD | - | GPIO / 3.3V | DP83867 | LED_2 | _ | VDDIO |
| P23 | GBE0_MDI2- | Bi-Dir | - | GBE MDI | DP83867 | TD_M_C | _ | VDDIO |
| P24 | GBE0_MDI2+ | Bi-Dir | - | GBE MDI | DP83867 | TD_P_C | _ | VDDIO |
| P25 | GBE0_LINK_ACT# | Out/OD | - | GPIO / 3.3V | DP83867 | LED_0 | _ | VDDIO |
| P26 | GBE0_MDI1- | Bi-Dir | - | GBE MDI | DP83867 | TD_M_B | _ | VDDIO |
| P27 | GBE0_MDI1+ | Bi-Dir | - | GBE MDI | DP83867 | TD_P_B | _ | VDDIO |
| P28 | GBE0_CTREF | PWR | - | - | - | - | _ | - |
| P29 | GBE0_MDI0- | Bi-Dir | - | GBE MDI | DP83867 | TD_M_A | _ | VDDIO |
| P30 | GBE0_MDI0+ | Bi-Dir | - | GBE MDI | DP83867 | TD_P_A | _ | VDDIO |
| P31 | SPI0_CS1# | - | - | - | N.C. | N.C. | _ | - |

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|---|---|---|---|---|---|---|---|---|
| P32 | GND | - | - | - | - | - | - | - |
| P33 | SDIO_WP | In | - | SD2 / 3.3V | i.MX8M | SD2_WP | ALT0 | NVCC_SD2 |
| P34 | SDIO_CMD | Bi-Dir | - | SD2 / 3.3V | i.MX8M | SD2_CMD | ALT0 | NVCC_SD2 |
| P35 | SDIO_CD# | In | - | SD2 / 3.3V | i.MX8M | SD2_CD | ALT0 | NVCC_SD2 |
| P36 | SDIO_CK | Out | - | SD2 / 3.3V | i.MX8M | SD2_CLK | ALT0 | NVCC_SD2 |
| P37 | SDIO_PWR_EN | Out | - | GPIO / 3.3V | i.MX8M | GPIO1_IO12 | ALT0 | NVCC_GPIO1 |
| P38 | GND | - | - | - | - | - | | |
| P39 | SDIO_D0 | Bi-Dir | - | SD2 / 3.3V | i.MX8M | SD2_DATA0 | ALT0 | NVCC_SD2 |
| P40 | SDIO_D1 | Bi-Dir | - | SD2 / 3.3V | i.MX8M | SD2_DATA1 | ALT0 | NVCC_SD2 |
| P41 | SDIO_D2 | Bi-Dir | - | SD2 / 3.3V | i.MX8M | SD2_DATA2 | ALT0 | NVCC_SD2 |
| P42 | SDIO_D3 | Bi-Dir | - | SD2 / 3.3V | i.MX8M | SD2_DATA3 | ALT0 | NVCC_SD2 |
| P43 | SPI0_CS0# | Out | - | SPI / 1.8V | i.MX8M | ECSPI2_SS0 | ALT0 | NVCC_ECSPI |
| P44 | SPI0_CK | Out | - | SPI / 1.8V | i.MX8M | ECSPI2_SCLK | ALT0 | NVCC_ECSPI |
| P45 | SPI0_DIN | In | - | SPI / 1.8V | i.MX8M | ECSPI2_MISO | ALT0 | NVCC_ECSPI |
| P46 | SPI0_DO | Out | - | SPI / 1.8V | i.MX8M | ECSPI2_MOSI | ALT0 | NVCC_ECSPI |
| P47 | GND | - | - | - | - | - | - | - |
| P48 | SATA_TX+ | - | - | - | N.C. | N.C. | - | - |
| P49 | SATA_TX- | - | - | - | N.C. | N.C. | - | - |
| P50 | GND | - | - | - | - | - | - | - |
| P51 | SATA_RX+ | - | - | - | N.C. | N.C. | - | - |
| P52 | SATA_RX- | - | - | - | N.C. | N.C. | - | - |
| P53 | GND | - | - | - | - | - | - | - |
| P54 | ESPI_CS0# / SPI1_CS0# | Out | - | SPI / 1.8V | i.MX8M | ECSPI1_SS0 | ALT0 | NVCC_ECSPI |
| P55 | ESPI_CS1# / SPI1_CS1# | - | - | - | N.C. | N.C. | - | - |
| P56 | ESPI_CK / SPI1_CK | Out | - | SPI / 1.8V | i.MX8M | ECSPI1_SCLK | ALT0 | NVCC_ECSPI |
| P57 | ESPI_IO_1 / SPI1_DIN | In | - | SPI / 1.8V | i.MX8M | ECSPI1_MISO | ALT0 | NVCC_ECSPI |
| P58 | ESPI_IO_0 / SPI1_DO | Out | - | SPI / 1.8V | i.MX8M | ECSPI1_MOSI | ALT0 | NVCC_ECSPI |
| P59 | GND | - | - | - | - | - | | |
| P60 | USB0+ | Bi-Dir | - | USB | i.MX8M | USB1_DP | | USB1_VDD33 |
| P61 | USB0- | Bi-Dir | - | USB | i.MX8M | USB1_DN | | USB1_VDD33 |
| P62 | USB0_EN_OC# | In | PU-10K | GPIO / 3.3V | i.MX8M | GPIO1_IO13 | ALT0 | NVCC_GPIO1 |
| P63 | USB0_VBUS_DET | PWR | - | USB | i.MX8M | USB1_VBUS | - | USB1_VDD33 |

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|---|---|---|---|---|---|---|---|---|
| P64 | USB0_OTG_ID | In | - | USB | i.MX8M | USB1_ID | _ | USB1_VDD33 |
| P65 | USB1+ | Bi-Dir | - | USB | USB Hub (CYUSB3314) | DS3_DP | _ | AVDD33 |
| P66 | USB1- | Bi-Dir | - | USB | USB Hub (CYUSB3314) | DS3_DM | _ | AVDD33 |
| P67 | USB1_EN_OC# | In | - | GPIO / 3.3V | USB Hub (CYUSB3314) | DS3_OVRCURR | _ | AVDD33 |
| P68 | GND | - | - | - | - | - | | |
| P69 | USB2+ | Bi-Dir | - | USB | USB Hub (CYUSB3314) | DS2_DP | _ | AVDD33 |
| P70 | USB2- | Bi-Dir | - | USB | USB Hub (CYUSB3314) | DS2_DM | _ | AVDD33 |
| P71 | USB2_EN_OC# | In | - | GPIO / 3.3V | USB Hub (CYUSB3314) | DS2_OVRCURR | _ | AVDD33 |
| P72 | RSVD | - | - | - | N.C. | N.C. | | |
| P73 | RSVD | - | - | - | N.C. | N.C. | | |
| P74 | USB3_EN_OC# | In | - | GPIO / 3.3V | USB Hub (CYUSB3314) | DS1_OVRCURR | _ | AVDD33 |
| P75 | PCIE_A_RST# | Out | - | GPIO / 3.3V | i.MX8M | SAI1_TXC | ALT5 | NVCC_SAI1 |
| P76 | USB4_EN_OC# | In | - | GPIO / 3.3V | USB Hub (CYUSB3314) | DS4_OVRCURR | _ | AVDD33 |
| P77 | PCIE_B_CKREQ# | - | - | - | N.C. | N.C. | _ | - |
| P78 | PCIE_A_CKREQ# | - | - | - | N.C. | N.C. | _ | - |
| P79 | GND | - | - | - | - | - | _ | - |
| P80 | PCIE_C_REFCK+ | Out | - | - | N.C. | N.C. | _ | - |
| P81 | PCIE_C_REFCK- | Out | - | - | N.C. | N.C. | _ | - |
| P82 | GND | - | - | - | - | - | _ | - |
| P83 | PCIE_A_REFCK+ | Out | - | PCIe | 9FGV0441AKILF | DIF3 | _ | VDDDIG1p8 |
| P84 | PCIE_A_REFCK- | Out | - | PCIe | 9FGV0441AKILF | DIF3\ | _ | VDDDIG1p8 |
| P85 | GND | - | - | | - | - | _ | - |
| P86 | PCIE_A_RX+ | In | - | PCIe | i.MX8M | PCIE2_RXN_P | _ | PCIE_VPH |
| P87 | PCIE_A_RX- | In | - | PCIe | i.MX8M | PCIE2_RXN_N | _ | PCIE_VPH |
| P88 | GND | - | - | - | - | - | _ | - |
| P89 | PCIE_A_TX+ | Out | Serial-0.1uF | PCIe | i.MX8M | PCIE2_TXN_P | _ | PCIE_VPH |
| P90 | PCIE_A_TX- | Out | Serial-0.1uF | PCIe | i.MX8M | PCIE2_TXN_N | _ | PCIE_VPH |
| P91 | GND | - | - | - | - | - | | |
| P92 | HDMI_D2+ / DP1_LANE0+ | Out | - | HDMI | i.MX8M | HDMI_TX_P_LN_2 | _ | HDMI_AVDDIO |
| P93 | HDMI_D2- / DP1_LANE0- | Out | - | HDMI | i.MX8M | HDMI_TX_N_LN_2 | _ | HDMI_AVDDIO |
| P94 | GND | - | - | - | - | - | _ | - |
| P95 | HDMI_D1+ / DP1_LANE1+ | Out | - | HDMI | i.MX8M | HDMI_TX_P_LN_1 | | HDMI_AVDDIO |
| P96 | HDMI_D1- / DP1_LANE1- | Out | - | HDMI | i.MX8M | HDMI_TX_N_LN_1 | | HDMI_AVDDIO |

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|---|---|---|---|---|---|---|---|---|
| P97 | GND | - | - | - | - | - | _ | - |
| P98 | HDMI_D0+ / DP1_LANE2+ | Out | - | HDMI | i.MX8M | HDMI_TX_P_LN_0 | _ | HDMI_AVDDIO |
| P99 | HDMI_D0- / DP1_LANE2- | Out | - | HDMI | i.MX8M | HDMI_TX_N_LN_0 | _ | HDMI_AVDDIO |
| P100 | GND | - | - | - | - | - | _ | - |
| P101 | HDMI_CK+ / DP1_LANE3+ | Out | - | HDMI | i.MX8M | HDMI_TX_P_LN_3 | _ | HDMI_AVDDIO |
| P102 | HDMI_CK- / DP1_LANE3- | Out | - | HDMI | i.MX8M | HDMI_TX_N_LN_3 | ` | HDMI_AVDDIO |
| P103 | GND | - | - | - | - | - | _ | - |
| P104 | HDMI_HPD / DP1_HPD | In | | HDMI | i.MX8M | HDMI_HPD | _ | HDMI_AVDDIO |
| P105 | HDMI_CTRL_CK / DP1_AUX+ | Out | PU-2.2K / PD-100K | HDMI | i.MX8M | HDMI_DDC_SCL(H) HDMI_AUXP(L) | - | HDMI_AVDDIO |
| P106 | HDMI_CTRL_DAT / DP1_AUX- | Bi-Dir | PU-2.2K / PD-100K | HDMI | i.MX8M | HDMI_DDC_SDA(H) HDMI_AUXN(L) | - | HDMI_AVDDIO |
| P107 | DP1_AUX_SEL | In | PD-1M | HDMI | TS5A23159RSER | - | _ | - |
| P108 | GPIO0 / CAM0_PWR# | Out | PU-470K | GPIO / 1.8V | i.MX8M | GPIO1_IO03 | ALT0 | NVCC_GPIO1 |
| P109 | GPIO1 / CAM1_PWR# | Out | PU-470K | GPIO / 1.8V | i.MX8M | GPIO1_IO05 | ALT0 | NVCC_GPIO1 |
| P110 | GPIO2 / CAM0_RST# | Out | PU-470K | GPIO / 1.8V | i.MX8M | GPIO1_IO06 | ALT0 | NVCC_GPIO1 |
| P111 | GPIO3 / CAM1_RST# | Out | PU-470K | GPIO / 1.8V | i.MX8M | GPIO1_IO06 | ALT0 | NVCC_GPIO1 |
| P112 | GPIO4 / HDA_RST# | Out | PU-470K | GPIO / 1.8V | TCA9535 | P04 | _ | VDD_1V8 |
| P113 | GPIO5 / PWM_OUT | Out | PU-470K | GPIO / 1.8V | TCA9535 | P05 | _ | VDD_1V8 |
| P114 | GPIO6 / TACHIN | In | PU-470K | GPIO / 1.8V | TCA9535 | P06 | _ | VDD_1V8 |
| P115 | GPIO7 | In | PU-470K | GPIO / 1.8V | TCA9535 | P07 | _ | VDD_1V8 |
| P116 | GPIO8 | In | PU-470K | GPIO / 1.8V | TCA9535 | P10 | _ | VDD_1V8 |
| P117 | GPIO9 | In | PU-470K | GPIO / 1.8V | TCA9535 | P11 | _ | VDD_1V8 |
| P118 | GPIO10 | In | PU-470K | GPIO / 1.8V | TCA9535 | P12 | _ | VDD_1V8 |
| P119 | GPIO11 | In | PU-470K | GPIO / 1.8V | TCA9535 | P13 | _ | VDD_1V8 |
| P120 | GND | - | - | - | - | - | | |
| P121 | I2C_PM_CK | Out | PU-2k2 | I2C2 | i.MX8M | I2C2_SCL | ALT0 | NVCC_I2C |
| P122 | I2C_PM_DAT | Bi-Dir | PU-2k2 | I2C2 | i.MX8M | I2C2_SDA | ALT0 | NVCC_I2C |
| P123 | BOOT_SEL0# | In | PU-4k7 | GPIO / 1.8V | BMC | PB0 | _ | +1V8SMC |
| P124 | BOOT_SEL1# | In | PU-4k7 | GPIO / 1.8V | BMC | PB1 | _ | +1V8SMC |
| P125 | BOOT_SEL2# | In | PU-4k7 | GPIO / 1.8V | BMC | PB2 | _ | +1V8SMC |
| P126 | RESET_OUT# | Out | - | GPIO / 1.8V | BMC | PB15 | _ | +1V8SMC |
| P127 | RESET_IN# | In | PU-4K7 | GPIO / 1.8V | BMC | PB14 | _ | +1V8SMC |

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|---|---|---|---|---|---|---|---|---|
| P128 | POWER_BTN# | In | PU-4K7 | GPIO / 1.8V | BMC | PB4 | _ | +1V8SMC |
| P129 | SER0_TX | Out | - | UART / 1.8V | i.MX8M | UART2_TXD | ALT0 | NVCC_UART |
| P130 | SER0_RX | In | - | UART / 1.8V | i.MX8M | UART2_RXD | ALT0 | NVCC_UART |
| P131 | SER0_RTS# | In | - | UART / 1.8V | i.MX8M | UART4_TXD | ALT1 | NVCC_UART |
| P132 | SER0_CTS# | Out | - | UART / 1.8V | i.MX8M | UART4_RXD | ALT1 | NVCC_UART |
| P133 | GND | - | - | - | - | - | _ | - |
| P134 | SER1_TX | Out | - | UART / 1.8V | i.MX8M | UART1_TXD | ALT0 | NVCC_UART |
| P135 | SER1_RX | In | - | UART / 1.8V | i.MX8M | UART1_RXD | ALT0 | NVCC_UART |
| P136 | SER2_TX | - | - | - | N.C. | N.C. | _ | - |
| P137 | SER2_RX | - | - | - | N.C. | N.C. | _ | - |
| P138 | SER2_RTS# | - | - | - | N.C. | N.C. | _ | - |
| P139 | SER2_CTS# | - | - | - | N.C. | N.C. | _ | - |
| P140 | SER3_TX | Out | - | UART / 1.8V | i.MX8M | UART3_TXD | ALT0 | NVCC_UART |
| P141 | SER3_RX | In | - | UART / 1.8V | i.MX8M | UART3_RXD | ALT0 | NVCC_UART |
| P142 | GND | - | - | - | - | - | _ | - |
| P143 | CAN0_TX | Out | - | CAN | MCP2517FD | TXCAN | _ | VDD_3V3 |
| P144 | CAN0_RX | In | - | CAN | MCP2517FD | RXCAN | _ | VDD_3V3 |
| P145 | CAN1_TX | - | - | - | N.C. | N.C. | | |
| P146 | CAN1_RX | - | - | - | N.C. | N.C. | | |
| P147 | VDD_IN | PWR | - | - | R69 | - | _ | 3 ~ 5.25 V |
| P148 | VDD_IN | PWR | - | - | R69 | - | _ | 3 ~ 5.25 V |
| P149 | VDD_IN | PWR | - | - | R69 | - | _ | 3 ~ 5.25 V |
| P150 | VDD_IN | PWR | - | - | R69 | - | _ | 3 ~ 5.25 V |
| P151 | VDD_IN | PWR | - | - | R69 | - | _ | 3 ~ 5.25 V |
| P152 | VDD_IN | PWR | - | - | R69 | - | _ | 3 ~ 5.25 V |
| P153 | VDD_IN | PWR | - | - | R69 | - | _ | 3 ~ 5.25 V |
| P154 | VDD_IN | PWR | - | - | R69 | - | _ | 3 ~ 5.25 V |
| P155 | VDD_IN | PWR | - | - | R69 | - | _ | 3 ~ 5.25 V |
| P156 | VDD_IN | PWR | - | - | R69 | - | _ | 3 ~ 5.25 V |
| S1 | CSI1_TX+ / I2C_CAM1_CK | In | PU-2k2 | I2C3 | i.MX8M | I2C3_SCL | ALT0 | NVCC_I2C |
| S2 | CSI1_TX- / I2C_CAM1_DAT | In | PU-2k2 | I2C3 | i.MX8M | I2C3_SDA | ALT0 | NVCC_I2C |
| S3 | GND | - | - | - | - | - | _ | - |
| S4 | RSVD | In | - | - | N.C. | N.C. | _ | - |

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|---|---|---|---|---|---|---|---|---|
| S5 | CSI0_TX- / I2C_CAM0_CK | Out | PU-2k2 | I2C4 | i.MX8M | I2C4_SCL | ALT0 | NVCC_I2C |
| S6 | CAM_MCK | Out | - | GPIO / 1.8V | i.MX8M | GPIO1_IO15 | **ALT6** | NVCC_GPIO1 |
| S7 | CSI0_TX+ / I2C_CAM0_DAT | Bi-Dir | PU-2k2 | I2C4 | i.MX8M | I2C4_SDA | ALT0 | NVCC_I2C |
| S8 | CSI0_CK+ | In | - | MIPI-CSI | i.MX8M | MIPI_CSI1_CLK_P | _ | MIPI_VDDHA |
| S9 | CSI0_CK- | In | - | MIPI-CSI | i.MX8M | MIPI_CSI1_CLK_N | _ | MIPI_VDDHA |
| S10 | GND | - | - | - | - | - | _ | - |
| S11 | CSI0_RX0+ | In | - | MIPI-CSI | i.MX8M | MIPI_CSI1_D0_P | _ | MIPI_VDDHA |
| S12 | CSI0_RX0- | In | - | MIPI-CSI | i.MX8M | MIPI_CSI1_D0_N | _ | MIPI_VDDHA |
| S13 | GND | - | - | - | - | - | _ | - |
| S14 | CSI0_RX1+ | In | - | MIPI-CSI | i.MX8M | MIPI_CSI1_D1_P | _ | MIPI_VDDHA |
| S15 | CSI0_RX1- | In | - | MIPI-CSI | i.MX8M | MIPI_CSI1_D1_N | _ | MIPI_VDDHA |
| S16 | GND | - | - | - | - | - | _ | - |
| S17 | GBE1_MDI0+ | Bi-Dir | - | GBE MDI | I210 | MDI_PLUS[0] | _ | - |
| S18 | GBE1_MDI0- | Bi-Dir | - | GBE MDI | I210 | MDI_MINUS[0] | _ | - |
| S19 | GBE1_LINK100# | Out | - | GPIO / 3.3V | I210 | LED0 | _ | VDD3P3 |
| S20 | GBE1_MDI1+ | Bi-Dir | - | GBE MDI | I210 | MDI_PLUS[1] | _ | - |
| S21 | GBE1_MDI1- | Bi-Dir | - | GBE MDI | I210 | MDI_MINUS[1] | _ | - |
| S22 | GBE1_LINK1000# | Out | - | GPIO / 3.3V | I210 | LED2 | _ | -VDD3P3 |
| S23 | GBE1_MDI2+ | Bi-Dir | - | GBE MDI | I210 | MDI_PLUS[2] | _ | - |
| S24 | GBE1_MDI2- | Bi-Dir | - | GBE MDI | I210 | MDI_MINUS[2] | _ | - |
| S25 | GND | - | - | - | - | - | _ | - |
| S26 | GBE1_MDI3+ | Bi-Dir | - | GBE MDI | I210 | MDI_PLUS[3] | _ | - |
| S27 | GBE1_MDI3- | Bi-Dir | - | GBE MDI | I210 | MDI_MINUS[3] | _ | - |
| S28 | GBE1_CTREF | - | - | - | N.C. | N.C. | _ | - |
| S29 | PCIE_D_TX+ / SERDES_1_TX+ | - | - | - | N.C. | N.C. | _ | - |
| S30 | PCIE_D_TX- / SERDES_1_TX- | - | - | - | N.C. | N.C. | _ | - |
| S31 | GBE1_LINK_ACT# | Out | - | GPIO / 3.3V | I210 | LED1 | _ | VDD3P3 |
| S32 | PCIE_D_RX+ / SERDES_1_RX+ | - | - | - | N.C. | N.C. | _ | - |
| S33 | PCIE_D_RX- / SERDES_1_RX- | - | - | - | N.C. | N.C. | _ | - |
| S34 | GND | - | - | - | - | - | | |
| S35 | USB4+ | Bi-Dir | - | USB | USB Hub (CYUSB3314) | DS4_DP | _ | - AVDD33 |
| S36 | USB4- | Bi-Dir | - | USB | USB Hub (CYUSB3314) | DS4_DM | _ | AVDD33 |

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|---|---|---|---|---|---|---|---|---|
| S37 | USB3_VBUS_DET | - | - | - | N.C. | N.C. | _ | - |
| S38 | AUDIO_MCK | Out | - | SAI / 1.8V | i.MX8M | SAI2_MCLK | ALT0 | NVCC_SAI2 |
| S39 | I2S0_LRCK | Bi-Dir | - | SAI / 1.8V | i.MX8M | SAI2_TXFS | ALT0 | NVCC_SAI2 |
| S40 | I2S0_SDOUT | Out | - | SAI / 1.8V | i.MX8M | SAI2_TXD0 | ALT0 | NVCC_SAI2 |
| S41 | I2S0_SDIN | In | - | SAI / 1.8V | i.MX8M | SAI2_RXD0 | ALT0 | NVCC_SAI2 |
| S42 | I2S0_CK | Bi-Dir | - | SAI / 1.8V | i.MX8M | SAI2_TXC | ALT0 | NVCC_SAI2 |
| S43 | ESPI_ALERT0# | In | - | SAI / 1.8V | i.MX8M | SAI1_RXFS | ALT5 | NVCC_SAI1 |
| S44 | ESPI_ALERT1# | - | - | - | N.C. | N.C. | | |
| S45 | MDIO_CLK | - | - | - | N.C. | N.C. | | |
| S46 | MDIO_DAT | - | - | - | N.C. | N.C. | | |
| S47 | GND | - | - | - | - | - | | |
| S48 | I2C_GP_CK | Out | PU-2.2K | I2C3 | i.MX8M | I2C3_SCL | ALT0 | NVCC_I2C |
| S49 | I2C_GP_DAT | Bi-Dir | PU-2.2K | I2C3 | i.MX8M | I2C3_SDA | ALT0 | NVCC_I2C |
| S50 | HDA_SYNC / I2S2_LRCK | - | - | SAI / 1.8V | i.MX8M | SAI3_TXFS | ALT0 | NVCC_SAI3 |
| S51 | HDA_SDO / I2S2_SDOUT | - | - | SAI / 1.8V | i.MX8M | SAI3_TXD | ALT0 | NVCC_SAI3 |
| S52 | HDA_SDI / I2S2_SDIN | - | - | SAI / 1.8V | i.MX8M | SAI3_RXD | ALT0 | NVCC_SAI3 |
| S53 | HDA_CK / I2S2_CK | - | - | SAI / 1.8V | i.MX8M | SAI3_TXC | ALT0 | NVCC_SAI3 |
| S54 | SATA_ACT# | - | - | - | N.C. | N.C. | _ | - |
| S55 | USB5_EN_OC# | - | - | - | N.C. | N.C. | _ | - |
| S56 | ESPI_IO_2 | - | - | - | N.C. | N.C. | _ | - |
| S57 | ESPI_IO_3 | - | - | - | N.C. | N.C. | _ | - |
| S58 | ESPI_RESET# | Out | - | GPIO / 1.8V | BMC | PB15 | _ | +1V8SMC |
| S59 | USB5+ | - | - | - | N.C. | N.C. | _ | - |
| S60 | USB5- | - | - | - | N.C. | N.C. | _ | - |
| S61 | GND | - | - | - | - | - | _ | - |
| S62 | USB3_SSTX+ | Out | Serial-0.1uF | USB SS | USB Hub (CYUSB3314) | DS1_TXP | _ | - AVDD33 |
| S63 | USB3_SSTX- | Out | Serial-0.1uF | USB SS | USB Hub (CYUSB3314) | DS1_TXM | _ | AVDD33 |
| S64 | GND | - | - | - | - | - | _ | - |
| S65 | USB3_SSRX+ | In | - | USB SS | USB Hub (CYUSB3314) | DS1_RXP | _ | AVDD33 |
| S66 | USB3_SSRX- | In | - | USB SS | USB Hub (CYUSB3314) | DS1_RXM | _ | AVDD33 |
| S67 | GND | - | - | - | - | - | _ | - |
| S68 | USB3+ | Bi-Dir | - | USB | USB Hub (CYUSB3314) | DS1_DP | _ | AVDD33 |
| S69 | USB3- | Bi-Dir | - | USB | USB Hub (CYUSB3314) | DS1_DM | _ | AVDD33 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| S70 | GND | - | - | - | - | - | _ | - |
| S71 | USB2_SSTX+ | Out | Serial-0.1uF | USB SS | USB Hub (CYUSB3314) | DS2_TXP | _ | AVDD33 |
| S72 | USB2_SSTX- | Out | Serial-0.1uF | USB SS | USB Hub (CYUSB3314) | DS2_TXM | _ | AVDD33 |
| S73 | GND | - | - | - | - | - | _ | - |
| S74 | USB2_SSRX+ | In | - | USB SS | USB Hub (CYUSB3314) | DS2_RXP | _ | AVDD33 |
| S75 | USB2_SSRX- | In | - | USB SS | USB Hub (CYUSB3314) | DS2_RXM | _ | AVDD33 |
| S76 | PCIE_B_RST# | Out | - | GPIO / 3.3V | i.MX8M | NAND_ALE | ALT5 | NVCC_NAND |
| S77 | PCIE_C_RST# | - | - | - | N.C. | N.C. | _ | - |
| S78 | PCIE_C_RX+ / SERDES_2_RX+ | - | - | - | N.C. | N.C. | _ | - |
| S79 | PCIE_C_RX- / SERDES_2_RX- | - | - | - | N.C. | N.C. | _ | - |
| S80 | GND | - | - | - | - | - | _ | - |
| S81 | PCIE_C_TX+ / SERDES_2_TX+ | - | - | - | N.C. | N.C. | _ | - |
| S82 | PCIE_C_TX- / SERDES_2_TX- | - | - | - | N.C. | N.C. | _ | - |
| S83 | GND | - | - | - | - | - | _ | - |
| S84 | PCIE_B_REFCK+ | Out | - | PCIe | 9FGV0441AKILF | DIF1 | _ | VDDDIG1p8 |
| S85 | PCIE_B_REFCK- | Out | - | PCIe | 9FGV0441AKILF | DIF1\ | _ | VDDDIG1p8 |
| S86 | GND | - | - | - | - | - | _ | - |
| S87 | PCIE_B_RX+ | In | - | PCIe | i.MX8M | PCIE1_RXN_P | _ | PCIE_VPH |
| S88 | PCIE_B_RX- | In | - | PCIe | i.MX8M | PCIE1_RXN_N | _ | PCIE_VPH |
| S89 | GND | - | - | - | - | - | _ | - |
| S90 | PCIE_B_TX+ | Out | Serial-0.1uF | PCIe | i.MX8M | PCIE1_TXN_P | _ | PCIE_VPH |
| S91 | PCIE_B_TX- | Out | Serial-0.1uF | PCIe | i.MX8M | PCIE1_TXN_N | _ | PCIE_VPH |
| S92 | GND | - | - | - | - | - | _ | - |
| S93 | DP0_LANE0+ | - | - | - | N.C. | N.C. | _ | - |
| S94 | DP0_LANE0- | - | - | - | N.C. | N.C. | _ | - |
| S95 | DP0_AUX_SEL | - | - | - | N.C. | N.C. | _ | - |
| S96 | DP0_LANE1+ | - | - | - | N.C. | N.C. | _ | - |
| S97 | DP0_LANE1- | - | - | - | N.C. | N.C. | _ | - |
| S98 | DP0_HPD | - | - | - | N.C. | N.C. | _ | - |
| S99 | DP0_LANE2+ | - | - | - | N.C. | N.C. | _ | - |
| S100 | DP0_LANE2- | - | - | - | N.C. | N.C. | _ | - |
| S101 | GND | - | - | - | - | - | _ | - |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| S102 | DP0_LANE3+ | - | - | - | N.C. | N.C. | _ | - |
| S103 | DP0_LANE3- | - | - | - | N.C. | N.C. | _ | - |
| S104 | USB3_OTG_ID | - | - | - | N.C. | N.C. | _ | - |
| S105 | DP0_AUX+ | - | - | - | N.C. | N.C. | _ | - |
| S106 | DP0_AUX- | - | - | - | N.C. | N.C. | _ | - |
| S107 | LCD1_BKLT_EN | - | - | - | N.C. | N.C. | _ | - |
| S108 | LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+ | Out | Serial-0R | LVDS | SN65DSI84 | B_CLKP | - | - |
| S109 | LVDS1_CK- / eDP1_AUX- / DSI1_CLK- | Out | Serial-0R | LVDS | SN65DSI84 | B_CLKN | - | - |
| S110 | GND | - | - | - | | | _ | - |
| S111 | LVDS1_0+ / eDP1_TX0+ / DSI1_D0+ | Out | Serial-0R | LVDS | SN65DSI84 | B_Y0P | - | - |
| S112 | LVDS1_0- / eDP1_TX0- / DSI1_D0- | Out | Serial-0R | LVDS | SN65DSI84 | B_Y0N | - | - |
| S113 | eDP1_HPD / DSI1_TE | - | - | - | N.C. | N.C. | _ | - |
| S114 | LVDS1_1+ / eDP1_TX1+ / DSI1_D1+ | Out | Serial-0R | LVDS | SN65DSI84 | B_Y1P | - | - |
| S115 | LVDS1_1- / eDP1_TX1- / DSI1_D1- | Out | Serial-0R | LVDS | SN65DSI84 | B_Y1N | - | - |
| S116 | LCD1_VDD_EN | - | - | - | N.C. | N.C. | _ | - |
| S117 | LVDS1_2+ / eDP1_TX2+ / DSI1_D2+ | Out | Serial-0R | LVDS | SN65DSI84 | B_Y2P | - | - |
| S118 | LVDS1_2- / eDP1_TX2- / DSI1_D2- | Out | Serial-0R | LVDS | SN65DSI84 | B_Y2N | - | - |
| S119 | GND | - | - | - | - | - | _ | - |
| S120 | LVDS1_3+ / eDP1_TX3+ / DSI1_D3+ | Out | Serial-0R | LVDS | SN65DSI84 | B_Y3P | - | - |
| S121 | LVDS1_3- / eDP1_TX3- / DSI1_D3- | Out | Serial-0R | LVDS | SN65DSI84 | B_Y3N | - | - |
| S122 | LCD1_BKLT_PWM | - | - | - | N.C. | N.C. | _ | - |
| S123 | GPIO13 | - | - | - | N.C. | N.C. | _ | - |
| S124 | GND | - | - | - | - | - | _ | - |
| S125 | LVDS0_0+ / eDP0_TX0+ / DSI0_D0+ | Out | Serial-0R | LVDS | SN65DSI84 | A_Y0P | - | - |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| S126 | LVDS0_0- / eDP0_TX0- / DSI0_D0- | Out | Serial-0R | LVDS | SN65DSI84 | A_Y0N | - | - |
| S127 | LCD0_BKLT_EN | Out | - | GPIO / 1.8V | i.MX8M | GPIO1_IO00 | - | NVCC_GPIO1 |
| S128 | LVDS0_1+ / eDP0_TX1+ / DSI0_D1+ | Out | Serial-0R | LVDS | SN65DSI84 | A_Y1P | - | - |
| S129 | LVDS0_1- / eDP0_TX1- / DSI0_D1- | Out | Serial-0R | LVDS | SN65DSI84 | A_Y1N | - | - |
| S130 | GND | - | - | - | - | - | - | - |
| S131 | LVDS0_2+ / eDP0_TX2+ / DSI0_D2+ | Out | Serial-0R | LVDS | SN65DSI84 | A_Y2P | - | - |
| S132 | LVDS0_2- / eDP0_TX2- / DSI0_D2- | Out | Serial-0R | LVDS | SN65DSI84 | A_Y2N | - | - |
| S133 | LCD0_VDD_EN | Out | - | GPIO/1.8V | i.MX8M | GPIO1_IO04 | - | NVCC_GPIO1 |
| S134 | LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+ | Out | Serial-0R | LVDS | SN65DSI84 | A_CLKP | - | - |
| S135 | LVDS0_CK- / eDP0_AUX- / DSI0_CLK- | Out | Serial-0R | LVDS | SN65DSI84 | A_CLKN | - | - |
| S136 | GND | - | - | - | - | - | - | - |
| S137 | LVDS0_3+ / eDP0_TX3+ / DSI0_D3+ | Out | Serial-0R | LVDS | SN65DSI84 | A_Y3P | - | - |
| S138 | LVDS0_3- / eDP0_TX3- / DSI0_D3- | Out | Serial-0R | LVDS | SN65DSI84 | A_Y3N | - | - |
| S139 | I2C_LCD_CK | Out | PU-2.2K | I2C4 | i.MX8M | I2C4_SCL | ALT0 | NVCC_I2C |
| S140 | I2C_LCD_DAT | Bi-Dir | PU-2.2K | I2C4 | i.MX8M | I2C4_SCL | ALT0 | NVCC_I2C |
| S141 | LCD0_BKLT_PWM | Out | - | GPIO / 1.8V | i.MX8M | GPIO1_IO01 | ALT1 | NVCC_GPIO1 |
| S142 | GPIO12 | In | PU-10K | GPIO / 1.8V | BMC | PC14 | - | +1V8SMC |
| S143 | GND | - | - | - | - | - | - | - |
| S144 | eDP0_HPD / DSI0_TE | - | - | - | N.C. | N.C. | - | - |
| S145 | WDT_TIME_OUT# | Out | - | GPIO / 1.8V | BMC | PD2 | - | +1V8SMC |
| S146 | PCIE_WAKE# | In | - | GPIO / 3.3V | i.MX8M | SAI1_TXFS | ALT5 | NVCC_SAI1 |
| S147 | VDD_RTC | PWR | - | - | RV-3028-C7 | VDD | - | - |
| S148 | LID# | In | PU-4.7K | GPIO / 1.8V | i.MX8M | SAI5_MCLK | ALT5 | NVCC_SAI5 |
| S149 | SLEEP# | In | PU-4.7K | GPIO / 1.8V | i.MX8M | SAI5_RXFS | ALT5 | NVCC_SAI5 |
| S150 | VIN_PWR_BAD# | In | PU-10K | GPIO / 1.8V | BMC | PB7 | - | +1V8SMC |
| S151 | CHARGING# | Out | PU-68K | GPIO / 1.8V | i.MX8M | SAI5_RXC | ALT5 | NVCC_SAI5 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| S152 | CHARGER_PRSNT# | Out | PU-100K | GPIO / 1.8V | i.MX8M | SAI5_RXD0 | ALT5 | NVCC_SAI5 |
| S153 | CARRIER_STBY# | Out | - | GPIO / 1.8V | BMC | PB5 | - | +1V8SMC |
| S154 | CARRIER_PWR_ON | Out | - | GPIO / 1.8V | BMC | PB6 | - | +1V8SMC |
| S155 | FORCE_RECOV# | In | PU-10K | GPIO /3.3V | 74LVC1G04 | 2 | - | VDD_3V3 |
| S156 | BATLOW# | In | PU-4.7K | GPIO / 1.8V | i.MX8M | SAI5_RXD2 | ALT5 | NVCC_SAI5 |
| S157 | TEST# | In | PU-4.7K | GPIO / 1.8V | i.MX8M | SAI5_RXD1 | ALT5 | NVCC_SAI5 |
| S158 | GND | - | - | - | - | - | - | - |

# 5. Software Support

### 5.1.1 Uboot / Yocto

Goto : https://github.com/adlink

Yocto source-code and compiling instructions are available

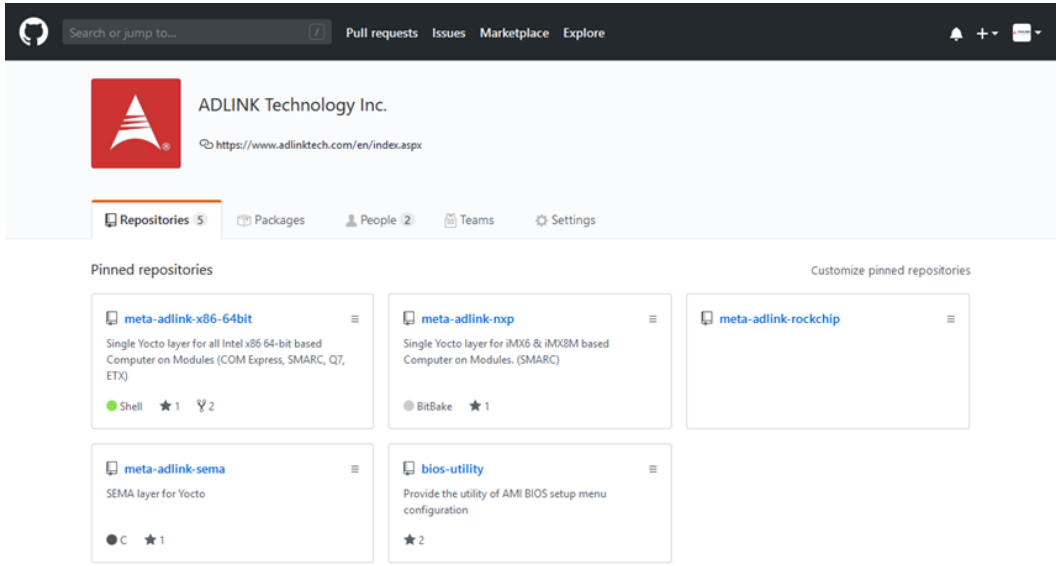
### 5.1.2 Ubuntu

Build instruction from source, are available on Github

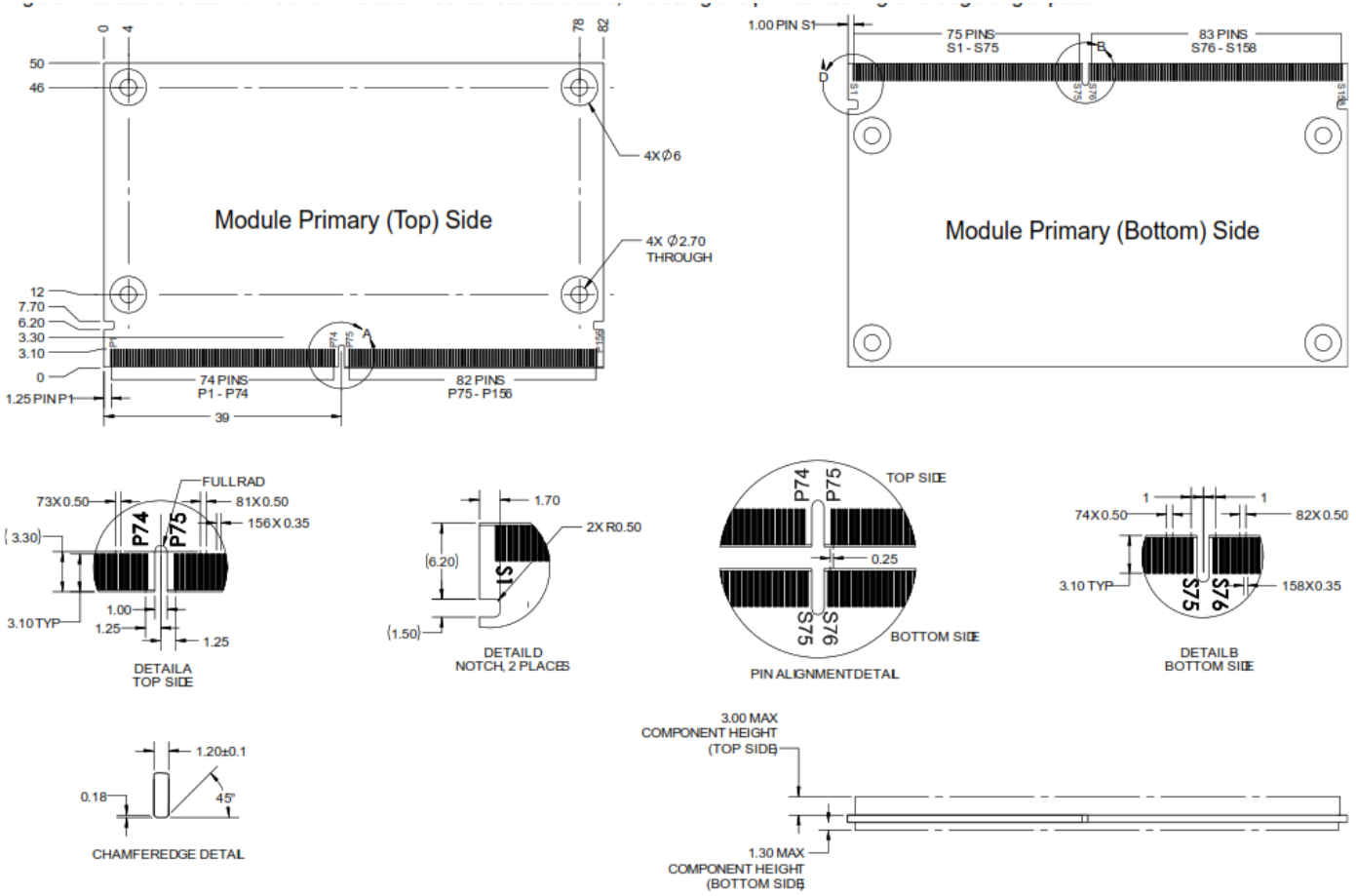
### 5.1.3 Android

Goto : https://github.com/adlink

Android source-code and compiling instructions are available

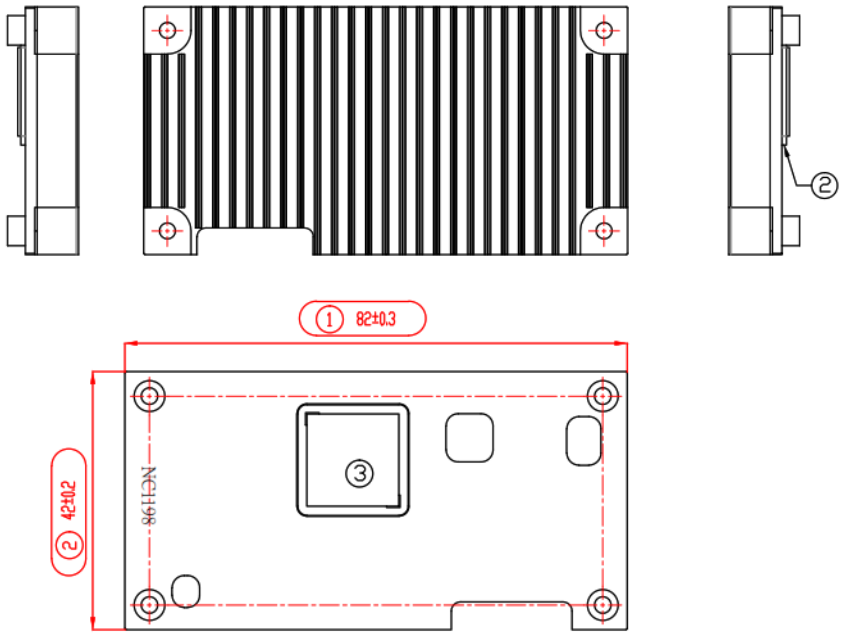


# 6. Mechanical



# 7. Thermal Solutions

LEC-IMX8M has to be cooled by a passive Heatsink / Heat-spreader optionally available for ordering




| | |
|---|---|
| HTS-sIMX8M | Heatspreader for LEC-iMX8M |
| THS-sIMX8M | Low profile heatsink for LEC-iMX8M |