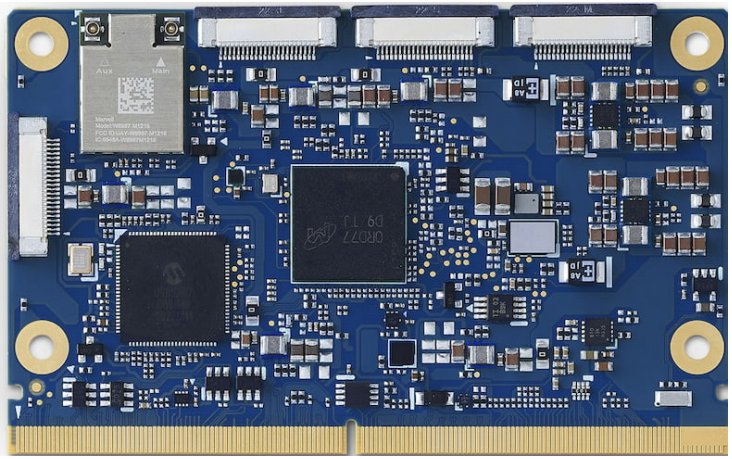
LEC-RB5(N)

User's Guide

Qualcomm



SMARC module

Revision:	Rev. 1.1
Date:	2025-11-04
Part Number:	50M-72515-1010

ADLINK
LEADING EDGE COMPUTING

Revision History

Revision	Description	Date	Author
1.0	Initial release	2025-03-28	AL
1.1	Specifications and pinout and signal descriptions	2025-11-04	AL

Preface

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Product names mentioned herein are used for identification purposes only and may be trademarks / registered trademarks of respective companies.

Safety Instructions

For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

Conventions

The following conventions may be used throughout this manual, denoting special levels of information

Note: This information adds clarity or specifics to text and illustrations.

Caution: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

Warning: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

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1. Introduction

1.1 LEC-RB5(N)

ADLINK LEC-RB5(N) is a SMARC R2.1-compliant module that features Qualcomm® Kyro™ 585 CPU, with 8x Arm Cortex-A77 cores, and offers exceptional performance per watt. It includes Qualcomm® Hexagon™ Tensor Accelerator (HTA) running up to 15 TOPS and supports 4K HDMI/MIPI DSI display, MIPI CSI cameras, 2x PCIe x2 Gen3, 2x GbE Ethernet, 2x USB 3.1/2.0, 4x USB 2.0, GPIO/SD and UFS.

1.2 The SMARC Form Factor

The SMARC ("Smart Mobility ARChitecture") is a versatile small form factor Computer on Module definition targeting applications that require low power and high performance at low costs. Typically under 6W, the modules often utilize ARM and other alternative low-power option CPUs, and are used in many familiar handheld devices, such as tablet computers and smart phones.

Two module sizes are defined in SMARC: 82 mm x 50 mm and 82 mm x 80 mm.

The module PCBs have 314 edge fingers that mate with a low-profile 314 pin 0.5 mm pitch right angle connector (the connector is sometimes identified as a 321-pin connector, with 7 pins used by the key).

SMARC modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE and a single channel LVDS display transmitter are concentrated on the module. Modules are used with application-specific carrier boards that implement other features such as audio codecs, touch controllers, wireless devices, etc.

The modular approach allows scalability, faster time to market and upgradability while still maintaining low costs, low power, and small physical size.

SGeT STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

SMARC module and carrier specifications are available online at: https://www.sget.org/standards/smarc.html

2. Specifications

2.1 Core System

SoC

QRB5165
Kryo™ 585 Octa-core CPU:

- Kryo Gold prime @ 2.84GHZ
- 3 Kryo Gold @ 2.42GHz
- 4 Kryo Silver @ 1.81GHz

Memory

• Four-channel PoP high speed memory LPDDR4 SDRAM @ 2133MHz, up to 8GB

• Four-channel PoP high speed memory LPDDR5 SDRAM @ 2750MHz, up to 16GB

L2 Cache

System L2 cache (ECC)

- Gold core 256 KB
- Gold Prime core 512 KB
- Silver core 128 KB

Security

Qualcomm Secure Processing Unit

2.2 Video

2.2.1 DPU / GPU / VPU

DPU Core

Adreno DPU 995, supports up to 3x 4K display, up to 5040 × 2160 at 60Hz

GPU Core

Adreno GPU 650, Fmax at 587MHz – 4K 60 fps UI or 2X 2K 60 fps UI OpenGL ES 3.2, Vulkan 1.1, DX12 FL 12_1OpenCL 2.0 full profile

VPU Core

Adreno VPU 665 – 5th gen UHD video processing unit Video, decode up to 4K240/8K60 Video, encode up to 4K120/8K30

2.2.2 Display Interfaces

MIPI DSI

1x MIPI DSI 4 lane, compliant with MIPI-DSI standard v1.2
Maximum resolution 1K p60 with 24-bit RGB

HDMI

- HDMI interface is obtained from DSI0/1 over a DSI2HDMI chip (need 8 lanes)
- HDMI 2.0B complaint
- Supports a maximum display resolution of 1K p60

2.3 Camera

Supports CSI0 2Lane and CSI1 4-lane MIPI CSI2 camera input.

CSI2/3/4/5 on module feature connector (4 lanes)

Note: Only 4x RGB and 2x YUV camera modules supported.

2.4 Audio

Supports I2S audio codec on carrier

2.5 Dual Wired Ethernet

Primary LAN

10/100/1000 Ethernet Controller over USB 3.1

Supports 10/100/1000-Mbps data transfer rates, both full-duplex and half-duplex

Secondary LAN

10/100/1000 Ethernet Controller over USB 3.1

Supports 10/100/1000-Mbps data transfer rates, both full-duplex and half-duplex

2.6 Wi-Fi / Bluetooth

Optional M.2 1216 industry standard footprint with support for PCIe solder down modules

2.7 Extension Busses

PCIe
2x 2-lane R3.0

USB
2x USB 3.1 Gen 1, 4x USB 2.0

UART
3x UART interfaces SER0,1,2

CANbus
Optional CAN0 Supports CAN2.0B only or mixed CAN2.0B and CAN FD mode, data bit rate up to 8 Mbps (Optional over SPI1)

SPI
2x SPI

I2S / Sound Wire
1x I2S with audio resolution from 16-bits to 32-bits and sample rate up to 192KHz (see Audio Codec support)

I2C

3x I2C interfaces

- Support for 7-bit mode
- Software programmable clock frequency of 100 kbit/s in Standard-mode, 400 kbit/s in the Fast-mode, or 1 Mbit/s in Fast-mode Plus

GPIO

14x GPIO with interrupt, one GPIO with PWM

2.8 System Storage

SDIO

1x SDIO (4-bit) compatible with SD3.0, MMC ver. 4.51 to edge connector

Storage

Up to 512 GB on-module UFS

2.9 Board Controller

BMC lite for power sequence

SEMA BMC Error Code

Exception Code	Error Code
0	NOERROR
2	NO_VIN
3	NO_SDM_RESIN_N
4	NO_SDM_RESIN_N

2.10 Debug Header DB30

Multipurpose Connector: ADLINK standard 30-pin FPC with the following pins

- Boot Select strap pins
- Serial port
- LITE BMC

2.11 Power

Power Modes:	ON / OFF / SUSPEND
Power on / off Behavior	AT (always boot)
Voltage Input:	5.0V +/- 5%

Operating Temperatures

Standard Operating Temperature:	0 to 60°C	commercial grade BOM (memory, eMMC, USB hub, SoC)
Rugged Operating Temperature:	-20 to 70°C	industrial grade BOM (memory, eMMC, USB hub, SoC)

Humidity:	5-90% RH operating, non-condensing
	5-95% RH storage (and operating with conformal coating).
EMI:	EN55022 Class B inside an enclosure

Shock and Vibration:	HALT testing, with test report that confirms Extended Operating Temp range during and after vibration. Separate Shock test report to MIL-STD-202F, Method 213B, Table 213-I, Condition A. In addition, when installed on baseboard shall operate under 18 sawtooth mechanical shocks (3 shocks in each direction) with a peak acceleration of 40g for a duration of 18 msec each and 75g for a duration of 6 msec each. Capable of supporting Random Vibration: MIL-STD-202F, Method 214A, Table 214-I, Condition D. If HALT testing shows equal or better performance, a separate vibration test report is not necessary.
MTBF:	300,000 hrs (at 40°C), 100,000 hrs (at 70°C),

3. Functional Block Diagram

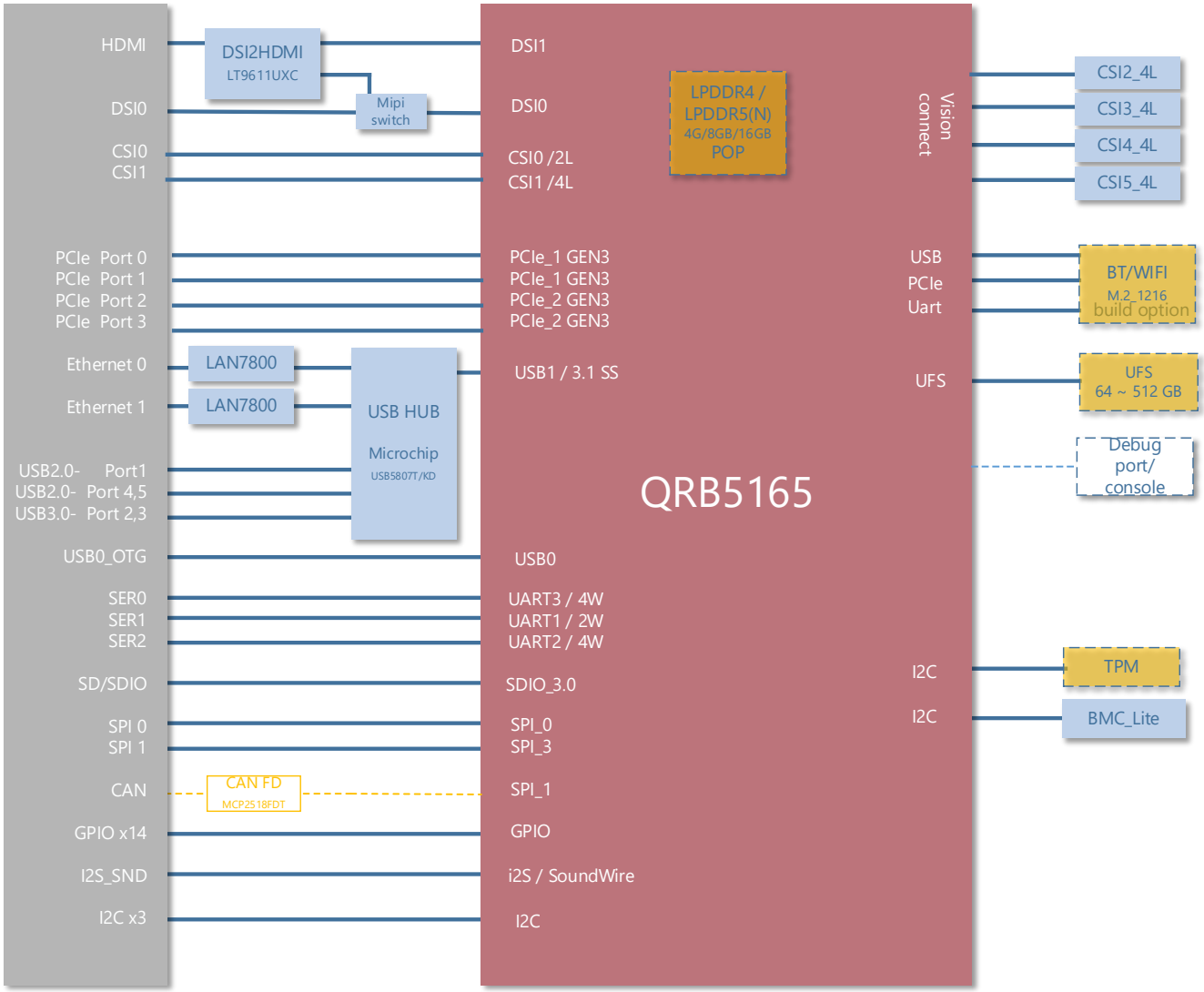

Figure 1 – Module functional block diagram

4. Pinout and Signal Descriptions

4.1 Pin Summary

The below table is a comprehensible list of all signal pins on the MXM 3 connector in the standard specification SMARC 2.1.
Not all signals are available in each design, for specific product specs check the detailed tables in this document. Signals described in the specification but not supported on the LEC-RB5(N) are marked with ~~strikethrough~~.

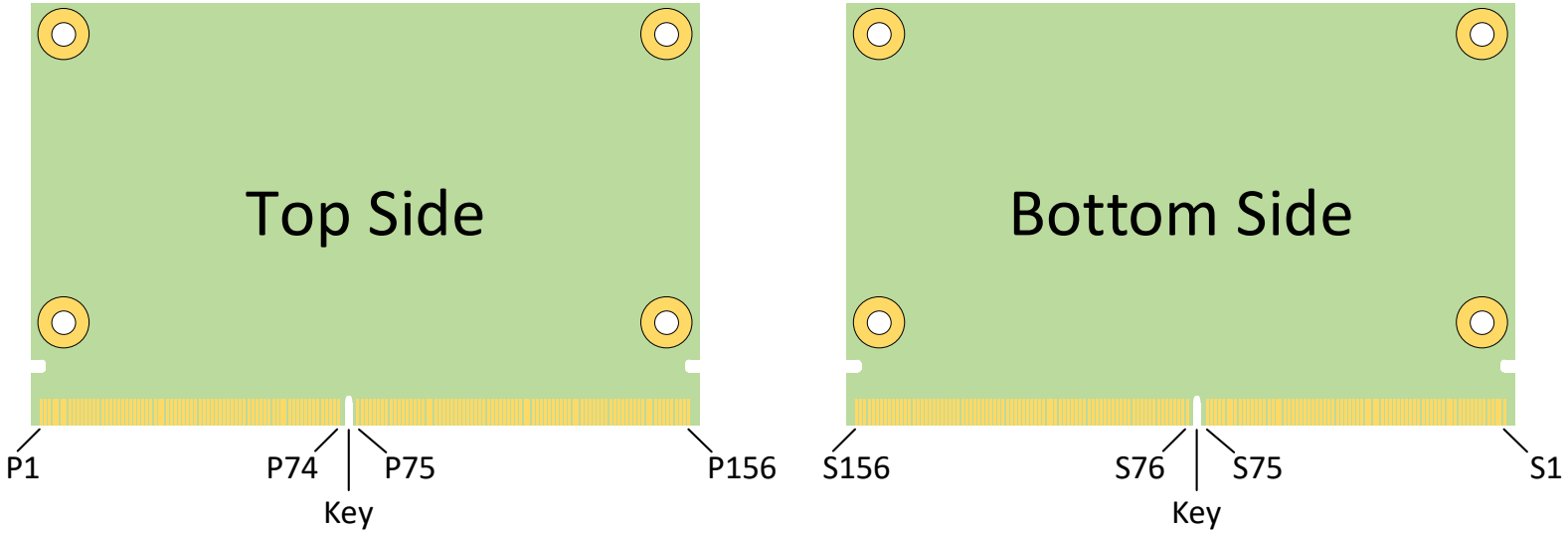

Figure 2 – Module top/bottom side pin numbering

P-Pin	Primary (Top) Side
P1	SMB_ALERT_1V8#
P2	GND
P3	CSI1_CK+
P4	CSI1_CK-
P5	GBE1_SDP
P6	GBE0_SDP
P7	CSI1_RX0+
P8	CSI1_RX0-
P9	GND
P10	CSI1_RX1+
P11	CSI1_RX1-
P12	GND
P13	CSI1_RX2+
P14	CSI1_RX2-
P15	GND
P16	CSI1_RX3+
P17	CSI1_RX3-
P18	GND
P19	GBE0_MDI3-
P20	GBE0_MDI3+
P21	GBE0_LINK100#
P22	GBE0_LINK1000#
P23	GBE0_MDI2-
P24	GBE0_MDI2+
P25	GBE0_LINK_ACT#
P26	GBE0_MDI1-
P27	GBE0_MDI1+
P28	GBE0_CTREF
P29	GBE0_MDI0-
P30	GBE0_MDI0+
P31	SPI0_CS1#
P32	GND
P33	SDIO_WP
P34	SDIO_CMD

S-Pin	Secondary (Bottom) Side
S1	CSI1_TX+ / I2C_CAM1_CK
S2	CSI1_TX- / I2C_CAM1_DAT
S3	GND
S4	RSVD
S5	CSI0_TX- / I2C_CAM0_CK
S6	CAM_MCK
S7	CSI0_TX+ / I2C_CAM0_DAT
S8	CSI0_CK+
S9	CSI0_CK-
S10	GND
S11	CSI0_RX0+
S12	CSI0_RX0-
S13	GND
S14	CSI0_RX1+
S15	CSI0_RX1-
S16	GND
S17	GBE1_MDI0+
S18	GBE1_MDI0-
S19	GBE1_LINK100#
S20	GBE1_MDI1+
S21	GBE1_MDI1-
S22	GBE1_LINK1000#
S23	GBE1_MDI2+
S24	GBE1_MDI2-
S25	GND
S26	GBE1_MDI3+
S27	GBE1_MDI3-
S28	GBE1_CTREF
S29	PCIE_D_TX+ / SERDES_1_TX+
S30	PCIE_D_TX- / SERDES_1_TX-
S31	GBE1_LINK_ACT# (build option)
S32	PCIE_D_RX+ / SERDES_1_RX+
S33	PCIE_D_RX- / SERDES_1_RX-
S34	GND
S35	USB4+

P-Pin	Primary (Top) Side
P35	SDIO_CD#
P36	SDIO_CK
P37	SDIO_PWR_EN
P38	GND
P39	SDIO_D0
P40	SDIO_D1
P41	SDIO_D2
P42	SDIO_D3
P43	SPI0_CS0#
P44	SPI0_CK
P45	SPI0_DIN
P46	SPI0_DO
P47	GND
P48	SATA_TX+
P49	SATA_TX-
P50	GND
P51	SATA_RX+
P52	SATA_RX-
P53	GND
P54	ESPI_CS0# / SPI1_CS0#
P55	ESPI_CS1# / SPI1_CS1#
P56	ESPI_CK / SPI1_CK
P57	ESPI_IO_1 / SPI1_DIN
P58	ESPI_IO_0 / SPI1_DO
P59	GND
P60	USB0+
P61	USB0-
P62	USB0_EN_OC#
P63	USB0_VBUS_DET
P64	USB0_OTG_ID
P65	USB1+
P66	USB1-
P67	USB1_EN_OC#
P68	GND
P69	USB2+

S-Pin	Secondary (Bottom) Side
S36	USB4-
S37	USB3_VBUS_DET
S38	AUDIO_MCK
S39	I2S0_LRCK
S40	I2S0_SDOUT
S41	I2S0_SDIN
S42	I2S0_CK
S43	ESPI_ALERT0#
S44	ESPI_ALERT1#
S45	MDIO_CLK
S46	MDIO_DAT
S47	GND
S48	I2C_GP_CK
S49	I2C_GP_DAT
S50	HDA_SYNC / I2S2_LRCK
S51	HDA_SDO / I2S2_SDOUT
S52	HDA_SDI / I2S2_SDIN
S53	HDA_CK / I2S2_CK
S54	SATA_ACT#
S55	USB5_EN_OC#
S56	ESPI_IO_2
S57	ESPI_IO_3
S58	ESPI_RESET#
S59	USB5+
S60	USB5-
S61	GND
S62	USB3_SSTX+
S63	USB3_SSTX-
S64	GND
S65	USB3_SSRX+
S66	USB3_SSRX-
S67	GND
S68	USB3+
S69	USB3-
S70	GND

P-Pin	Primary (Top) Side
P70	USB2-
P71	USB2_EN_OC#
P72	RSVD
P73	RSVD
P74	USB3_EN_OC#
	Key
P75	PCIE_A_RST#
P76	USB4_EN_OC#
P77	PCIE_B_CKREQ#
P78	PCIE_A_CKREQ#
P79	GND
~~P80~~	~~PCIE_C_REFCK+~~
~~P81~~	~~PCIE_C_REFCK-~~
P82	GND
P83	PCIE_A_REFCK+
P84	PCIE_A_REFCK-
P85	GND
P86	PCIE_A_RX+
P87	PCIE_A_RX-
P88	GND
P89	PCIE_A_TX+
P90	PCIE_A_TX-
P91	GND
P92	HDMI_D2+ /
P93	HDMI_D2- / DP1_LANE0-
P94	GND
P95	HDMI_D1+ /
P96	HDMI_D1- / DP1_LANE1-
P97	GND
P98	HDMI_D0+ /
P99	HDMI_D0- / DP1_LANE2-
P100	GND
P101	HDMI_CK+ /

S-Pin	Secondary (Bottom) Side
S71	USB2_SSTX+
S72	USB2_SSTX-
S73	GND
S74	USB2_SSRX+
S75	USB2_SSRX-
	Key
S76	PCIE_B_RST#
~~S77~~	~~PCIE_C_RST#~~
S78	PCIE_C_RX+ / SERDES_2_RX+
S79	PCIE_C_RX- / SERDES_2_RX-
S80	GND
S81	PCIE_C_TX+ / SERDES_2_TX+
S82	PCIE_C_TX- / SERDES_2_TX-
S83	GND
S84	PCIE_B_REFCK+
S85	PCIE_B_REFCK-
S86	GND
S87	PCIE_B_RX+
S88	PCIE_B_RX-
S89	GND
S90	PCIE_B_TX+
S91	PCIE_B_TX-
S92	GND
S93	DP0_LANE0+
S94	DP0_LANE0-
S95	DP0_AUX_SEL
S96	DP0_LANE1+
S97	DP0_LANE1-
S98	DP0_HPD
S99	DP0_LANE2+
S100	DP0_LANE2-
S101	GND
S102	DP0_LANE3+

P-Pin	Primary (Top) Side
P102	HDMI_CK- / DP1_LANE3-
P103	GND
P104	HDMI_HPD / DP1_HPD
P105	HDMI_CTRL_CK /
P106	HDMI_CTRL_DAT /
P107	DP1_AUX_SEL
P108	GPIO0 / CAM0_PWR#
P109	GPIO1 / CAM1_PWR#
P110	GPIO2 / CAM0_RST#
P111	GPIO3 / CAM1_RST#
P112	GPIO4 / HDA_RST#
P113	GPIO5 / PWM_OUT
P114	GPIO6 / TACHIN
P115	GPIO7
P116	GPIO8
P117	GPIO9
P118	GPIO10
P119	GPIO11
P120	GND
P121	I2C_PM_CK
P122	I2C_PM_DAT
P123	BOOT_SEL0#
P124	BOOT_SEL1#
P125	BOOT_SEL2#
P126	RESET_OUT#
P127	RESET_IN#
P128	POWER_BTN#
P129	SER0_TX
P130	SER0_RX
P131	SER0_RTS#
P132	SER0_CTS#
P133	GND
P134	SER1_TX
P135	SER1_RX
P136	SER2_TX

S-Pin	Secondary (Bottom) Side
S103	DP0_LANE3-
S104	USB3_OTG_ID
S105	DP0_AUX+
S106	DP0_AUX-
S107	LCD1_BKLT_EN
S108	LVDS1_CK+ / DSI1_CLK+
S109	LVDS1_CK- / DSI1_CLK-
S110	GND
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-
S113	eDP1_HPD / DSI1_TE
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-
S116	LCD1_VDD_EN
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-
S119	GND
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-
S122	LCD1_BKLT_PWM
S123	GPIO13
S124	GND
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-
S127	LCD0_BKLT_EN
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-
S130	GND
S131	LVDS0_2+/eDP0_TX2+/ DSI0_D2+
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-
S133	LCD0_VDD_EN
S134	LVDS0_CK+/eDP0_AUX/ DSI0_CLK+
S135	LVDS0_CK-/eDP0_AUX-/ DSI0_CLK-
S136	GND
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+

P-Pin	Primary (Top) Side
P137	SER2_RX
P138	SER2_RTS#
P139	SER2_CTS#
P140	SER3_TX
P141	SER3_RX
P142	GND
P143	CAN0_TX
P144	CAN0_RX
P145	CAN1_TX
P146	CAN1_RX
P147	VDD_IN

S-Pin	Secondary (Bottom) Side
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-
S139	I2C_LCD_CK
S140	I2C_LCD_DAT
S141	LCD0_BKLT_PWM
S142	GPIO12
S143	GND
S144	eDP0_HPD / DSI0_TE
S145	WDT_TIME_OUT#
S146	PCIE_WAKE#
S147	VDD_RTC
S148	LID#

P-Pin	Primary (Top) Side
P148	VDD_IN
P149	VDD_IN
P150	VDD_IN
P151	VDD_IN
P152	VDD_IN
P153	VDD_IN
P154	VDD_IN
P155	VDD_IN
P156	VDD_IN

S-Pin	Secondary (Bottom) Side
S149	SLEEP#
S150	VIN_PWR_BAD#
S151	CHARGING#
S152	CHARGER_PRSNT#
S153	CARRIER_STBY#
S154	CARRIER_PWR_ON
S155	FORCE_RECOV#
S156	BATLOW#
S157	TEST#
S158	GND

Note: Above is the **complete** SMARC function set, not all signals are available

4.2 Signal Terminology Descriptions

Definitions of terms used for signal description tables.

Term	Description
I	Input to the Module
O	Output from the Module
I/O	Bi-directional input/output
OD	Open drain
PU	PU (pull-up) resistor
PD	PD (pull-down) resistor
CMOS	Logic input or output
GBE MDI	Differential analogue signalling for gigabit media dependent interface
DP	Low voltage differential signal for DisplayPort interface
D-PHY	Low voltage differential signal for MIPI CSI-2 cameras and DSI displays
M-PHY	Low voltage differential signal for MIPI CSI-3 cameras
LVDS	Low voltage differential signal for LCD displays
PCIE	Low voltage differential signal for PCIe
SATA	Low voltage differential signal for SATA
TMDS HDMI	Transition minimized differential signal for HDMI displays
USB	DC coupled differential signalling for traditional (non-Superspeed) USB signals
USB SS	Differential signal for SuperSpeed USB signals
USB VBUS 5V	5V tolerant input for USB VBUS detection
VDD_IN	Main power source from Carrier to Module
3.3V	3.3V power domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
1.8V	1.8V power domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
3.3Vsb	3.3V standby power domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)
1.8Vsb	1.8V standby power domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)
Sleep	Module is in its lowest power state
Runtime	Module is full on. CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
Standby	Module is in standby state or higher

4.3 Signal Description by function

4.3.1 Primary Display Interface

HDMI and DSI are supported on this module, eDP is NOT supported. DSI0 is 4 lanes

DSI 0/1 are used over a DSI to HDMI bridge to provide HDMI output

Channel 1

Pin #	LVDS Name	MIPI DSI Name	eDP Name		Pin #	LVDS Name	MIPI DSI Name	eDP Name
S125	~~LVDS0_0+~~	DSI0_D0+	~~eDP0_TX0+~~		S111	~~LVDS1_0+~~	DSI1_D0+	~~eDP1_TX0+~~
S126	~~LVDS0_0-~~	DSI0_D0-	~~eDP0_TX0-~~		S112	~~LVDS1_0-~~	DSI1_D0-	~~eDP1_TX0-~~
S128	~~LVDS0_1+~~	DSI0_D1+	~~eDP0_TX1+~~		S114	~~LVDS1_1+~~	DSI1_D1+	~~eDP1_TX1+~~
S129	~~LVDS0_1-~~	DSI0_D1-	~~eDP0_TX1-~~		S115	~~LVDS1_1-~~	DSI1_D1-	~~eDP1_TX1-~~
S131	~~LVDS0_2+~~	DSI0_D2+	~~eDP0_TX2+~~		S117	~~LVDS1_2+~~	DSI1_D2+	~~eDP1_TX2+~~
S132	~~LVDS0_2-~~	DSI0_D2-	~~eDP0_TX2-~~		S118	~~LVDS1_2-~~	DSI1_D2-	~~eDP1_TX2-~~
S137	~~LVDS0_3+~~	DSI0_D3+	~~eDP0_TX3+~~		S120	~~LVDS1_3+~~	DSI1_D3+	~~eDP1_TX3+~~
S138	~~LVDS0_3-~~	DSI0_D3-	~~eDP0_TX3-~~		S121	~~LVDS1_3-~~	DSI1_D3-	~~eDP1_TX3-~~
S134	~~LVDS0_CK+~~	DSI0_CLK+	~~eDP0_AUX+~~		S108	~~LVDS1_CK+~~	DSI1_CLK+	~~eDP1_AUX+~~
S135	~~LVDS0_CK-~~	DSI0_CLK-	~~eDP0_AUX-~~		S109	~~LVDS1_CK-~~	DSI1_CLK-	~~eDP1_AUX-~~
S133	~~LCD0_VDD_EN~~	LCD0_VDD_EN	~~LCD0_VDD_EN~~		S116	~~LCD1_VDD_EN~~	LCD1_VDD_EN	~~LCD1_VDD_EN~~
S127	~~LCD0_BKLT_EN~~	LCD0_BKLT_EN	~~LCD0_BKLT_EN~~		S107	~~LCD1_BKLT_EN~~	LCD1_BKLT_EN	~~LCD1_BKLT_EN~~
S141	~~LCD0_BKLT_PWM~~	LCD0_BKLT_PWM	~~LCD0_BKLT_PWM~~		S122	~~LCD1_BKLT_PWM~~	LCD1_BKLT_PWM	~~LCD1_BKLT_PWM~~
S144		DSI0_TE	~~eDP0_HPD~~		S113	-	DSI1_TE	~~eDP1_HPD~~
					S139	~~I2C_LCD_CK~~	I2C_LCD_CK	~~I2C_LCD_CK~~
					S140	I2C_LCD_DAT	~~I2C_LCD_DAT~~	~~I2C_LCD_DAT~~

4.3.1.1 DSI0 Mode

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
DSI0_D0+ DSI0_D0- DSI0_D1+ DSI0_D1- DSI0_D2+ DSI0_D2- DSI0_D3+ DSI0_D3-	S125 S126 S128 S129 S131 S132 S137 S138	Primary DSI panel differential pair data lines	O D-PHY		Runtime		No blocking capacitors or termination required. Layout for 90 Ohms differential impedance.
DSI0_CLK+ DSI0_CLK-	S134 S135	Primary DSI panel differential pair clock lines.	O D-PHY		Runtime		
LCD0_VDD_EN	S133	Primary panel power enable	O CMOS	1.8V	Runtime		Active high
LCD0_BKLT_EN	S127	Primary panel backlight enable	O CMOS	1.8V	Runtime		Active high
LCD0_BKLT_PWM	S141	Primary panel brightness control through pulse width modulation (PWM)	O CMOS	1.8V	Runtime		Through pulse width modulation (PWM)
DSI0_TE	S144	Primary DSI panel tearing effect signal	I CMOS	1.8V	Runtime	1M PD	
I2C_LCD_DAT	S140	DDC data line used for flat panel detection and control	I/O OD CMOS	1.8V	Runtime	PU 2k2	
I2C_LCD_CK	S139	DDC clock line used for flat panel detection and control	O OD CMOS	1.8V	Runtime	PU 2k2	

4.4 Secondary Display Interface

4.4.1 HDMI Mode

HDMI is bridged from DSI0/1 with a Lontium LT9611UXC DSI2HDMI 4K chip

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
HDMI_D2+ HDMI_D2- HDMI_D1+ HDMI_D1- HDMI_D0+ HDMI_D0-	P92 P93 P95 P96 P98 P99	HDMI port, differential pair data lines	O TMDS HDMI		Runtime		AC coupled off module
HDMI_CK+ HDMI_CK-	P101 P102	HDMI port, differential pair clock lines	O TMDS HDMI		Runtime		AC coupled off module
HDMI_CTRL_CK	P105	I2C_CLK line dedicated to HDMI	O OD COMS	1.8V	Runtime	PU 100K	Level shifter FET and 5V PU resistor shall be placed between the Module and the HDMI connector. Stronger pull-up is demanded to the carrier board. The pull-ups may be part of an integrated HDMI ESD protection and control-line level shift device, such as the Texas Instruments TPD12S016. If discrete Carrier pull-ups are used, the value depends on the individual carrier board implementation.
HDMI_CTRL_DAT	P106	I2C_DAT line dedicated to HDMI	I/O OD CMOS	1.8V	Runtime	PU 100K	Level shifter FET and 5V PU resistor shall be placed between the Module and the HDMI connector. Stronger pull-up is demanded to the carrier board. The pull-ups may be part of an integrated HDMI ESD protection and control-line level shift device, such as the Texas Instruments TPD12S016. If discrete Carrier pull-ups are used, the value depends on the individual carrier board implementation.
HDMI_HPD	P104	HDMI Hot plug active high detection signal that serves as an interrupt request	I CMOS	1.8V	Runtime	PD 1M	Important: Module shall tolerate high level in stand-by mode

4.4.2 MIPI Camera Support

4.4.2.1 CSI0 (2 lanes)

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CSI0_RX0+ CSI0_RX0- CSI0_RX1+ CSI0_RX1-	S11 S12 S14 S15	CSI0 differential input (point to point)	I D-PHY / I M-PHY		Runtime		
CSI0_CK+ CSI0_CK-	S8 S9	CSI0 differential clock intput (point to point)	I D-PHY		Runtime		
I2C_CAM0_DAT /CSI0_TX-	S7	I2C data for serial camera data support link or differential data lane	I/O OD CMOS / O M-PHY	1.8V	Runtime	PU 2.2k	MIPI-CSI 2.0 uses I2C_CAM0_DAT which requires PU MIPI-CSI 3.0 uses CSI0_TX-, no PU required
I2C_CAM0_CK / CSI0_TX+	S5	I2C clock for serial camera data support link or differential data lane	O OD CMOS / O M-PHY	1.8V	Runtime	PU 2.2k	MIPI-CSI 2.0 uses I2C_CAM0_CK which requires PU MIPI-CSI 3.0 uses CSI0_TX+, no PU required
CAM0_PWR# / GPIO0	P108	Camera 0 Power Enable, active low output.	O CMOS	1.8V	Runtime	PU 470k	Shared with GPIO0
CAM0_RST# / GPIO2	P110	Camera 0 reset, active low output	O CMOS	1.8V	Runtime	PU 470k	Shared with GPIO2
CAM_MCK	S6	Master clock output	O CMOS	1.8V	Runtime		

4.4.2.2 CSI1 (4 lanes)

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CSI1_RX0+ CSI1_RX0- CSI1_RX1+ CSI1_RX1- CSI1_RX2+ CSI1_RX2- CSI1_RX3+ CSI1_RX3-	P7 P8 P10 P11 P13 P14 P16 P17	CSI1 differential input	I LVDS D-PHY / I LVDS M-PHY		Runtime		
CSI1_CK+ CSI1_CK-	P3 P4	CSI1 differential clock input (point to point)	I LVDS D-PHY		Runtime		
I2C_CAM1_DAT / CSI1_TX-	S2	I2C data for serial camera data support link or differential data lane	I/O OD CMOS / O LVDS M-PHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 uses I2C_CAM0_DAT which requires PU MIPI-CSI 3.0 uses CSI0_TX-, no PU required
I2C_CAM1_CK / CSI1_TX+	S1	I2C clock for serial camera data support link or differential data lane	O OD CMOS / O LVDS M-PHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 uses I2C_CAM0_CK which requires PU MIPI-CSI 3.0 uses CSI0_TX+, no PU required
CAM1_PWR# / GPIO1	P109	Camera 1 Power Enable, active low output.	O CMOS	1.8V	Runtime	PU 470k	Shared with GPIO1
CAM1_RST# / GPIO3	P111	Camera 1 reset, active low output	O CMOS	1.8V	Runtime	PU 470k	Shared with GPIO 3
CAM_MCK	S6	Master clock output	O CMOS	1.8V	Runtime		

Note: LEC-RB5 has support for up to 6 cameras. CSI 0,1 go to the carrier while CSI 2,3,4,5 are located on feature connectors of the module.

4.4.3 CSI Feature Connectors

All feature connectors use a 22-pin FPC to connect the camera module, the 22-pin connector has a 0.5mm pin pitch.

Name	Pin #	Description
GND	**1**	Ground
CAM_D0_N	**2**	MIPI Data Lane 0 Negative
CAM_D0_P	**3**	MIPI Data Lane 0 Positive
GND	**4**	Ground
CAM_D1_N	**5**	MIPI Data Lane 1 Negative
CAM_D1_P	**6**	MIPI Data Lane 1 Positive
GND	**7**	Ground
CAM_CK_N	**8**	MIPI Clock Lane Negative
CAM_CK_P	**9**	MIPI Clock Lane Positive
GND	**10**	Ground
CAM_D2_N	**11**	MIPI Data Lane 2 Negative
CAM_D2_P	**12**	MIPI Data Lane 2 Positive
GND	**13**	Ground
CAM_D3_N	**14**	MIPI Data Lane 3 Negative
CAM_D3_P	**15**	MIPI Data Lane 3 Positive
GND	**16**	Ground
CAM_IO0	**17**	Power Enable
CAM_IO1	**18**	LED Indicator
GND	**19**	Ground
CAM_SCL	**20**	I2C SCL
CAM_SDA	**21**	I2C SDA
CAM_3V3	**22**	3.3V Power Output

4.5 Audio Interfaces

4.5.1 I2S0

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
I2S0_LRCK	S39	I2S0 Left & Right synchronization clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
I2S0_SDOUT	S40	I2S0 Digital audio Output	O CMOS	1.8V	Runtime		
I2S0_SDIN	S41	I2S0 Digital audio Input	I CMOS	1.8V	Runtime		
I2S0_CK	S42	I2S0 Digital audio clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
AUDIO_MCK	S38	Master clock output to I2S codec(s)	O CMOS	1.8V	Runtime		Shared with I2S2

Note: I2S1 signalling has been removed during update to SMARC 2.0 specification

4.6 USB Ports

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
USB0+ USB0-	P60 P61	USB differential data pairs for port 0	I/O USB	USB	Standby		From SOC
USB0_EN_OC#	P62	USB over-current sense for port 0	I/O OD CMOS	3.3V note 1	Standby	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB0_VBUS_DET	P63	USB port 0 host power detection, when this port is used as a device.	I USB VBUS 5V	USB VBUS 5V	Standby		When this Port is used as a device it can be connected to a USB client port VBUS pin
USB0_OTG_ID	P64	Input pin to announce OTG device insertion on USB 2.0 port			Standby		Resistor value to ground according to USB specification
USB1+ USB1-	P65 P66	USB differential data pairs for port 1	I/O USB	USB	Standby		From SOC
USB1_EN_OC#	P67	USB over-current sense for port 1	I/O OD CMOS	3.3V note 1	Standby	PU 10k	Pulled low by Module OD driver to disable USB1 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB2+ USB2-	P69 P70	USB differential data pairs for port 2	I/O USB	USB	Standby		From USB 3.0 Hub
USB2_SSRX+ USB2_SSRX-	S74 S75	Receive signal differential pairs for SuperSpeed on port 2	I USB SS	USB SS	Standby		DC blocking capacitors 100nF ***shall*** be placed on the Carrier
USB2_SSTX+ USB2_SSTX-	S71 S72	Transmit signal differential pairs for SuperSpeed on port 2	O USB SS	USB SS	Standby		DC blocking capacitors 100nF ***shall*** be placed on the Carrier
USB2_EN_OC#	P71	USB over-current sense for port 2	I/O OD CMOS	3.3V note 1	Standby	PU 10k	Pulled low by Module OD driver to disable USB2 power. Pulled low by Carrier OD driver to indicate over-current situation.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
USB3+ USB3-	S68 S69	USB differential data pairs for port 3	I/O USB	USB	Standby		From USB 3.0 HUB
USB3_SSRX+ USB3_SSRX-	S65 S66	Receive signal differential pairs for SuperSpeed on port 3	I USB SS	USB SS	Standby		DC blocking capacitors 100nF shall be placed on the Carrier
USB3_SSTX+ USB3_SSTX-	S62 S63	Transmit signal differential pairs for SuperSpeed on port 3	O USB SS	USB SS	Standby		DC blocking capacitors 100nF shall be placed on the Carrier
USB3_EN_OC#	P74	USB over-current sense for port 3	I/O OD CMOS	3.3V note 1	Standby	PU 10k	Pulled low by Module OD driver to disable USB3 power. Pulled low by Carrier OD driver to indicate over-current situation.
~~USB3_VBUS_DET~~	~~S37~~	~~USB port 3 host power detection, when this port is used as a device.~~	~~I USB VBUS 5V~~	~~USB VBUS 5V~~	~~Standby~~	-	-
~~USB3_OTG_ID~~	~~S104~~	~~Input pin to announce OTG device insertion on USB 3.0 port~~	~~I CMOS~~	~~3.3V~~	~~Standby~~	-	-
USB4+ USB4-	S35 S36	USB differential data pairs for port 4	I/O USB	USB	Standby		From SOC
USB4_EN_OC#	P76	USB over-current sense for port 4	I/O OD CMOS	3.3V note 1	Standby	PU 10k	Pulled low by Module OD driver to disable USB4 power. Pulled low by Carrier OD driver to indicate over-current situation.
~~USB5+ USB5-~~	~~S59 S60~~	~~USB differential data pairs for port 5~~	~~I/O USB~~	~~USB~~	~~Standby~~	-	
~~USB5_EN_OC#~~	~~S55~~	~~USB over-current sense for port 5~~	~~I/O OD CMOS~~	~~3.3V~~ note 1	~~Standby~~	~~PU 10k~~	Pulled low by Module OD driver to disable USB5 power. Pulled low by Carrier OD driver to indicate over-current situation.

Note:

1. 3.3V or switched 3.3V: if a USB channel is not used, then USB[0:5]_EN_OC# pull-up rails may be held at GND to prevent current leakage.
2. USB0 is directly connected to the SoC and offers OTG, while others use a shared bandwidth through a USB 2.0/3.1HUB.

4.7 PCIe Ports

PORT A – Dual lane PCIe Gen 3.0

PORT B – Second lane

PORT C – Dual lane PCIe Gen 3.0

PORT D – second lane

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
PCIE_A_TX+ PCIE_A_TX-	P89 P90	Differential PCIe link A transmit data pair	O LVDS PCIE		Runtime		Series AC coupled on module
PCIE_A_RX+ PCIE_A_RX-	P86 P87	Differential PCIe link A receive data pair	I LVDS PCIE		Runtime		Series AC coupled off module
PCIE_A_REFCK+ PCIE_A_REFCK-	P83 P84	Differential PCIe Link A reference clock output	O LVDS PCIE		Runtime		
PCIE_A_RST#	P75	PCIe Port A reset output	O CMOS	3.3V	Runtime		
PCIE_A_CKREQ#	P78	PCIe Port A clock request	I OD CMOS	3.3V	Runtime		Can be used for power saving mode on PCIe - Pulled up or terminated on Module
PCIE_B_TX+ PCIE_B_TX-	S90 S91	Differential PCIe link B transmit data pair	O LVDS PCIE		Runtime		Series AC coupled on module
PCIE_B_RX+ PCIE_B_RX-	S87 S88	Differential PCIe link B receive data pair	I LVDS PCIE		Runtime		Series AC coupled off module
PCIE_B_REFCK+ PCIE_B_REFCK-	S84 S85	Differential PCIe Link B reference clock output	O LVDS PCIE		Runtime		
PCIE_B_RST#	S76	PCIe Port B reset output	O CMOS	3.3V	Runtime		
PCIE_B_CKREQ#	P77	PCIe Port B clock request	I OD CMOS	3.3V	Runtime		Can be used for power saving mode on PCIe - Pulled up or terminated on Module

PCIE_C_TX+ PCIE_C_TX-	S81 S82	Differential PCIe link C transmit data pair	O LVDS PCIE		Runtime		Series AC coupled on module
PCIE_C_RX+ PCIE_C_RX-	S78 S79	Differential PCIe link C receive data pair	I LVDS PCIE		Runtime		Series AC coupled off module
~~PCIE_C_REFCK+ PCIE_C_REFCK-~~	~~P80 P81~~	~~Differential PCIe Link C reference clock output~~	~~O LVDS PCIE~~	~~-~~	~~Runtime~~		
~~PCIE_C_RST#~~	~~S77~~	~~PCIe Port C reset output~~	~~O CMOS~~	~~3.3V~~	~~Runtime~~		

4.8 UART

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SER0_TX	P129	Asynchronous serial data output port 0	O CMOS	1.8V	Runtime		
SER0_RX	P130	Asynchronous serial data input port 0	I CMOS	1.8V	Runtime		
SER0_RTS#	P131	"Request to Send" handshake line for port 0	O CMOS	1.8V	Runtime		
SER0_CTS#	P132	"Clear to Send" handshake line for port 0	I CMOS	1.8V	Runtime		
SER1_TX	P134	Asynchronous serial data output port 1	O CMOS	1.8V	Runtime		
SER1_RX	P135	Asynchronous serial data input port 1	I CMOS	1.8V	Runtime		

SER2_TX	P136	Asynchronous serial data output port 2	O CMOS	1.8V	Runtime	-	-
SER2_RX	P137	Asynchronous serial data input port 2	I CMOS	1.8V	Runtime	-	-
SER2_RTS#	P138	"Request to Send" handshake line for port 2	O CMOS	1.8V	Runtime	-	-
SER2_CTS#	P139	"Clear to Send" handshake line for port 2	I CMOS	1.8V	Runtime	-	-

4.9 Dual LAN Ports

4.9.1 GBE0

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	P30 P29 P27 P26 P24 P23 P20 P19	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations	I/IO GBE MDI		Standby		Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000 100 10 _ MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-
GBE0_LINK100#	P21	Link Speed Indication LED for GBE 0 100Mbps	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current
GBE0_LINK1000#	P22	Link Speed Indication LED for GBE 0 1000Mbps	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current
GBE0_LINK_ACT#	P25	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current
~~GBE0_CTREF~~	~~P28~~	~~Center-Tap reference voltage for Carrier board Ethernet magnetic (if required by the Module GBE PHY)~~	~~Analog~~	~~0 to 3.3V max~~	~~Standby~~	-	-
~~GBE0_SDP~~	~~P6~~	~~IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol)~~	~~IO CMOS~~	~~3.3V~~	~~Standby~~	-	-

Note: LAN ports are derived from USB. There are no native LAN port in the QRB5165 SoC

4.9.2 GBE1

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GBE1_MDI0+ GBE1_MDI0- GBE1_MDI1+ GBE1_MDI1- GBE1_MDI2+ GBE1_MDI2- GBE1_MDI3+ GBE1_MDI3-	S17 S18 S20 S21 S23 S24 S26 S27	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations	I/IO GBE MDI		Standby		Gigabit Ethernet Controller 1: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000 100 10 MDI[0]+/- B1_DA+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-
GBE1_LINK100#	S19	Link Speed Indication LED for GBE 1 100Mbps	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current
GBE1_LINK1000#	S22	Link Speed Indication LED for GBE 1 1000Mbps	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current
GBE1_LINK_ACT#	S31	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current
~~GBE1_CTREF~~	~~S28~~	~~Center-Tap reference voltage for Carrier board Ethernet magnetic `~~ ~~(if required by the Module GBE PHY)`~~	~~Analog~~	~~0 to 3.3V max~~	~~Standby~~	-	-
~~GBE1_SDP~~	~~P5~~	~~IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol)~~	~~IO CMOS~~	~~3.3V~~	~~Standby~~	-	-

Note: LAN ports are derived from USB. There are no native LAN port in the QRB5165 SoC

4.10 SDIO Card (4-bit)

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SDIO_D0 SDIO_D1 SDIO_D2 SDIO_D3	P39 P40 P41 P42	SDIO Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
SDIO_WP	P33	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I OD CMOS	3.3V	Runtime	PU 10k	Pulled up on module
SDIO_CMD	P34	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
SDIO_CD#	P35	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	I OD CMOS	3.3V	Runtime	PU 10k	Pulled up on module
SDIO_CK	P36	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	O CMOS	1.8V or 3.3V	Runtime		
SDIO_PWR_EN	P37	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	O CMOS	3.3V	Runtime		should be driven low in STB Mode by the module

4.11 SPI interfaces

4.11.1 SPI0

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SPI0_CS0#	P43	SPI0 Master Chip Select 0	O CMOS	1.8V	Standby		
~~SPI0_CS1#~~	~~P31~~	~~SPI0 Master Chip Select 1~~	~~O CMOS~~	~~1.8V~~	~~Standby~~		
SPI0_CK	P44	SPI0 Clock	O CMOS	1.8V	Standby		
SPI0_DIN	P45	SPI0 Master input / Slave output	I CMOS	1.8V	Standby		also referred to as MISO
SPI0_DO	P46	SPI0 Master output / Slave input	O CMOS	1.8V	Standby		also referred to as MOSI

4.11.2 SPI1

SPI Mode

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SPI1_CS0#	P54	SPI1 Master Chip Select 0	O CMOS	1.8V	Standby		
~~SPI1_CS1#~~	~~P55~~	~~SPI1 Master Chip Select 1~~	~~O CMOS~~	~~1.8V~~	~~Standby~~	~~-~~	~~can also be used as ESPI_CS1#~~
SPI1_CK	P56	SPI1 Clock	O CMOS	1.8V	Standby		can also be used as ESPI_CK
SPI1_DIN	P57	SPI1 Master input / Slave output	I CMOS	1.8V	Standby		also referred to as MISO can also be used as ESPI_IO_1
SPI1_DO	P58	SPI1 Master output / Slave input	O CMOS	1.8V	Standby		also referred to as MOSI can also be used as ESPI_IO_0

4.12 GPIO

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GPIO0 / CAM0_PWR#	P108	General purpose I/O pin 0.	I/O CMOS	1.8V	Runtime	PU 470k [1]	alternate use is Camera 0 Power Enable, active low output
GPIO1 / CAM1_PWR#	P109	General purpose I/O pin 1.	I/O CMOS	1.8V	Runtime	PU 470k [1]	alternate use is Camera 1 Power Enable, active low output
GPIO2 / CAM0_RST#	P110	General purpose I/O pin 2.	I/O CMOS	1.8V	Runtime	PU 470k [1]	alternate use is Camera 0 Reset, active low output
GPIO3 / CAM1_RST#	P111	General purpose I/O pin 3.	I/O CMOS	1.8V	Runtime	PU 470k [1]	alternate use is Camera 1 Reset, active low output
GPIO4 / HDA_RST#	P112	General purpose I/O pin 4.	I/O CMOS	1.8V	Runtime	PU 470k [1]	alternative use is HD Audio Reset, active low output
GPIO5 / PWM_OUT	P113	General purpose I/O pin 5.	I/O CMOS	1.8V	Runtime	PU 470k [1]	alternate use is PWM output
GPIO6 / TACHIN	P114	General purpose I/O pin 6.	I/O CMOS	1.8V	Runtime	PU 470k [1]	FAN Tachometer input (used with GPIO5 PWM_OUT)
GPIO7	P115	General purpose I/O pin 7.	I/O CMOS	1.8V	Runtime	PU 470k [1]	
GPIO8	P116	General purpose I/O pin 8.	I/O CMOS	1.8V	Runtime	PU 470k [1]	
GPIO9	P117	General purpose I/O pin 9.	I/O CMOS	1.8V	Runtime	PU 470k [1]	
GPIO10	P118	General purpose I/O pin 10.	I/O CMOS	1.8V	Runtime	PU 470k [1]	
GPIO11	P119	General purpose I/O pin 11.	I/O CMOS	1.8V	Runtime	PU 470k [1]	
GPIO12	S142	General purpose I/O pin 12	I/O CMOS	1.8V	Runtime	PU 470k [1]	advised as INT signal to any expander on carrier.
GPIO13	S123	General purpose I/O pin 13	I/O CMOS	1.8V	Runtime	PU 470k [1]	

Note: In-SoC Pull-Ups allowed. These can be ≤ 10k. Max 2.2k PD should be implemented on Carrier if a low level needs to be ensured.

4.13 CAN Bus

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CAN0_TX	P143	CAN port 0 Transmit output	O CMOS	1.8V	Runtime		
CAN0_RX	P144	CAN port 0 Receive input	I CMOS	1.8V	Runtime		

Note: CAN bus is derived from SPI to CAN adapter (BOM option).

4.14 Miscellaneous

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
TEST#	S157	Held Low by Carrier to Invoke Module Vendor Specific Test Functions	I OD CMOS	1.8 to 5 V	Runtime	PU	Module must implement PU but actual value is depended on particular Module design. Carrier Board should leave this pin floating for normal operation. Driven by OD on Carrier
WDT_TIME_OUT#	S145	Watch-Dog-Timer Output, low active.	O CMOS	1.8V	Runtime		
PWM_OUT / GPIO5	P113	Pulse Width Modulation (PWM) output	I/O CMOS	1.8V	Runtime	PU 470k	PWM is the default pin configuration

4.15 Power and System Management

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
BATLOW#	S156	Battery low indication to Module. Carrier to float the line in inactive state.	I OD CMOS	1.8V to 5V	Standby/ Sleep	PU 10k	Driven by OD on Carrier. Pulled up on module.
CARRIER_PWR_ON	S154	Carrier Board circuits (apart from power management and power path circuits) ***should not*** be powered up until the Module asserts the CARRIER_PWR_ON signal.	O CMOS	1.8V	Standby		On x86 designs this pin should utilize a standby related power signal i.e. RSM_RST# or SLP_A# signal.
CARRIER_STBY#	S153	The Module ***shall*** drive this signal low when the system is in a standby power state.	O CMOS	1.8V	Standby		On x86 designs this pin should utilize the SUS_S3# signal.
CHARGER_PRSNT#	S152	Held low by Carrier if DC input for battery charger is present.	I OD CMOS	1.8V to 5V	Standby/ Sleep	PU 10k	Driven by OD on Carrier. Pulled up on module.
CHARGING#	S151	Held low by Carrier during battery charging. Carrier to float the line when charge is complete.	I OD CMOS	1.8V to 5V	Standby/ Sleep	PU 10k	Driven by OD on Carrier. Pulled up on module.
VIN_PWR_BAD#	S150	Power bad indication from Carrier Board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) ***shall not*** be enabled while this signal is held low by the Carrier.	I OD CMOS	VDD_IN		PU 10k	Driven by OD on Carrier Module must implement PU but actual value is depended on particular module design.
SLEEP#	S149	Sleep indicator from Carrier Board. ***May*** be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. ***Should*** be de-bounced on the Module.	I OD CMOS	1.8V to 5V	Standby	PU 10k	Driven by OD on Carrier. Pulled up on module.
LID#	S148	Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. ***Should*** be de-bounced on the Module.	I OD CMOS	1.8V to 5V	Standby	PU 10k	Driven by OD on Carrier. Pulled up on module.
POWER_BTN#	P128	Power-button input from Carrier Board. Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module.	I OD CMOS	1.8V to 5V	Standby	PU 10k	Driven by OD on Carrier. Pulled up on module.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
POWER_BTN#	P128	Power-button input from Carrier Board. Carrier to float the line in in-active state. Active low, level sensitive. ***Should*** be debounced on the Module.	I OD CMOS	1.8V to 5V	Standby	PU 10k	Driven by OD on Carrier. Pulled up on module.
RESET_OUT#	P126	General purpose reset output to Carrier board.	O CMOS	1.8V	Standby		
RESET_IN#	P127	Reset input from Carrier Board. Carrier drives low to force a Module reset, floats the line otherwise. This signal ***Shall*** be level triggered during bootup to allow to stop booting of the module. After bootup it ***May*** act as an edge triggered signal.	I OD CMOS	1.8V to 5V	Standby	PU 10k	Driven by OD on Carrier. Pulled up on module.
I2C_PM_DAT	P122	Power management I2C bus DATA	I/O OD CMOS	1.8V	Standby/ Sleep	PU 2k2	On x86 systems these serve as SMB DATA. Pulled up on module.
I2C_PM_CK	P121	Power management I2C bus CLK	O OD CMOS	1.8V	Standby/ Sleep	PU 2k2	On x86 systems these serve as SMB CLK. Pulled up on module.
~~SMB_ALERT_1V8#~~	~~P1~~	~~SMBus Alert# (interrupt) signal~~	~~I OD CMOS~~	~~1.8V to 5V~~	~~Standby/ Sleep~~	~~PU 2k2~~	~~only used on x86 design~~

4.15.1 Boot Select

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
BOOT_SEL0# BOOT_SEL1# BOOT_SEL2#	P123 P124 P125	Input straps determine the Module boot	I OD CMOS	1.8V	Standby	PU 10k	Driven by OD on Carrier. Pulled up on module. booting from UFS only
FORCE_RECOV#	S155		I OD CMOS	1.8V	Standby	PU 10k	Driven by OD on Carrier. Pulled up on module. Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based Force Recovery functions, then a low on the Module FORCE_RECOV# pin may invoke the SOC native Force Recovery mode – such as over a Serial Port. For x86 systems this signal may be used to load BIOS defaults. Pulled up on Module. Driven by OD part on Carrier.

4.15.2 Power

Name	Pin #	Description	I/O Type	Power Rail / Tolerance	PU / PD	Comments
VDD_IN	P147, P148, P149, P150, P151, P152, P153, P154, P155, P156	Module power input voltage 4.75 min to 5.25V max	P Not defined within Signal Terminology Descriptions. Should we define a specific rail?	5V +/- 5%		
GND	P2, P9, P12, P15, P18, P32, P38, P47, P50, P53, P59, P68, P79, P82, P85, P88, P91, P94, P97, P100, P103, P120, P133, P142, S3, S10, S16, S25, S34, S47, S61, S64, S67, S70, S73, S80, S83, S86, S89, S92, S101, S110, S119, S124, S130, S136, S143, S158	Module signal and power return, and GND reference	P Not defined within Signal Terminology Descriptions. Should we define a specific rail?	Ground		
VDD_RTC	S147	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based Lithium cell or Super Cap.	P Not defined within Signal Terminology Descriptions. Should we define a specific rail?	[2 to 3.25] / 3.25V		

5. Software Support

5.1 Yocto

Go to www.github.com/ADLINK/meta-adlink-qualcomm for Yocto support.

5.2 Ubuntu

Standard OS

6. Mechanical

6.1 Module Dimensions

SMARC Short Size: 82x 50mm

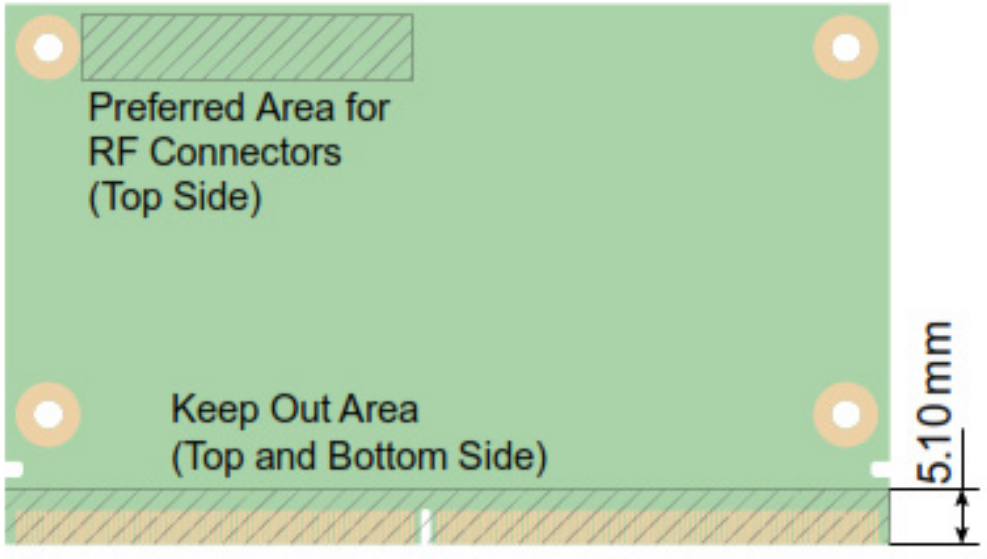

Figure 3 – Module dimensions

7. Thermal Solutions

7.1 Heatspreader – HTS

Sustainable temperature range with high performance LAB copper heatsink

with high airflow = -40~85°C ambient

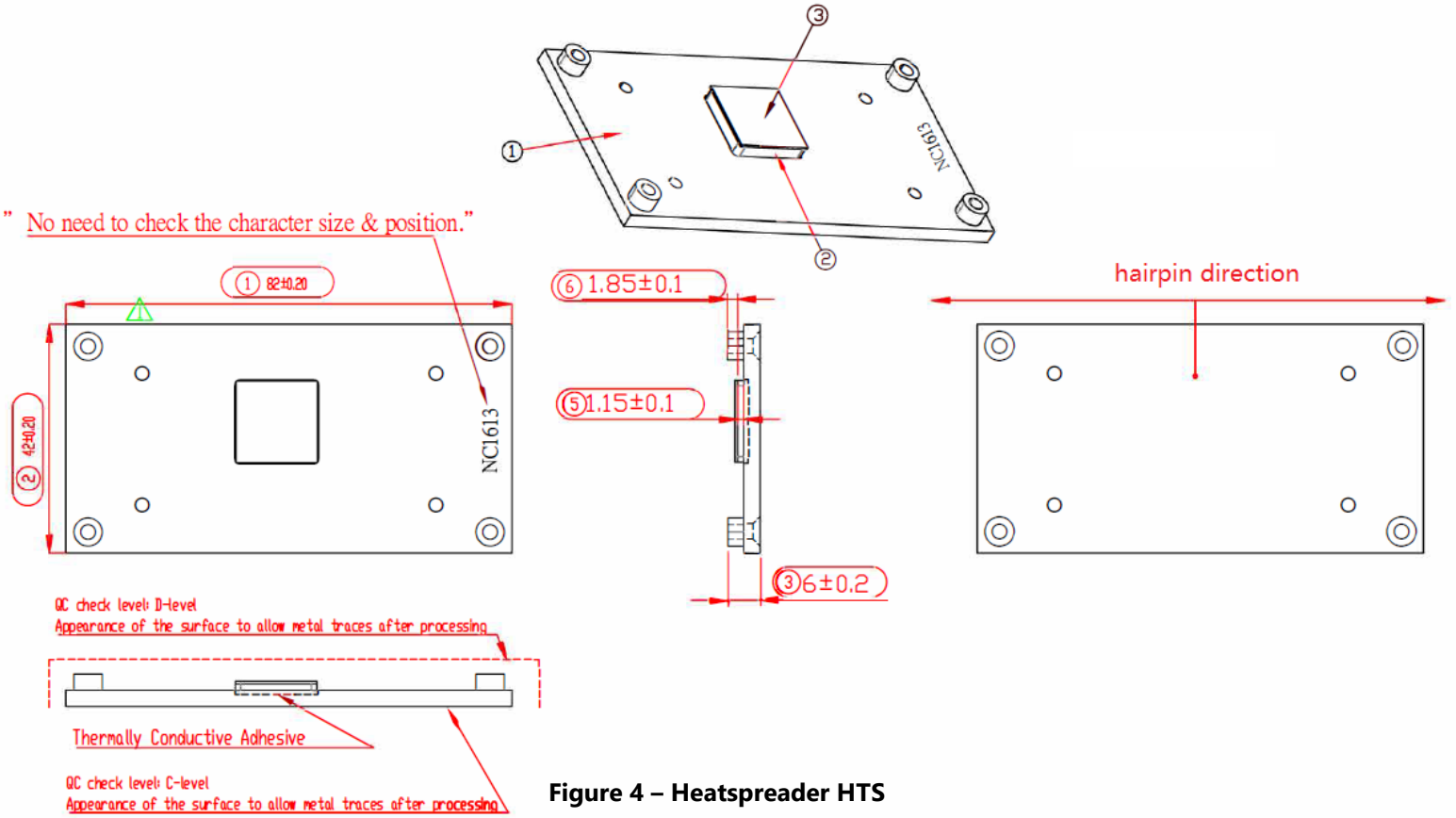

Figure 4 – Heatspreader HTS

7.2 Heatsink – THS

Sustainable temperature range with moderate airflow = 0~60°C ambient

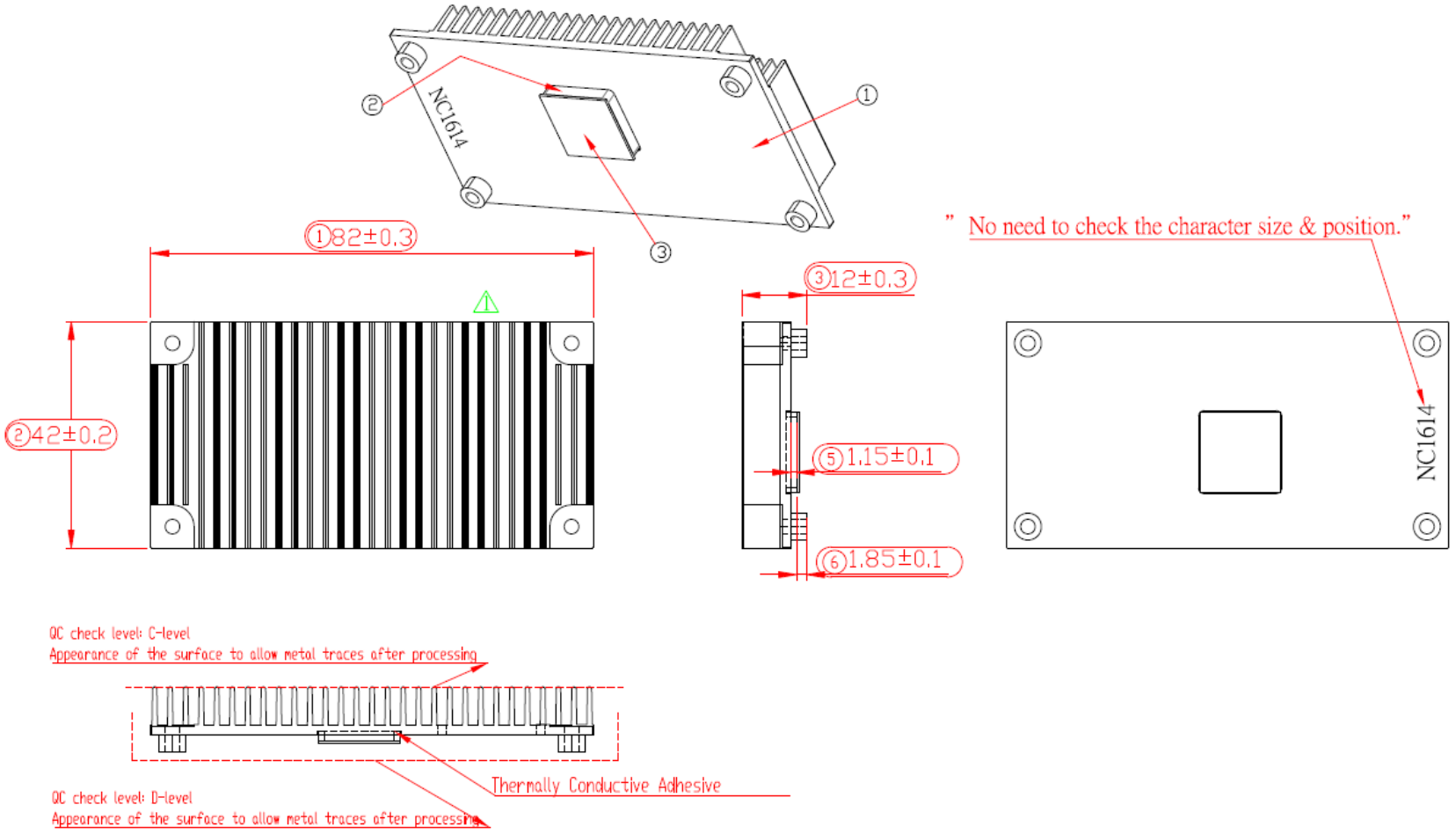

Figure 5 – Heatsink THS