VPX3-TL Series

SOSA-aligned Rugged 3U VPX Processor Blade
with Intel® Xeon® W11865MRE

User's Manual

Manual Rev.: 1.1

Revision Date: October 19, 2023

Part No: 50M-31129-1010

LEADING EDGE COMPUTING

Revision History

Revision	Release Date	Description of Change(s)
1.0	2023-07-05	Initial release
1.1	2023-10-19	Update storage specifications

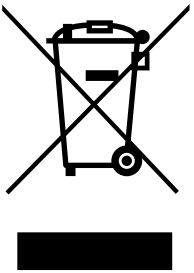
Preface

Disclaimer

The information in this document is subject to change without prior notice in order to improve reliability, design, and function and does not represent a commitment on the part of the manufacturer.

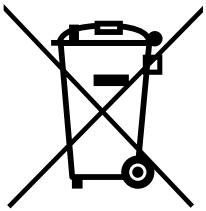
In no event will the manufacturer be liable for direct, indirect, special, incidental, or consequential damages arising out of the use or inability to use the product or documentation, even if advised of the possibility of such damages.

Environmental Responsibility



ADLINK is committed to fulfill its social responsibility to global environmental preservation through compliance with the European Union's Restriction of Hazardous Substances (RoHS) directive and Waste Electrical and Electronic Equipment (WEEE) directive. Environmental protection is a top priority for ADLINK. We have enforced measures to ensure that our products, manufacturing processes, components, and raw materials have as little impact on the environment as possible. When products are at their end of life, our customers are encouraged to dispose of them in accordance with the product disposal and/or recovery programs prescribed by their nation or company.

Battery Labels (for products with battery)



California Proposition 65 Warning

WARNING: This product can expose you to chemicals including acrylamide, arsenic, benzene, cadmium, Tris(1,3-dichloro-2-propyl)phosphate (TDCPP), 1,4-Dioxane, formaldehyde, lead, DEHP, styrene, DINP, BBP, PVC, and vinyl materials, which are known to the State of California to cause cancer, and acrylamide, benzene, cadmium, lead, mercury, phthalates, toluene, DEHP, DIDP, DnHP, DBP, BBP, PVC, and vinyl materials, which are known to the State of California to cause birth defects or other reproductive harm. For more information go to www.P65Warnings.ca.gov**.**

Trademarks

Product names mentioned herein are used for identification purposes only and may be trademarks and/or registered trademarks of their respective companies.

Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

NOTE: Additional information, aids, and tips that help users perform tasks.

CAUTION: Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

WARNING: Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

Table of Contents

List of Figures

This page intentionally left blank.

List of Tables

This page intentionally left blank.

1 Introduction

1.1 Overview

The VPX3-TL Series is a 3U VPX processor blade based on the Intel® Xeon® W11865MRE Processor (formerly "Tiger Lake-H"), supporting up to 64GB DDR4-2666 soldered ECC memory, 2x 10GBASE-KR or 2x 1GBASE-KX, one XMC expansion slot with PCIe x8 Gen3 to P1 & P2 rear I/O, USB 3.0 and SATA 6GB/s; as well as a high performance NVMe/SATA M.2 slot for storage expansion up to 1TB (by BOM option). The SOSA-aligned design offers embedded computing capabilities that are easily reconfigurable and upgradable, highly cost-effective, and quick to develop and deploy.

The VPX3-TL Series with work station grade Intel® processor brings high-bandwidth, high-powered computing and artificial intelligence to demanding applications that expose hardware to extreme temperatures, vibration, and operating conditions.

Interoperability between different systems - including Command, Control, Communications, Computers, Intelligence, Surveillance and Reconnaissance (C4ISR), electronic warfare (EW), signals intelligence (SIGINT), cognitive radio and radar - is critical. The SOSA standard is one of several standards that fall broadly within the MOSA initiative. SOSA centers on key interfaces and open standards, based on the VPX standard (VITA 46/48/65), and aims to develop a common, modular hardware architecture across next-generation, mission-critical applications.

1.2 Features

- Intel® Xeon® W11865MRE Processor (formerly “Tiger Lake-H”); up to 8 cores with 45 watt TDP
- SOSA-aligned and VITA 46/47/48/65 compliant for quick deployment
- 32GB DDR4-2666 soldered ECC SDRAM (roadmap to 64GB)
- Supports NVMe and SATA SSD up to 1TB (by BOM option)
- One XMC expansion slot with PCIe x8 Gen3
- Ethernet connectivity: 1x 2.5GBASE-T to P2; 2x 10GBASE-KR to P1; optional 2x 1GBASE-KX to P1
- 1x DisplayPort to P2, supports DP++ with resolution up to 8K/60Hz

1.3 Block Diagrams

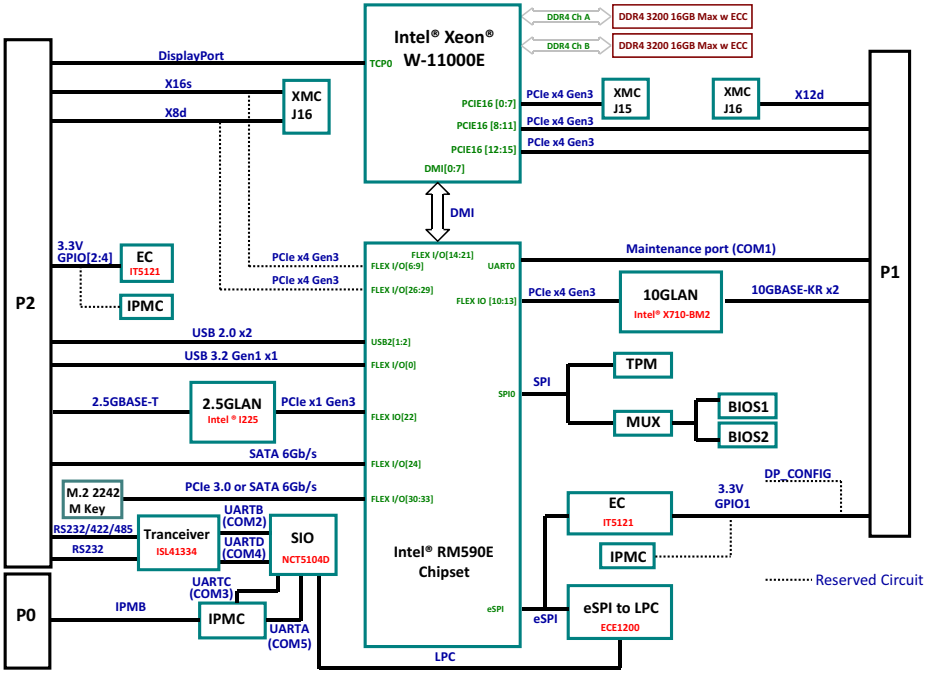


Figure 1-1: VPX3-TL Functional Block Diagram

1.4 Model Number Decoder - Processor Blade

VPX3-TL/W11865MRE/M32/XMC1.0-R2

(A) (B) (C) (D)

(A) CPU Code

- ▷ **W11865MRE** = Intel® Xeon® W11865MRE Processor, 8 cores, 45W TDP

(B) Memory Size Code

- ▷ **M32** = 32GB DDR4-2666 ECC soldered SDRAM

(C) PCI Express interface code

- ▷ **XMC1.0** = XMC 1.0 interface, 2x PCIe x4 Gen3 to P1
- ▷ **XMC2.0** = XMC 2.0 interface, 2x PCIe x4 Gen3 to P1
- ▷ **P16** = 2x PCIe x4 Gen3 to P1 + 2x PCIe x4 Gen3 to P1

(D) Ruggedized Level Code

- ▷ **R2** = Conduction Cooled version supporting -40°C to +85°C at card edge

VPX3-TL SKU Table

Function	XMC1.0	XMC2.0	P16
XMC	1.0 connector for expansion X16s+X8d to P2 and X12d to P1	2.0 connector for expansion X16s+X8d to P2 and X12d to P1	N/A
PCIe	2x PCIe x4 Gen3 to P1	2x PCIe x4 Gen3 to P1	2x PCIe x4 Gen3 to P1 2x PCIe x4 Gen3 to P2

Table 1-1: VPX3-TL SKU Table

1.5 Package Contents

The VPX3-TL is packaged with the following components. If any of the items on the contents list are missing or damaged, retain the shipping carton and packing material and contact the dealer for inspection. Please obtain authorization before returning any product to ADLINK. The packing contents of the VPX3-TL are non-standard configurations and may vary depending on customer requests.

Processor Blade

- VPX3-TL
  - CPU and memory specifications will differ depending on options selected
  - Thermal module is assembled on the board

Rear Transition Module (optional)

- VPX3-TL-RL1 RTM

Test Backplane (optional)

- tBP-VPX3-TL test backplane

The contents of non-standard VPX3-TL configurations may vary depending on the customer requirements.

This product must be protected from static discharge and physical shock. Never remove any of the components except at a static-free workstation. Use the anti-static bag shipped with the product when putting the board on a surface. Wear an anti-static wrist strap properly grounded on one of the system's ESD ground jacks when installing or servicing system components.

This page intentionally left blank.

2 Specifications

2.1 VPX3-TL Blade Specifications

VITA Standards	• VITA 46, 47, 48, 65 compliant • SOSA aligned
Module Profile	• MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15-2
Slot Profile	• SLT3-PAY-1F1F2U1TU1T1U1T- 14.2.16
Processor	• Intel® Xeon® W11865MRE, up to 8 cores, 45W TDP
Chipset	• Intel® RM590E Chipset
Memory	• 32GB DDR4 soldered with ECC (roadmap to 64GB)
USB	• 2x USB 2.0 to P2 • 1x USB 3.2 Gen1 to P2 • Supports USB 3.0 power to P1/G7 (supply 0.9A) with over current protection • Supports USB 2.0 power to P2/G9 (supply 0.5A) with over current protection
XMC	• 1x PCIe x8 to J15 • Rear I/O (X16s + X8d) to P2 and X12d to P1 from J16
Gigabit Ethernet	• 1x 2.5GBASE-T to P2 supporting PXE and Wake on LAN (WOL)
PCI Express	• 2x PCIe x4 co-layout with XMC X8d+X16s on P2 (PCIe NT function not supported)
Storage	• 1x M2. 2242 onboard (M-Key), supports NVMe and SATA • 1x SATA 6Gb/s to P2 • M.2 devices supporting spec S1, S2, S3, D1, D2, D3, D4 • M.2 capacity up to 1TB
Graphics	• 1x DisplayPort to P2 • Resolution up to 8K/60Hz • Supports passive DP to HDMI dongle with BIOS selection
GPIO	• 1x GPIO to P1 • 3x GPIO to P2 • Supports +3.3V (default) or +5V GPIO (BOM option) • GPI with edge trigger or level trigger interrupt

Table 2-1: VPX3-TL Blade Specifications

Serial	**COM1:** • 2-wire TX/RX on P1 supporting TIA-232 & LVCOMS (3.3V) mode selected by BIOS option **COM2:** • 1x RS-232/422/485 to P2 (RS232, 2-wire) • Max. data rate for RS232/422/485 is 115200bps • RS485 mode supports auto flow control • RS232/422/485 mode selected by BIOS option **COM3:** • 1x RS-232 to P2 (2-wire, available when COM2 is set RS232
TPM	• Discrete TPM 2.0 chip • Supports Intel Secure Boot (UEFI)
LEDs	• Power and SATA Activity LEDs on front panel • Reserved LED (for customer definition) • Embedded Controller Status LED on front panel
Reset Button	• On front panel
Watchdog Timer	• Provided by SEMA
Environmental	**Operating Temp.** -40°C to +85°C at wedge locks (VITA47.0, ECC4-CC4) **Storage Temp:** -55°C to +105°C **Vibration:** • Random: 12Grms, 5Hz to 2000Hz (VITA47.0, ECC4-V3) • Sinusoidal: 5g, 20Hz to 2000Hz **Shock:** 40g, 11 ms (VITA47.0, ECC4-OS2) **Relative Humidity:** 95% non-condensing **Altitude:** 60,000 ft. (operating)
EMC	• CE (EN555032 / EN55035) ; FCC Part 15B Class A

Table 2-1: VPX3-TL Blade Specifications

Note: Specifications are subject to change without prior notice.

2.2 VPX3-TL-RL1 RTM Specifications

Ethernet	• 2x 10GBASE-KR via RP1 • 1x 2.5GBASE-T via RP1
Graphics	• 1x DisplayPort signal via RP1
SATA	• 1x SATA 6Gb/s via RP1 (7-pin vertical SATA connector)
USB	• 1x USB 3.0 (backwards compatible) via RP1
Serial	• Serial Port 1: RS232 (2T2R) via RP1 (DB-9 connector) • Serial Port 2: RS232 (2T2R) via RP2 (2x5 pin header)
GPIO	• 1 bit GPIO signal via RP1, 3 bits GPIO signals via RP2
PCIe	• 1x PCIe x4 via RP0 • 2x PCIe x4 via RP1 • 2x PCIe x4 via RP2
XMC	• X12D via RP1 • X8D via RP2 • X16S via RP2
JTAG	• JTAG via RP0 (2x5 pin header)
Reset	• Reset via RP0
SMBus	• SMBus signal via RP0
Power	• Power terminal for +12V, +5V, +3.3V, GND

Table 2-2: VPX3-TL-RL1 RTM Specifications

Note: Specifications are subject to change without prior notice.

2.3 Power Consumption

This section provides information on the power consumption of the VPX3-TL when using the Intel® Xeon® W-11865MRE processor with Dual Channel 16GB DDR4-2666 soldered memory. The VPX3-TL is powered by 12V. Windows 10 idle mode power consumption was measured running BurnInTest at 100% loading. Windows 10 Max Loading power consumption was measured running Intel TAT test at 100% loading.

Processor	Xeon® W-11865MRE (2.6 GHz)
Windows Idle mode, EIST Enabled	
12V (A)	2.55
Power Cons. (W)	32.48
Windows Idle mode, EIST Disabled	
12V (A)	2.53
Power Cons. (W)	32.17
Windows Max Loading mode, EIST Enabled	
Package Power reading (TAT)	49.86
Package Temperature reading (TAT)	88
CPU DTS reading (TAT)	87
CPU frequency reading (TAT)	2867
12V (A)	6.64
Power Cons. (W)	81.83
Windows Max Loading mode, EIST Disabled	
Package Power reading (TAT)	45.72
Package Temperature reading (TAT)	83
CPU DTS reading (TAT)	82
CPU frequency reading (TAT)	2600
12V (A)	6.28
Power Cons. (W)	77.26

3 Functional Description

The following sections describe the VPX3-TL features and functions.

3.1 Processors

The Intel® Xeon® W-11865MRE is a 64-bit, multi-core processor built on 14-nanometer process technology. The processor is designed for a two-chip platform consisting of a processor and chipset. The platform enables higher performance, lower cost, easier validation, and improved x-y footprint. The processor includes an Integrated Display Engine, Processor Graphics and Integrated Memory Controller.

Features	Intel® Xeon® W-11865MRE
Configurable TDP-up Base Freq.	2.6 GHz
Configurable TDP-down Base Freq.	2.1 GHz
Max. Turbo Freq.	4.7 GHz
Last Level Cache	24MB
No. of Cores/Threads	8/16
Maximum Power (TDP[1])	45 W
$T_{Junction}$[2]	100°C

Notes:

1. The highest expected sustainable power while running known power intensive applications. TDP is not the maximum power that the processor can dissipate.
2. The maximum temperature allowed at the processor die.

Supported Technologies

- Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
- Intel® Virtualization Technology (Intel® VT-x)
- Intel® VT-x with Extended Page Tables (EPT)
- Intel® Hyper-Threading Technology
- Intel® Turbo Boost Technology
- Intel® Speed Shift Technology
- Thermal Monitoring Technologies

Interfaces

- Dual channel DDR4 memory with two channel of soldered SDRAM
- Memory DDR4 data transfer rates of 3200 MT/s
- 64-bit wide channels plus 8-bits of ECC support for each channel
- System Memory Interface I/O Voltage of 1.2V
- The PCI Express lanes are fully-compliant with the PCI Express Base Specification, Revision 3.0, including support for 8 GT/s transfer speeds.

3.2 Intel® Turbo Boost Technology

Intel Turbo Boost Technology is a feature that allows the processor to opportunistically and automatically run faster than its rated operating core and/or render clock frequency when there is sufficient power headroom, and the product is within specified temperature and current limits. The Intel Turbo Boost Technology feature is designed to increase performance of both multi-threaded and single-threaded workloads. The processor supports a Turbo mode where the processor can use the thermal capacity associated with package and run at power levels higher than TDP power for short durations. This improves the system responsiveness for short, bursty usage conditions.

Turbo Mode availability is independent of the number of active cores; however, the Turbo Mode frequency is dynamic and dependent on the instantaneous application power load, the number of active cores, user configurable settings, operating environment, and system design. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay with its TDP limit.

3.3 Chipset

The Mobile Intel® 500 Series Chipset provides extensive I/O support. Functions and capabilities include:

- PCI Express Base Specification, Revision 3.0
- Interrupt controller and timer functions
- Integrated Serial ATA host controller 3.2, supports data transfer rates up to 6Gb/s on all ports
- USB Revision 3.2/2.0
- Integrated 10/100/1000 Gigabit Ethernet MAC with System Defense
- System Management Bus (SMBus) Specification, Version 2.0 with additional support for I2C devices
- Intel® High Definition Audio
- Intel® Rapid Storage Technology
- Intel® Platform Trust Technology
- Serial Peripheral Interface (SPI) Support

3.4 USB

The VPX3-TL provides one USB 3.2 Gen1 port to the P2 connector supporting data transfers up to 5Gb/s, and one USB 2.0 port to the P2 connector supporting data transfers up to 480 Mb/s.

3.5 SPI BIOS

The VPX3-TL implements a dual BIOS feature. Each SPI flash has a capacity of 256Mb. When the main BIOS crashes, the backup BIOS will be used to boot the device.

3.6 System Management Bus

The PCH provides a System Management Bus (SMBus) Specification Version 2.0 compliant Host Controller as well as an SMBus Slave Interface. The PCH provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves) as well as I2C compatible devices.

3.7 Real Time Clock

The PCH contains a real-time clock with 256 bytes of battery-backed RAM. The internal RTC module provides two key functions: keeping the time of day and storing system data, even when the system is powered down. The RTC operates on a 32.768 KHz crystal.

3.8 Serial ATA Controller

The VPX3-TL has one SATA port capable of 6Gb/s transfers with all capable SATA devices.

3.9 PCI Express Interface

The VPX3-TL is compatible with the VPX ANSI/VITA 46.0-2007 standard. The VPX3-TL supports 1 x8 or 2 x4 PCIe bus to the XMC module and 2x PCIe x4 Gen3 to P2.

3.10 Intel ® Gigibit Ethernet Controller I225-IT

The VPX3-TL has one 2.5GBASE-T LAN interface for network access. The Intel® 2.5 Gigabit Ethernet Controller I225 is a single-port, compact, low power Gigabit Ethernet (GbE) controller. It is a fully-integrated GbE Media Access Control (MAC) and Physical Layer (PHY) device, offering 10/100/1000/2500 Mb/s data rates. The interface-to-host system is a one lane PCIe Gen 2 version 3.1.

3.11 Ethernet for 10GbE

The VPX3-TL has two 10GBASE-KR LAN interfaces for network access. The dual 10GBASE-KR is implemented via an Intel® Ethernet Controller X710-BM2, a dual-port 10GBASE-KR controller via PCIe x4 Gen3 from the TGL-H host.

3.12 Graphics

The VPX3020 provides one DisplayPort consisting of a Main Link, Auxiliary channel and a Hot-Plug Detect signal. The DisplayPort supports VESA DisplayPort 1.2 specifications.

3.13 GPIO Expander PCA9554

The VPX3-TL offers 4x GPIO pins which are configurable as input or output signals, 3.3V tolerant, and SCI (GPE) and IOAPIC interrupt capable.

3.14 UART NCT5104D

The NCT5104D is a LPC to UART IC, which supports 4 high-speed serial communication ports (UART). Each UART includes a 128-byte send/receive FIFO, a programmable baud rate generator, complete modem-control capability, and a processor interrupt system. The UART supports legacy speeds up to 115.2K bps as well as even higher baud rates of 230K, 460K, or 921K bps to support higher speed modems.

In addition to UART, the NCT5104D provides flexible I/O control functions through a set of general purpose I/O (GPIO) ports. These GPIO ports may serve as simple I/O ports or may be individually configured to provide alternative functions. The

NCT5104D supports port 80 decode on the LPC bus and could output the signal via SOUTC. It also supports LED control.

3.15 TPM

The Infineon SLB 9665 TPM 2.0 is a fully standard compliant TPM based on the latest Trusted Computing Group (TCG) specification 2.0 and features Low Pin Count (LPC) interface.

3.16 Embedded Controller

The VPX3-TL implements an ITE IT5121VG as embedded controller. The IT5121VG communicates with the host system through an eSPI v1.0 interface.

3.17 XMC Site

The VPX3-TL Series supports one XMC site for rear I/O expansion. The XMC site provides a x8 PCI Express Gen 3.0 lane. Jn2 rear XMC I/O connector is compliant to VITA 46.9, X8d+X12d+X16S.

4 VPX3-TL Board Interfaces

This chapter illustrates the board layout, connector pin assignments, and jumper settings to familiarize users with the VPX3-TL.

4.1 VPX3-TL Board Layout

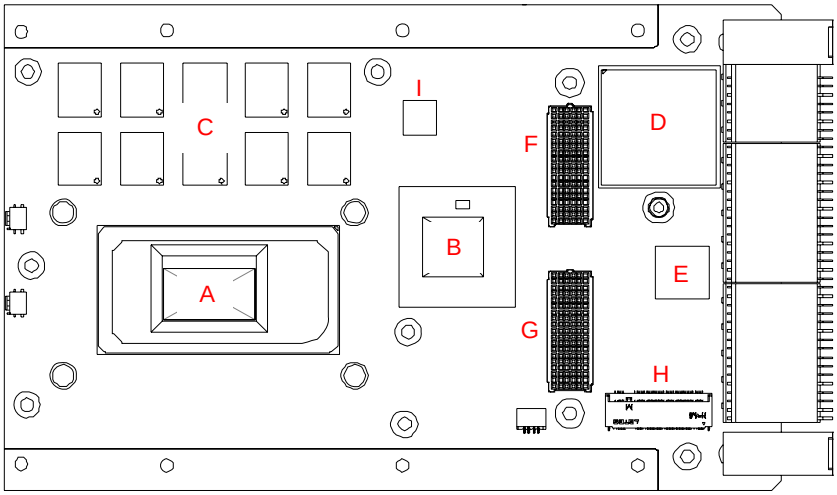


Figure 4-1: VPX3-TL Top Side Layout

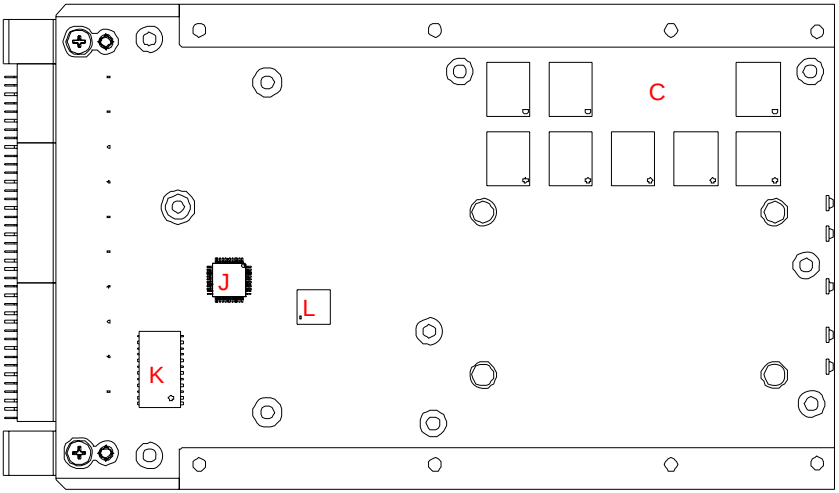


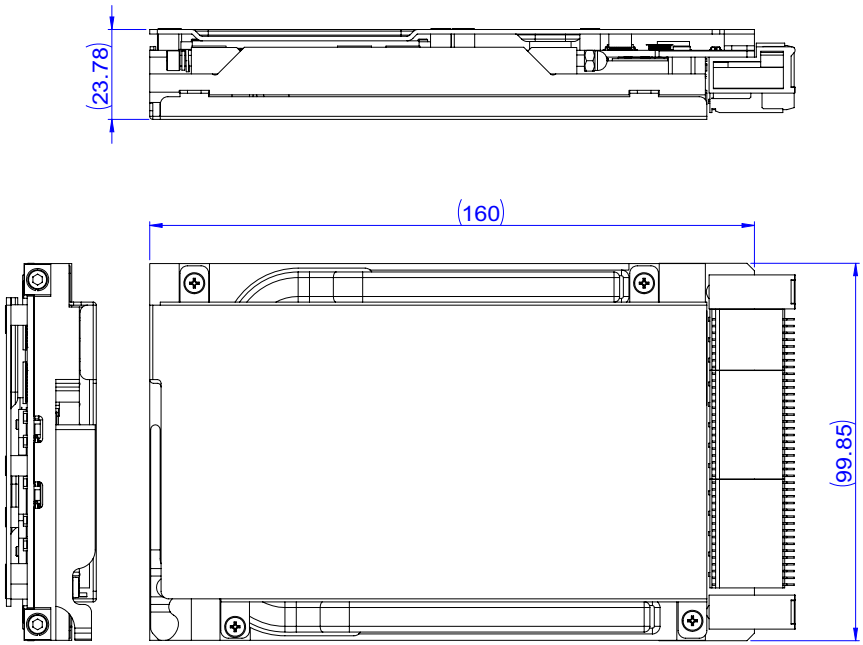
Figure 4-2: VPX3-TL Bottom Side Layout

A	CPU (W-11865MRE)	**G**	XMC Connector (X8d+X12d+X16s)
B	Chipset (PCH RM590E)	**H**	M.2 Connector (M Key)
C	DDR4 ECC Memory	**I**	Embedded Controller (IT5121)
D	Ethernet Controller (FTX710-BM2)	**J**	Super IO (NCT5104D)
E	IPMC	**K**	LAN Transformer
F	XMC Primary Connector	**L**	Ethernet Controller (I215IT)

Table 4-1: VPX3-TL Board Layout Legend

4.2 VPX3-TL Mechanical Dimensions

Conduction-Cooled Version

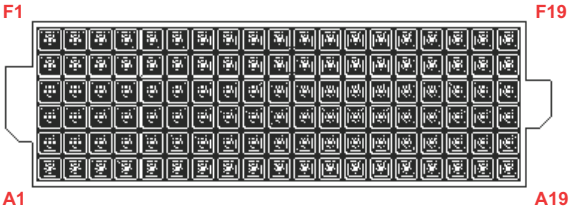


Dimensions in mm

Figure 4-3: VPX3-TL Conduction-Cooled Mechanical Dimensions

4.3 VPX3-TL Connector Pin Assignments

XMC Connectors



JN15 Connector Pin Definition (Primary)

Pin	A	B	C	D	E	F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR
2	GND	GND	TRST#	GND	GND	RESET#
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR
4	GND	GND	TCK	GND	GND	PULL UP
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR
6	GND	GND	TMS	GND	GND	12V_AUX
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR
8	GND	GND	TDI	GND	GND	-12V_AUX
9	NC	NC	NC	NC	NC	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	PER0p0	PER0n0	MBIST#	PER0p1	PER0n1	VPWR
12	GND	GND	GA1	GND	GND	PRSNT#
13	PER0p2	PER0n2	3.3V_AUX	PER0p3	PER0n3	VPWR
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	NC	PER0p5	PER0n5	VPWR
16	GND	GND	XMC_NVMRO	GND	GND	MSCL
17	PER0p6	PER0n6	NC	PER0p7	PER0n7	NC
18	GND	GND	NC	GND	GND	NC
19	REF_CLK+	REF_CLK-	NC	WAKE#	NC	NC

NOTE:

The signal definitions of the primary XMC connector (J15) are presented relative to the XMC Mezzanine card.

J16 Connector Pin Definition (X8d+X12d+X16s)

Pin	A	B	C	D	E	F
1	XMC_A1+	XMC_B1-	NC	XMC_D1+	XMC_E1-	NC
2	GND	GND	NC	GND	GND	NC
3	XMC_A3+	XMC_B3-	NC	XMC_D3+	XMC_E3-	NC
4	GND	GND	NC	GND	GND	NC
5	XMC_A5+	XMC_B5-	NC	XMC_D5+	XMC_E5-	NC
6	GND	GND	NC	GND	GND	NC
7	XMC_A7+	XMC_B7-	NC	XMC_D7+	XMC_E7-	NC
8	GND	GND	NC	GND	GND	NC
9	XMC_A9+	XMC_B9-	NC	XMC_D9+	XMC_E9-	NC
10	GND	GND	NC	GND	GND	NC
11	XMC_A11+	XMC_B11-	NC	XMC_D11+	XMC_E11-	NC
12	GND	GND	XMC_C12	GND	GND	XMC_F12
13	XMC_A13+	XMC_B13-	XMC_C13	XMC_D13+	XMC_E13-	XMC_F13
14	GND	GND	XMC_C14	GND	GND	XMC_F14
15	XMC_A15+	XMC_B15-	XMC_C15	XMC_D15+	XMC_E15-	XMC_F15
16	GND	GND	XMC_C16	GND	GND	XMC_F16
17	XMC_A17+	XMC_B17-	XMC_C17	XMC_D17+	XMC_E17-	XMC_F17
18	GND	GND	XMC_C18	GND	GND	XMC_F18
19	XMC_A19+	XMC_B19-	XMC_C19	XMC_D19+	XMC_E19-	XMC_F19

M.2 Connector Pin Definition

Signal	Pin	Pin	Signal
GND	1	2	P_+3V3
GND	3	4	P_+3V3
PCH_PCIE20_RX_R_N	5	6	NC
PCH_PCIE20_RX_R_P	7	8	NC
GND	9	10	NC
PCH_PCIE20_TX_C_N	11	12	P_+3V3
PCH_PCIE20_TX_C_P	13	14	P_+3V3
GND	15	16	P_+3V3
PCH_PCIE19_RX_R_N	17	18	P_+3V3
PCH_PCIE19_RX_R_P	19	20	NC
GND	21	22	NC
PCH_PCIE19_TX_C_N	23	24	NC

Signal	Pin	Pin	Signal
PCH_PCIE19_TX_C_P	25	26	NC
GND	27	28	NC
PCH_PCIE18_RX_R_N	29	30	NC
PCH_PCIE18_RX_R_P	31	32	NC
GND	33	34	GND
PCH_PCIE18_TX_C_N	35	36	NC
PCH_PCIE18_TX_C_P	37	38	DEVSLP_M2_CON_R
GND	39	40	NC
PCH_PCIE17_SATA4_RX_R_P	41	42	NC
PCH_PCIE17_SATA4_RX_R_N	43	44	NC
GND	45	46	NC
PCH_PCIE17_SATA4_TX_C_N	47	48	NC
PCH_PCIE17_SATA4_TX_C_P	49	50	M2_RST-L
GND	51	52	CLK_REQ_M2_R-L
C_PCIECLK2_100M_N	53	54	NC
C_PCIECLK2_100M_P	55	56	NC
GND	57	58	NC
Key			
NC	67	68	NC
M2TYPE_PEDET	69	70	P3V3
GND	71	72	P3V3
GND	73	74	P3V3
GND	75	76	NA

VPX Connectors

P0 Connector

Row	G	F	E	D	C	B	A
1	+12V (VS1)	+12V (VS1)	+12V (VS1)	NC	NC (VS2)	NC (VS2)	NC (VS2)
2	+12V (VS1)	+12V (VS1)	+12V (VS1)	NC	NC (VS2)	NC (VS2)	NC (VS2)
3	NC (VS3)	NC (VS3)	NC (VS3)	NC	NC (VS3)	NC (VS3)	NC (VS3)
4	IPM1_CLK	IPM1_DAT	GND	NC (-12V_AUX)	GND	SYSRESET#	NVMRO
5	GAP#	GA4#	GND	+3.3V_AUX	GND	IPM2_CLK	IPM2_DAT
6	GA3#	GA2#	GND	NC (+12V_AUX)	GND	GA1#	GA0#
7	IPMB_JTCK	GND	IPMB_JTDO	IPMB_JTDI	GND	IPMB_JTMS	IPMB_JTRST-L
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND

P1 Connector

Row	G	F	E	D	C	B	A
1	GDiscrete1#	GND	PCIE1_TX0-	PCIE1_TX0+	GND	PCIE1_RX0-	PCIE1_RX0+
2	GND	PCIE1_TX1-	PCIE1_TX1+	GND	PCIE1_RX1-	PCIE1_RX1+	GND
3	P1_VBAT	GND	PCIE1_TX2-	PCIE1_TX2+	GND	PCIE1_RX2-	PCIE1_RX2+
4	GND	PCIE1_TX3-	PCIE1_TX3+	GND	PCIE1_RX3-	PCIE1_RX3+	GND
5	SYSCON#	GND	PCIE2_TX0-	PCIE2_TX0+	GND	PCIE2_RX0-	PCIE2_RX0+
6	GND	PCIE2_TX1-	PCIE2_TX1+	GND	PCIE2_RX1-	PCIE2_RX1+	GND
7	+5V_USB1 (for USB3.0)	GND	PCIE2_TX2-	PCIE2_TX2+	GND	PCIE2_RX2-	PCIE2_RX2+
8	GND	PCIE2_TX3-	PCIE2_TX3+	GND	PCIE2_RX3-	PCIE2_RX3+	GND
9	COM1_TX	GND	J16-A5	J16-B5	GND	J16-D5	J16-E5
10	GND	J16-A7	J16-B7	GND	J16-D7	J16-E7	GND
11	COM1_RX	GND	J16-A9	J16-B9	GND	J16-D9	J16-E9
12	GND	J16-A15	J16-B15	GND	J16-D15	J16-E15	GND
13	GPIO1(DP_ CONFIG)	GND	J16-A17	J16-B17	GND	J16-D17	J16-E17
14	GND	J16-A19	J16-B19	GND	J16-D19	J16-E19	GND
15	MASKABLE RESET#	GND	KR-TX0-	KR-TX0+	GND	KR-RX0-	KR-RX0+
16	GND	KR-TX1-	KR-TX1+	GND	KR-RX1-	KR-RX1+	GND

Signal Types:

1. **Data Plane:** 1x PCIe x4 (PCIE1_xx)
2. **Expansion Plane:** 1x PCIe x4 (PCIE2_xx)
3. **XMC X12d Mapping:** (J16-xx)
4. **Maintenance Port:** (COM1_xx)
5. **10GBASE-KR x2:** (KR-xx)

P2 Connector

Row	G	F	E	D	C	B	A
1	SER_TX1-/ DATA1-/TX1	GND	DP_L1-	DP_L1+	GND	DP_L0-	DP_L0+
2	GND	DP_L3-	DP_L3+	GND	DP_L2-	DP_L2+	GND
3	SER_TX1+/ DATA1+/TX2	GND	DP_PWR	DP_HPD	GND	DP_AUX-	DP_AUX+
4	GND	USB2.0_2_D-	USB2.0_2_D+	GND	USB2.0_1_D-	USB2.0_1_D+	GND
5	SER_RX1-/ RX1	GND	USB3_TX-	USB3_TX+	GND	USB3_RX-	USB3_RX+
6	GND	SATA3_TX-	SATA3_TX+	GND	SATA3_RX-	SATA3_RX+	GND
7	SER_RX1+/ RX2	GND	TB-	TB+	GND	TA-	TA+
8	GND	TD-	TD+	GND	TC-	TC+	GND
9	+5V_USB2 (for USB2)	GND	J16-C12/ PCIE3_TX0-	J16-C13/ PCIE3_TX0+	GND	J16-F12/ PCIE3_RX0-	J16-F13/ PCIE3_RX0+
10	GND	J16-C14/ PCIE3_TX1-	J16-C15/ PCIE3_TX1+	GND	J16-F14/ PCIE3_RX1-	J16-F15/ PCIE3_RX1+	GND
11	GPIO2	GND	J16-C16/ PCIE3_TX2-	J16-C17/ PCIE3_TX2+	GND	J16-F16/ PCIE3_RX2-	J16-F17/ PCIE3_RX2+
12	GND	J16-C18/ PCIE3_TX3-	J16-C19/ PCIE3_TX3+	GND	J16-F18/ PCIE3_RX3-	J16-F19/ PCIE3_RX3+	GND
13	GPIO3	GND	J16-A1/ PCIE4_TX0-	J16-B1/ PCIE4_TX0+	GND	J16-D1/ PCIE4_RX0-	J16-E1/ PCIE4_RX0+
14	GND	J16-A3/ PCIE4_TX1-	J16-B3/ PCIE4_TX1+	GND	J16-D3/ PCIE4_RX1-	J16-E3/ PCIE4_RX1+	GND
15	GPIO4	GND	J16-A11/ PCIE4_TX2-	J16-B11/ PCIE4_TX2+	GND	J16-D11/ PCIE4_RX2-	J16-E11/ PCIE4_RX2+
16	GND	J16-A13/ PCIE4_TX3-	J16-B13/ PCIE4_TX3+	GND	J16-D13/ PCIE4_RX3-	J16-E13/ PCIE4_RX3+	GND

Signal Types:

1. **1x Display Port:** DP_xx
2. **1x USB 3.2 Gen1:** (USB3_xx)
3. **2x USB 2.0:** (USB2.0_1_xx, USB2.0_2_xx)
4. **1x SATA 6Gb/s:** (SATA3_xx)
5. **1x 2.5GBASE-T:** (TA/TB/TC/TD +/-)
6. **XMC X16s Mapping:** co-layout with 1x PCIe x4 or 2x PCIe x2 or 4x PCIe x1 (J16-Fxx, J16-Cxx, PCIE3_xx)
7. **XMC X8d Mapping:** co-layout with 1x PCIe x4 or 2x PCIe x2 or 4x PCIe x1 (J16-Axx, J16-Bxx, J16-Dxx, J16-Exx, PCIE4_xx)

4.4 Status LEDs

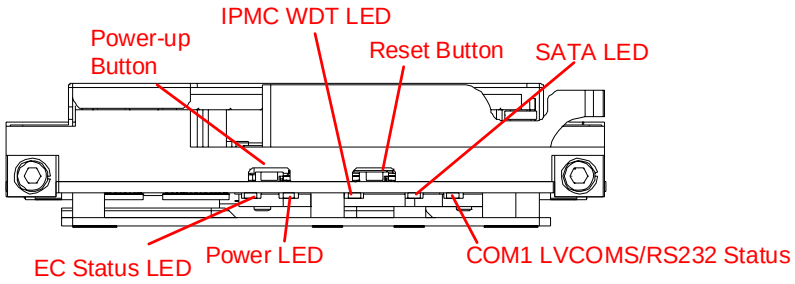


Figure 4-4: VPX3-TL Front View

Reset Button

Press this button to perform a hard system reset.

Power-up Button

Press this button to power-up in ATX mode.

LEDs

Description	Indication
Power LED	Green: On when blade is receiving power
SATA LED	Yellow: Blinks when SATA is active
IPMC WDT LED	TBD
Embedded Controller (EC) Status LED	Red (error codes TBD)
COM1 LVCOMS/ RS232 Status LED	On: RS232 mode Off: LVCOMS mode

5 VPX3-TL-RL1 RTM

This chapter illustrates the board layout, connector pin assignments, and jumper settings to familiarize users with the VPX3-TL-RL1 RTM.

5.1 Connector Allocation

Function	Rear	Top	RPx	Connector Type
DisplayPort	1	—	RP1	4 lanes DDI to Mini DisplayPort
2.5GBASE-T MDI	1	—	RP1	4 lanes MDI to RJ45 port
USB 3.0/2.0	1	—	RP1	USB 2.0 + USB 3.0 combo port
USB 2.0	1	—	RP1	USB2.0 port
Maintenance Port	1	—	RP1	RJ45
SATA Gen3	—	1	RP1	7 Pin SATA connector
COM Port	—	1	RP1	Box 2x5 pin header
IPMB JTAG	—	1	RP0	2x5 pin header
IPMB SMBus	—	1	RP0	Wafer ML 1*5P ST D1.25
VPX MB RTC Power Source	—	1	RP0	Wafer ML 1x2P RT D1.25
IPMB SMBus Switch	—	1	RP0	SW DIP SPST 4-POS ST
VPX Utility Test Jumper	—	1	RP0	2x3 pin header
VPX GPIO Test Jumper	—	1	RP1/ RP2	2x5 pin header
2x 10GBASE-KR	—	1	RP1	Board to Board Connector
XMC X12d			RP1	
XMC X8d			RP2	
XMC X16s			RP2	

5.2 VPX3-TL-RL1 Block Diagram

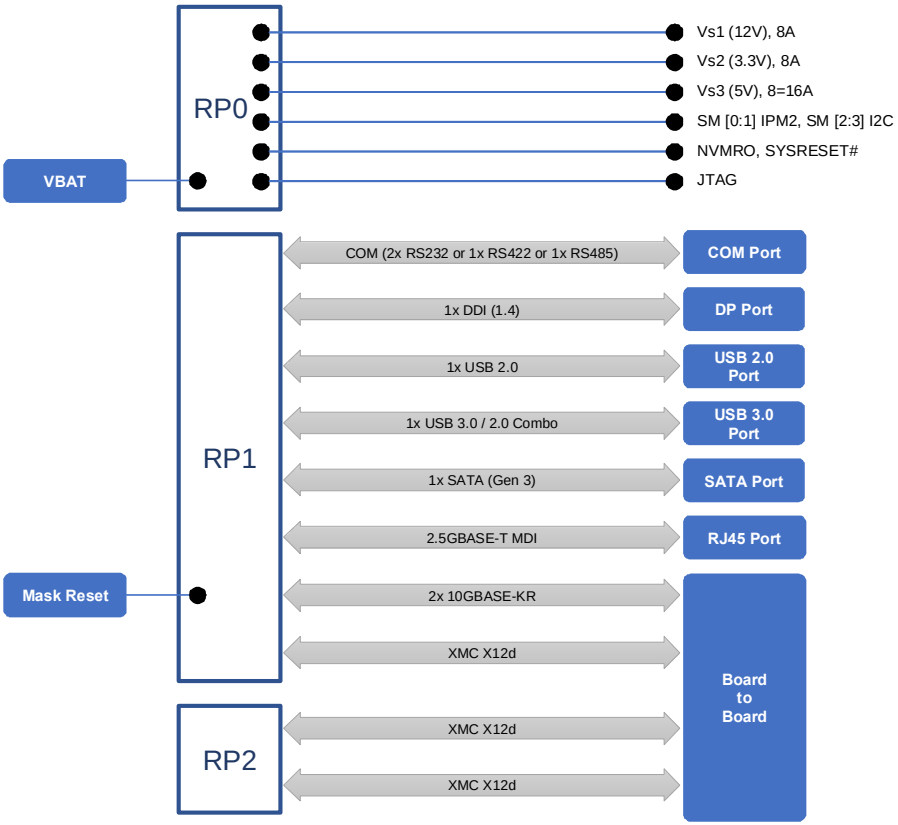


Figure 5-1: VPX3-TL-RL1 RTM Functional Block Diagram

5.3 VPX3-TL-RL1 RTM Board Layout

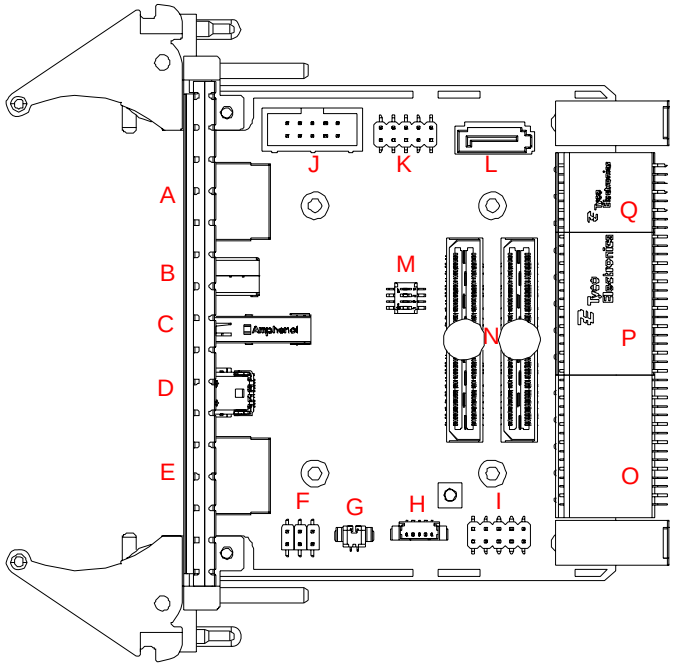


Figure 5-2: VPX3-TL-RL1 RTM Board Layout

A	LAN Port	**J**	COM Port
B	USB 2.0 Port	**K**	VPX GPIO Test Jumper
C	USB 3.0 + USB 2.0 Combo Port	**L**	SATA Port
D	Mini DP Port	**M**	IPMB SMBus Switch
E	Maintenance Port (MGMT)	**N**	RTM L2 B2B Connector (reserved)
F	VPX Utility Test Jumper	**O**	VPX RP0 Connector
G	VPX MB RTC Power Source	**P**	VPX RP1 Connector
H	IPMB SMBus	**Q**	VPX RP2 Connector
I	IPMB JTAG		

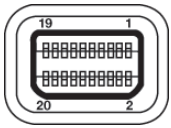
Table 5-1: VPX3-TL-RL1 RTM Board Layout Legend

5.4 VPX3-TL-RL1 RTM Connector Pin Assignments

Rear I/O Connectors

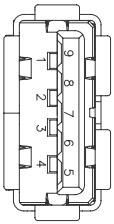
Mini DisplayPort Connector

Pin	Signal	Pin	Signal
1	GND	11	DP1_TXN1_CN
2	DP_CN_HPD	12	DP1_TXN3_CN
3	DP1_TXP0_CN	13	GND
4	DP1_CFG1_CN	14	GND
5	DP1_TXN0_CN	15	DP1_TXP2_CN
6	DP1_CFG2_CN	16	DP_AUX_C_P
7	GND	17	DP1_TXN2_CN
8	GND	18	DP_AUX_C_N
9	DP1_TXP1_CN	19	GND
10	DP1_TXP3_CN	20	P_+3V3_DP1_CN



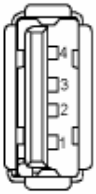
USB 3.0 Connectors

Pin #	Signal Name
1	USB3.0_P5VA
2	USB2_CMAN
3	USB2_CMAP
4	GND
5	USB3A_CMRXN
6	USB3A_CMRXP
7	GND
8	USB3A_CMTXN
9	USB3A_CMTXP



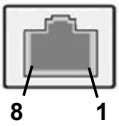
USB 2.0 Connectors

Pin #	Signal Name
1	Vcc
2	UV0-
3	UV0+
4	GND



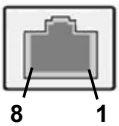
Serial Port (RJ-45)

Pin #	Signal
1	NC
2	NC
3	MTN_TXD
4	GND
5	GND
6	MTN_RXD
7	NC
8	NC



System LAN Port (RJ-45)

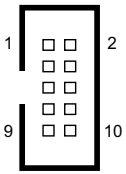
Pin #	Signal
1	MDIA_P
2	MDIA_N
3	MDIB_P
4	MDIC_P
5	MDIC_N
6	MDIB_N
7	MDID_P
8	MDID_N



Onboard Connectors

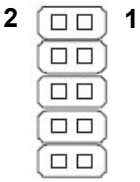
COM Port (COM1)

Pin #	Signal	Pin #	Signal
1	NC	2	NC
3	COM1_RX_RX-	4	COM2_TX_TX+
5	COM1_TX_TX-	6	COM2_RX_RX+
7	NC	8	NC
9	GND	10	NC



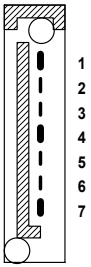
JTAG Header

Pin #	Signal
1	GND
2	TCK
3	NC
4	TDO
5	+3.3V
6	TMS
7	TRST
8	+3.3V
9	GND
10	TDI



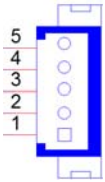
SATA Connectors

Pin #	Signal
1	GND
2	TXP
3	TXN
4	GND
5	RXN
6	RXP
7	GND



IPMB Connector

Pin #	Signal
1	IPMB_SDA
2	GND
3	IPMB_SCL
4	+5V
5	+5V



This page intentionally left blank.

6 Getting Started

This chapter describes the installation of the following components to the VPX3-TL and rear transition modules:

- VPX Blade installation to chassis
- RTM installation to chassis

6.1 Installing the VPX3-TL to the Chassis

These instructions are for reference only. Refer to the user guide that comes with the chassis for more information.

1. Be sure to select the system slot to install the blade. The system power may be powered either on or off.
2. Align the module's top and bottom edges to the chassis card guides, and then carefully slide the module into the chassis. A slight resistance may be felt when inserting the module. If a strong resistance is felt, check if the wedge locks are expanded or if the board's connector pins are not properly aligned with connectors on the backplane. Then push the board until it is completely flush with the chassis.
3. Ensure the module in place, and then screw the wedge lock on the module

6.2 Installing the VPX3-TL-RL1 RTM to the Chassis

The installation and removal procedures for a RTM are the same as those for VPX boards. Because they are shorter than front boards, pay careful attention when inserting or removing RTMs.

Refer to previous sections for peripheral connectivity of all I/O ports on the RTM. When installing the VPX3-TL Series and related RTMs, make sure the RTM is the correct matching model.

6.3 Driver Installation

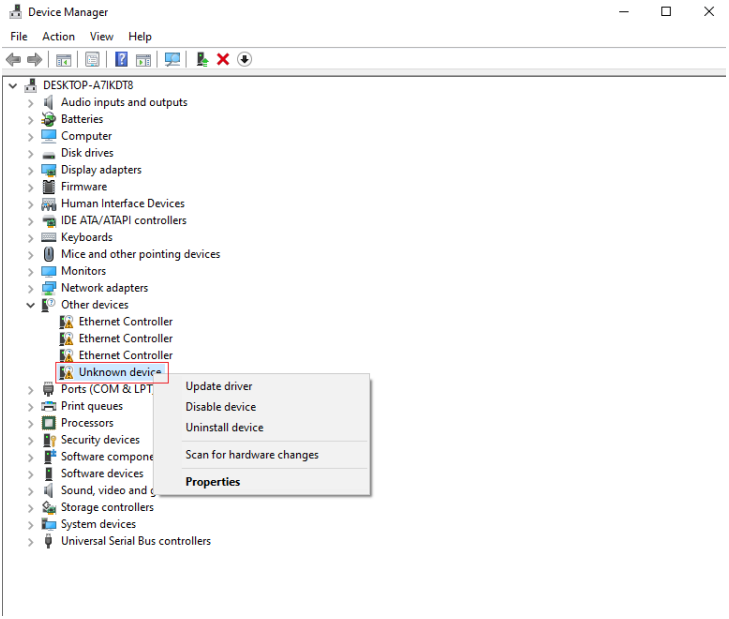
The VPX3-TL drivers are available from the ADLINK website at www.adlinktech.com/Products/VPX/VPX3UProcessorBlades/VPX3-TL. ADLINK provides validated drivers for Windows 10 IoT Enterprise LTSC 21H2. We recommend using the drivers provided on the ADLINK website to ensure compatibility.

Follow the steps below to install the drivers for Windows 10.

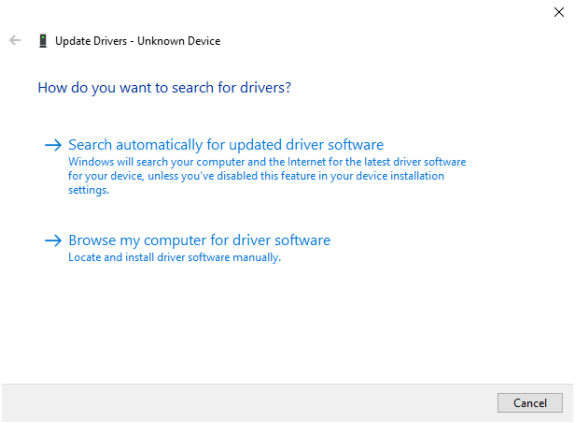
1. Install the Windows operating system before installing any driver. Most standard I/O device drivers are installed during Windows installation.
2. Install the chipset driver by extracting and running the application "**SetupChipset.exe**" in the **Intel® Chipset Device Software** directory.
3. Install the graphics driver by extracting and running the application "**Installer.exe**" in the **Intel® UHD Graphics** directory.
4. Install the management engine driver by extracting and running the application "**SetupME.exe**" in the **Intel® Management Engine Components/SW/ME_SW_DCH** directory.
5. Install the GPIO/Serial I/O driver by extracting and running the application "**SetupSerialIO.exe**" in the **Intel® SerialIO** directory.

6. Install the Intel Trace Hub driver by extracting the contents of the Intel Trace Hub directory, and perform the following steps:

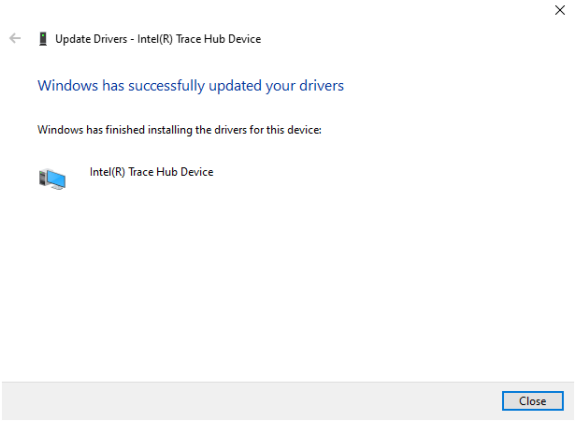
   a. In the Device Manager, right-click on "Unknown device" and click on “Update driver”.



   b. Click on "Browse my computer for driver software”.

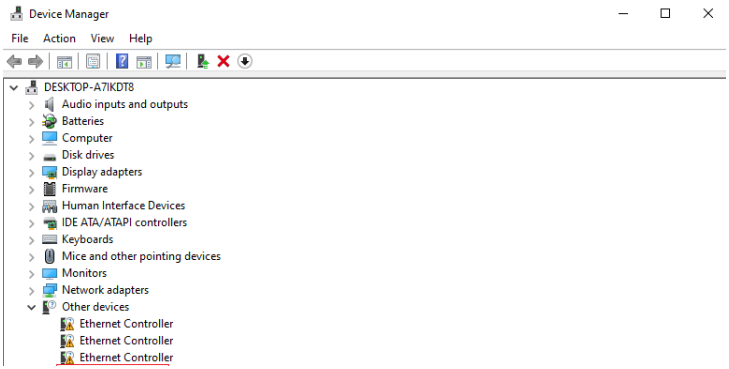


c. Navigate to the "Intel Trace Hub" directory, click “OK” to search/install the driver. Click "Close" when done.

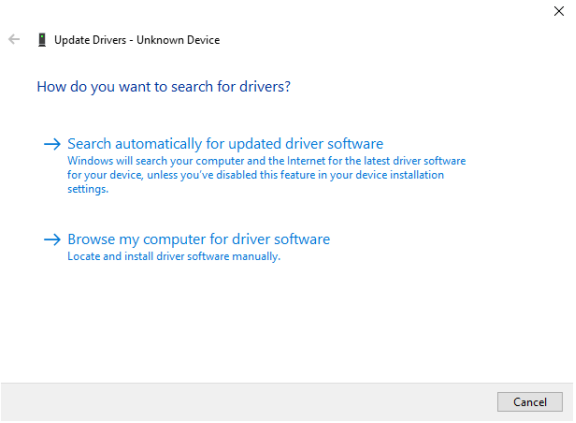


7. Install the Intel Network drivers by extracting the contents of the Intel network connections directory, and performing the following steps.

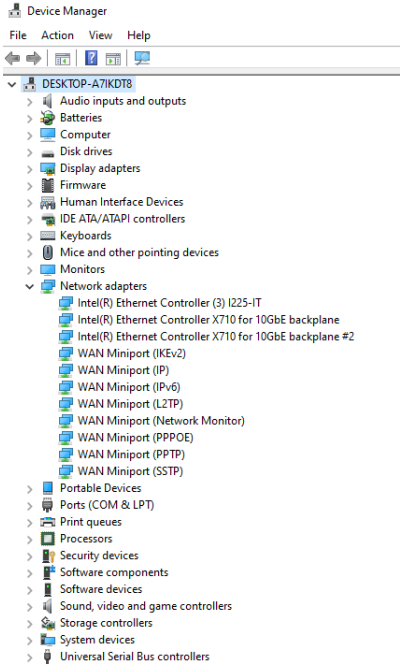
   a. In the Device Manager, right-click on "Unknown device" and click on “Update driver”.



b. Click on "Browse my computer for driver software".



c. Navigate to the "Intel Trace Hub" directory, click “OK” to search/install the driver. Click "Close" when done. Repeat for the other two "Ethernet Controller" under "Other devices"



d. The drivers for Intel Ethernet Controllers i225-IT and X710 are now successfully installed.

7 Utilities

7.1 SEMA

Hardware monitoring and Watchdog Timer functionality are provided by ADLINK's Smart Embedded Management Agent (SEMA), which operates via a Board Management Controller and communicates with the CPU through the SMBus. A graphical user interface program and command line interface are available to allow you to communicate with SEMA. Please refer to the SEMA user's manual, available the SEMA GitHub page:
https://adlinktech.github.io/sema/index.html

7.2 Watchdog Timer

The VPX3-TL's watchdog timer (WDT) is implemented by SEMA. For detailed information on how to program the WDT, refer to the SEMA user's manual WDT section on the SEMA GitHub page:
https://adlinktech.github.io/sema/WatchDog.html#sysfs-In

This page intentionally left blank.

8 BIOS Setup

The following chapter describes basic navigation for the AMIBIOS®8 BIOS setup utility.

8.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keyboard when you see the following text prompt:
   < Press DEL to run Setup >
3. After you press the < Delete > key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu.

In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

Setup Menu

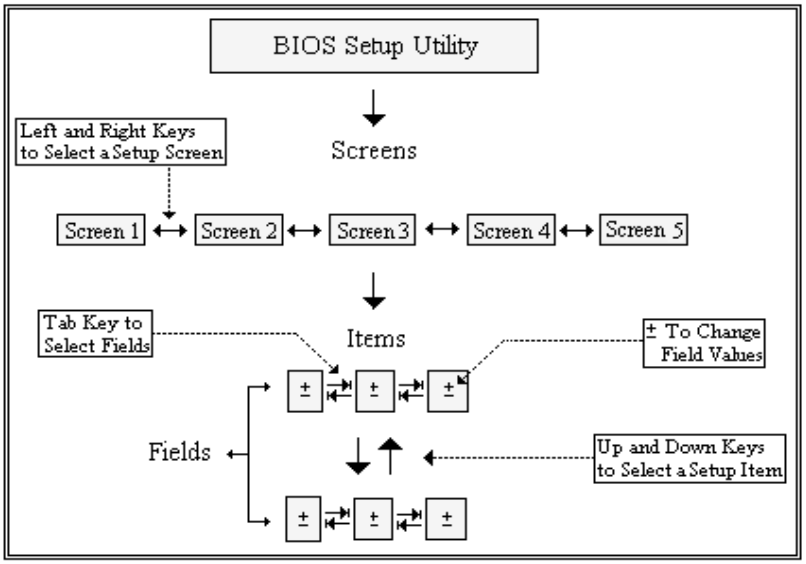
The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed" options cannot be configured, "Blue" options can be.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

Navigation

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process.



NOTE: There is a hot key legend located in the right frame on most setup screens.

→←	Left/Right. The Left and Right < Arrow > keys allow you to select a setup screen. For example: Main screen, Advanced screen, Chipset screen, and so on.
↑↓	Up/Down The Up and Down < Arrow > keys allow you to select a setup item or sub-screen.
+-	Plus/Minus The Plus and Minus < Arrow > keys allow you to change the field value of a particular setup item. For example: Date and Time.
Tab	The < Tab > key allows you to select setup fields.
ESC	The < Esc > key allows you to discard any changes you have made and exit the Setup. Press the < Esc > key to exit the setup without saving your changes. Press the < Enter > key to discard changes and exit. You can also use the < Arrow > key to select Cancel and then press the < Enter > key to abort this function and return to the previous screen.

8.2 Setup Menus

Refer to the document *VPX3-TL BIOS User's Manual* for detailed BIOS setup menu information, available for download from the ADLINK website at www.adlinktech.com/Products/VPX/VPX3U ProcessorBlades/VPX3-TL.

This page intentionally left blank.

Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

A Lithium-type battery may be provided for uninterrupted, backup or emergency power.

Risk of explosion if battery is replaced with one of an incorrect type. Dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

Getting Service

Ask an Expert: https://www.adlinktech.com/en/Askanexpert.aspx

ADLINK Technology, Inc.
No. 66, Huaya 1st Rd., Guishan Dist.,
Taoyuan City 333411, Taiwan
Tel: +886-3-216-5088
Fax: +886-3-328-5706
Email: service@adlinktech.com

Ampro ADLINK Technology, Inc.
6450 Via Del Oro
San Jose, CA 95119-1208, USA
Tel: +1-408-360-0200
Toll Free: +1-800-966-5200 (USA only)
Fax: +1-408-600-1189
Email: info@adlinktech.com

ADLINK Technology (China) Co., Ltd.
300 Fang Chun Rd., Zhangjiang Hi-Tech Park
Pudong New Area, Shanghai, 201203 China
Tel: +86-21-5132-8988
Fax: +86-21-5132-3588
Email: market@adlinktech.com

ADLINK Technology GmbH
Hans-Thoma-Strasse 11
D-68163 Mannheim, Germany
Tel: +49-621-43214-0
Fax: +49-621 43214-30
Email: emea@adlinktech.com

Please visit the Contact page at **www.adlinktech.com** for information on how to contact the ADLINK regional office nearest you.