VPX3020 Series

Performance Rugged Conduction Cooled
3U VPX Intel® Xeon® Processor E
Processor Blade

User's Manual

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Part No: 50M-00050-1000

LEADING EDGE COMPUTING

Revision History

Revision	Release Date	Description of Change(s)
1.0	2022/08/25	Initial release

Preface

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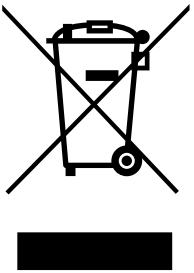

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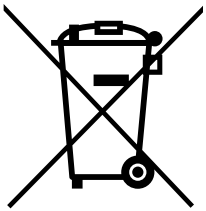

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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

Additional information, aids, and tips that help users perform tasks.

Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

Table of Contents

List of Figures

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List of Tables

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1 Introduction

1.1 Overview

The VPX3020 Series is a 3U VPX processor blade based on the Intel® Xeon® Processor E-2254ML (formerly "Coffee Lake-H Refresh"), supporting DDR4-2666 ECC soldered memory up to 16GB. For storage, the VPX3020 provides a high endurance soldered 32GB SLC SSD. The VPX3020 is compliant with the VITA 48 and VITA 65 specifications.

The VPX3020 Series with server grade Intel® processor brings extreme computing power with low power consumption. A total of PCIe x16 Gen3 lanes are supported, with PCIe x8 to rear supporting DMA and non-transparent bridge for peer-to-peer communication and PCIe x8 Gen3 to XMC. Graphics is supported by integrated Intel GPU with DisplayPort to P2.

The ADLINK VPX3020 provides an Infineon TPM 2.0 chip for system security, dual BIOS functionality, as well as an ADLINK ABS-Diag self-diagnosis tool. These features bring additional value by ensuring high reliability. All components on the VPX3020 Series are soldered on the PCB board to ensure product reliability and quality, and enable compliance with MIL-STD-810G shock and vibration. The VPX3020 supports a wide operating temperature range from -40°C to +75°C (optionally up to +85°C).

The VPX3020 Series is available in a rugged conduction cooled version with conformal coating and an air cooled version to meet different application needs. A VPX-R3020 Rear Transition Module is available to access rear I/O signals for users to validate VPX3020 functionality.

1.2 Features

- Intel® Xeon® Processor E-2254ML
  (formerly "Coffee Lake-H Refresh")
- DDR4-2666 soldered ECC SDRAM up to 16GB
- 32GB SATA SLC SSD option
- Up to PCIe x16 Gen3 interface supporting non-transparent bridge
- One XMC expansion slot, PCIe x8 Gen3 with Rear I/O to P2

1.3 Block Diagrams

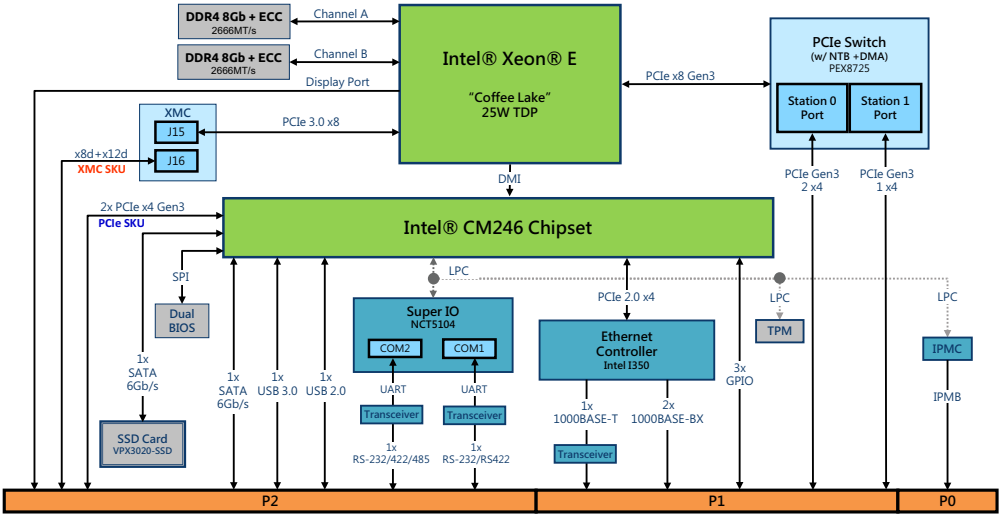

Figure 1-1: VPX3020 Functional Block Diagram

1.4 Model Number Decoder - Processor Blade

VPX3020/2254/M16/S32/XMC-R2

(A) (B) (C) (D) (E)

(A) CPU Code

- **E-2254ML** = Intel® processor E-2254ML, 4 cores, 25W TDP

(B) Memory Size Code

- **M16** = 16GB DDR4-2666 ECC soldered SDRAM

(C) SATA NAND Flash Size Code

- **S32** = SLC NAND flash 32GB SATA 6Gb/s via add-on card

(D) PCI Express interface code

- XMC = XMC interface
- P8 = PCI Express x8 Gen3 (BOM option)

(E) Ruggedized Level Code

- R1 = Conduction Cooled version supporting -40°C to +75°C at card edge
- R2 = Conduction Cooled version supporting -40°C to +85°C at card edge
- A1 = Air Cooled version supporting -40°C to +75°C

VPX3020 SKU Table

Function	XMC Version	PCIe Version
XMC	PCIe x8 Gen3 (or 2x PCIe x4) w/ rear IO to P2 (X8d+X12d)	N/A
Ethernet	1x 1000BASE-T + 2x 1000BASE-BX to P1	
PCI Express	PCIe Switch downstream port to P1 Station 0 port: 2 x4 Station 1 port: 1 x4	
	N/A	2x PCIe Gen3 x4 to P2
SATA 6Gbps	SATA 6Gb/s to P2	
	SATA 6Gb/s SLC NAND flash 32GB	
GPIO	3x GPIO	
Serial	1x RS-232/422 (COM1) to P2	
	1x RS-232/422/485 (COM2) to P2 (BOM option as 4x GPIO)	

Table 1-1: VPX3020 SKU Table

Note: Items in red differ between SKU options.

1.5 Package Contents

The VPX3020 is packaged with the following components. If any of the items on the contents list are missing or damaged, retain the shipping carton and packing material and contact the dealer for inspection. Please obtain authorization before returning any product to ADLINK. The packing contents of the VPX3020 are non-standard configurations and may vary depending on customer requests.

Processor Blade

- VPX3020
  - CPU and memory specifications will differ depending on options selected
  - Thermal module is assembled on the board

Rear Transition Module (optional)

- VPX-R3020 RTM

Test Backplane (optional)

- tBP-VPX3020 test backplane

The contents of non-standard VPX3020 configurations may vary depending on the customer requirements.

This product must be protected from static discharge and physical shock. Never remove any of the components except at a static-free workstation. Use the anti-static bag shipped with the product when putting the board on a surface. Wear an anti-static wrist strap properly grounded on one of the system's ESD ground jacks when installing or servicing system components.

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2 Specifications

2.1 VPX3020 Blade Specifications

VITA Standards	• VITA 46.0 VPX Base Standard • VITA 46.4 PCI Express on VPX Fabric Connector • VITA 46.6 Gigabit Ethernet Control Plane on VPX • VITA 46.9 PMC/XMC/Ethernet Signal Mapping to 3U/6U VPX • VITA 46.10 Rear Transition Module on VPX • VITA 46.11 System Management on VPX • VITA 48.0 Ruggedized Enhanced Design Implementation Mechanical Base Specification • VITA 65 OpenVPX Architecture Framework for VPX
Mechanical	• Conduction-cooled 3U VPX • Air-cooled 3U VPX
Processor	• Intel® Xeon® Processor E-2254ML, 4 cores, 25W TDP
Chipset	• Intel® CM246 Chipset
Memory	• Dual channel 1.2V DDR4 2666MT/s SDRAM with ECC, up to 16GB
USB	• 1x USB 3.0 (backwards compatible) to P2 (can be separated to USB 3.0 only + USB 2.0)
XMC	• PCIe x8 Gen3 w/ rear IO (X8d+X12d) to P2 (XMC SKU only)
Gigabit Ethernet	• 1x 10/100/1000BASE-T + 2x 10/100/1000BASE-BX to P1
PCI Express	• 2x PCIe switch downstream port configuration to P1: ▫ Station 0 port: 2 x4 ▫ Station 1 port: 1 x4 • 2x PCIe 3.0 x4 to P2 (PCIe SKU only)
SATA	• SATA 6Gb/s to P2 • SATA 6Gb/s SLC NAND flash 32GB
Graphics	• 1x DisplayPort to P2 • Integrated Intel® GPU engine
IPMC	• Smart Fusion A2F200 with VPX code base
GPIO	• 3x GPIO to P1

Table 2-1: VPX3020 Blade Specifications

Serial	• 1x RS-232/422 (COM1) to P2 • 1x RS-232/422/485 (COM2) to P2 **Note:** RS-422 on COM1 & RS-485 on COM2 are not simultaneously supported.
RTC	• To P1
TPM	• Infineon TPM version 2.0
LEDs	• Status LEDs on front and rear
Reset Button	• On front panel
Watchdog Timer	• System reset or NMI with programmable interva
Environmental	• Operating Temperature: -40°C to +85°C at wedge locks • Storage Temperature: -50°C to +100°C • Relatively Humidity: 95% non-condensing • Shock: sawtooth 40G, 11ms, each axis, operating • Vibration: 15Hz-2KHz, 12Grms, random, each axis, operating • Thermal Dissipation: convection and conduction • Operating Altitude: 60,000 feet (VITA 47)
EMI	• CE, FCC Class A

Table 2-1: VPX3020 Blade Specifications

Note: Specifications are subject to change without prior notice.

2.2 VPX-R3020 RTM Specifications

Ethernet	• 2x 1000BASE-BX via RP1 • 1x 1000BASE-T via RP1
Graphics	• 1x DisplayPort signal via RP1
SATA	• 1x SATA 6Gb/s via RP1 (7 pin vertical SATA connector)
USB	• 1x USB 3.0 (backwards compatible) via RP1
Serial	• Serial Port 1: RS232 (2T2R) via RP1 (DB-9 connector) • Serial Port 2: RS232 (2T2R) via RP2 (2x5 pin header)
GPIO	• 2-bit GPIO signal via RP1 (2x3 pin header)
PCIe	• 1x PCIe x4 via RP0, 2x PCIe x4 via RP1 • 2x PCIe x4 via RP2
JTAG	• JTAG via RP0 (2x5 pin header)
Reset	• Reset via RP0
SMBus	• SMBus signal via RP0
Power	• Power terminal for +12V, +5V, +3.3V, GND

Table 2-2: VPX-R3020 RTM Specifications

Note: Specifications are subject to change without prior notice.

2.3 Power Consumption

This section provides information on the power consumption of the VPX3020 Series when using Intel® Xeon® E-2254ML processors with Dual Channel 8GB DDR4-2666 soldered memory and SATA SSD. The VPX3020 is powered by 5V and 3.3V. Windows 10 Typical power consumption was measured running BurnInTest at 100% loading. Windows 10 Max Loading power consumption was measured running Intel TAT test at 100% loading.

Processor	Xeon® E-2254ML (1.7 GHz)
Windows Idle mode, EIST Enabled	
3.3V (A)	2.03
5V (A)	0.77
Power Cons. (W)	10.55
Windows Idle mode, EIST Disabled	
3.3V (A)	2.02
5V (A)	0.78
Power Cons. (W)	10.57
Windows Typical mode, EIST Enabled	
3.3V (A)	3.5
5V (A)	6.3
Power Cons. (W)	43.05
Windows Typical mode, EIST Disabled	
3.3V (A)	3.1
5V (A)	6.1
Power Cons. (W)	40.73
Windows Max Loading mode, EIST Enabled	
Package Power reading (TAT)	25.00W
Package Temperature reading (TAT)	74°C
CPU DTS reading (TAT)	72°C
CPU frequency reading (TAT)	1287MHz
3.3V (A)	2.7
5V (A)	6.45
Power Cons. (W)	41.74

Processor	Xeon® E-2254ML (1.7 GHz)
Windows Max Loading mode, EIST Disabled	
Package Power reading (TAT)	24.98W
Package Temperature reading (TAT)	72°C
CPU DTS reading (TAT)	72°C
CPU frequency reading (TAT)	1287MHz
3.3V (A)	2.7
5V (A)	6.45
Power Cons. (W)	41.16

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3 Functional Description

The following sections describe the VPX3020 features and functions.

3.1 Processors

The Intel® Xeon® E Processor is a 64-bit, multi-core processor built on 14-nanometer process technology. The processor is designed for a two-chip platform consisting of a processor and chipset. The platform enables higher performance, lower cost, easier validation, and improved x-y footprint. The processor includes an Integrated Display Engine, Processor Graphics and Integrated Memory Controller.

Features	Xeon® E-2254ML
Clock	1.7 GHz
Max. Single Core Turbo Freq.	3.5 GHz
Last Level Cache	8MB
No. of Cores/Threads	4/8
Maximum Power (TDP[1])	25 W
$T_{case,MAX}$ [2]	100°C
Operating Temperature	-40°C to 85°C

Notes:

1. The highest expected sustainable power while running known power intensive applications. TDP is not the maximum power that the processor can dissipate.
2. The maximum supported operating temperature.

Supported Technologies

- Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
- Intel® Virtualization Technology (Intel® VT-x)
- Intel® VT-x with Extended Page Tables (EPT)
- Intel® Hyper-Threading Technology (Xeon® E-2254ML only)
- Intel® 64 Architecture
- Execute Disable Bit
- Intel® Turbo Boost Technology 2.0
- Intel® TSX-NI
- Enhanced Intel SpeedStep® Technology
- Thermal Monitoring Technologies

Interfaces

- Dual channel DDR4 memory with two channel of soldered SDRAM
- Memory DDR4 data transfer rates of 2666 MT/s
- 64-bit wide channels plus 8-bits of ECC support for each channel
- System Memory Interface I/O Voltage of 1.2V
- The PCI Express lanes are fully-compliant with the PCI Express Base Specification, Revision 3.0, including support for 8.0 GT/s transfer speeds.

3.2 Intel® Turbo Boost Technology

Intel Turbo Boost Technology is a feature that allows the processor to opportunistically and automatically run faster than its rated operating core and/or render clock frequency when there is sufficient power headroom, and the product is within specified temperature and current limits. The Intel Turbo Boost Technology feature is designed to increase performance of both multi-threaded and single-threaded workloads. The processor supports a Turbo mode where the processor can use the thermal capacity associated with package and run at power levels higher than TDP power for short durations. This improves the system responsiveness for short, bursty usage conditions.

Turbo Mode availability is independent of the number of active cores; however, the Turbo Mode frequency is dynamic and dependent on the instantaneous application power load, the number of active cores, user configurable settings, operating environment, and system design. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay with its TDP limit.

3.3 Chipset

The Mobile Intel® C240 Series Chipset provides extensive I/O support. Functions and capabilities include:

- PCI Express Base Specification, Revision 3.0
- ACPI Power Management Logic Support, Revision 4.0a
- Interrupt controller and timer functions
- Integrated Serial ATA host controller 3.2, supports data transfer rates up to 6Gb/s on all ports
- XHCI USB 3.1 Controller
- Integrated 10/100/1000 Gigabit Ethernet MAC with System Defense
- System Management Bus (SMBus) Specification, Version 2.0 with additional support for I2C devices
- Support Intel® High Definition Audio
- Support Intel® Rapid Storage Technology
- Support Intel® Virtualization Technology for Directed I/O
- Integrated Clock Controller
- Analog and Digital Display ports
- Low Pin Count (LPC) Interface
- Firmware Hub (FWH) Interface Support
- Serial Peripheral Interface (SPI) Support

3.4 USB

The VPX3020 provides one USB 3.0 port to the P2 connector supporting data transfers up to 5Gb/s, and one USB 2.0 port to the P2 connector supporting data transfers up to 480 Mb/s.

3.5 SPI BIOS

The VPX3020 implements a dual BIOS feature. Each SPI flash has a capacity of 256Mb. When the main BIOS crashes, the backup BIOS will be used to boot the device.

3.6 System Management Bus

The PCH provides a System Management Bus (SMBus) Specification Version 2.0 compliant Host Controller as well as an SMBus Slave Interface. The PCH provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves) as well as I2C compatible devices.

3.7 Real Time Clock

The PCH contains a real-time clock with 256 bytes of battery-backed RAM. The internal RTC module provides two key functions: keeping the time of day and storing system data, even when the system is powered down. The RTC operates on a 32.768 KHz crystal.

3.8 Serial ATA Controller

The VPX3020 has up to three SATA 6Gb/s ports capable of independent DMA operation. The SATA controller supports Intel® Rapid Storage Technology, providing both AHCI and integrated RAID functionality.

3.9 PCI Express Interface

The VPX3020 is compatible with the VPX ANSI/VITA 46.0-2007 standard and is equipped with an onboard PCIe Switch (PEX8725) to configure the PCIe bus and support the following configurations:

- Station 0 Downstream Ports: 2 x4
- Station 1 Downstream Port: 1 x4

The VPX3020 supports 1 x8 or 2 x4 PCIe bus to the XMC module.

3.10 Intel ® Gigibit Ethernet Controller I350

On the VPX-3020, the Intel® Ethernet Controller I350 offers one port 1000BASE-T and two ports 1000BASE-BX implementations using integrated PHYs.

3.11 Graphics

The VPX3020 provides one DisplayPort consisting of a Main Link, Auxiliary channel, and a Hot-Plug Detect signal. The DisplayPort supports VESA DisplayPort 1.2 specifications.

3.12 GPIO Expander PCA9554

The VPX3020 offers 4x GPIO pins which are configurable as input or output signals, 3.3V tolerant, and SCI (GPE) and IOAPIC interrupt capable.

3.13 UART NCT5104

The NCT5104 is a LPC to UART IC, which supports 4 high-speed serial communication ports (UART). Each UART includes a 128-byte send/receive FIFO, a programmable baud rate generator, complete modem-control capability, and a processor interrupt system. The UART supports legacy speeds up to 115.2K bps as well as even higher baud rates of 230K, 460K, or 921K bps to support higher speed modems.

In addition to UART, the NCT5104D provides flexible I/O control functions through a set of general purpose I/O (GPIO) ports. These GPIO ports may serve as simple I/O ports or may be individually configured to provide alternative functions. The NCT5104D supports port 80 decode on the LPC bus and could output the signal via SOUTC. It also supports LED control.

3.14 TPM

The Infineon SLB 9665 TPM 2.0 is a fully standard compliant TPM based on the latest Trusted Computing Group (TCG) specification 2.0 and features Low Pin Count (LPC) interface.

3.15 XMC Site

The VPX3020 Series supports one XMC site for rear I/O expansion. The XMC site provides a x8 PCI Express Gen 3.0 lane. Jn2 rear XMC I/O connector is compliant to VITA 46.9, X8d+X12d.

4 VPX3020 Board Interfaces

This chapter illustrates the board layout, connector pin assignments, and jumper settings to familiarize users with the VPX3020.

4.1 VPX3020 Board Layout

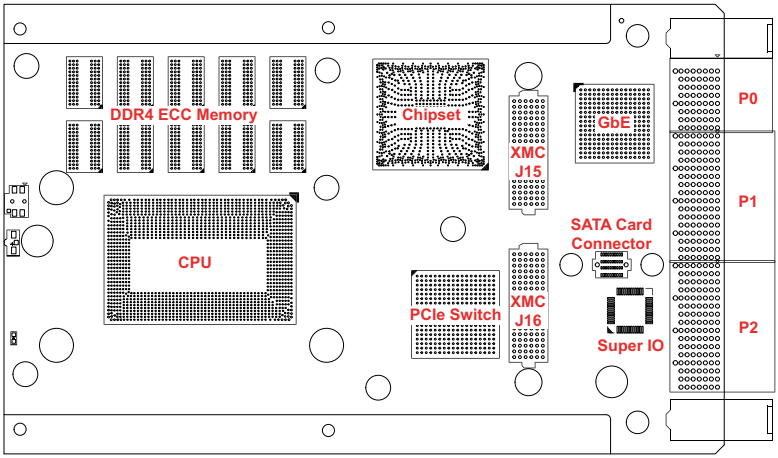


Figure 4-1: VPX3020 Top Side Layout

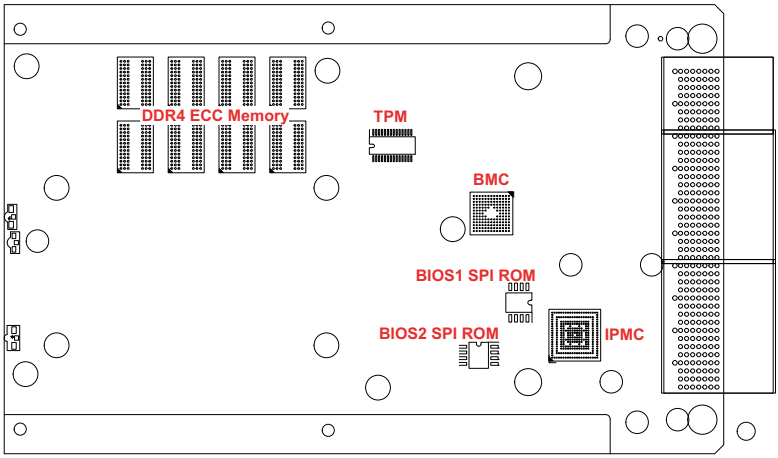
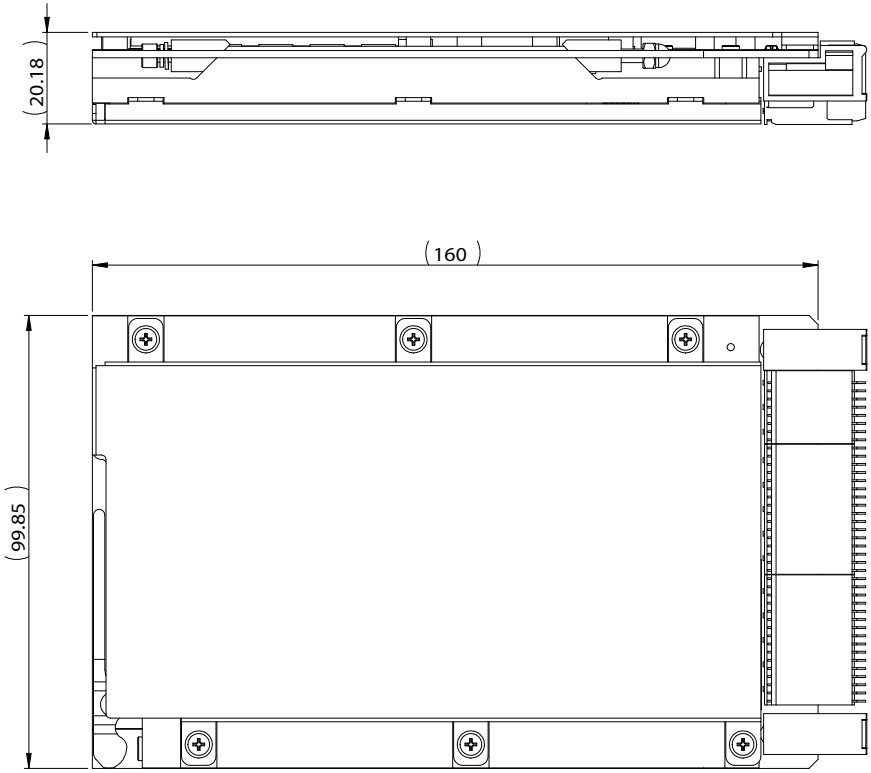


Figure 4-2: VPX3020 Bottom Side Layout

4.2 VPX3020 Mechanical Dimensions

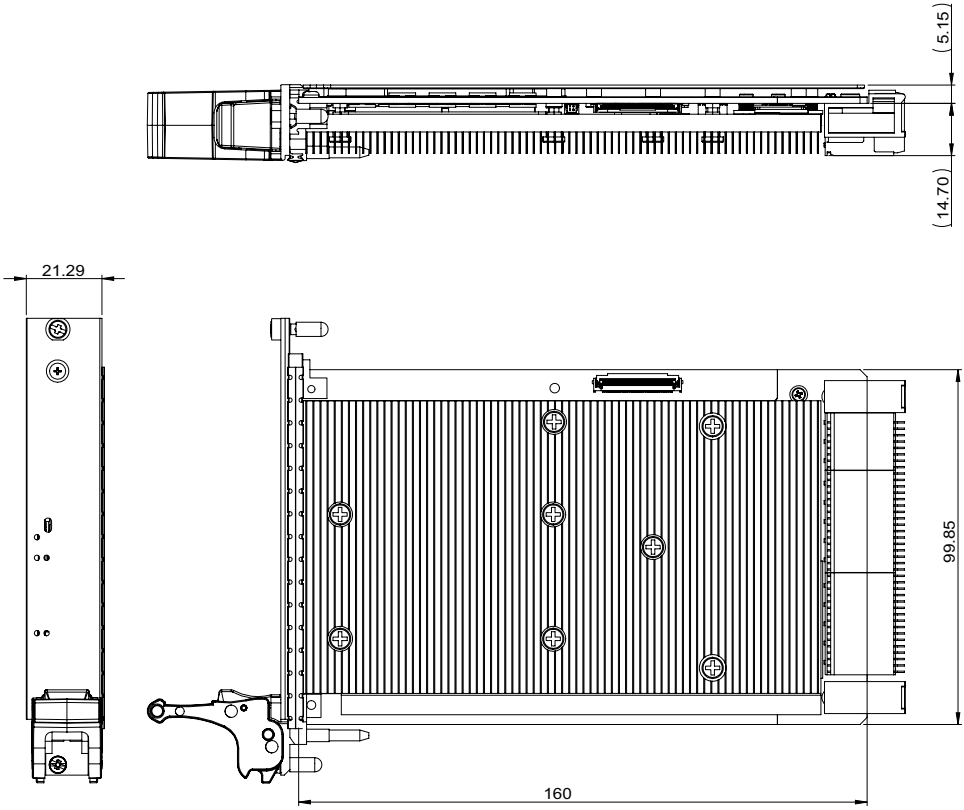
Conduction-Cooled Version



Dimensions in mm

Figure 4-3: VPX3020 Conduction-Cooled Mechanical Dimensions

Air-Cooled Version

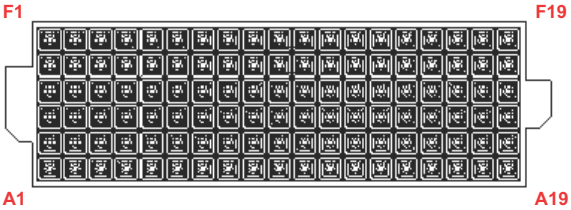


Dimensions in mm

Figure 4-4: VPX3020 Air-Cooled Mechanical Dimensions

4.3 VPX3020 Connector Pin Assignments

XMC Connectors



JN15 Connector Pin Definition (Primary)

Pin	A	B	C	D	E	F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR
2	GND	GND	TRST#	GND	GND	RESET#
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR
4	GND	GND	TCK	GND	GND	PULL UP
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR
6	GND	GND	TMS	GND	GND	12V_AUX
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR
8	GND	GND	TDI	GND	GND	-12V_AUX
9	NC	NC	NC	NC	NC	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	PER0p0	PER0n0	MBIST#	PER0p1	PER0n1	VPWR
12	GND	GND	GA1	GND	GND	PRSNT#
13	PER0p2	PER0n2	3.3V_AUX	PER0p3	PER0n3	VPWR
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	NC	PER0p5	PER0n5	VPWR
16	GND	GND	XMC_NVMRO	GND	GND	MSCL
17	PER0p6	PER0n6	NC	PER0p7	PER0n7	NC
18	GND	GND	NC	GND	GND	NC
19	REF_CLK+	REF_CLK-	NC	WAKE#	NC	NC

NOTE: The signal definitions of the primary XMC connector (J15) are presented relative to the XMC Mezzanine card.

J16 Connector Pin Definition (X8d+X12d)

Pin	A	B	C	D	E	F
1	XMC_A1+	XMC_B1-	NC	XMC_D1+	XMC_E1-	NC
2	GND	GND	NC	GND	GND	NC
3	XMC_A3+	XMC_B3-	NC	XMC_D3+	XMC_E3-	NC
4	GND	GND	NC	GND	GND	NC
5	XMC_A5+	XMC_B5-	NC	XMC_D5+	XMC_E5-	NC
6	GND	GND	NC	GND	GND	NC
7	XMC_A7+	XMC_B7-	NC	XMC_D7+	XMC_E7-	NC
8	GND	GND	NC	GND	GND	NC
9	XMC_A9+	XMC_B9-	NC	XMC_D9+	XMC_E9-	NC
10	GND	GND	NC	GND	GND	NC
11	XMC_A11+	XMC_B11-	NC	XMC_D11+	XMC_E11-	NC
12	GND	GND	NC	GND	GND	NC
13	XMC_A13+	XMC_B13-	NC	XMC_D13+	XMC_E13-	NC
14	GND	GND	NC	GND	GND	NC
15	XMC_A15+	XMC_B15-	NC	XMC_D15+	XMC_E15-	NC
16	GND	GND	NC	GND	GND	NC
17	XMC_A17+	XMC_B17-	NC	XMC_D17+	XMC_E17-	NC
18	GND	GND	NC	GND	GND	NC
19	XMC_A19+	XMC_B19-	NC	XMC_D19+	XMC_E19-	NC

VPX Connectors

P0 Connector

Pin	G	F	E	D	C	B	A
1	12V	12V	12V	NC	3.3V	3.3V	3.3V
2	12V	12V	12V	NC	3.3V	3.3V	3.3V
3	5V	5V	5V	NC	5V	5V	5V
4	IPM1_CLK	IPM1_DAT	GND	N12V_AUX	GND	SYSRESET#	NVMRO
5	GAP	GA4	GND	3.3V_AUX	GND	IPM2_CLK	IPM2_DAT
6	GA3	GA2	GND	P12V_AUX	GND	GA1	GA0
7	IPMB_ JTCK	GND	IPMB_ JTDO	IPMB_ JTDI	GND	IPMB_ JTMS	IPMB_ JTRST-L
8	GND	REF_CLK-	REF_CLK+	GND	H_CLK_P0_ 100M_N/ RES_BUS-	H_CLK_P0_ 100M_P/ RES_BUS+	GND

P1 Connector

Pin	G	F	E	D	C	B	A
1	GDISC1#	GND	L0-TX-	L0-TX+	GND	L0-RX-	L0-RX+
2	GND	L1-TX-	L1-TX+	GND	L1-RX-	L1-RX+	GND
3	P1_VBAT	GND	L2-TX-	L2-TX+	GND	L2-RX-	L2-RX+
4	GND	L3-TX-	L3-TX+	GND	L3-RX-	L3-RX+	GND
5	SYSCON#	GND	L4-TX-	L4-TX+	GND	L4-RX-	L4-RX+
6	GND	L5-TX-	L5-TX+	GND	L5-RX-	L5-RX+	GND
7	NC	GND	L6-TX-	L6-TX+	GND	L6-RX-	L6-RX+
8	GND	L7-TX-	L7-TX+	GND	L7-RX-	L7-RX+	GND
9	RTM_PWROK	GND	L8-TX-	L8-TX+	GND	L8-RX-	L8-RX+
10	GND	L9-TX-	L9-TX+	GND	L9-RX-	L9-RX+	GND
11	NC	GND	L10-TX-	L10-TX+	GND	L10-RX-	L10-RX+
12	GND	L11-TX-	L11-TX+	GND	L11-RX-	L11-RX+	GND
13	GPIO0	GND	ETH-T01B-	ETH-T01B+	GND	ETH-T01A-	ETH-T01A+
14	GND	ETH-T01D-	ETH-T01D+	GND	ETH-T-01C-	ETH-T01C+	GND
15	GPIO1/ MASKABLE RESET	GND	BX-TX1-	BX-TX1+	GND	BX-RX1-	BX-RX1+
16	GND	BX-TX0-	BX-TX0+	GND	BX-RX0-	BX-RX0+	GND

Signal Types:

1. **PCIe Station 0:** 2x PCIe x4 (L0-xx - L3-xx, L4-xx - L7-xx)
2. **PCIe Station 1:** 1x PCIe x4 (L8-xx - L11-xx)
3. **1000BASE-T:** ETH-xx
4. **1000BASE-BX:** BX-xx

P2 Connector

Pin	G	F	E	D	C	B	A
1	COM1_TXD[1] COM1_TX+[2]	GND	DP_L1-	DP_L1+	GND	DP_L0-	DP_L0+
2	GND	DP_L3-	DP_L3+	GND	DP_L2-	DP_L2+	GND
3	COM1_RXD[1] COM1_RX+[2]	GND	DP_CFG	DP_HPD	GND	DP_AUX-	DP_AUX+
4	GND	SATA3_TX-	SATA3_TX+	GND	SATA3_RX-	SATA3_RX+	GND
5	COM1_CTS#[1] COM1_RX-[2]	GND	USB3.0_ 3_TX-	USB3.0_ 3_TX+	GND	USB3.0_ 3_RX-	USB3.0_ 3_RX+
6	GND	P3V3_DP	P5V_USB1	GND	USB2.0_3_D-	USB2.0_3_D+	GND
7	COM1_RTS#[1] COM1_TX-[2]	GND	J16-A1	J16-B1	GND	J16-D1	J16-E1
8	GND	J16-A3	J16-B3	GND	J16-D3	J16-E3	GND
9	COM2_TXD[1] COM2_TX-[2] COM2_DATA-[3]	GND	J16-A11/ PCIE1_TX0-	J16-B11/ PCIE1_TX0+	GND	J16-D11/ PCIE1_RX0-	J16-E11/ PCIE1_ RX0+
10	GND	J16-A13/ PCIE1_TX1-	J16-B13/ PCIE1_TX1+	GND	J16-D13/ PCIE1_RX1-	J16-E13/ PCIE1_RX1+	GND
11	COM2_RXD[1] COM2_RX+[2]	GND	J16-A5/ PCIE1_TX2-	J16-B5/ PCIE1_TX2+	GND	J16-D5/ PCIE1_RX2-	J16-E5/ PCIE1_RX2+
12	GND	J16-A7/ PCIE1_TX3-	J16-B7/ PCIE1_TX3+	GND	J16-D7/ PCIE1_RX3-	J16-E7/ PCIE1_RX3+	GND
13	COM2_RTS#[1] COM2_TX-[2] COM2_DATA+[3]	GND	J16-A9/ PCIE2_TX0-	J16-B9/ PCIE2_TX0+	GND	J16-D9/ PCIE2_RX0-	J16-E9/ PCIE2_RX0+
14	GND	J16-A15/ PCIE2_TX1-	J16-B15/ PCIE2_TX1+	GND	J16-D15/ PCIE2_RX1-	J16-E15/ PCIE2_RX1+	GND
15	COM2_CTS#[1] COM2_RX-[2]	GND	J16-A17/ PCIE2_TX2-	J16-B17/ PCIE2_TX2+	GND	J16-D17/ PCIE2_RX2-	J16-E17/ PCIE2_RX2+
16	GND	J16-A19/ PCIE2_TX3-	J16-B19/ PCIE2_TX3+	GND	J16-D19/ PCIE2_RX3-	J16-E19/ PCIE2_RX3+	GND

[1]RS-232; [2]RS-422, [2]RS-485

Signal Types:

1. **Display Port:** DP_xx
2. **USB 3.0:** USB3.0_xx
3. **USB 2.0:** USB2.0_xx
4. **XMC x8d+x12d (XMC SKU):** J16-xx
5. **PCIe x4 (PCIe SKU):** PCIE2_xx

4.4 Status LEDs

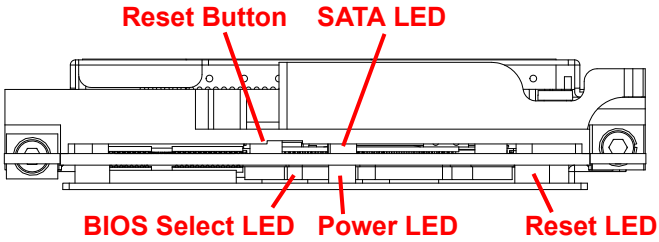


Figure 4-5: VPX3020 Front View

Reset Button

Press this button to perform a hard system reset.

LEDs

Description	Indication
Power LED	Green: On when blade is receiving power
SATA LED	Yellow: Blinks when SATA is active
Reset LED	Lights for 1 seconds after system reset
BIOS Select LED	Green: BIOS1 working properly
	Orange: BIOS2 working properly
	Off: BIOS1 and BIOS2 failure

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5 VPX-R3020 RTM

This chapter illustrates the board layout, connector pin assignments, and jumper settings to familiarize users with the VPX-R3020 RTM.

5.1 Connector Allocation

Function	Rear	Top	RPx	Connector Type
DisplayPort	1	—	RP1	DisplayPort connector
2x SerDes-1000BASE-BX	—	1	RP1	InfiniBand 4X Latch vertical connector
1000BASE-T	—	2	RP1	Vertical RJ45 connector
SATA	—	2	RP1	7 Pin SATA connector
USB 3.0/2.0 (Front)	1		RP2	Type-A connector
COM0 (RS232/422)	—	1	RP1	DB-9 connector
COM2 (RS-232/422/485)	—	1	RP2	2x5 pin header
GPIO, 2-bit	—	1	RP1	2x3 pin header
JTAG	—	1	RP0	2x5 pin header
Reset button	—	1	RP0	Push button
IPMB	—	1	RP0	Wafer ML 1x5P D 1.25
Power Terminals	—	4	RP0	12V, 5V, 3.3V, GND

5.2 VPX-R3020 Block Diagram

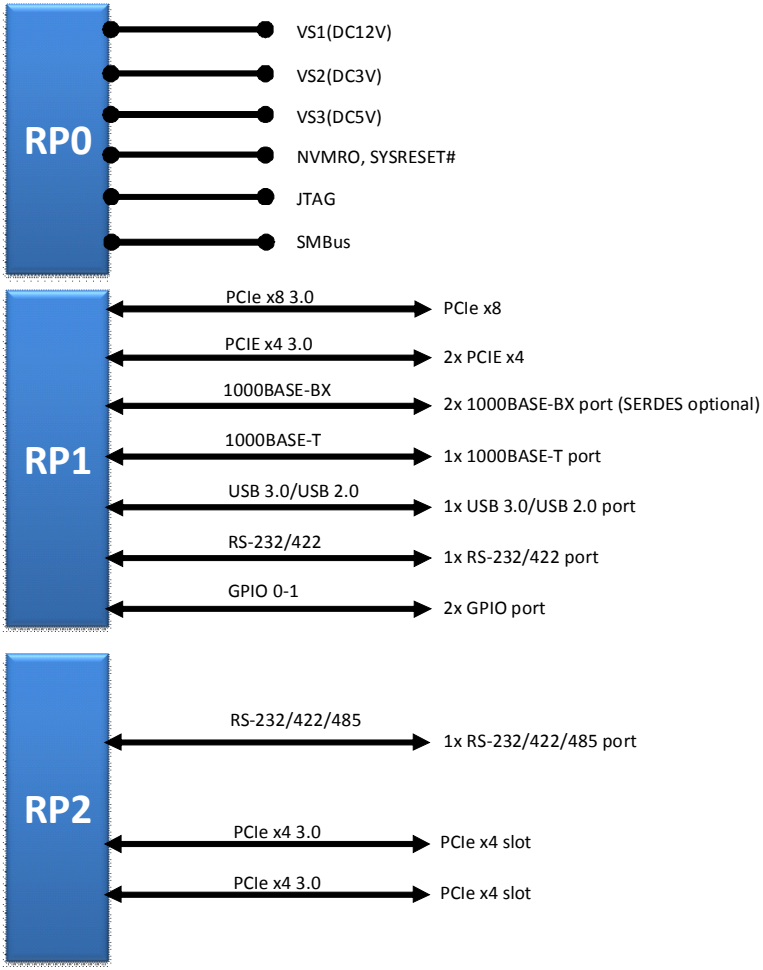


Figure 5-1: VPX-R3020 RTM Functional Block Diagram

5.3 VPX-R3020 RTM Board Layout

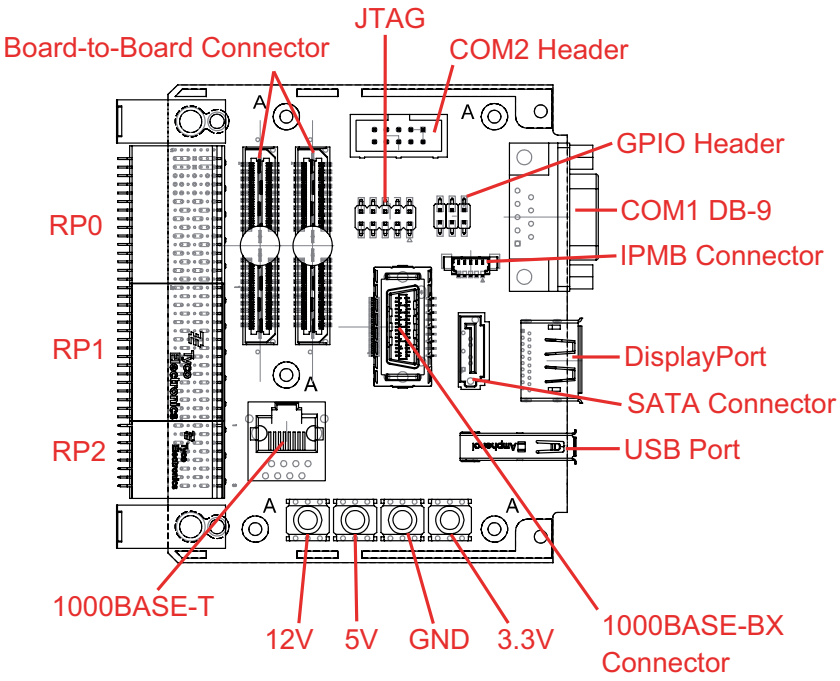


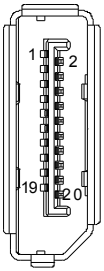
Figure 5-2: VPX-R3020 RTM Board Layout

5.4 VPX-R3020 RTM Connector Pin Assignments

Rear I/O Connectors

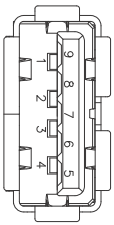
DisplayPort Connector

Pin #	Signal	Pin #	Signal
1	CN_DP0_P	2	Ground
3	CN_DP0_N	4	CN_DP1_P
5	Ground	6	CN_DP1_N
7	CN_DP2_P	8	Ground
9	CN_DP2_N	10	CN_DP3_P
11	Ground	12	CN_DP3_N
13	CN_CAD-L	14	CN_CEC
15	CN_AUX_P	16	Ground
17	CN_AUX_N	18	DDP_HPD
19	Ground	20	P3V3



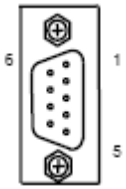
USB 3.0 Connectors

Pin #	Signal Name
1	USB3.0_P5VA
2	USB2_CMAN
3	USB2_CMAP
4	GND
5	USB3A_CMRXN
6	USB3A_CMRXP
7	GND
8	USB3A_CMTXN
9	USB3A_CMTXP



COM1 Connector (DB-9)

Pin #	RS-232	RS-422
1	NC	—
2	COM1_RXD	COM1_RX+
3	COM1_TXD	COM1_TX+
4	NC	—
5	GND	GND
6	NC	—
7	COM1_RTS#	COM1_TX-
8	COM1_CTS#	COM1_RX-
9	NC	—



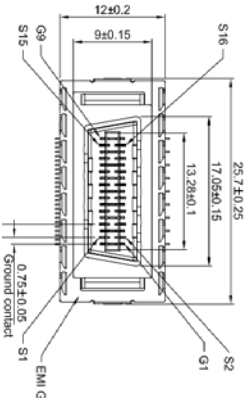
NOTE:

COM1 mode by BIOS setting.

Onboard Connectors

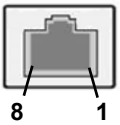
2x SerDes-1000BASE-BX Connector

Pin	Signal	Pin	Signal
S1	SER0_P	S14	SET1_P
S2	SER0_N	S15	SET0_N
S3	SER1_P	S16	SET0_P
S4	SER1_N	G1	GND
S5	NC	G2	GND
S6	NC	G3	GND
S7	NC	G4	GND
S8	NC	G5	GND
S9	NC	G6	GND
S10	NC	G7	GND
S11	NC	G8	GND
S12	NC	G9	GND
S13	SET1_N		



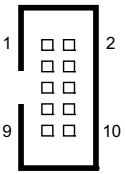
1000BASE-T (RJ-45)

Pin #	Signal
1	MX0+
2	MX0-
3	MX1+
4	MX2+
5	MX2-
6	MX1-
7	MX3+
8	MX3-



RS-232/422/485 Header (COM2)

Pin #	RS-232	RS-422/485 full duplex	RS-485 half duplex
1	NC	NC	NC
2	NC	NC	NC
3	COM2_RXD	COM2_RX+	NC
4	COM2_RTS#	COM2_TX+	COM2_DATA+
5	COM2_TXD	COM2_TX-	COM2_DATA-
6	COM2_CTS#	COM2_RX-	NC
7	NC	NC	NC
8	NC	NC	NC
9	GND	GND	GND
10	NC	NC	NC

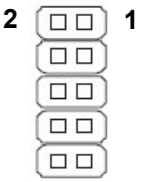


NOTE:

COM2 mode by BIOS setting.

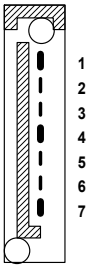
JTAG Header

Pin #	Signal
1	GND
2	TCK
3	NC
4	TDO
5	+3.3V
6	TMS
7	TRST
8	+3.3V
9	GND
10	TDI



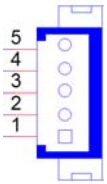
SATA Connectors

Pin #	Signal
1	GND
2	TXP
3	TXN
4	GND
5	RXN
6	RXP
7	GND



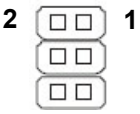
IPMB Connector

Pin #	Signal
1	IPMB_SDA
2	GND
3	IPMB_SCL
4	+5V
5	+5V



GPIO Header

Pin #	Signal
1	GPIO0
2	GPIO1
3	NC
4	NC
5	NC
6	NC



6 Getting Started

This chapter describes the installation of the following components to the VPX3020 and rear transition modules:

- VPX Blade installation to chassis
- RTM installation to chassis

6.1 Installing the VPX3020 to the Chassis

These instructions are for reference only. Refer to the user guide that comes with the chassis for more information.

1. Be sure to select the system slot to install the blade. The system power may now be powered on or off.
2. Align the module's top and bottom edges to the chassis card guides, and then carefully slide the module into the chassis. A slight resistance may be felt when inserting the module. If the resistance it too strong, check if there are wedge lock screwed or if the board's connector pins are not properly aligned with connectors on the back-plane. Then push the board until it is completely flush with the chassis.
3. Ensure the module in place, and then screw the wedge lock on the module

6.2 Installing the VPX-R3020 to the Chassis

The installation and removal procedures for a RTM are the same as those for VPX boards. Because they are shorter than front boards, pay careful attention when inserting or removing RTMs.

Refer to previous sections for peripheral connectivity of all I/O ports on the RTM. When installing the VPX3020 Series and related RTMs, make sure the RTM is the correct matching model.

6.3 Driver Installation

The VPX3020 drivers are available from the ADLINK website (**www.adlinktech.com**). ADLINK provides validated drivers for Windows 7. We recommend using the drivers provided on the ADLINK website to ensure compatibility. VxWorks BSPs can also be downloaded from the VPX3020 product page.

Detailed driver info TBD.

7 Utilities

7.1 Watchdog Timer

This section describes the operation of the VPX3020's watchdog timer (WDT). The primary function of the WDT is to monitor the VPX3020's operation and to reset the system if a software application fails to function as programmed. The following WDT functions may be controlled using a software application:

- enabling and disabling
- set and get current configuration
- reloading timeout value

The VPX3020 custom WDT circuit is implemented using the IPMC and operated by IPMI commands.

Watchdog Timer IPMI Commands

The following section describes the IPMI commands for controlling watchdog timer (WDT) functions. For more details about IPMI commands, please refer to the IPMI specification: "*Intelligent Platform Management Interface Specification Second Generation v2.0*" .

WDT Command Table

Command	NetFn Code	Cmd Code
Reset Watchdog Timer	App (06h)	22h
Set Watchdog Timer	App (06h)	24h
Get Watchdog Timer	App (06h)	25h

The WDT IPMI commands allow the user to set the countdown period and reload the timeout value periodically to keep it from resetting the system. If the timer countdown value is not reloaded, the watchdog resets the system hardware after its counter reaches zero.

Reset Watchdog Timer

This command is used to reload the WDT.

Action	Byte	Value	Description
Request	0	18h	NetFn/LUN
	1	22h	Defined command
Response	0	Complete Code	00h means OK

Set Watchdog Timer:

This command is used to set the parameters of the WDT.

Action	Byte	Value	Description
Request	0	18h	NetFn/LUN
	1	24h	Defined command
	2	[7] - 1b = don't log [6] - 1b = don't stop timer [5:3] - reserved [2:0] - timer use 000b = reserved 001b = BIOS FRB2 010b = BIOS/POST 011b = OS Load 100b = SMS/OS 101b = OEM 110b -111b = reserved	Timer Use
	3	[7] - reserved [6:4] - pre-timeout interrupt 000b = none 001b = SMI (optional) 010b = NMI / Diagnostic Interrupt (optional) 011b = Messaging Interrupt 100b,111b = reserved [3] - reserved [2:0] - timeout action 000b = no action 001b = Hard Reset 010b = Power Down 011b = Power Cycle 100b,111b = reserved	Timer Actions

Action	Byte	Value	Description
Request	4	1h~ffh (‘1h’ based.)	Pre-timeout interval in seconds.
	5	[7] - reserved [6] - reserved [5] - OEM [4] - SMS/OS [3] - OS Load [2] - BIOS/POST [1] - BIOS FRB2 [0] - reserved 0b = leave alone 1b = clear timer use expiration bit	Timer Use Expiration flags clear
	6	00h~ffh, LS byte (100 ms/count)	Initial countdown value
	7	00h~ffh, MS byte (100 ms/count)	Initial countdown value
Response	0	Complete Code	00h means OK

Get Watchdog Timer

This command is used to get the current configuration in WDT.

Action	Byte	Value	Description
Request	0	18h	NetFn/LUN
	1	25h	Defined command
Response	0	Complete Code	00h means OK
	1	[7] - 1b = don’t log [6] - 1b = don’t stop timer [5:3] - reserved [2:0] - timer use 000b = reserved 001b = BIOS FRB2 010b = BIOS/POST 011b = OS Load 100b = SMS/OS 101b = OEM 110b -111b = reserved	Timer Use

Action	Byte	Value	Description
Response	2	[7] - reserved [6:4] - pre-timeout interrupt 000b = none 001b = SMI (optional) 010b = NMI / Diagnostic Interrupt (optional) 011b = Messaging Interrupt 100b,111b = reserved [3] - reserved [2:0] - timeout action 000b = no action 001b = Hard Reset 010b = Power Down 011b = Power Cycle 100b,111b = reserved	Timer Actions
	3	1h~ffh ('1h' based.)	Pre-timeout interval in seconds.
	4	[7] - reserved [6] - reserved [5] - OEM [4] - SMS/OS [3] - OS Load [2] - BIOS/POST [1] - BIOS FRB2 [0] - reserved 0b = leave alone 1b = clear timer use expiration bit	Timer Use Expiration flags clear
	5	00h~ffh, LS byte (100 ms/count)	Initial countdown value
	6	00h~ffh, MS byte (100 ms/count)	Initial countdown value
	7	00h~ffh, LS byte (100 ms/count)	Present countdown value
	8	00h~ffh, MS byte (100 ms/count)	Present countdown value

Example of WDT Process

The sample program written in C shown below offers an interactive way to test the Watchdog Timer under DOS.

Configure WDT Parameters

```
0x40 : Don't stop timer.
0x01 : Hard Reset.
0x01 : Pre-timeout interval in 1 second.
0x08 : Timer Use Expiration flags clear by OS Load.
0x50 : 80 count. 100ms * 80 = 8000ms = 8 seconds.

[18 00 24 40 01 01 08 50 00]
```

Reset WDT

```
[18 00 22]
```


NOTE:

After setting a new configuration, the Reset WDT command must be sent. Then the WDT will be activated.

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8 BIOS Setup

The following chapter describes basic navigation for the AMIBIOS®8 BIOS setup utility.

8.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keyboard when you see the following text prompt:
   < Press DEL to run Setup >
3. After you press the < Delete > key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu.

In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

Setup Menu

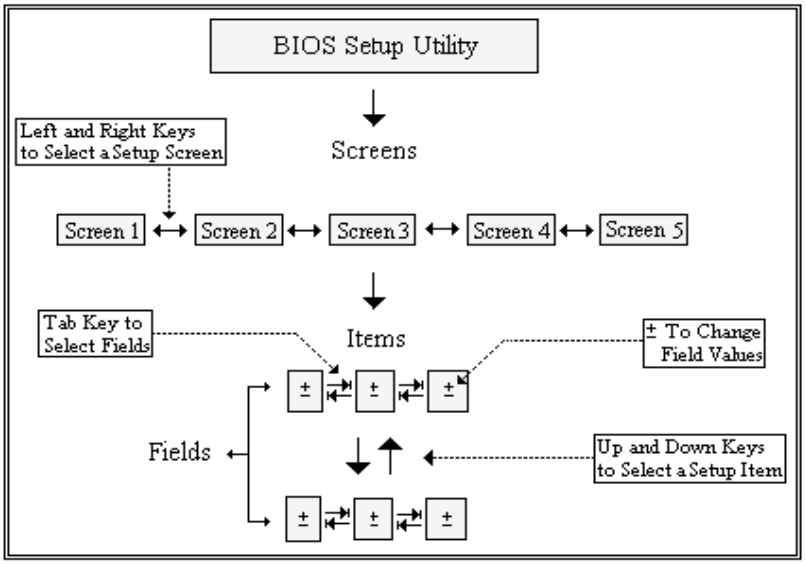
The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed" options cannot be configured, "Blue" options can be.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

Navigation

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process.



NOTE: There is a hot key legend located in the right frame on most setup screens.

→←	Left/Right. The Left and Right < Arrow > keys allow you to select a setup screen. For example: Main screen, Advanced screen, Chipset screen, and so on.
↑↓	Up/Down The Up and Down < Arrow > keys allow you to select a setup item or sub-screen.
+-	Plus/Minus The Plus and Minus < Arrow > keys allow you to change the field value of a particular setup item. For example: Date and Time.
Tab	The < Tab > key allows you to select setup fields.
ESC	The < Esc > key allows you to discard any changes you have made and exit the Setup. Press the < Esc > key to exit the setup without saving your changes. Press the < Enter > key to discard changes and exit. You can also use the < Arrow > key to select Cancel and then press the < Enter > key to abort this function and return to the previous screen.

8.2 Main Setup Menu

When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. The Main BIOS Setup menu is shown below.

Main	Advanced	Server Mgmt	Chipset	Security	Boot	Save & Exit
- BIOS Information - System Information - Board ► Information - System Date - System Time	- CPU ► Configuration - Power ► Management - USB ► Configuration - CSM ► Configuration - Super IO ► Configuration - COM Port Configuration ► - Serial Console Redirection ► - Trusted ► Computing - VPX3020 ► Configuration - Network Stack Configuration ►	- BMC Information	- PCIe Scan Delay - System Agent (SA) ► Configuration - PCI-IO ► Configuraiton	- Password ► Description - Secure Boot Menu ► - HDD Security Configuration ►	- Boot ► Configuration	- Save Changes and Exit - Save options - Boot Override

NOTE:

► indicates a submenu
Gray text indicates info only

8.2.1 Main Setup

BIOS Information

Feature	Options	Description
BIOS Vendor	Info only	BIOS Vendor
BIOS Version	Info only	Display BIOS version
Build Date	Info only	Display BIOS build Date
MCR Version	Info only	Display Memory Reference Code
GOP Version	Info only	Display GOP version
ME FW Version	Info only	Display ME Firmware version
SPI ROM Order	Info only	Display Bootup BIOS ROM Number

System Information

Feature	Options	Description
Project Version	Info only	Display ADLINK project name
CPU Board Version	Info only	Display CPU board version
CPU Board String	Info only	Display the CPU model name
CPU Stepping	Info only	Display CPU Stepping.
GT Info	Info only	Display GT info of Intel Graphics.
CPU Frequency	Info only	Display CPU frequency
Total Memory	Info only	Display installed memory size.
Memory Frequency	Info only	Display memory frequency
PCH SKU	Info only	Display chipset brand name
PCH Stepping	Info only	Display PCH Stepping.

Board Information

Feature	Options	Description
Serial Number	Info only	Display board serial number
Manufacturing Date	Info only	Display manufacturing date

8.3 Advanced

This menu contains the settings for most of the user interfaces in the system.

8.3.1 CPU Configuration

Feature	Options	Description
Type	Info only	Manufacturer, model, speed
Package	Info only	Display CPU package
CPU Stepping	Info only	Display CPU stepping
Number of Processors	Info only	Display number of processors
ID	Info only	Display CPU ID
Microcode Revision	Info only	Display Microcode Patch.
CPU Speed	Info only	Display CPU Speed.
L1 Data Cache	Info only	Display cache info.
L1 Code Cache	Info only	Display cache info.
L2 Cache	Info only	Display cache info.
L3 Cache	Inf o only	Display cache info.
L4 Cache	Inf o only	Display cache info.
VMX	Info only	Display Intel VMX Technology support or not
Intel SMX Technology	Info only	Display Intel SMX Technology support or not.
CPU Flex Ratio	**Disabled** Enabled	Enable/Disable CPU Flex Ratio Programming
Boot performance mode	Max Battery **Max Non-Turbo Performance** Trubo Performance	Select the performance state that the BIOS will set starting from reset vector.
Hyper-threading	Disabled **Enabled**	Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled only one thread per enabled core is enabled.
Intel(R) SpeedStep(TM)	Disabled **Enabled**	Allows more than two frequency ranges to be supported.
Intel(R) Speed Shift Technology	Disabled **Enabled**	Enable/Disable Intel® Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states.

Feature	Options	Description
Turbo Mode	Disabled **Enabled**	Enable/Disable turbo mode.
Configurable TDP Boot Mode	**Nominal** Deactivate	Configure TDP Mode as Nominal/Down/Disabled. Disabled option will set MSR to Nominal and MMIO to Zero.
Platform PL1 Enable	**Disabled** Enabled	Enable/Disable Platform Power Limit 1 programming. If this option is enabled, it activates the PL1 value to be used by the processor to limit the average power of given
C States	Disabled **Enabled**	Enable/Disable CPU Power Management. Allow CPU to go to C states when it's not 100% utilized.
Package C State limit	**Auto** CPU Default C10 C9 C8 C7S C7 C6 C3 C2 C0/C1	Package C State limit
Active Processor Cores	**All** 1 2 3	Number of cores to enable in each processor package.
VT-d	Disabled **Enabled**	VT-d capability

8.3.2 Power Management

Feature	Options	Description
Enable ACPI Auto	**Disabled** Enabled	Enables or Disables BIOS ACPI Auto Configuration.
Enable Hibernation	Disabled **Enabled**	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may not be effective with some operating systems.
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.

8.3.3 USB Configuration

Feature	Options	Description
XHCI Disable Compliance Mode	**Disabled** Enabled	Option to enable Compliance Mode. Default is to disable Compliance Mode. Change to enabled for Compliance Mode testing.
XDCI Support	**Disabled** Enabled	Enable/Disable XDCI (USB OTG Device)
USB Port Disable Override	**Disabled** Select Per-Pin	Selectively Enable/Disable the corresponding USB port from reporting a Device Connection to the controller.

8.3.4 CSM Configuration

Feature	Options	Description
CSM Support	**Enabled** Disable	This option controls if CSM will be launched.
CSM16 Module Version	Info only	
GateA20 Active	**Upon Request** Always	Upon Request: GA20 can be disabled using BIOS services. Always: do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.
Boot Option filter	**UEFI and Legacy** Legacy only UEFI only	This option controls what devices system can to boot.
Option ROM execution	Info only	
Network	**Do not launch** UEFI only Legacy only	Controls the execution of UEFI and Legacy PXE OpROM.
Storage	Do not launch **UEFI only** Legacy only	Controls the execution of UEFI and Legacy Storage OpROM.
Video	Do not launch **UEFI only** Legacy only	Controls the execution of UEFI and Legacy Video OpROM.
Other PCI devices	Do not launch **UEFI** Legacy OpROM	For PCI devices other than Network, Mass storage or Video defines which OpROM to launch.

8.3.5 Super IO Configuration

Feature	Options	Description
NCT5104D Super IO Configuration	Info only	
Serial Port 1(COM3) Configuration Serial Port Device Settings Change Settings	**Enabled** Disabled IO=3F8h; IRQ=4 **Auto** IO=3F8h; IRQ=4 IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12	Enable/Disable Serial Port (COM). Fixed configuration of serial port. Select an optimal setting for Super IO device.
Serial Port 2(COM1) Configuration Serial Port Device Settings Change Settings	**Enabled** Disabled IO=2F8h; IRQ=5 **Auto** IO=2F8h; IRQ=3 IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12	Enable/Disable Serial Port (COM). Fixed configuration of serial port. Select an optimal setting for Super IO device.
Serial Port 3(COM4) Configuration Serial Port Device Settings Change Settings	**Enabled** Disabled IO=3E8h; IRQ=3 **Auto** IO=3E8h; IRQ=7 IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12 IO=220h; IRQ=3,4,5,6,7,9,10,11,12 IO=228h; IRQ=3,4,5,6,7,9,10,11,12	Enable/Disable Serial Port (COM). Fixed configuration of serial port. Select an optimal setting for Super IO device.

Feature	Options	Description
Serial Port 4(COM2) Configuration	**Enabled** Disabled	Enable/Disable Serial Port (COM).
Serial Port Device Settings	IO=2E8h; IRQ=10	Fixed configuration of serial port.
Change Settings	**Auto** IO=2E8h; IRQ=7 IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12 IO=220h; IRQ=3,4,5,6,7,9,10,11,12 IO=228h; IRQ=3,4,5,6,7,9,10,11,12	Select an optimal setting for Super IO device.

8.3.6 COM Port Configuration

Feature	Options	Description
COM Port Speed	**Legacy** High-Speed(500K)	Select COM Port Speed as legacy or High-Speed (500K)
COM1 Port Standard	**RS-232** RS-422 TM Master RS-422 TM Slave RS-422 (Non-TM)	Select Serial Port Standard of COM1
COM2 Port Standard	**RS-232** RS-422 TM Master RS-422 TM Slave RS-422 (Non-TM) RS-485 TM RS-485 (Non-TM)	Select Serial Port Standard of COM2

8.3.7 Serial Console Redirection

Feature	Options	Description
COM1	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	
COM2	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	
COM3	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	
COM4	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	

Console Redirection Settings

Feature	Options	Description
Console Redirection Settings	Info only	
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed.
Data Bits	7 **8**	Select Data Bits.
Parity	**None** Even Odd Mark Space	Select Parity.
Stop Bits	**1** 2	Select number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Select flow control.
VT-UTF8 Combo Key Support	Disabled **Enable**	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.
Recorder Mode	**Disabled** Enable	With this mode enabled only text will be sent. This is to capture Terminal data.
Resolution 100x31	**Disabled** Enable	Enables or disables extended terminal resolution
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.

Legacy Console Redirection Settings

Feature	Options	Description
Legacy Serial Redirection Port	**COM0** COM1 COM2 COM3	Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages.
Legacy OS Redirection	**80x24** 80x25	On Legacy OS, the Number of Rows and Columns supported redirection
Redirection After BIOS Post	**Always Enabled** BootLoader	The Settings specify if BootLoader is selected than Legacy console redirection is disabled before booting to Legacy OS. Default value is Always Enable which means Legaacy console Redirection is enabled for Legacy OS.

8.3.8 Trusted Computing

Feature	Options	Description
Security Device	**Disabled** Enabled	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not e available.

8.3.9 VPX3020 Configuration

Feature	Options	Description
GPIO Configuration	Submenu	
System Reset Bi-direction	**Disabled** Enabled	Switch to Enable/Disable Bi-direction System Reset from IPMC
XMC Bifurcation	**1x8** 2x4	Select bifurcation for XMC
PCIe Station 0	4x2 **2x4** 1x8	Select PCIe Station 0 bifurcation
PCIe Station 1	2x2 **1x4**	Select PCIe Station 1 bifurcation
PCIe Speed	Gen1 Gen2 **Gen3**	Configure PCIe Switch link speed

GPIO Configuration

Feature	Options	Description
GDISC1#_R	**Output** Input	Select Configuration of GPIO GDISC1#_R
GPIO Status	**High** Low	
GPIO0_R	**Output** Input	Select Configuration of GPIO GPIO0_R
GPIO Status	**High** Low	
GPIO1_R	**Output** Input	Select Configuration of GPIO GPIO1_R
GPIO Status	**High** Low	

8.3.10 Network Stack Configuration

Feature	Options	Description
Network Stack	Info only	
Network Stack	Enabled **Disabled**	Enable/Disable UEFI network stack.
Network Stack Options	Info only	
Ipv4 PXE Support	**Enabled** Disabled	Enable/Disable Ipv4 PXE Support
Ipv4 HTTP Support	Enabled **Disabled**	Enable/Disable Ipv4 HTTP Support
Ipv6 PXE Support	Enabled **Disabled**	Enable/Disable Ipv6 PXE Support
Ipv6 HTTP Support	Enabled **Disabled**	Enable/Disable Ipv6 HTTP Support
IPSEC Certificate	**Enabled** Disabled	Enable/Disable IPSEC Certificate

8.4 Server Mgmt

Feature	Options	Description
BMC Self Test Status	Info only	Display BMC Self Test Status
BMC Device ID	Info only	Display BMC Device ID
BMC Device Revision	Info only	Display BMC Device Revision
BMC Firmware Revision	Info only	Display BMC Firmware Revision
IPMI Version	Info only	Display IPMI Version
BMC Interface(s)	Info only	Display BMC Interface(s)
BMC Support	**Enabled** Disabled	Enable/Disable interfaces to communicate with BMC

8.5 Chipset

Feature	Options	Description
PCIe Scan Delay	**0**	System delay before PCIe scan. Unit is second and maximum value is 60 seconds.
System Agent (SA) Configuration	Submenu	
PCI-IO Configuration	Submenu	

8.5.1 System Agent (SA) Configuration

Feature	Options	Description
SA PCIe Code Version	Info only	Display SA PCIe code version
Memory Configuraiton	Submenu	
Graphics Configuration	Submenu	
PEG Port Configuration	Submenu	

Memory Configuration

Feature	Options	Description
Memory RC Version	Info only	Display memory RC version
Memory Frequency	Info only	Display memory frequency
Memory Voltage	Info only	Display memory voltage
Memory Timings (tCL-tRCD-tRP-tRAS)	Info only	Display memory timimgs
Channel 0 Slot 0	Info only	Display size, number of ranks, manufacturer
Channel 1 Slot 0	Info only	Display size, number of ranks, manufacturer
Maximum Memory Frequency	**Auto** 1067 1200 1333 1400 1600 1800 1867 2000 2133 2200 2400 2666	Maximum Memory Frequency Selections in Mhz. Valid values should match the refclk, i.e. divide by 133 or 100
Max TOLUD	**Dynamic** 1 GB 1.25 GB 1.5 GB 1.75 GB 2 GB 2.25 GB 2.5 GB 2.75 GB 3 GB 3.25 GB 3.5 GB	Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.

Graphics Configuration

Feature	Options	Description
Skip Scaning of External Gfx Card	**Disabled** Enabled	If Enable, it will not scan for External Gfx Card on PEG and PCH PCIE Ports
Primary Display	**Auto** IGFX PEG PCI SG	Select which of IGFX/PEG/PCI Graphics device should be Primary Display or select SG for switchable Gfx.
Select PCIE Card	**Auto** Elk Creek 4 PEG Eval	Select the card used on the platform Auto: Skip GPIO based Power Enable to dGPU Elk Creek 4: DGPU Power Enable = ActiveLow PEG Eval: DGPU Power
Internal Graphics	**Auto** Disabled Enabled	Keep IGFX enabled based on the setup options.
GTT Size	2MB 4MB **8MB**	Select the GTT Size
Aperture Size	128MB **256MB** 512MB 1024MB 2048MB	Select the Aperture Size Note: Above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM support.
DVTM Pre-Allocated	4M 8M 16M **32M** 64M	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory Size used by the Internal Graphics Device.
DVMT Total Gfx Mem	128M **256M** MAX	Select DVMT5.0 Total Graphc Memory Size used by the Interal Graphics Device.

PEG Port Configuration

Feature	Options	Description
PEG 0:1:0	Info only	
Enable Root Port	Disabled Enabled **Auto**	Enable or Disable the Root Port
Max Link Speed	**Auto** Gen1 Gen2 Gen3	Configure PEG 0:1:0 Max Speed
PEG0 Slot Power Limit Value	**75**	Sets the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying this value by the Slot Power Limit Scale. Values 0-255
PEG0 Slot Power Limit Scale	**1.0x** 0.1x 0.01x 0.001x	Select the scale used for the Slot Power Limit Value.
PEG0 Physical Slot Number	**1**	Set the physical slot number attached to this Port. The number has to be globally unique within the chassis. Values 0-8191
PEG0 Max Payload Size	**Auto** 128 256 TLP	Select PEG0 Max Payload Size; Choose Auto(Default Device Capability) or force to 128/256 Bytes.
PEG 0:1:1	Info only	
Enable Root Port	Disabled Enabled **Auto**	Enable or Disable the Root Port
Max Link Speed	**Auto** Gen1 Gen2 Gen3	Configure PEG 0:1:1 Max Speed
PEG1 Slot Power Limit Value	**75**	Sets the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying this value by the Slot Power Limit Scale. Values 0-255
PEG1 Slot Power Limit Scale	**1.0x** 0.1x 0.01x 0.001x	Select the scale used for the Slot Power Limit Value.
PEG1 Physical Slot Number	**2**	Set the physical slot number attached to this Port. The number has to be globally unique within the chassis. Values 0-8191

Feature	Options	Description
PEG 0:1:2	Info only	
Enable Root Port	Disabled Enabled **Auto**	Enable or Disable the Root Port
Max Link Speed	**Auto** Gen1 Gen2 Gen3	Configure PEG 0:1:2 Max Speed
PEG2 Slot Power Limit Value	**75**	Sets the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying this value by the Slot Power Limit Scale. Values 0-255
PEG2 Slot Power Limit Scale	**1.0x** 0.1x 0.01x 0.001x	Select the scale used for the Slot Power Limit Value.
PEG2 Physical Slot Number	**3**	Set the physical slot number attached to this Port. The number has to be globally unique within the chassis. Values 0-8191
PEG 0:6:0	Info only	
Enable Root Port	Disabled Enabled **Auto**	Enable or Disable the Root Port
Max Link Speed	**Auto** Gen1 Gen2 Gen3	Configure PEG 0:1:2 Max Speed
PEG3 Slot Power Limit Value	**75**	Sets the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying this value by the Slot Power Limit Scale. Values 0-255
PEG3 Slot Power Limit Scale	**1.0x** 0.1x 0.01x 0.001x	Select the scale used for the Slot Power Limit Value.
PEG3 Physical Slot Number	**3**	Set the physical slot number attached to this Port. The number has to be globally unique within the chassis. Values 0-8191
Gen3 RxCTLE Control	Submenu	
PCIe Rx CEM Test Mode	**Disabled** Enabled	Enable/Disable PEG Rx CEM Loopback Mode
PCIe Spread Spectrum	**Disabled** Enabled	Allows disabling Spread Spectrum Clocking for compliance testing

PEG Port Configuration > Gen3 RxCTLE Control

Feature	Options	Description
Bundle0	**0**	Gen3 RxCTLE setting for Bundle0
Bundle1	**0**	Gen3 RxCTLE setting for Bundle1
Bundle3	**0**	Gen3 RxCTLE setting for Bundle3
Bundle4	**0**	Gen3 RxCTLE setting for Bundle4
Bundle5	**0**	Gen3 RxCTLE setting for Bundle5
Bundle6	**0**	Gen3 RxCTLE setting for Bundle6
Bundle7	**0**	Gen3 RxCTLE setting for Bundle7
PEG10 RxCTLE Override	**Disabled** Enabled	When Enabled, it overrides PEG0 RxCTLE adaptive behavior
PEG11 RxCTLE Override	**Disabled** Enabled	When Enabled, it overrides PEG1 RxCTLE adaptive behavior
PEG11 RxCTLE Override	**Disabled** Enabled	When Enabled, it overrides PEG2 RxCTLE adaptive behavior
DMI RxCTLE Override	**Disabled** Enabled	When Enabled, it overrides DMI RxCTLE adaptive behavior

8.5.2 PCH-IO Configuration

Feature	Options	Description
PCI Express Configuration	Submenu	
SATA And RST Configuration	Submenu	
Serial IRQ Mode	**Continuous**	Configure Serial IRQ Mode.
High Precision Timer	Enabled Disabled	Enable or Disable the High Precision Event Timer.

PCI Express Configuration

Feature	Options	Description
PCI Express Clock Gating	**Enabled** Disabled	PCI Express Clock Gating Enable/Disable for each root port.
DMI Link ASPM Control	Disable L0s L1 L0sL1 **Auto**	The control of Active State Power Management of the DMI Link.
PCIE Port assigned to LAN	**Disabled**	Fixed
Compliance Test Mode	**Disabled** Enabled	Enable when using Compliance Load Board
PCIe-USB Glitch W/A	**Disabled** Enable	PCIe-USB Glitch W/A for bad USB device(s) connected behind PCIE/PEG Port.
PCIe function swap	Disabled **Enabled**	When Disabled, prevents PCIE rootport function swap. If any function other than 0^{th} is enabled, 0^{th} will become visible.
PCI Express Root Port5	Submenu	
PCI Express Root Port21	Submenu	

PCI Express Configuration > PCI Express Root Port x

Feature	Options	Description
PCI Express Root Port_x	**Enabled** Disabled	PCI Express Clock Gating Enable/Disable for each root port.
Disable Gen2 Pll Shutdown and L1 Controller Power gating	**Disabled** Enabled	When Enabled, disables Gen2 PLL Shutdown and L1 Controller power gating, Enable this option if using Titan Ridge A0/Alpine Ridge thunderbolt controller.
Connection Type	**Slot**	
ASPM 0	Disabled L0s L1 L0sL1 **Auto**	Set the ASPM Level: Force L0s – Force all links to L0s State AUTO – BIOS auto configure DISABLE – Disables ASPM
L1 Substates	Disables L1.1 **L1.1 & L1.2**	PCI Express L1 Substates settings.
Gen3 Eq Phase3 Method	**Hardware** Static Coeff.	PCIe Gen3 Equalization Phase 3 Method

Feature	Options	Description
UPTP	**5**	Upstream Port Transmitter Preset
DPTP	**7**	Downstream Port Transmitter Preset
ACS	Disabled **Enabled**	Enable/Disable Access Control Services Extended Capability
PTM	Disabled **Enabled**	Enable/Disable Precision Time Measurement
DPC	Disabled **Enabled**	Enable/Disable Downsteam Port Containment
EDPC	Disabled **Enabled**	Enable/Disable Rootport extensions for Downstream Port containment
URR	**Disabled** Enabled	PCI Express Unsupported Request Reporting Enable/Disable
FER	**Disabled** Enabled	PCI Express Device Fatal Error Reporting Enable/Disable
NFER	**Disabled** Enabled	PCI Express Device Non-Fatal Error Reporting Enable/Disable.
CER	**Disabled** Enabled	PCI Express Device Correctable Error Reporting Enable/Disable.
CTO	**Disabled** Enabled	PCI Express Completion Timer to Enable/Disable.
SEFE	**Disabled** Enabled	Root PCI Express System Error on Fatal Error Enable/Disable.
SENFE	**Disabled** Enabled	Root PCI Express System Error on Non-Fatal Error Enable/Disable
SECE	**Disabled** Enabled	Root PCI Express System Error on Correctable Error Enable/Disable.
PME SCI	Disabled **Enabled**	PCI Express PME SCI Enable/Disable.
Hot Plug	Disabled **Enabled**	PCI Express Hot Plug Enable/Disable.
Advanced Error Reporting	Disabled **Enabled**	Advanced Error Reporting Enable/Disable.
PCIe Speed	**Auto** Gen1 Gen2 Gen3	Configure PCIe Speed
Transmitter Half Swing	**Disabled** Enabled	Transmitter Half Swing Enable/Disable
Detect Timeout	**0**	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.

Feature	Options	Description
Extra Bus Reserved	**0**	Extra Bus Reserved (0-7) for bridges behind this Root Bridge.
Reserved Memory	**10**	Reserved Memory for this Root Bridge (1-20) MB
Reserved I/O	**4**	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.
PCH PCIe LTR Configuration	Info only	
LTR	Disabled **Enabled**	PCH PCIE Latency Reporting Enable/Disable
Snoop Latency Override	Disabled Manual **Auto**	Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Non Snoop Latency Override	Disabled Manual **Auto**	Non Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Force LTR Override	**Disabled** Enabled	Force LTR Override for PCH PCIE. Disabled: LTR override values will not be forced. Enable: LTR override values will be forced and LTR messages from the device will be ignored.
LTR Lock	**Disabled** Enabled	PCIE LTR Configuration Lock
Extra options	Submenu	

PCI Express Root Port x > Extra options

Feature	Options	Description
Detect Non-Compliance	**Disabled** Enabled	Detect Non-Compliance PCI Express Device. If enable, it will take more time at POST time.
Prefetchable Memory	**10**	Prefetchable Memory Range for this Root Bridge
Reserved Memory Alignment	**1**	Reserved Memory Alignment (0-31 bits)
Prefetchable Memory Alignment	**1**	Prefetchable Memory Alignment (0-31 bits_

SATA and RST Configuration

Feature	Options	Description
SATA Controller(s)	**Enabled** Disabled	Enable/Disable SATA Deice
SATA Mode Selection	**AHCI** Intel RST Premium with Intel Optane System Acceleration	Determinces how SATA Controller(s) operate.
SATA Test Mode	Enabled **Disabeld**	Test Mode Enable/Disable (Loop Back).
Software Feature Mask Configuration	Submenu	
Aggressive LPM Support	Disabled **Enabled**	Enable PCH to aggressively enter link power state.
SATA Controller Speed	Default Gen1 Gen2 **Gen3**	Indicates the maximum speed the SATA controller can support.
Serial ATA Port x (x=0~7)	Info only	
Port x	Disabled **Enabled**	Enable or Disable SATA Port
Hot Plug	**Disabled** Enabled	Designates this port as Hot Pluggable.
External	**Disabled** Enabled	Marks this port as external.
Spin Up Device	**Disabled** Enabled	If enabled for any of ports Staggerred Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	**Hard Disk Drive** Solid State Drive	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive
SATA Port x DevSlp	**Disabled** Enabled	Enable/Disable SATA Port x DevSlp. For DevSlp to work, both hard drive and SATA port need to support DevSlp function, otherwise an unexpected beharvior ight happen.
DITO Configuration	**Disabled** Enabled	Enable/Disable DITO Configuration
DITO Value	Info only	Display DITO value
DM Value	Info only	Display DM value

SATA and RST Configuration > Software Feature Mask Configuration

Feature	Options	Description
HDD Unlock	**Enabled** Disabled	If enabled, indicates that the HDD password unlock in the OS is enabled.
LED Locate	**Enabled** Disabled	If enabled, indicates that the HDD password unlock in the OS is enabled.

8.6 Boot

8.6.1 *Boot Configuration*

Feature	Options	Description
Boot Configuration	Info only	
Setup Prompt Timeout	**3**	Number of seconds to wait for setup activation key. 65535(0Xffff) means indefinite waiting.
Bootup NumLock State	**On** Off	Select the keyboard Numlock state
Quiet Boot	Disabled **Enabled**	Enables or disables Quiet Boot option
Fast Boot	Disable **Enable**	Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.
SATA Support	**Last Boot SATA Devices Only** All SATA Devices	If Last Boot SATA Devices only, only last boot SATA device will be available in Post. If All SATA Devices, all SATA devices will be available in OS and Post.
VGA Support	Auto **EFI Driver**	If Auto, only install Legacy OpRom with Legacy OS and logo would NOT be shown during post. EFI driver will still be installed with EFI OS.
USB Support	Disabled **Full Initial** Partial Initial	If Disabled, all USB devices will NOT be available until after OS boot. If Partial Initial, USB Mass Storage and specific USB port/device will NOT be available before OS boot. If Enabled, all USB devices will be available in OS and Post.
PS2 Devices Support	Disable **Enable**	If Disabled, PS2 device will be skipped.
Network Stack Driver	Disabled **Enabled**	If Disabled, Network Stack Driver will be skipped.
Redirection Support	**Disabled** Enabled	If Disabled, Redirection function will be disabled.
BIOS mode select	LEGACY **UEFI**	Select boot mode LEGACY/UEFI
Boot Configuration	Info only	
Boot Option #1	Hard Disk	Sets the system boot order
Boot Option #2	CD/DVD	Sets the system boot order
Boot Option #3	USB Hard Disk	Sets the system boot order

Feature	Options	Description
Boot Option #4	USB CD/DVD	Sets the system boot order
Boot Option #5	USB Key	Sets the system boot order
Boot Option #6	USB Floppy	Sets the system boot order
Boot Option #7	USB Lan	Sets the system boot order
Boot Option #8	Network	Sets the system boot order

8.7 Save & Exit

8.7.1 Reset Options

Feature	Options	Description
Save Changes and Reset	Save changes and reset the system.	Save Changes and Reset
Discard Changes and Reset	Reset the system without saving any changes.	Discard Changes and Reset

8.7.2 Save Options

Feature	Options	Description
Save Changes		Save Changes done so far to any of the setup options.
Discard Changes		Discard Changes done so far to any of the setup options.
Restore Defaults		Restore/Load Default values for all the setup options.
Save as User Defaults		Save the changes done so far as User Defaults.
Restore User Defaults		Restore the User Defaults to all the setup options.

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Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

A Lithium-type battery may be provided for uninterrupted, backup or emergency power.

Risk of explosion if battery is replaced with one of an incorrect type. Dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

Getting Service

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