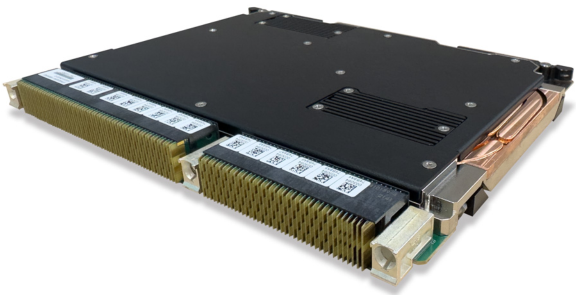
VPX6200

VPX Dual Node Blade with
Intel® Xeon®
W-11865MRE

User's Manual



Manual Rev.:	1.0
Revision Date:	May 3, 2024
Part No:	50M-31428-1000

Leading **EDGE COMPUTING**

Revision History

Revision	Release Date	Description of Change(s)
1.0	2024-05-03	Initial release

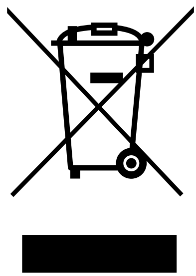
Preface

Disclaimer

The information in this document is subject to change without prior notice in order to improve reliability, design, and function and does not represent a commitment on the part of the manufacturer.

In no event will the manufacturer be liable for direct, indirect, special, incidental, or consequential damages arising out of the use or inability to use the product or documentation, even if advised of the possibility of such damages.

Environmental Responsibility



ADLINK is committed to fulfill its social responsibility to global environmental preservation through compliance with the European Union's Restriction of Hazardous Substances (RoHS) directive and Waste Electrical and Electronic Equipment (WEEE) directive. Environmental protection is a top priority for ADLINK. We have enforced measures to ensure that our products, manufacturing processes, components, and raw materials have as little impact on the environment as possible. When products are at their end of life, our customers are encouraged to dispose of them in accordance with the product disposal and/or recovery programs prescribed by their nation or company.

Battery Labels

California Proposition 65 Warning

WARNING: This product can expose you to chemicals including acrylamide, arsenic, benzene, cadmium, Tris(1,3-dichloro-2-propyl)phosphate (TDCPP), 1,4-Dioxane, formaldehyde, lead, DEHP, styrene, DINP, BBP, PVC, and vinyl materials, which are known to the State of California to cause cancer, and acrylamide, benzene, cadmium, lead, mercury, phthalates, toluene, DEHP, DIDP, DnHP, DBP, BBP, PVC, and vinyl materials, which are known to the State of California to cause birth defects or other reproductive harm. For more information go to www.P65Warnings.ca.gov**.**

Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

NOTE:	Additional information, aids, and tips that help users perform tasks.

CAUTION:	Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

WARNING:	Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

Table of Contents

List of Figures

This page intentionally left blank.

List of Tables

This page intentionally left blank.

1 Introduction

1.1 Overview

The VPX6200 is a 6U VPX processor blade with 11th Gen Intel® Xeon® W11865MRE processor that provides high-performance data processing. The dual node architecture is designed for redundancy, fulfilling the reliability requirement in mission-critical applications.

The VPX6200 features a PCIe switch that allows it to be configured as end-point mode VPX6200 for multiple processor blade computing applications by connecting to the host VPX6200.

Each node comes with dual channel 32GB DDR4-3200 soldered ECC memory, an M.2 2242 slot for NVMe or SATA SSD installation, 2x 10GBase-KX4 as data plane for high-speed backplane communication, 1x HDMI for video, 6x USB + 2x RS232/422 for I/O connectivity, and additional 3x SATA for flexible storage.

The VPX6200 is a conduction-cooled 6U VPX blade compliant with VITA 46/48/65, and the rugged design supports VITA47.0, ECC4 standard that provides faster deployment for military-grade subsystems in harsh environments.

1.2 Features

- Dual nodes, redundant architecture
- 1x Intel ® Xeon ® W-11865MRE processor per node (formerly Tiger Lake-H)
- Dual channel 32GB DDR4-3200 soldered with ECC per node
- 1x M.2 2242 slot per node (1TB by BOM option)
- VITA 46/48/65 compliant for quick deployment
- Supports Windows 10 IoT Enterprise LTSC 21H2 and Linux (kernel 5.13 and higher)
- Module profile: MOD6-PAY-4F2T-12.2.2 (default SKU)
- Slot profile: SLT6-PAY-4F2T-10.2.2 (default SKU)

1.3 Functional Block Diagrams

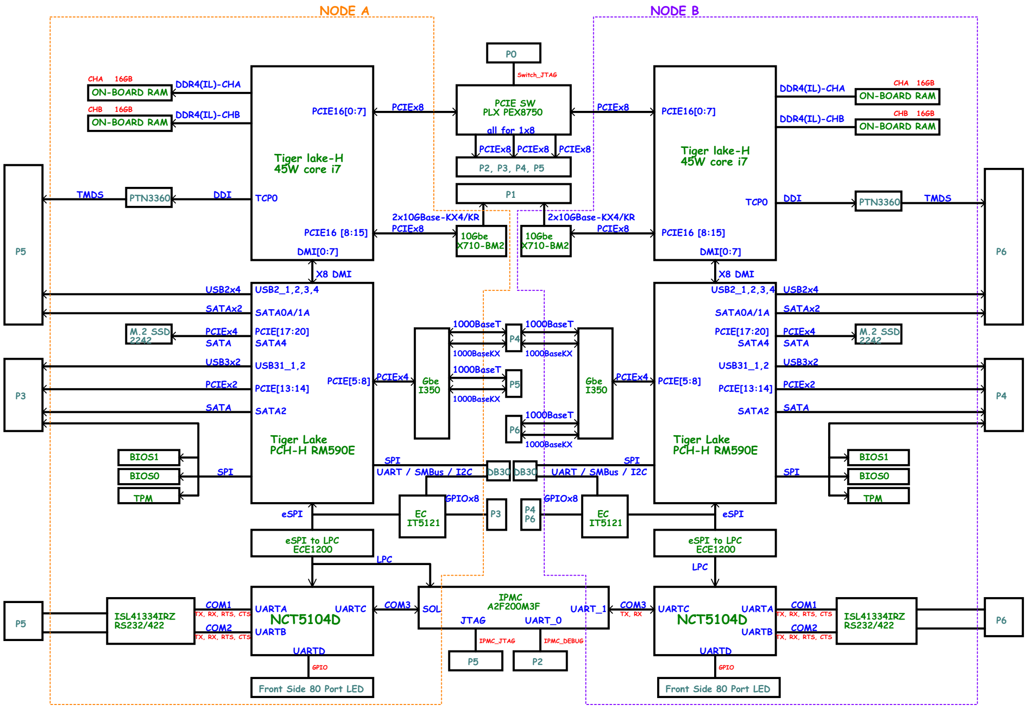


Figure 1-1: VPX6200 Functional Block Diagram

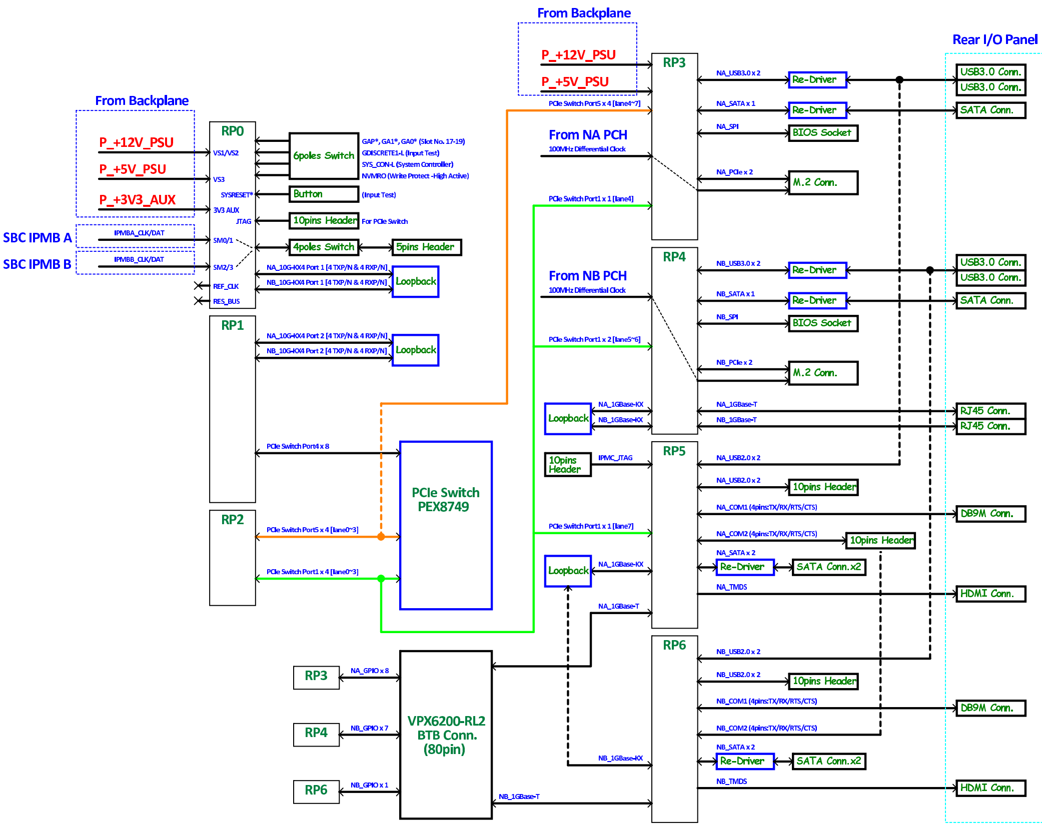


Figure 1-2: VPX6200-RL1 RTM Functional Block Diagram

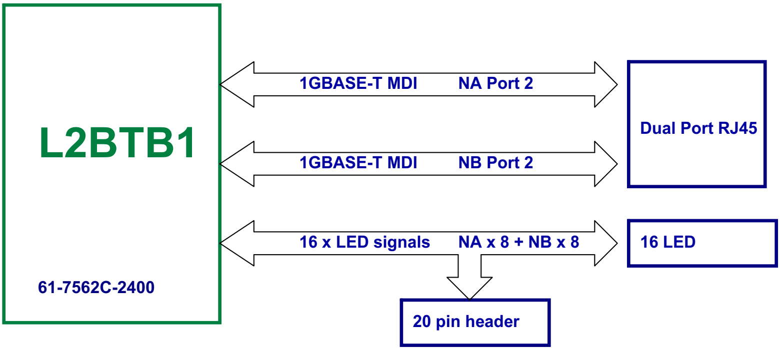


Figure 1-3: VPX6200-RL2 RTM Functional Block Diagram

1.4 Model Number Decoder - Processor Blade

VPX6200/W11865MRE/M32/S128/10GBase-KR

(A) (B) (C) (D)

(A) CPU Code

- ▷ **W1186MRE** = Dual node 8-core Intel® Xeon® W11865MRE processor

(B) Memory Size Code

- ▷ **M32** = Onboard 32GB DDR4-3200 memory (each node)

(C) NVMe SSD Size Code

- ▷ **S128** = NVMe 128GB (each node)

(D) Customization Code

- ▷ **10GBase-KR** = 1x 10GBase-KR per node instead of 2x 10GBase-KX4

1.5 Package Contents

The VPX6200 is packaged with the following components. If any of the items on the contents list are missing or damaged, retain the shipping carton and packing material and contact the dealer for inspection. Please obtain authorization before returning any product to ADLINK. The packing contents of the VPX6200 are non-standard configurations and may vary depending on customer requests.

Processor Blade

- VPX6200
  - CPU and memory specifications will differ depending on options selected
  - Thermal module is assembled on the board

Rear Transition Module

- VPX6200-RL1 RTM
- VPX6200-RL2 RTM

NOTE:

The contents of non-standard VPX6200 configurations may vary depending on the customer requirements.

CAUTION:

This product must be protected from static discharge and physical shock. Never remove any of the components except at a static-free workstation. Use the anti-static bag shipped with the product when putting the board on a surface. Wear an anti-static wrist strap properly grounded on one of the system's ESD ground jacks when installing or servicing system components.

2 Specifications

2.1 VPX6200 Blade Specifications

Architecture	• Dual nodes, redundant architecture
CPU	• 1x Intel ® Xeon ® W-11865MRE per node (formerly Tiger Lake-H) TDP 45W
Chipset	• 1x Intel ® RM590E chipset per node
Memory	• Dual channel 32GB DDR4-3200 soldered with ECC per node
BIOS	• AMI ® UEFI BIOS, Dual BIOS per node • 32MB SPI flash memory per node
VITA Standards	• VITA 46/48/65 compliant
Data Transport	• 2x 10GBASE-KX4 to P1 per node (default SKU) • 1x 1000BASE-T to P4 per node • 1x 10GBASE-KR to P1 per node (BOM option: 10GBASE-KR SKU) • 1x 1000BASE-KX to P4 per node • 1x 1000BASE-T + 1x 1000BASE-BX to P5 for node A (BOM option: 1000BASE-KX) • 1x 1000BASE-T + 1x 1000BASE-BX to P6 for node B (BOM option: 1000BASE-KX) • 3x PCIe Gen3 x8 to P2, P3, P4, P5 • 1x PCIe Gen3 x2 to P3 for node A • 1x PCIe Gen3 x2 to P4 for node B
Video	• 1x HDMI 1.4 to P5 for node A • 1x HDMI 1.4 to P6 for node B (HDMI is not hot-pluggable in BIOS mode)
USB	• 2x USB 3.2 Gen 1 to P3 for node A • 2x USB 3.2 Gen 1 to P4 for node B • 4x USB • 2.0 to P5 for node A • 4x USB • 2.0 to P6 for node B • Supports USB 3.0 power (supply 0.9A) with overcurrent protection • Supports USB 2.0 power (supply 0.5A) with overcurrent protection

Table 2-1: VPX6200 Blade Specifications

Serial Port	• 2x RS-232/422 to P5 for node A (COM1, COM2) • 2x RS-232/422 to P6 for node B (COM1, COM2) • Max. data rate for RS-232/422 is 115200bps • RS-232/422 mode configuration via BIOS
GPIO	• 8x GPIO to P3 for node A • 8x GPIO to P4, P6 for node B • 3.3V sig • naling • GPIO pins routed to RTM (3.3V with level trigger)
SATA	• 1x SATA 6Gb/s to P3 + 2x SATA 6Gb/s to P5 for node A • 1x SATA 6Gb/s to P4 + 2x SATA 6Gb/s to P6 for node B
M.2	• 1x M.2 M key 2242 slot per node • Supports interface: PCIe3.0 x4 and SATA3.0 • Supports module height: S1, S2, D1, D2 (D2 is default) • 128GB 3D TLC NVMe with Windows 10 IoT Enterprise LTSC 21H2 preinstalled per node (OS licenses are not included)
TPM	• Discrete TPM 2.0 chip • Supports Intel Secure Boot (UEFI)
BIOS	• Dual BIOS support
Operating System	• Windows 10 IoT Enterprise LTSC 21H2 • Linux (kernel 5.13 and higher)
Power Requirement	• 12V (VS1/VS2) • 5V (VS3) • 3.3V_AUX only • Max. 100W

Table 2-1: VPX6200 Blade Specifications

Miscellaneous	• Watchdog Timer System reset and NMI, with programmable interval, 0-6553 seconds via IPMC • Hardware Monitor Monitors CPU temperature, system temperature, Vcore and DC voltages • IPMC SmartFusion SoC provides IPMI software functions Firmware updateable (via JTAG pin header on VPX6200-RL1) • Serial Over LAN SOL port via IPMC (COM3) for node A • Management Port Management port via UART (COM3) for node B • DB30 Port 2x DB30 ports on the front panel of each node to flash BIOS and EC (even if the system is unbootable) • Heater Built-in heater enhances low operating temperature capability • LEDs Status LEDs on front panel • Reset Button Reset button on front panel • Thermal Safety When the PCIe switch temperature reaches 95°C, IPMC will automatically shut down the VPX6200
Mechanical	• Form Factor 6U VPX, conduction-cooled construction, 0.85” pitch (VITA 48.2) • Thermal Dissipation Conduction-cooling by wedge lock • M.2 Storage Cover Aluminum covers with heatsink design per node for M.2 storage installation

Table 2-1: VPX6200 Blade Specifications

Environmental	• Operating Temperature -40°C to +85°C at wedge locks (VITA47.0, ECC4-CC4) • Storage Temperature -55°C to +105°C • Vibration Random: 12Grms, 5Hz to 2000Hz (VITA47.0, ECC4-V3) Sinusoidal: 5g, 20Hz to 2000Hz • Shock 40g, 11 ms (VITA47.0, ECC4-OS2) • Relative Humidity 95% non-condensing • Altitude 40,000 ft. (operating) • MTBF 105,594 hours (without SSD) and 104,313 hours (with 128GB 3D TLC NVMe, according to MIL HDBK 217F Notice 2)
EMC	• CE (EN555032/EN55035) ; FCC Part 15B Class A

Table 2-1: VPX6200 Blade Specifications

Note: Specifications are subject to change without prior notice.

2.2 VPX6200-RL1 RTM Specifications

VITA Standards	• VITA 46.10 Rear Transition Module on VPX
PCIe Switch Communication	• Broadcom PEX8749 • PCIe Port 1 x4 (lane0-3) to RP2 • PCIe Port 1 x1 (lane4) to RP3 • PCIe Port 1 x2 (lane5-6) to RP4 • PCIe Port 1 x1 (lane7) to RP5 • PCIe Port 4 x 8 (lane0-7) to RP1 • PCIe Port 5 x4 (lane0-3) to RP2 • PCIe Port 5 x4 (lane4-7) to RP3
Node A & Node B Loopback	• 1x 10GBASE-KX4 from RP0 for node A & • 1x 10GBASE-KX4 from RP0 for node B loopback (port 1) • 1x 10GBASE-KX4 from RP1 for node A & • 1x 10GBASE-KX4 from RP1 for node B loopback (port 2) • 1x 1000BASE-KX from RP4 for node A & • 1x 1000BASE-KX from RP4 for node B loopback • 1x 1000BASE-KX from RP5 for node A & • 1x 1000BASE-KX from RP6 for node B loopback
Ethernet	• 2x RJ45 connectors from RP4 2x 1000BASE-T per node
Video	• 1x HDMI Type A from RP5 for node A • 1x HDMI Type A from RP6 for node B
USB	• 2x USB Type A from RP3 2x USB 3.2 Gen 1 + RP5 2x USB 2.0 for node A • 2x USB Type A from RP4 2x USB 3.2 Gen 1 + RP6 2x USB 2.0 for node B • 1x 10-pin header from RP5 2x USB2.0 for node A • 1x 10-pin header from RP6 2x USB2.0 for node B
Serial Port	• 1x DB9 from RP5 RS-232/422 for node A (COM1) • 1x DB9 from RP6 RS-232/422 for node B (COM1) • 1x 10-pin header from RP5 & RP6 RS-232/422 for node A & node B (COM2)

Table 2-2: VPX6200-RL1 RTM Specifications

Storage	• SATA 1x SATA connector from RP3 1x SATA 6Gb/s for node A 1x SATA connector from RP4 1x SATA 6Gb/s for node B 2x onboard SATA connectors from RP5 2x STAT 6Gb/s for node A 2x onboard SATA connectors from RP6 2x STAT 6Gb/s for node B • M.2 1x M.2 B key 2242 from RP3 1x PCIe x2 for node A 1x M.2 B key 2242 from RP4 1x PCIe x2 for node B
Environmental	• Operating Temp. -40°C to +85°C • Storage Temp. -55°C to +105°C • Relative Humidity: 95% non-condensing • Shock: 40g, 11ms • Vibration Random: 12Grms, 5Hz to 2000Hz Sinusoidal: 5g, 20Hz to 2000Hz Altitude: 40,000 ft. (operating)
EMC	• CE, FCC, Class A
Miscellaneous	• GA Switch 1x 3-poles switch for GA16-19 switch • IPMC F/W Update Firmware updateable via JTAG pin header • Debug Port 1x 3-pin header for NVMRO 1x JTAG pin header for PCIe switch 1x 4-poles switch + 1x 5-pin header for IPMB • Reset Button On board reset button • Battery
Board-to-Board Connector (VPX-6200 RTM L2 board)	• Inter-connect with VPX-6200-RL1 via connector link to VPX-6200-RL2 1x 1000BASE-T from RP5 for node A 1x 1000BASE-T from RP6 for node B 8x GPIO to P3 for node A 8x GPIO to P4, P6 for node B

Table 2-2: VPX6200-RL1 RTM Specifications

Note: Specifications are subject to change without prior notice.

2.3 VPX6200-RL2 RTM Specifications

Ethernet	• 2x RJ45 (4 lanes MDI from BTB connector)
LED	• 16 LEDs (8 LEDs controlled by Node A EC, 8 LEDs controlled by Node B EC)
Power	• Power provided from VPX6200-RL1 as LED power source 3.3V
Environmental	• Operating Temp. -40°C to +85°C • Storage Temp. -55°C to +105°C • Relative Humidity: 95% non-condensing • Shock: 40g, 11ms • Vibration Random: 12Grms, 5Hz to 2000Hz Sinusoidal: 5g, 20Hz to 2000Hz Altitude: 40,000 ft. (operating)
EMC	• CE, FCC, Class A

Table 2-3: VPX6200-RL2 RTM Specifications

Note: Specifications are subject to change without prior notice.

2.4 Power Consumption

This section provides information on the power consumption of the VPX6200.

Test Configuration (Node A / Node B)	
Processor	Intel® Xeon® W-11865MRE @ 2.60GHz
Memory Channel 1	Micron DDR4 3200 16GB
Memory Channel 2	Micron DDR4 3200 16GB
Graphics	Intel® UHD Graphics
Power Supply	FSP FSP500-70AGB 500W

OS/Mode (cTDP 25W)	EIST Enabled	EIST Disabled
Windows 10 x64, Idle Mode	65.3 W	66.07 W
Windows 10 x64, Typical Mode	104.99 W	105.53 W
Windows 10 x64, Max. Mode	106.12 W	106.27 W
OS/Mode (cTDP 35W)	**EIST Enabled**	**EIST Disabled**
Windows 10 x64, Idle Mode	65.55 W	65.35 W
Windows 10 x64, Typical Mode	127.5 W	116.26 W
Windows 10 x64, Max. Mode	131.93 W	133.3 W
OS/Mode (cTDP 45W)	**EIST Enabled**	**EIST Disabled**
Windows 10 x64, Idle Mode	66.63 W	66.17 W
Windows 10 x64, Typical Mode	152.38 W	114.95 W
Windows 10 x64, Max. Mode	154.35 W	135.42 W

Table 2-4: VPX6200 Power Consumption

Notes:

- The system set to idle mode and stays idle for 10 minutes.
- Run BurnInTest™ that includes CPU, memory, video and 2D/3- graphics. Set all test items to 100% loading and run for 10 minutes.
- Run Intel® Thermal Analysis Tool that includes CPU, graphics and memory. Set all test items to 100% loading and run for 10 minutes.

3 Board Interfaces

3.1 VPX6200 Board Layout

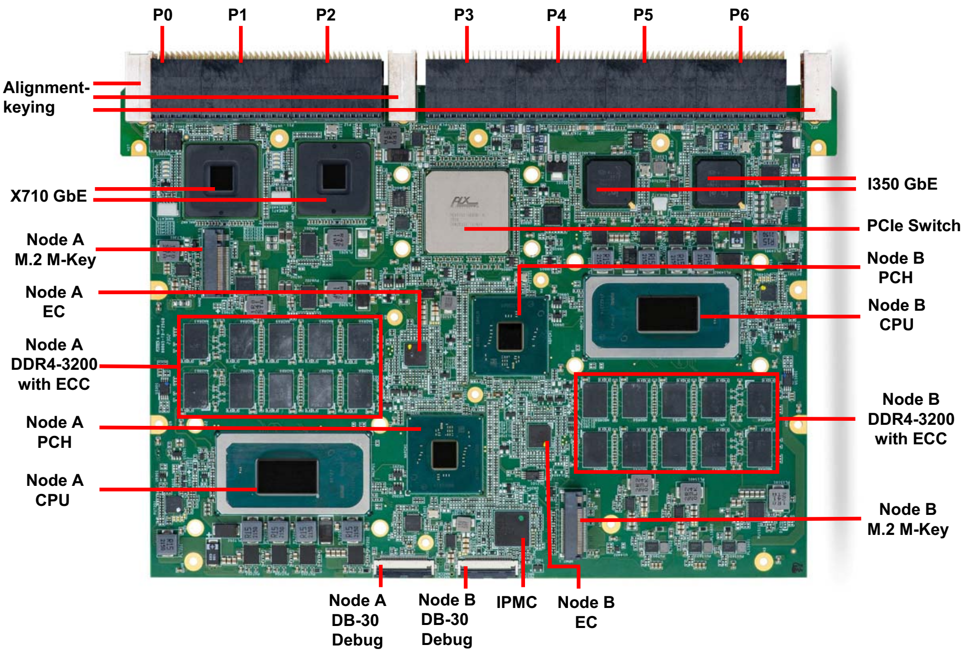


Figure 3-1: VPX6200 Board Layout - Top View

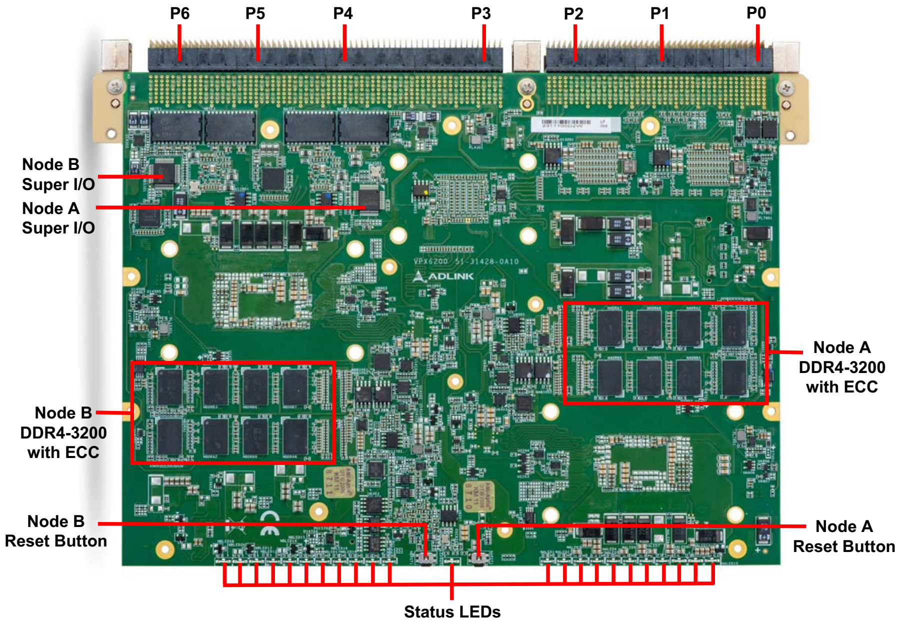


Figure 3-2: VPX6200 Board Layout - Bottom View

VPX6200 Status LEDs

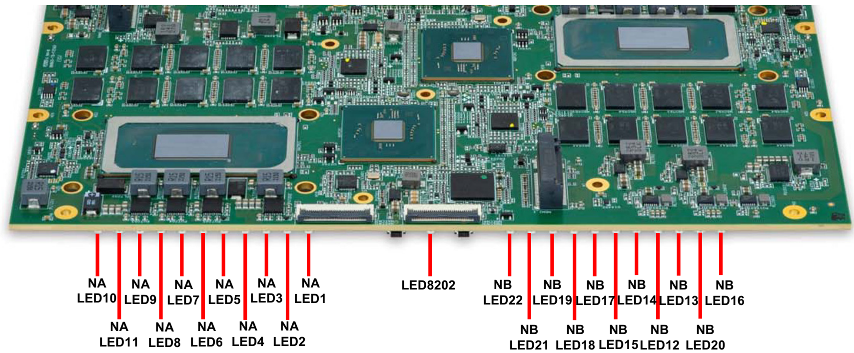


Figure 3-3: VPX6200 Status LEDs - Front Side

Location	Color	Description
NALED10	Green	Node A System On Status
NALED11	Yellow	Node A SATA ACT Status
NALED9	Red	Node A EC Status
NALED8	Yellow	Node A Port 80 bit7
NALED7	Yellow	Node A Port 80 bit6
NALED6	Yellow	Node A Port 80 bit5
NALED5	Yellow	Node A Port 80 bit4
NALED4	Yellow	Node A Port 80 bit3
NALED3	Yellow	Node A Port 80 bit2
NALED2	Yellow	Node A Port 80 bit1
NALED1	Yellow	Node A Port 80 bit0
LED8202	Red	IPMC WDT Status*
NBLED22	Yellow	Node B Port 80 bit0
NBLED21	Yellow	Node B Port 80 bit1
NBLED19	Yellow	Node B Port 80 bit2
NBLED18	Yellow	Node B Port 80 bit3
NBLED17	Yellow	Node B Port 80 bit4
NBLED15	Yellow	Node B Port 80 bit5

Table 3-1: VPX6200 Status LEDs - Front Side

Location	Color	Description
NBLED14	Yellow	Node B Port 80 bit6
NBLED12	Yellow	Node B Port 80 bit7
NBLED13	Red	Node B EC Status
NBLED20	Yellow	Node B SATA ACT Status
NBLED16	Green	Node B System On Status

Table 3-1: VPX6200 Status LEDs - Front Side

***IPMC WDT Status LED**

- LED on indicates a single board issue (either Node A or Node B has failed)
- LED blinking indicates a time-out issue in multiple board configuration
- GA17: either GA18 or GA19 is undetectable
- GA18: GA19 is undetectable
- GA19: N/A

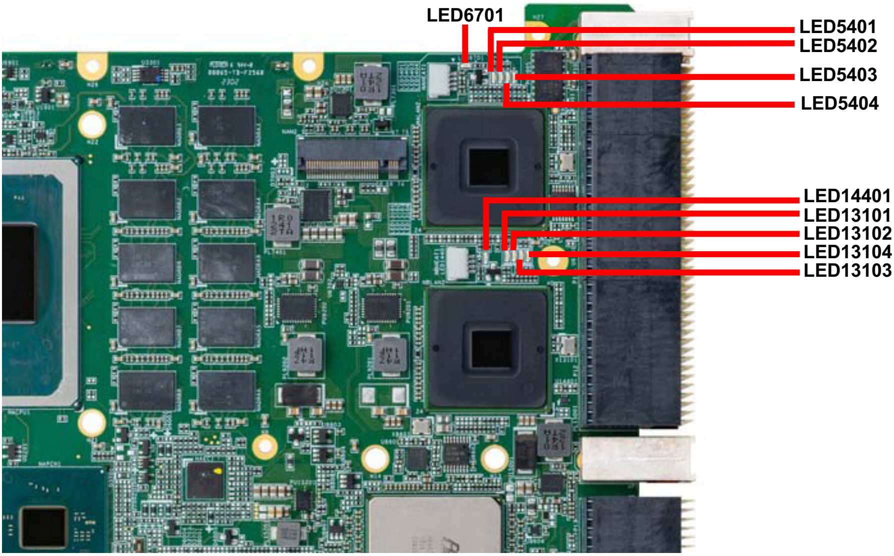


Figure 3-4: VPX6200 Status LEDs - Top Side

Location	Color	Description
LED6701	Red	Node A Heater status
LED5401	Green	Node A X710 10G Link Status
LED5402	Blue	Node A X710 Activity Status
LED5403	Green	Node A X710 10G Link Status
LED5404	Blue	Node A X710 Activity Status
LED14401	Red	Node B Heater status
LED1301	Green	Node B X710 10G Link Status
LED1302	Blue	Node B X710 Activity Status
LED1303	Green	Node B X710 10G Link Status
LED1304	Blue	Node B X710 Activity Status

Table 3-2: VPX6200 Status LEDs - Top Side

3.2 VPX6200 Front Panel LEDs

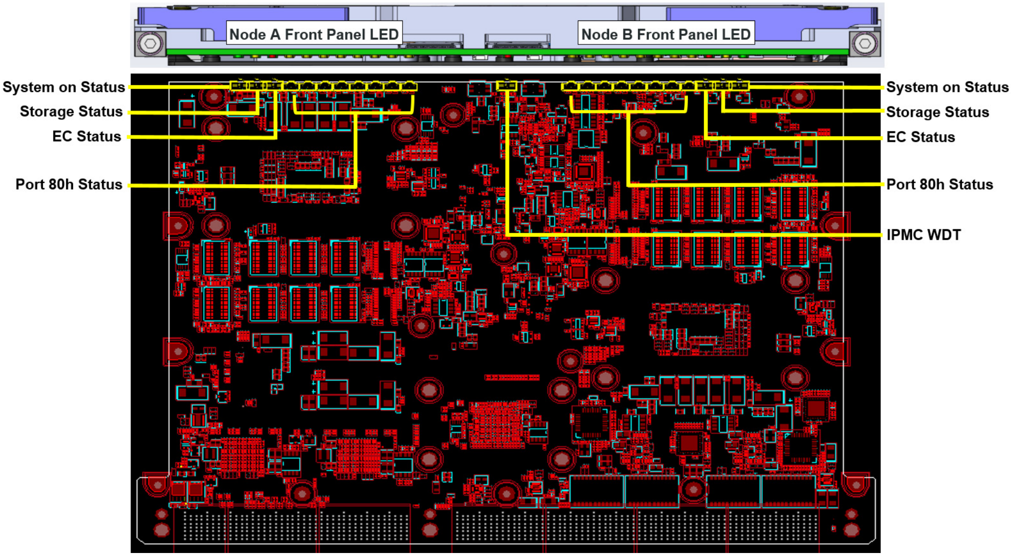


Figure 3-5: VPX6200 Front Panel LEDs - Front Side

VPX6200 System on Status LED

Figure 3-6: VPX6200 System on Status LED

Location	Color	Description
System on Status	Green	On/off when platform reset desserts/asserts.

Table 3-3: VPX6200 System on Status LED

VPX6200 Storage Status LED

Figure 3-7: VPX6200 Storage Status LED

Location	Color	Description
Storage Status	Yellow	Blinks when storage is active.

Table 3-4: VPX6200 Storage Status LED

VPX6200 EC Status LED

Figure 3-8: VPX6200 EC Status LED

Location	Color	Description
EC Status	Red	Error code follows ADLINK standard (see below).

Table 3-5: VPX6200 EC Status LED

EC Status LED Indication

Number of Blinks	Event	Description
0	NO_ERROR	No issues found.
2	NO_SUSCLK (not used)	Reserved (for BMC)
3	NO_SLP_S5	S5 to S0 mode, PCH PMC_SLP_S5_N didn't assertion.
4	NO_SLP_S4	S5 to S0 mode, PCH PMC_SLP_S4_N didn't assertion.

Table 3-6: EC Status LED Indication

5	NO_SLP_S3	S5 to S0 mode, PCH PMC_SLP_S3_N didn't assertion.
6	BIOS_FAIL	S0 mode, EC didn't reserve BIOS alive command and indicated BIOS fail. If select Failsafe BIOS, EC will switch to the second BIOS for 3rd boot when the module is booted for the two time in first BIOS without reserved BIOS alive command.
7	RESET_FAIL	S5 to S0 mode, PCH PMC_PLTRST_N didn't assertion.
8	RESETIN_FAIL	S0 mode, When press Reset button, EC will log System reset event.
9	NO_CB_PWROK	From S5 to S0 or S0 mode, didn't reserve carrier board CN_CB_PWROK signal.
10	CRITICAL_TEMP	When the CPU temperature is overheated, EC receives THERMTRIP_N event from CPU and EC shutdown system.
11	POWER_FAIL	S0 mode, EC monitor ADC and power good pin without response, then it means power fail. EC will do the power cycle.(Sx to G3 to S0)ADC pin -> P_+VCCIN_S0 , P_+3V3_A , P_+1V2_VDDQ , P_+3V3 , P_+VCC_RTC_EC , P_+12V_PSU , P_+5V_APower good pin -> PG_P_+3V3_A , PG_P_+VCCD_X710 , PG_P_+1V2_VDDQ , ALL_SYS_PWRGD , IMVP_VR_READY.
12	VOLTAGE_FAIL	When EC monitor ADC pin lower than -5%, it means voltage fail. EC will do the power cycle (Sx to G3 to S0)ADC pin -> P_+VCCIN_S0 , P_+3V3_A , P_+1V2_VDDQ , P_+3V3 , P_+VCC_RTC_EC , P_+12V_PSU , P_+5V_A
13	NO_RSMRST_PG	G3 to S5 mode, The last voltage (Before RSMRST) no work.
14	NO_VDDQ_PG	S5 to S0 mod, ?DDR4 power(P_+1V2_VDDQ)no work.
15	NO_V1P05A_PG	G3 to S5 mode, P_+1V05_A power no work.
16	NO_VCORE_PG	S5 to S0 mode, VCORE power(P_+VCCIN_S0) no work.

Table 3-6: EC Status LED Indication

17	NO_SYS_GD	S5 to S0 mode, No ALL_SYS_PWRGD which means one of P_+1V05_VCCIO_CPU, P_+1V05_VCCST, P_+1V05_S0 and PCH_RSMRST-L abnormal.
18	NO_V5SBY (not used)	Reserved (for BMC)
19	NO_V3P3A	G3 to S5 mode, P_+3V3_A power no work.
20	NO_V5_DUAL (not used)	Reserved (for BMC)
21	NO_PWRSRC_GD	When boot from G3 to S5 mode, Power supply support to ATX mode - 5VSB(P_+5V_STB) power lower than 4.3V, Power supply support to AT mode - 12V(P_+12V) power lower than 8V
22	NO_P_5V_3V3_S0 _PG (not used)	Reserved (for BMC)
23	NO_SAME_CHAN NEL	EC detected eSPI_EN#(CN_ESPI_EN-L) and PCH_ESPI_ID-L if not Mach then LED blink.eSPI_EN# --> High: LPC mode, Low: ESPI modePCH_ESPI_ID-L --> High: LPC mode, Low: ESPI mode
24	NO_PCH_PG	S5 to S0 mode, The last voltage (Before RSMRST) no work

Table 3-6: EC Status LED Indication

VPX6200 Port 80h Status LED

Figure 3-9: VPX6200 Port 80h Status LED

Location	Color	Description

Table 3-7: VPX6200 Port 80h Status LED

Port 80h Status	Yellow	Each node has 8 LEDs (Bit 0 to Bit 7) indicating its Port 80h status (see BIOS manual).

Table 3-7: VPX6200 Port 80h Status LED

VPX6200 IPMC WDT LED

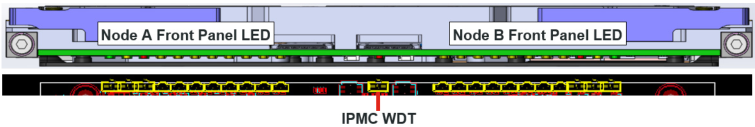


Figure 3-10: VPX6200 IPMC WDT LED

Location	Color	Description
IPMC WDT	Red	▶ Blinks when there is an internal/ external PCIe port connection issue. ▶ On when Node B boot-up exceeds 3 minutes. **Note:** PCIe port connection issues supersede Node B boot-up time.

Table 3-8: VPX6200 IPMC WDT LED

3.3 VPX6200-RL1 RTM Board Layout

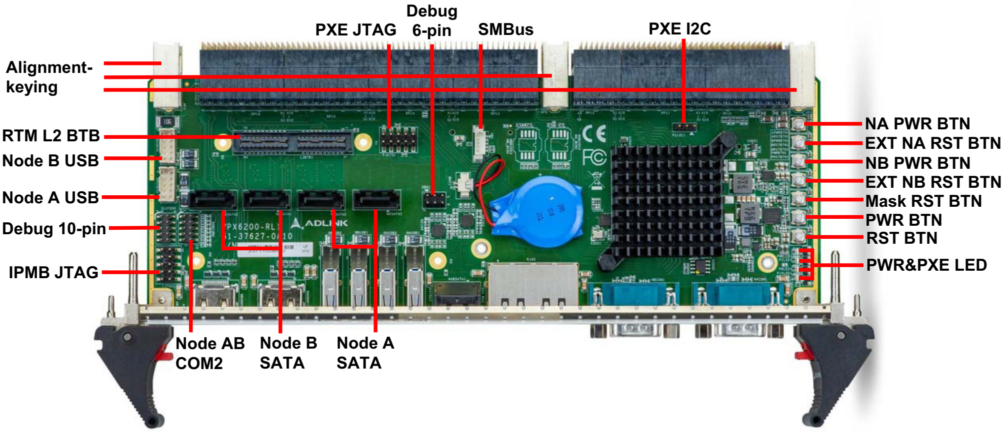


Figure 3-11: VPX6200-RL1 RTM Board Layout - Top View

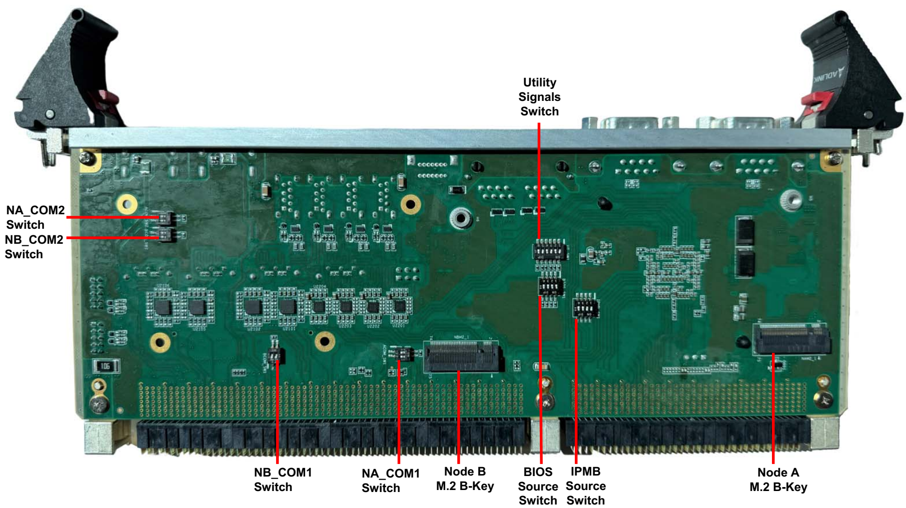


Figure 3-12: VPX6200-RL1 RTM Board Layout - Bottom View

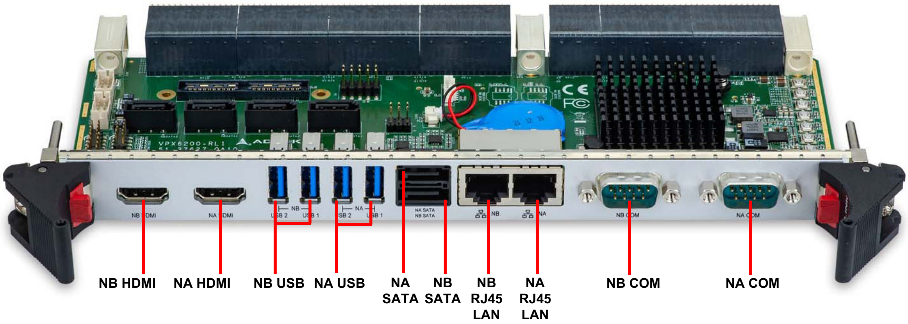


Figure 3-13: VPX6200-RL1 RTM Board Layout - Front View

VPX6200-RL1 Status LEDs

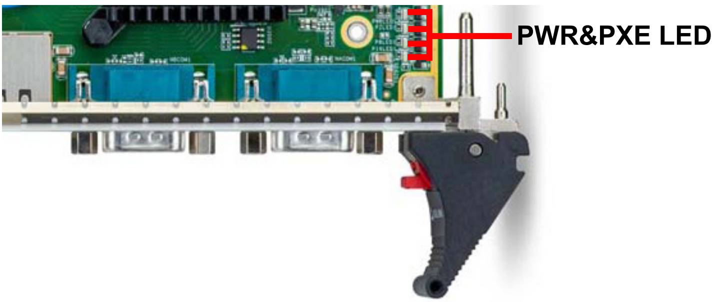


Figure 3-14: VPX6200-RL1 Status LEDs

Location	Color	Description
PWRLED1	Green	all RTM powers are ready
PZLED1	Green	RTM PCIe Switch Port 0 establish the link w/ SBC
P8LED1	Green	RTM PCIe Switch Port 8 establish the link w/ SBC
P16LED1	Green	RTM PCIe Switch Port 16 establish the link w/ SBC

Table 3-9: VPX6200-RL1 Status LEDs

3.4 VPX6200-RL1 RTM Board Layout

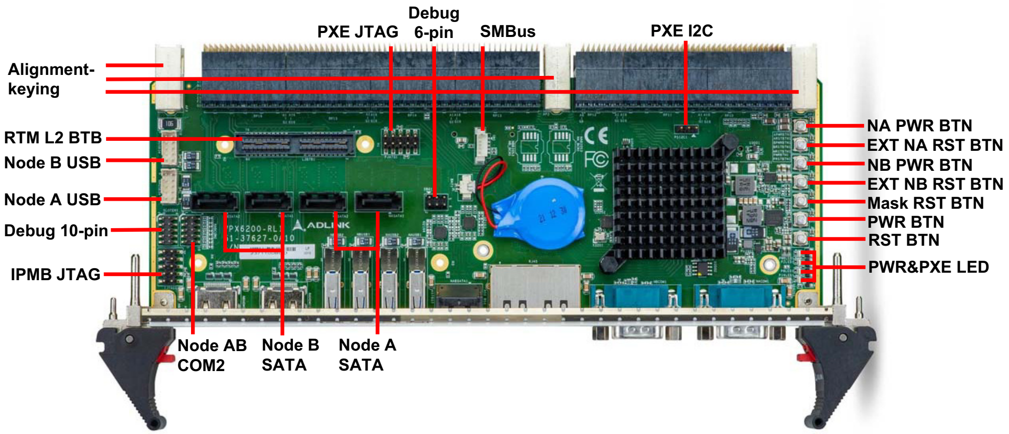


Figure 3-15: VPX6200-RL1 RTM Board Layout - Top View

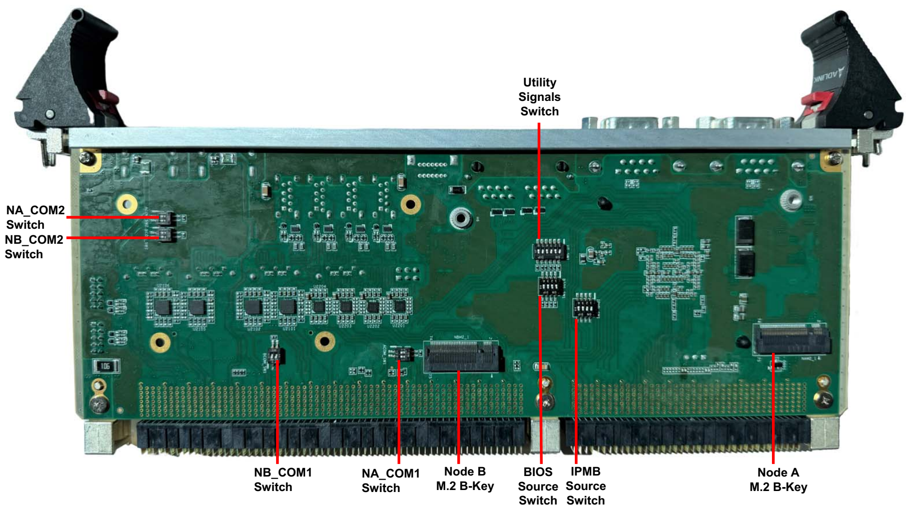


Figure 3-16: VPX6200-RL1 RTM Board Layout - Bottom View

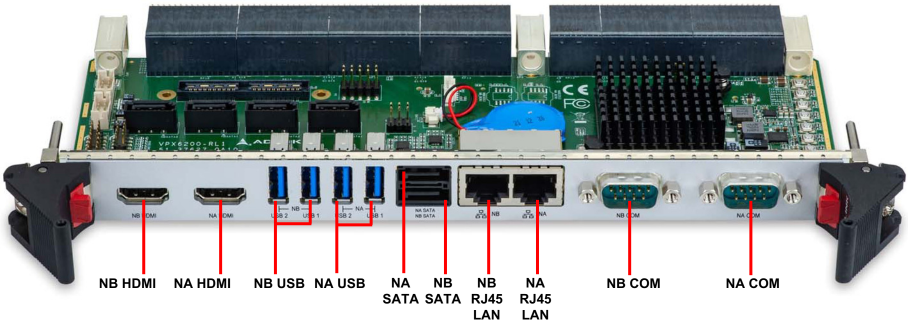


Figure 3-17: VPX6200-RL1 RTM Board Layout - Front View

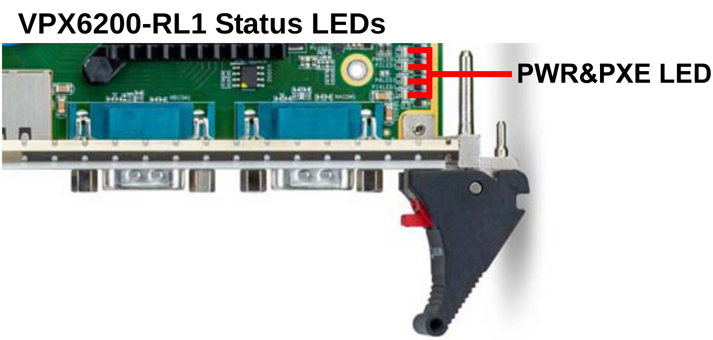


Figure 3-18: VPX6200-RL1 Status LEDs

Location	Color	Description
PWRLED1	Green	all RTM powers are ready
PZLED1	Green	RTM PCIe Switch Port 0 establish the link w/ SBC
P8LED1	Green	RTM PCIe Switch Port 8 establish the link w/ SBC
P16LED1	Green	RTM PCIe Switch Port 16 establish the link w/ SBC

Table 3-10: VPX6200-RL1 Status LEDs

3.5 VPX6200-RL2 RTM Board Layout

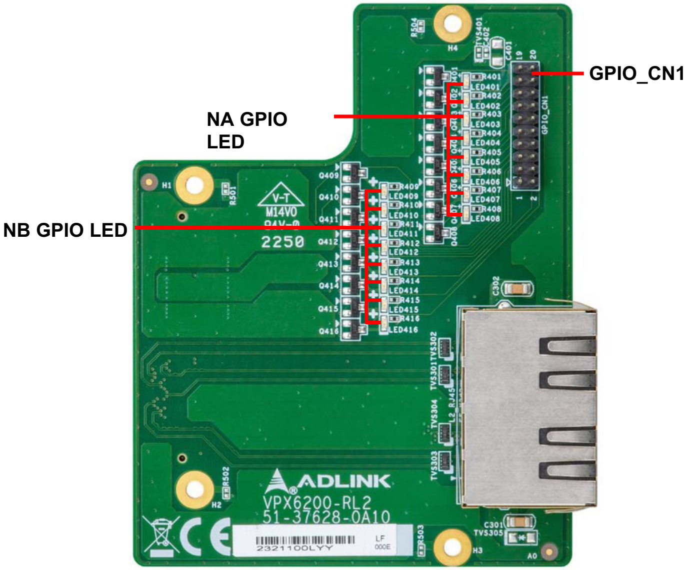


Figure 3-19: VPX6200-RL2 RTM Board Layout - Top View

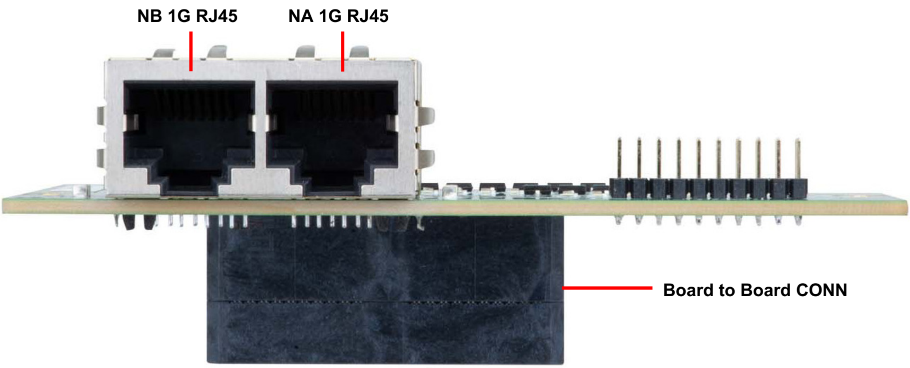


Figure 3-20: VPX6200-RL2 RTM Board Layout - Front View

VPX6200-RL2 Status LEDs

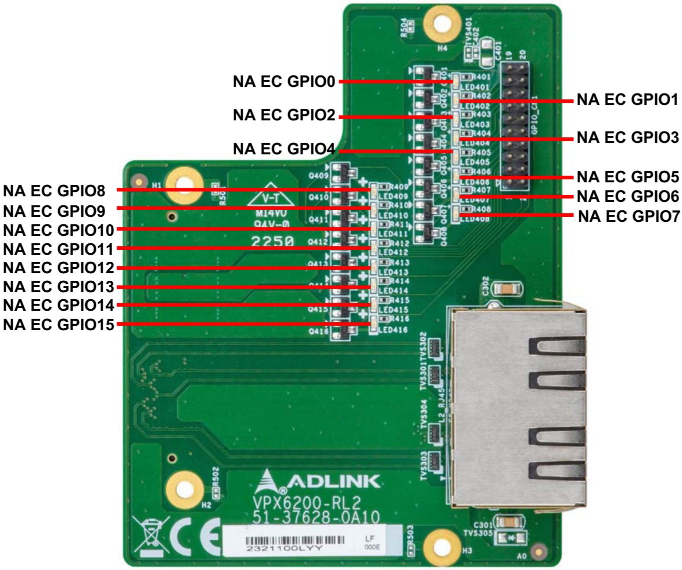


Figure 3-21: VPX6200-RL2 Status LEDs

Location	Color	Description
NA EC GPIO0	Green	Node A LED function when using VPX6200
NA EC GPIO1	Green	Node A LED function when using VPX6200
NA EC GPIO2	Green	Node A LED function when using VPX6200
NA EC GPIO3	Green	Node A LED function when using VPX6200
NA EC GPIO4	Green	Node A LED function when using VPX6200
NA EC GPIO5	Green	Node A LED function when using VPX6200
NA EC GPIO6	Green	Node A LED function when using VPX6200
NA EC GPIO7	Green	Node A LED function when using VPX6200
NB EC GPIO8	Yellow	Node B LED function when using VPX6200
NB EC GPIO9	Yellow	Node B LED function when using VPX6200
NB EC GPIO10	Yellow	Node B LED function when using VPX6200
NB EC GPIO11	Yellow	Node B LED function when using VPX6200
NB EC GPIO12	Yellow	Node B LED function when using VPX6200

Table 3-11: VPX6200-RL2 Status LEDs

Location	Color	Description
NB EC GPIO13	Yellow	Node B LED function when using VPX6200
NB EC GPIO14	Yellow	Node B LED function when using VPX6200
NB EC GPIO15	Yellow	Node B LED function when using VPX6200

Table 3-11: VPX6200-RL2 Status LEDs

3.6 VPX6200 Onboard Connector Pin Assignments

M.2 2242 M-Key Connector

(Node A: NAM2_1; Node B: NBM2_1)

Signal	Pin	Pin	Signal
GND	1	2	P_+3V3
GND	3	4	P_+3V3
PCH_PCIE20_RX_R_N	5	6	NC
PCH_PCIE20_RX_R_P	7	8	NC
GND	9	10	NC
PCH_PCIE20_TX_C_N	11	12	P_+3V3
PCH_PCIE20_TX_C_P	13	14	P_+3V3
GND	15	16	P_+3V3
PCH_PCIE19_RX_R_N	17	18	P_+3V3
PCH_PCIE19_RX_R_P	19	20	NC
GND	21	22	NC
PCH_PCIE19_TX_C_N	23	24	NC
PCH_PCIE19_TX_C_P	25	26	NC
GND	27	28	NC
PCH_PCIE18_RX_R_N	29	30	NC
PCH_PCIE18_RX_R_P	31	32	NC
GND	33	34	GND
PCH_PCIE18_TX_C_N	35	36	NC
PCH_PCIE18_TX_C_P	37	38	DEVSLP_M2_CON_R
GND	39	40	NC
PCH_PCIE17_SATA4_RX_R_P	41	42	NC
PCH_PCIE17_SATA4_RX_R_N	43	44	NC
GND	45	46	NC
PCH_PCIE17_SATA4_TX_C_N	47	48	NC

Signal	Pin	Pin	Signal
PCH_PCIE17_SATA4_TX_C_P	49	50	M2_RST-L
GND	51	52	CLK_REQ_M2_R-L
C_PCIECLK2_100M_N	53	54	NC
C_PCIECLK2_100M_P	55	56	NC
GND	57	58	NC
Key			
NC	67	68	NC
M2TYPE_PEDET	69	70	P3V3
GND	71	72	P3V3
GND	73	74	P3V3
GND	75	76	NA

DB30 Debug Connector

(Node A: NAECN1; Node B: NBAECN3)

Pin #	DB30 Signal Name	Pin #	DB30 Signal Name
1	EC_DB_UART_RX1	2	EC_DB_UART_TX1
3	EC_STATUS-L	4	CN_CB_PWROK
5	CN_RSTBTN-L	6	CN_PWRBTN-L
7	EC_SMB_CLK_A	8	EC_SMB_DAT_A
9	DB30_GND	10	P_+3V3_EC_A
11	EC_I2C4_CLK	12	EC_I2C4_DAT
13	F_BIOS_MODE	14	F_SEL_BIOS
15	DB30_GND	16	DB30_GND
17	P_+3V3_A	18	EC_WRST#_BTN
19	PCH_SLP_S5-L	20	PMC_SLP_S4-L
21	PMC_SLP_S3-L	22	POSTWDT_DIS-L
23	SPI_CS1-L	24	PCH_PLTRST-L_BUF
25	DB30_GND	26	DB30_SPI_CLK
27	DB30_SPI_DATAIN	28	DB30_SPI_DATAOUT

29	DB30_SPI_CS0-L	30	P_+3V3_SPI_A

3.7 VPX6200 VPX Connector Pin Assignments

P0 Connector Pin Assignment

	A	B	C	D	E	F	G
1	P_+12V_PSU_P0	P_+12V_PSU_P0	P_+12V_PSU_P0	No PAD	P_+12V_PSU_P0	P_+12V_PSU_P0	P_+12V_PSU_P0
2	P_+12V_PSU_P0	P_+12V_PSU_P0	P_+12V_PSU_P0	No PAD	P_+12V_PSU_P0	P_+12V_PSU_P0	P_+12V_PSU_P0
3	P_+5V_PSU_P0	P_+5V_PSU_P0	P_+5V_PSU_P0	No PAD	P_+5V_PSU_P0	P_+5V_PSU_P0	P_+5V_PSU_P0
4	NVMRO_EXT_IN	P0_RST-L	GND	NC	GND	IPMBB_DAT_P0	IPMBB_CLK_P0
5	IPMBA_DAT_P0	IPMBA_CLK_P0	GND	P3V3_AUX	GND	GA4	GAP
6	GA0	GA1	GND	NC	GND	GA2	GA3
7	PEX_TRST-L	PEX_TMS	GND	PEX_TDI	PEX_TDO	GND	PEX_TCK
8	GND	NC	NC	GND	NC	NC	GND

P0 Pinout Description

Signal	Pin	Description	I/O	PU/PD	Comment
P_+12V_PSU_P0	A1	Primary power supply input: +12V nominal. All available P_+12V_PSU_P0 pins on the connector(s) shall be used.	Power		
P_+12V_PSU_P0	A2	Primary power supply input: +12V nominal. All available P_+12V_PSU_P0 pins on the connector(s) shall be used.	Power		
P_+12V_PSU_P0	B1	Primary power supply input: +12V nominal. All available P_+12V_PSU_P0 pins on the connector(s) shall be used.	Power		
P_+12V_PSU_P0	B2	Primary power supply input: +12V nominal. All available P_+12V_PSU_P0 pins on the connector(s) shall be used.	Power		
P_+12V_PSU_P0	C1	Primary power supply input: +12V nominal. All available P_+12V_PSU_P0 pins on the connector(s) shall be used.	Power		

Signal	Pin	Description	I/O	PU/PD	Comment
P_+12V_PSU_P0	C2	Primary power supply input: +12V nominal. All available P_+12V_PSU_P0 pins on the connector(s) shall be used.	Power		
P_+12V_PSU_P0	E1	Primary power supply input: +12V nominal. All available P_+12V_PSU_P0 pins on the connector(s) shall be used.	Power		
P_+12V_PSU_P0	E2	Primary power supply input: +12V nominal. All available P_+12V_PSU_P0 pins on the connector(s) shall be used.	Power		
P_+12V_PSU_P0	F1	Primary power supply input: +12V nominal. All available P_+12V_PSU_P0 pins on the connector(s) shall be used.	Power		
P_+12V_PSU_P0	F2	Primary power supply input: +12V nominal. All available P_+12V_PSU_P0 pins on the connector(s) shall be used.	Power		
P_+12V_PSU_P0	G1	Primary power supply input: +12V nominal. All available P_+12V_PSU_P0 pins on the connector(s) shall be used.	Power		
P_+12V_PSU_P0	G2	Primary power supply input: +12V nominal. All available P_+12V_PSU_P0 pins on the connector(s) shall be used.	Power		
P_+5V_PSU_P0	A3	Primary power supply input: +5V nominal. All available P_+5V_PSU_P0 pins on the connector(s) shall be used.	Power		
P_+5V_PSU_P0	B3	Primary power supply input: +5V nominal. All available P_+5V_PSU_P0 pins on the connector(s) shall be used.	Power		
P_+5V_PSU_P0	C3	Primary power supply input: +5V nominal. All available P_+5V_PSU_P0 pins on the connector(s) shall be used.	Power		
P_+5V_PSU_P0	E3	Primary power supply input: +5V nominal. All available P_+5V_PSU_P0 pins on the connector(s) shall be used.	Power		
P_+5V_PSU_P0	F3	Primary power supply input: +5V nominal. All available P_+5V_PSU_P0 pins on the connector(s) shall be used.	Power		
P_+5V_PSU_P0	G3	Primary power supply input: +5V nominal. All available P_+5V_PSU_P0 pins on the connector(s) shall be used.	Power		

Signal	Pin	Description	I/O	PU/PD	Comment
P_+3V3_AUX	D5	Auxiliary power supply input: +3.3V Standby.	Power		
9FGL0251_DIFF1_100M_CLK_P_P0	E8	PCI Express Reference Positive Clock output for all PCI Express Lanes	O PCIE		Reserved for PCIe Switch Reference Clock output
9FGL0251_DIFF1_100M_CLK_N_P0	F8	PCI Express Reference Negative Clock output for all PCI Express Lanes	O PCIE		Reserved for PCIe Switch Reference Clock output
IPMBA_CLK_P0	B5	System Management Bus A clock. Connected to the BMM via I2C buffers. These allow access to certain onboard resources from an external I2C master	O 3.3VA	PU 2.2K to P_+3V3_AUX	
IPMBA_DAT_P0	A5	System Management Bus A data. Connected to the BMM via I2C buffers. These allow access to certain onboard resources from an external I2C master	O 3.3VA	PU 2.2K to P_+3V3_AUX	
IPMBB_CLK_P0	G4	System Management Bus B clock	O 3.3VA	PU 2.2K to P_+3V3_AUX	
IPMBB_DAT_P0	F4	System Management Bus B data	O 3.3VA	PU 2.2K to P_+3V3_AUX	
PEX_TCK	G7	PCIe Switch PEX8750 JTAG Test Clock Input	I 3.3VA		
PEX_TDI	D7	PCIe Switch PEX8750 JTAG Test Data Input	I 3.3VA		
PEX_TDO	E7	PCIe Switch PEX8750 JTAG Test Data Output	O 3.3VA		
PEX_TMS	B7	PCIe Switch PEX8750 JTAG Test Mode Select	I 3.3VA		
PEX_TRST-L	A7	PCIe Switch PEX8750 JTAG Test Reset	I 3.3VA		
P0_RST-L	B4	The VPX6200 generates SYSREST# when it is configured as System Controller	I/O 3.3VA	PU 220ohm to P_+3V3_AUX	
NVMRO_EXT_IN	A4	The state of this signal is shown in the Backplane Status of Non-Volatile Memory Read Only and write protection	I/O 3.3VA		1 = Backplane NVMRO signal is asserted 0 = Backplane NVMRO signal is negated
GA0	A6	The settings of the Pins allocated for system-wide geographical addressing input.	I 3.3VA	PU 4.7K to P_+3V3_AUX	
GA1	B6	The settings of the Pins allocated for system-wide geographical addressing input.	I 3.3VA	PU 4.7K to P_+3V3_AUX	

Signal	Pin	Description	I/O	PU/PD	Comment
GA2	F6	The settings of the Pins allocated for system-wide geographical addressing input.	I 3.3VA	PU 4.7K to P_+3V3_AUX	
GA3	G6	The settings of the Pins allocated for system-wide geographical addressing input.	I 3.3VA	PU 4.7K to P_+3V3_AUX	
GA4	F5	The settings of the Pins allocated for system-wide geographical addressing input.	I 3.3VA	PU 4.7K to P_+3V3_AUX	
GAP	G5	The settings of the Pins allocated for system-wide geographical addressing input.	I 3.3VA	PU 4.7K to P_+3V3_AUX	
GND	A8	Ground			
GND	C4	Ground			
GND	C5	Ground			
GND	C6	Ground			
GND	C7	Ground			
GND	D8	Ground			
GND	E4	Ground			
GND	E5	Ground			
GND	E6	Ground			
GND	F7	Ground			
GND	G8	Ground			
NC	B8	No connection			
NC	C8	No connection			
NC	D1	No connection			
NC	D2	No connection			
NC	D3	No connection			
NC	D4	No connection			
NC	D6	No connection			

P1 Connector Pin Assignment

	VPX6200 - P1 (Project 1 KX SKU by BOM option) *X710 FW sets to KX						
	A	B	C	D	E	F	G
1	NA_10G_RX0_L0_C_P	NA_10G_RX0_L0_C_N	GND	NA_10G_TX0_L0_P	NA_10G_TX0_L0_N	GND	GDiscrete1#
2	GND	NA_10G_RX0_L1_C_P	NA_10G_RX0_L1_C_N	GND	NA_10G_TX0_L1_P	NA_10G_TX0_L1_N	GND
3	NA_10G_RX0_L2_C_P	NA_10G_RX0_L2_C_N	GND	NA_10G_TX0_L2_R_	NA_10G_TX0_L2_R_	GND	P_+VBAT
4	GND	NA_10G_RX0_L3_C_P	NA_10G_RX0_L3_C_N	GND	NA_10G_TX0_L3_P	NA_10G_TX0_L3_N	GND
5	NB_10G_RX0_L0_C_P	NB_10G_RX0_L0_C_N	GND	NB_10G_TX0_L0_R_P	NB_10G_TX0_L0_R_N	GND	SYS_CON-L
6	GND	NB_10G_RX0_L1_C_P	NB_10G_RX0_L1_C_N	GND	NB_10G_TX0_L1_P	NB_10G_TX0_L1_N	GND
7	NB_10G_RX0_L2_C_P	NB_10G_RX0_L2_C_N	GND	NB_10G_TX0_L2_P	NB_10G_TX0_L2_N	GND	NC
8	GND	NB_10G_RX0_L3_C_P	NB_10G_RX0_L3_C_N	GND	NB_10G_TX0_L3_P	NB_10G_TX0_L3_N	GND
9	NA_10G_RX1_L0_C_P	NA_10G_RX1_L0_C_N	GND	NA_10G_TX1_L0_P	NA_10G_TX1_L0_N	GND	BP_PWRBTN-L
10	GND	NA_10G_RX1_L1_C_P	NA_10G_RX1_L1_C_N	GND	NA_10G_TX1_L1_P	NA_10G_TX1_L1_N	GND
11	NA_10G_RX1_L2_C_P	NA_10G_RX1_L2_C_N	GND	NA_10G_TX1_L2_P	NA_10G_TX1_L2_N	GND	S1_PWR_EN
12	GND	NA_10G_RX1_L3_C_P	NA_10G_RX1_L3_C_N	GND	NA_10G_TX1_L3_P	NA_10G_TX1_L3_N	GND
13	NB_10G_RX1_L0_C_P	NB_10G_RX1_L0_C_N	GND	NB_10G_TX1_L0_P	NB_10G_TX1_L0_N	GND	S1_PWR_OK
14	GND	NB_10G_RX1_L1_C_P	NB_10G_RX1_L1_C_N	GND	NB_10G_TX1_L1_P	NB_10G_TX1_L1_N	GND
15	NB_10G_RX1_L2_C_P	NB_10G_RX1_L2_C_N	GND	NB_10G_TX1_L2_P	NB_10G_TX1_L2_N	GND	MASK_RESET-
16	GND	NB_10G_RX1_L3_C_P	NB_10G_RX1_L3_C_N	GND	NB_10G_TX1_L3_P	NB_10G_TX1_L3_N	GND

	VPX6200 - P1 (Project 2 KR SKU by BOM option) *X710 FW sets to KR						
	A	B	C	D	E	F	G
1	NA_10G_RX0_L0_C_P	NA_10G_RX0_L0_C_N	GND	NA_10G_TX0_L0_P	NA_10G_TX0_L0_N	GND	GDiscrete1#
2	GND	NA_10G_RX0_L1_C_P	NA_10G_RX0_L1_C_N	GND	NA_10G_TX0_L1_P	NA_10G_TX0_L1_N	GND
3	NB_10G_RX0_L0_P	NB_10G_RX0_L0_N	GND	NB_10G_TX0_L0_P	NB_10G_TX0_L0_N	GND	P_+VBAT
4	GND	NA_10G_RX0_L3_C_P	NA_10G_RX0_L3_C_N	GND	NA_10G_TX0_L3_P	NA_10G_TX0_L3_N	GND
5	NC	NC	GND	NC	NC	GND	SYS_CON-L
6	GND	NB_10G_RX0_L1_C_P	NB_10G_RX0_L1_C_N	GND	NB_10G_TX0_L1_P	NB_10G_TX0_L1_N	GND
7	NB_10G_RX0_L2_C_P	NB_10G_RX0_L2_C_N	GND	NB_10G_TX0_L2_P	NB_10G_TX0_L2_N	GND	NC
8	GND	NB_10G_RX0_L3_C_P	NB_10G_RX0_L3_C_N	GND	NB_10G_TX0_L3_P	NB_10G_TX0_L3_N	GND
9	NA_10G_RX1_L0_C_P	NA_10G_RX1_L0_C_N	GND	NA_10G_TX1_L0_P	NA_10G_TX1_L0_N	GND	BP_PWRBTN-L
10	GND	NA_10G_RX1_L1_C_P	NA_10G_RX1_L1_C_N	GND	NA_10G_TX1_L1_P	NA_10G_TX1_L1_N	GND
11	NA_10G_RX1_L2_C_P	NA_10G_RX1_L2_C_N	GND	NA_10G_TX1_L2_P	NA_10G_TX1_L2_N	GND	S1_PWR_EN
12	GND	NA_10G_RX1_L3_C_P	NA_10G_RX1_L3_C_N	GND	NA_10G_TX1_L3_P	NA_10G_TX1_L3_N	GND
13	NB_10G_RX1_L0_C_P	NB_10G_RX1_L0_C_N	GND	NB_10G_TX1_L0_P	NB_10G_TX1_L0_N	GND	S1_PWR_OK
14	GND	NB_10G_RX1_L1_C_P	NB_10G_RX1_L1_C_N	GND	NB_10G_TX1_L1_P	NB_10G_TX1_L1_N	GND
15	NB_10G_RX1_L2_C_P	NB_10G_RX1_L2_C_N	GND	NB_10G_TX1_L2_P	NB_10G_TX1_L2_N	GND	MASK_RESET-
16	GND	NB_10G_RX1_L3_C_P	NB_10G_RX1_L3_C_N	GND	NB_10G_TX1_L3_P	NB_10G_TX1_L3_N	GND

P1 Pinout Description

Signal	Pin	Description	I/O	PU/PD	Comment
P_+VBAT	G3	Real-time clock circuit-power input. Nominally +3.0V	Power		
NB_10G_TX1_L3_P	E16	10GBASE-KX4 Ethernet channel 2 transmit positive differential pairs 3	O KX4		Data Plane, Node B
NB_10G_TX1_L3_N	F16	10GBASE-KX4 Ethernet channel 2 transmit negative differential pairs 3	O KX4		Data Plane, Node B
NB_10G_TX1_L2_P	D15	10GBASE-KX4 Ethernet channel 2 transmit positive differential pairs 2	O KX4		Data Plane, Node B

Signal	Pin	Description	I/O	PU/PD	Comment
NB_10G_TX1_L2_N	E15	10GBASE-KX4 Ethernet channel 2 transmit negative differential pairs 2	O KX4		Data Plane, Node B
NB_10G_TX1_L1_P	E14	10GBASE-KX4 Ethernet channel 2 transmit positive differential pairs 1	O KX4		Data Plane, Node B
NB_10G_TX1_L1_N	F14	10GBASE-KX4 Ethernet channel 2 transmit negative differential pairs 1	O KX4		Data Plane, Node B
NB_10G_TX1_L0_P	D13	10GBASE-KX4 Ethernet channel 2 transmit positive differential pairs 0	O KX4		Data Plane, Node B
NB_10G_TX1_L0_N	E13	10GBASE-KX4 Ethernet channel 2 transmit negative differential pairs 0	O KX4		Data Plane, Node B
NB_10G_TX0_L3_P	E8	10GBASE-KX4 Ethernet channel 1 transmit positive differential pairs 3	O KX4		Data Plane, Node B
NB_10G_TX0_L3_N	F8	10GBASE-KX4 Ethernet channel 1 transmit negative differential pairs 3	O KX4		Data Plane, Node B
NB_10G_TX0_L2_P	D7	10GBASE-KX4 Ethernet channel 1 transmit positive differential pairs 2	O KX4		Data Plane, Node B
NB_10G_TX0_L2_N	E7	10GBASE-KX4 Ethernet channel 1 transmit negative differential pairs 2	O KX4		Data Plane, Node B
NB_10G_TX0_L1_P	E6	10GBASE-KX4 Ethernet channel 1 transmit positive differential pairs 1	O KX4		Data Plane, Node B
NB_10G_TX0_L1_N	F6	10GBASE-KX4 Ethernet channel 1 transmit negative differential pairs 1	O KX4		Data Plane, Node B
NB_10G_TX0_L0_R_P	D5	10GBASE-KX4 Ethernet channel 1 transmit positive differential pairs 0	O KX4/ KR		Data Plane, Node B, co-lay for KR SKU
NB_10G_TX0_L0_R_N	E5	10GBASE-KX4 Ethernet channel 1 transmit negative differential pairs 0	O KX4/ KR		Data Plane, Node B, co-lay for KR SKU
NB_10G_RX1_L3_C_P	B16	10GBASE-KX4 Ethernet channel 2 receive positive differential pairs 3	I KX4		Data Plane, Node B, AC coupled 10nF on VPX6200
NB_10G_RX1_L3_C_N	C16	10GBASE-KX4 Ethernet channel 2 receive negative differential pairs 3	I KX4		Data Plane, Node B, AC coupled 10nF on VPX6200
NB_10G_RX1_L2_C_P	A15	10GBASE-KX4 Ethernet channel 2 receive positive differential pairs 2	I KX4		Data Plane, Node B, AC coupled 10nF on VPX6200

Signal	Pin	Description	I/O	PU/PD	Comment
NB_10G_RX1_L2_C_N	B15	10GBASE-KX4 Ethernet channel 2 receive negative differential pairs 2	I KX4		Data Plane, Node B, AC coupled 10nF on VPX6200
NB_10G_RX1_L1_C_P	B14	10GBASE-KX4 Ethernet channel 2 receive positive differential pairs 1	I KX4		Data Plane, Node B, AC coupled 10nF on VPX6200
NB_10G_RX1_L1_C_N	C14	10GBASE-KX4 Ethernet channel 2 receive negative differential pairs 1	I KX4		Data Plane, Node B, AC coupled 10nF on VPX6200
NB_10G_RX1_L0_C_P	A13	10GBASE-KX4 Ethernet channel 2 receive positive differential pairs 0	I KX4		Data Plane, Node B, AC coupled 10nF on VPX6200
NB_10G_RX1_L0_C_N	B13	10GBASE-KX4 Ethernet channel 2 receive negative differential pairs 0	I KX4		Data Plane, Node B, AC coupled 10nF on VPX6200
NB_10G_RX0_L3_C_P	B8	10GBASE-KX4 Ethernet channel 1 receive positive differential pairs 3	I KX4		Data Plane, Node B, AC coupled 10nF on VPX6200
NB_10G_RX0_L3_C_N	C8	10GBASE-KX4 Ethernet channel 1 receive negative differential pairs 3	I KX4		Data Plane, Node B, AC coupled 10nF on VPX6200
NB_10G_RX0_L2_C_P	A7	10GBASE-KX4 Ethernet channel 1 receive positive differential pairs 2	I KX4		Data Plane, Node B, AC coupled 10nF on VPX6200
NB_10G_RX0_L2_C_N	B7	10GBASE-KX4 Ethernet channel 1 receive negative differential pairs 2	I KX4		Data Plane, Node B, AC coupled 10nF on VPX6200
NB_10G_RX0_L1_C_P	B6	10GBASE-KX4 Ethernet channel 1 receive positive differential pairs 1	I KX4		Data Plane, Node B, AC coupled 10nF on VPX6200
NB_10G_RX0_L1_C_N	C6	10GBASE-KX4 Ethernet channel 1 receive negative differential pairs 1	I KX4		Data Plane, Node B, AC coupled 10nF on VPX6200
NB_10G_RX0_L0_C_P	A5	10GBASE-KX4 Ethernet channel 1 receive positive differential pairs 0	I KX4/KR		Data Plane, Node B, AC coupled 10nF on VPX6200, co-lay for KR SKU
NB_10G_RX0_L0_C_N	B5	10GBASE-KX4 Ethernet channel 1 receive negative differential pairs 0	I KX4/KR		Data Plane, Node B, AC coupled 10nF on VPX6200, co-lay for KR SKU
NA_10G_TX1_L3_P	E12	10GBASE-KX4 Ethernet channel 2 transmit positive differential pairs 3	O KX4		Data Plane, Node A
NA_10G_TX1_L3_N	F12	10GBASE-KX4 Ethernet channel 2 transmit negative differential pairs 3	O KX4		Data Plane, Node A

Signal	Pin	Description	I/O	PU/PD	Comment
NA_10G_TX1_L2_P	D11	10GBASE-KX4 Ethernet channel 2 transmit positive differential pairs 2	O KX4		Data Plane, Node A
NA_10G_TX1_L2_N	E11	10GBASE-KX4 Ethernet channel 2 transmit negative differential pairs 2	O KX4		Data Plane, Node A
NA_10G_TX1_L1_P	E10	10GBASE-KX4 Ethernet channel 2 transmit positive differential pairs 1	O KX4		Data Plane, Node A
NA_10G_TX1_L1_N	F10	10GBASE-KX4 Ethernet channel 2 transmit negative differential pairs 1	O KX4		Data Plane, Node A
NA_10G_TX1_L0_P	D9	10GBASE-KX4 Ethernet channel 2 transmit positive differential pairs 0	O KX4		Data Plane, Node A
NA_10G_TX1_L0_N	E9	10GBASE-KX4 Ethernet channel 2 transmit negative differential pairs 0	O KX4		Data Plane, Node A
NA_10G_TX0_L3_P	E4	10GBASE-KX4 Ethernet channel 1 transmit positive differential pairs 3	O KX4		Data Plane, Node A
NA_10G_TX0_L3_N	F4	10GBASE-KX4 Ethernet channel 1 transmit negative differential pairs 3	O KX4		Data Plane, Node A
NA_10G_TX0_L2_R_P	D3	10GBASE-KX4 Ethernet channel 1 transmit positive differential pairs 2	O KX4/ KR		Data Plane, Node A, co-lay for KR SKU
NA_10G_TX0_L2_R_N	E3	10GBASE-KX4 Ethernet channel 1 transmit negative differential pairs 2	O KX4/ KR		Data Plane, Node A, co-lay for KR SKU
NA_10G_TX0_L1_P	E2	10GBASE-KX4 Ethernet channel 1 transmit positive differential pairs 1	O KX4		Data Plane, Node A
NA_10G_TX0_L1_N	F2	10GBASE-KX4 Ethernet channel 1 transmit negative differential pairs 1	O KX4		Data Plane, Node A
NA_10G_TX0_L0_P	D1	10GBASE-KX4 Ethernet channel 1 transmit positive differential pairs 0	O KX4		Data Plane, Node A
NA_10G_TX0_L0_N	E1	10GBASE-KX4 Ethernet channel 1 transmit negative differential pairs 0	O KX4		Data Plane, Node A
NA_10G_RX1_L3_C_P	B12	10GBASE-KX4 Ethernet channel 2 receive positive differential pairs 3	I KX4		Data Plane, Node A, AC coupled 10nF on VPX6200
NA_10G_RX1_L3_C_N	C12	10GBASE-KX4 Ethernet channel 2 receive negative differential pairs 3	I KX4		Data Plane, Node A, AC coupled 10nF on VPX6200

Signal	Pin	Description	I/O	PU/PD	Comment
NA_10G_RX1_L2_C_P	A11	10GBASE-KX4 Ethernet channel 2 receive positive differential pairs 2	I KX4		Data Plane, Node A, AC coupled 10nF on VPX6200
NA_10G_RX1_L2_C_N	B11	10GBASE-KX4 Ethernet channel 2 receive negative differential pairs 2	I KX4		Data Plane, Node A, AC coupled 10nF on VPX6200
NA_10G_RX1_L1_C_P	B10	10GBASE-KX4 Ethernet channel 2 receive positive differential pairs 1	I KX4		Data Plane, Node A, AC coupled 10nF on VPX6200
NA_10G_RX1_L1_C_N	C10	10GBASE-KX4 Ethernet channel 2 receive negative differential pairs 1	I KX4		Data Plane, Node A, AC coupled 10nF on VPX6200
NA_10G_RX1_L0_C_P	A9	10GBASE-KX4 Ethernet channel 2 receive positive differential pairs 0	I KX4		Data Plane, Node A, AC coupled 10nF on VPX6200
NA_10G_RX1_L0_C_N	B9	10GBASE-KX4 Ethernet channel 2 receive negative differential pairs 0	I KX4		Data Plane, Node A, AC coupled 10nF on VPX6200
NA_10G_RX0_L3_C_P	B4	10GBASE-KX4 Ethernet channel 1 receive positive differential pairs 3	I KX4		Data Plane, Node A, AC coupled 10nF on VPX6200
NA_10G_RX0_L3_C_N	C4	10GBASE-KX4 Ethernet channel 1 receive negative differential pairs 3	I KX4		Data Plane, Node A, AC coupled 10nF on VPX6200
NA_10G_RX0_L2_C_P	A3	10GBASE-KX4 Ethernet channel 1 receive positive differential pairs 2	I KX4/ KR		Data Plane, Node A, AC coupled 10nF on VPX6200, co-lay for KR SKU
NA_10G_RX0_L2_C_N	B3	10GBASE-KX4 Ethernet channel 1 receive negative differential pairs 2	I KX4/ KR		Data Plane, Node A, AC coupled 10nF on VPX6200, co-lay for KR SKU
NA_10G_RX0_L1_C_P	B2	10GBASE-KX4 Ethernet channel 1 receive positive differential pairs 1	I KX4		Data Plane, Node A, AC coupled 10nF on VPX6200
NA_10G_RX0_L1_C_N	C2	10GBASE-KX4 Ethernet channel 1 receive negative differential pairs 1	I KX4		Data Plane, Node A, AC coupled 10nF on VPX6200
NA_10G_RX0_L0_C_P	A1	10GBASE-KX4 Ethernet channel 1 receive positive differential pairs 0	I KX4		Data Plane, Node A, AC coupled 10nF on VPX6200
NA_10G_RX0_L0_C_N	B1	10GBASE-KX4 Ethernet channel 1 receive negative differential pairs 0	I KX4		Data Plane, Node A, AC coupled 10nF on VPX6200
S1_PWR_OK	G13	Slot 1 Power good signals	O 3.3VA		Node A and NodeB system power good indication from IPMC
S1_PWR_EN	G11	Slot 1 Power enable signals	I 3.3VA	PU 4.7K to P_+3V3_AUX	Base on slot numbering to receive enable signal.(Slot number = 17)

Signal	Pin	Description	I/O	PU/PD	Comment
SYS_CON-L	G5	System Controller indication	I 3.3VA	PU 10K to P_+3V3_AUX	1 = VPX6200 is installed into a System Controller slot (SYSCON backplane pin is low) 0 = VPX6200 is not installed into a system controller slot (SYSCON backplane pin not pulled low)
GDISCRETE1#_R	G1	Optional single ended general purpose I/O signal	I/O 3.3VA	PU 4.7K to P_+3V3_AUX	
BP_PWRBTN-L	G9	Additional Node A and Mode B Power Button Control at the same time	I 3.3VA	PU 4.7K to P_+3V3_AUX	Power button event from backplane
MASK_RESET_R-L	G15	Maskable Reset. Pulling this input low for a hard reset to the VPX6200. This pin can also be driven by the VPX6200 via the IPMC	I 3.3VA	PU 4.7K to P_+3V3_AUX	
GND	A2	Ground			
GND	A4	Ground			
GND	A6	Ground			
GND	A8	Ground			
GND	A10	Ground			
GND	A12	Ground			
GND	A14	Ground			
GND	A16	Ground			
GND	C1	Ground			
GND	C3	Ground			
GND	C5	Ground			
GND	C7	Ground			
GND	C9	Ground			
GND	C11	Ground			
GND	C13	Ground			
GND	C15	Ground			
GND	D2	Ground			
GND	D4	Ground			
GND	D6	Ground			
GND	D8	Ground			
GND	D10	Ground			
GND	D12	Ground			

Signal	Pin	Description	I/O	PU/PD	Comment
GND	D14	Ground			
GND	D16	Ground			
GND	F1	Ground			
GND	F3	Ground			
GND	F5	Ground			
GND	F7	Ground			
GND	F9	Ground			
GND	F11	Ground			
GND	F13	Ground			
GND	F15	Ground			
GND	G2	Ground			
GND	G4	Ground			
GND	G6	Ground			
GND	G8	Ground			
GND	G10	Ground			
GND	G12	Ground			
GND	G14	Ground			
GND	G16	Ground			
NC	G7	No connection			

P2 Connector Pin Assignment

	A	B	C	D	E	F	G
1	PCIE_SW_Port4_RXP16_P2	PCIE_SW_Port4_RXN16_P2	GND	PCIE_SW_Port4_TXP16_P2	PCIE_SW_Port4_TXN16_P2	GND	S2_PWR_EN
2	GND	PCIE_SW_Port4_RXP17_P2	PCIE_SW_Port4_RXN17_P2	GND	PCIE_SW_Port4_TXP17_P2	PCIE_SW_Port4_TXN17_P2	GND
3	PCIE_SW_Port4_RXP18_P2	PCIE_SW_Port4_RXN18_P2	GND	PCIE_SW_Port4_TXP18_P2	PCIE_SW_Port4_TXN18_P2	GND	S2_PWR_OK
4	GND	PCIE_SW_Port4_RXP19_P2	PCIE_SW_Port4_RXN19_P2	GND	PCIE_SW_Port4_TXP19_P2	PCIE_SW_Port4_TXN19_P2	GND
5	PCIE_SW_Port4_RXP20_P2	PCIE_SW_Port4_RXN20_P2	GND	PCIE_SW_Port4_TXP20_P2	PCIE_SW_Port4_TXN20_P2	GND	PEX_I2C_SCL0_P2
6	GND	PCIE_SW_Port4_RXP21_P2	PCIE_SW_Port4_RXN21_P2	GND	PCIE_SW_Port4_TXP21_P2	PCIE_SW_Port4_TXN21_P2	GND
7	PCIE_SW_Port4_RXP22_P2	PCIE_SW_Port4_RXN22_P2	GND	PCIE_SW_Port4_TXP22_P2	PCIE_SW_Port4_TXN22_P2	GND	PEX_I2C_SDA0_P2
8	GND	PCIE_SW_Port4_RXP23_P2	PCIE_SW_Port4_RXN23_P2	GND	PCIE_SW_Port4_TXP23_P2	PCIE_SW_Port4_TXN23_P2	GND
9	PCIE_SW_Port5_RXP24_P2	PCIE_SW_Port5_RXN24_P2	GND	PCIE_SW_Port5_TXP24_P2	PCIE_SW_Port5_TXN24_P2	GND	IPMI_DEB_RX
10	GND	PCIE_SW_Port5_RXP25_P2	PCIE_SW_Port5_RXN25_P2	GND	PCIE_SW_Port5_TXP25_P2	PCIE_SW_Port5_TXN25_P2	GND
11	PCIE_SW_Port5_RXP26_P2	PCIE_SW_Port5_RXN26_P2	GND	PCIE_SW_Port5_TXP26_P2	PCIE_SW_Port5_TXN26_P2	GND	IPMI_DEB_TX
12	GND	PCIE_SW_Port5_RXP27_P2	PCIE_SW_Port5_RXN27_P2	GND	PCIE_SW_Port5_TXP27_P2	PCIE_SW_Port5_TXN27_P2	GND
13	PCIE_SW_Port1_RXP8_P2	PCIE_SW_Port1_RXN8_P2	GND	PCIE_SW_Port1_TXP8_P2	PCIE_SW_Port1_TXN8_P2	GND	S3_PWR_EN
14	GND	PCIE_SW_Port1_RXP9_P2	PCIE_SW_Port1_RXN9_P2	GND	PCIE_SW_Port1_TXP9_P2	PCIE_SW_Port1_TXN9_P2	GND
15	PCIE_SW_Port1_RXP10_P2	PCIE_SW_Port1_RXN10_P2	GND	PCIE_SW_Port1_TXP10_P2	PCIE_SW_Port1_TXN10_P2	GND	S3_PWR_OK
16	GND	PCIE_SW_Port1_RXP11_P2	PCIE_SW_Port1_RXN11_P2	GND	PCIE_SW_Port1_TXP11_P2	PCIE_SW_Port1_TXN11_P2	GND

P2 Pinout Description

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_SW_PORT1_RXP8_P2	A13	PLX8750 PCI Express port1 channel 8, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT1_RXN8_P2	B13	PLX8750 PCI Express port1 channel 8, Receive Input negative differential pair	I PCIE		

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_SW_PORT1_RXP9_P2	B14	PLX8750 PCI Express port1 channel 9, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT1_RXN9_P2	C14	PLX8750 PCI Express port1 channel 9, Receive Input negative differential pair	I PCIE		
PCIE_SW_PORT1_RXP10_P2	A15	PLX8750 PCI Express port1 channel 10, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT1_RXN10_P2	B15	PLX8750 PCI Express port1 channel 10, Receive Input negative differential pair	I PCIE		
PCIE_SW_PORT1_RXP11_P2	B16	PLX8750 PCI Express port1 channel 11, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT1_RXN11_P2	C16	PLX8750 PCI Express port1 channel 11, Receive Input negative differential pair	I PCIE		
PCIE_SW_PORT1_TXP8_P2	D13	PLX8750 PCI Express port1 channel 8, Transmit Output positive differential pair	O PCIE		
PCIE_SW_PORT1_TXN8_P2	E13	PLX8750 PCI Express port1 channel 8, Transmit Output negative differential pair	O PCIE		
PCIE_SW_PORT1_TXP9_P2	E14	PLX8750 PCI Express port1 channel 9, Transmit Output positive differential pair	O PCIE		
PCIE_SW_PORT1_TXN9_P2	F14	PLX8750 PCI Express port1 channel 9, Transmit Output negative differential pair	O PCIE		
PCIE_SW_PORT1_TXP10_P2	D15	PLX8750 PCI Express port1 channel 10, Transmit Output positive differential pair	O PCIE		
PCIE_SW_PORT1_TXN10_P2	E15	PLX8750 PCI Express port1 channel 10, Transmit Output negative differential pair	O PCIE		
PCIE_SW_PORT1_TXP11_P2	E16	PLX8750 PCI Express port1 channel 11, Transmit Output positive differential pair	O PCIE		
PCIE_SW_PORT1_TXN11_P2	F16	PLX8750 PCI Express port1 channel 11, Transmit Output negative differential pair	O PCIE		
PCIE_SW_PORT4_RXP16_P2	A1	PLX8750 PCI Express port4 channel 16, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT4_RXN16_P2	B1	PLX8750 PCI Express port4 channel 16, Receive Input negative differential pair	I PCIE		

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_SW_PORT4_ RXP17_P2	B2	PLX8750 PCI Express port4 channel 17, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT4_ RXN17_P2	C2	PLX8750 PCI Express port4 channel 17, Receive Input negative differential pair	I PCIE		
PCIE_SW_PORT4_ RXP18_P2	A3	PLX8750 PCI Express port4 channel 18, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT4_ RXN18_P2	B3	PLX8750 PCI Express port4 channel 18, Receive Input negative differential pair	I PCIE		
PCIE_SW_PORT4_ RXP19_P2	B4	PLX8750 PCI Express port4 channel 19, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT4_ RXN19_P2	C4	PLX8750 PCI Express port4 channel 19, Receive Input negative differential pair	I PCIE		
PCIE_SW_PORT4_ RXP20_P2	A5	PLX8750 PCI Express port4 channel 20, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT4_ RXN20_P2	B5	PLX8750 PCI Express port4 channel 20, Receive Input negative differential pair	I PCIE		
PCIE_SW_PORT4_ RXP21_P2	B6	PLX8750 PCI Express port4 channel 21, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT4_ RXN21_P2	C6	PLX8750 PCI Express port4 channel 21, Receive Input negative differential pair	I PCIE		
PCIE_SW_PORT4_ RXP22_P2	A7	PLX8750 PCI Express port4 channel 22, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT4_ RXN22_P2	B7	PLX8750 PCI Express port4 channel 22, Receive Input negative differential pair	I PCIE		
PCIE_SW_PORT4_ RXP23_P2	B8	PLX8750 PCI Express port4 channel 23, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT4_ RXN23_P2	C8	PLX8750 PCI Express port4 channel 23, Receive Input negative differential pair	I PCIE		
PCIE_SW_PORT4_ TXP16_P2	D1	PLX8750 PCI Express port4 channel 16, Transmit Output positive differential pair	O PCIE		
PCIE_SW_PORT4_ TXN16_P2	E1	PLX8750 PCI Express port4 channel 16, Transmit Output negative differential pair	O PCIE		

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_SW_PORT4_TXP17_P2	E2	PLX8750 PCI Express port4 channel 17, Transmit Output positive differential pair	O PCIE		
PCIE_SW_PORT4_TXN17_P2	F2	PLX8750 PCI Express port4 channel 17, Transmit Output negative differential pair	O PCIE		
PCIE_SW_PORT4_TXP18_P2	D3	PLX8750 PCI Express port4 channel 18, Transmit Output positive differential pair	O PCIE		
PCIE_SW_PORT4_TXN18_P2	E3	PLX8750 PCI Express port4 channel 18, Transmit Output negative differential pair	O PCIE		
PCIE_SW_PORT4_TXP19_P2	E4	PLX8750 PCI Express port4 channel 19, Transmit Output positive differential pair	O PCIE		
PCIE_SW_PORT4_TXN19_P2	F4	PLX8750 PCI Express port4 channel 19, Transmit Output negative differential pair	O PCIE		
PCIE_SW_PORT4_TXP20_P2	D5	PLX8750 PCI Express port4 channel 20, Transmit Output positive differential pair	O PCIE		
PCIE_SW_PORT4_TXN20_P2	E5	PLX8750 PCI Express port4 channel 20, Transmit Output negative differential pair	O PCIE		
PCIE_SW_PORT4_TXP21_P2	E6	PLX8750 PCI Express port4 channel 21, Transmit Output positive differential pair	O PCIE		
PCIE_SW_PORT4_TXN21_P2	F6	PLX8750 PCI Express port4 channel 21, Transmit Output negative differential pair	O PCIE		
PCIE_SW_PORT4_TXP22_P2	D7	PLX8750 PCI Express port4 channel 22, Transmit Output positive differential pair	O PCIE		
PCIE_SW_PORT4_TXN22_P2	E7	PLX8750 PCI Express port4 channel 22, Transmit Output negative differential pair	O PCIE		
PCIE_SW_PORT4_TXP23_P2	E8	PLX8750 PCI Express port4 channel 23, Transmit Output positive differential pair	O PCIE		
PCIE_SW_PORT4_TXN23_P2	F8	PLX8750 PCI Express port4 channel 23, Transmit Output negative differential pair	O PCIE		
PCIE_SW_PORT5_RXP24_P2	A9	PLX8750 PCI Express port5 channel 24, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT5_RXN24_P2	B9	PLX8750 PCI Express port5 channel 24, Receive Input negative differential pair	I PCIE		

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_SW_PORT5_RXP25_P2	B10	PLX8750 PCI Express port5 channel 25, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT5_RXN25_P2	C10	PLX8750 PCI Express port5 channel 25, Receive Input negative differential pair	I PCIE		
PCIE_SW_PORT5_RXP26_P2	A11	PLX8750 PCI Express port5 channel 26, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT5_RXN26_P2	B11	PLX8750 PCI Express port5 channel 26, Receive Input negative differential pair	I PCIE		
PCIE_SW_PORT5_RXP27_P2	B12	PLX8750 PCI Express port5 channel 27, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT5_RXN27_P2	C12	PLX8750 PCI Express port5 channel 27, Receive Input negative differential pair	I PCIE		
PCIE_SW_PORT5_TXP24_P2	D9	PLX8750 PCI Express port5 channel 24, Transmit Output positive differential pair	O PCIE		AC coupled 220nF on VPX6200
PCIE_SW_PORT5_TXN24_P2	E9	PLX8750 PCI Express port5 channel 24, Transmit Output negative differential pair	O PCIE		AC coupled 220nF on VPX6200
PCIE_SW_PORT5_TXP25_P2	E10	PLX8750 PCI Express port5 channel 25, Transmit Output positive differential pair	O PCIE		AC coupled 220nF on VPX6200
PCIE_SW_PORT5_TXN25_P2	F10	PLX8750 PCI Express port5 channel 25, Transmit Output negative differential pair	O PCIE		AC coupled 220nF on VPX6200
PCIE_SW_PORT5_TXP26_P2	D11	PLX8750 PCI Express port5 channel 26, Transmit Output positive differential pair	O PCIE		AC coupled 220nF on VPX6200
PCIE_SW_PORT5_TXN26_P2	E11	PLX8750 PCI Express port5 channel 26, Transmit Output negative differential pair	O PCIE		AC coupled 220nF on VPX6200
PCIE_SW_PORT5_TXP27_P2	E12	PLX8750 PCI Express port5 channel 27, Transmit Output positive differential pair	O PCIE		AC coupled 220nF on VPX6200
PCIE_SW_PORT5_TXN27_P2	F12	PLX8750 PCI Express port5 channel 27, Transmit Output negative differential pair	O PCIE		AC coupled 220nF on VPX6200
PEX_I2C_SCL0_P2	G5	General purpose I²C port clock output/input of PLX8750	I/O OD 3.3VA	PU 1.4K to P_+3V3_AUX	Source PLX8750
PEX_I2C_SDA0_P2	G7	General purpose I²C port data I/O line of PLX8750	I/O OD 3.3VA	PU 1.4K to P_+3V3_AUX	Source PLX8750

Signal	Pin	Description	I/O	PU/PD	Comment
IPMI_DEB_RX	G9	Serial COM port 0 Receive Data signal for IPMC debugging	I CMOS		Source IPMC UART
IPMI_DEB_TX	G11	Serial COM port 0 Transmit Data signal for IPMC debugging	O CMOS		Source IPMC UART
S2_PWR_EN	G1	Slot 2 Power enable signals	I 3.3VA	PU 4.7K to P_+3V3_AUX	Input Pin: Slot 2 Power enable signals. Base on slot numbering to receive enable signal.(Slot number = 18)
S2_PWR_OK	G3	Slot 2 Power good signals	O 3.3VA		Node A and Node B system power good indication from IPMC
S3_PWR_EN	G13	Slot 3 Power enable signals	I 3.3VA	PU 4.7K to P_+3V3_AUX	Input Pin: Slot 3 Power enable signals. Base on slot numbering to receive enable signal.(Slot number = 19)
S3_PWR_OK	G15	Slot 3 Power good signals	O 3.3VA		Node A and Node B system power good indication from IPMC
GND	A2	Ground			
GND	A4	Ground			
GND	A6	Ground			
GND	A8	Ground			
GND	A10	Ground			
GND	A12	Ground			
GND	A14	Ground			
GND	A16	Ground			
GND	C1	Ground			
GND	C3	Ground			
GND	C5	Ground			
GND	C7	Ground			
GND	C9	Ground			
GND	C11	Ground			
GND	C13	Ground			
GND	C15	Ground			
GND	D2	Ground			
GND	D4	Ground			
GND	D6	Ground			
GND	D8	Ground			
GND	D10	Ground			

Signal	Pin	Description	I/O	PU/PD	Comment
GND	D12	Ground			
GND	D14	Ground			
GND	D16	Ground			
GND	F1	Ground			
GND	F3	Ground			
GND	F5	Ground			
GND	F7	Ground			
GND	F9	Ground			
GND	F11	Ground			
GND	F13	Ground			
GND	F15	Ground			
GND	G2	Ground			
GND	G4	Ground			
GND	G6	Ground			
GND	G8	Ground			
GND	G10	Ground			
GND	G12	Ground			
GND	G14	Ground			
GND	G16	Ground			

P3 Connector Pin Assignment

	VPX6200 - P3 (Project 1 KX SKU by BOM option)						
	A	B	C	D	E	F	G
1	NA_PCH_PCIE13_RX_P	NA_PCH_PCIE13_RX_N	GND	NA_PCH_PCIE13_C_TX_P	NA_PCH_PCIE13_C_TX_N	GND	NA_EC_GPIO3
2	GND	NA_PCH_PCIE14_RX_P	NA_PCH_PCIE14_RX_N	GND	NA_PCH_PCIE14_C_TX_P	NA_PCH_PCIE14_C_TX_N	GND
3	NA_USB3_1_RXP	NA_USB3_1_RXN	GND	NA_USB3_1_TXP	NA_USB3_1_TXN	GND	NA_EC_GPIO1
4	GND	NA_PCIE_CLK_100M_P	NA_PCIE_CLK_100M_N	GND	NA_RTM_BOOT#	NA_EXT_NODE_RST-L	GND
5	NA_SPI_MISO	NA_SPI_CS2-L	GND	NA_SPI_MOSI	NA_SPI_CLK	GND	NA_EC_GPIO2
6	GND	PCIE_SW_Port5_RXP28_P3	PCIE_SW_Port5_RXN28_P3	GND	PCIE_SW_Port5_TXP28_P3	PCIE_SW_Port5_TXN28_P3	GND
7	NC	NC	GND	NC	NC	GND	NC
8	GND	NC	NC	GND	NC	NA_PLTRST-L	GND
9	NA_USB3_2_RXP	NA_USB3_2_RXN	GND	NA_USB3_2_TXP	NA_USB3_2_TXN	GND	NA_EC_GPIO4
10	GND	NA_SATA_3_C_RXP	NA_SATA_3_C_RXN	GND	NA_SATA_3_C_TXP	NA_SATA_3_C_TXN	GND
11	PCIE_SW_Port5_RXP29_P3	PCIE_SW_Port5_RXN29_P3	GND	PCIE_SW_Port5_TXP30_P3	PCIE_SW_Port5_TXN30_P3	GND	NA_EC_GPIO5
12	GND	NA_EC_GPIO0	NC	GND	PCIE_SW_Port5_RXP30_P3	PCIE_SW_Port5_RXN30_P3	GND
13	PCIE_SW_Port5_RXP31_P3	PCIE_SW_Port5_RXN31_P3	GND	PCIE_SW_Port5_TXP31_P3	PCIE_SW_Port5_TXN31_P3	GND	NA_EC_GPIO6
14	GND	NA_BIOS_SEL1-L	NB_BIOS_SEL1-L	GND	PCIE_SW_Port1_TXP12_P3	PCIE_SW_Port1_TXN12_P3	GND
15	NC	NC	GND	PCIE_SW_Port1_RXP12_P3	PCIE_SW_Port1_RXN12_P3	GND	NA_EC_GPIO7
16	GND	P_+12V_PSU_P0	P_+12V_PSU_P0	GND	P_+5V_PSU_P0	P_+5V_PSU_P0	GND

	VPX6200 - P3 (Project 2 KR SKU by BOM option)						
	A	B	C	D	E	F	G
1	NA_PCH_PCIE13_RX_P	NA_PCH_PCIE13_RX_N	GND	NA_PCH_PCIE13_C_TX_P	NA_PCH_PCIE13_C_TX_N	GND	NA_EC_GPIO3
2	GND	NA_PCH_PCIE14_RX_P	NA_PCH_PCIE14_RX_N	GND	NA_PCH_PCIE14_C_TX_P	NA_PCH_PCIE14_C_TX_N	GND
3	NA_USB3_1_RXP	NA_USB3_1_RXN	GND	NA_USB3_1_TXP	NA_USB3_1_TXN	GND	NA_EC_GPIO1
4	GND	NA_PCIE_CLK_100M_P	NA_PCIE_CLK_100M_N	GND	NA_RTM_BOOT#	NA_EXT_NODE_RST-L	GND
5	NA_SPI_MISO	NA_SPI_CS2-L	GND	NA_SPI_MOSI	NA_SPI_CLK	GND	NA_EC_GPIO2
6	GND	PCIE_SW_Port5_RXP28_P3	PCIE_SW_Port5_RXN28_P3	GND	PCIE_SW_Port5_TXP28_P3	PCIE_SW_Port5_TXN28_P3	GND
7	NC	NC	GND	NC	NC	GND	NA_PLTRST-L
8	GND	NC	NC	GND	PCIE_SW_Port5_TXP29_P3	PCIE_SW_Port5_TXN29_P3	GND
9	NA_USB3_2_RXP	NA_USB3_2_RXN	GND	NA_USB3_2_TXP	NA_USB3_2_TXN	GND	NA_EC_GPIO4
10	GND	NA_SATA_3_C_RXP	NA_SATA_3_C_RXN	GND	NA_SATA_3_C_TXP	NA_SATA_3_C_TXN	GND
11	PCIE_SW_Port5_RXP29_P3	PCIE_SW_Port5_RXN29_P3	GND	PCIE_SW_Port5_TXP30_P3	PCIE_SW_Port5_TXN30_P3	GND	NA_EC_GPIO5
12	GND	NA_EC_GPIO0	NC	GND	PCIE_SW_Port5_RXP30_P3	PCIE_SW_Port5_RXN30_P3	GND
13	PCIE_SW_Port5_RXP31_P3	PCIE_SW_Port5_RXN31_P3	GND	PCIE_SW_Port5_TXP31_P3	PCIE_SW_Port5_TXN31_P3	GND	NA_EC_GPIO6

P3 Pinout Description

Signal	Pin	Description	I/O	PU/PD	Comment
P_+12V_PSU_P0	B16	Primary power supply input: +12V nominal. All available P_+12V_PSU_P0 pins on the connector(s) shall be used.	Power		
P_+12V_PSU_P0	C16	Primary power supply input: +12V nominal. All available P_+12V_PSU_P0 pins on the connector(s) shall be used.	Power		
P_+5V_PSU_P0	E16	Primary power supply input: +5V nominal. All available P_+5V_PSU_P0 pins on the connector(s) shall be used.	Power		
P_+5V_PSU_P0	F16	Primary power supply input: +5V nominal. All available P_+5V_PSU_P0 pins on the connector(s) shall be used.	Power		
PCIE_SW_PORT1_RXP12_P3	D15	PLX8750 PCI Express port1 channel 12, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT1_RXN12_P3	E15	PLX8750 PCI Express port1 channel 12, Receive Input negative differential pair	I PCIE		
PCIE_SW_PORT1_TXP12_P3	E14	PLX8750 PCI Express port1 channel 12, Transmit Output positive differential pair	O PCIE		AC coupled 220nF on VPX6200
PCIE_SW_PORT1_TXN12_P3	F14	PLX8750 PCI Express port1 channel 12, Transmit Output negative differential pair	O PCIE		AC coupled 220nF on VPX6200
PCIE_SW_PORT5_RXP28_P3	B6	PLX8750 PCI Express port5 channel 28, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT5_RXN28_P3	C6	PLX8750 PCI Express port5 channel 28, Receive Input negative differential pair	I PCIE		
PCIE_SW_PORT5_RXP29_P3	A11	PLX8750 PCI Express port5 channel 29, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT5_RXN29_P3	B11	PLX8750 PCI Express port5 channel 29, Receive Input negative differential pair	I PCIE		
PCIE_SW_PORT5_RXP30_P3	E12	PLX8750 PCI Express port5 channel 30, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT5_RXN30_P3	F12	PLX8750 PCI Express port5 channel 30, Receive Input negative differential pair	I PCIE		

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_SW_PORT5_RXP31_P3	A13	PLX8750 PCI Express port5 channel 31, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT5_RXN31_P3	B13	PLX8750 PCI Express port5 channel 31, Receive Input negative differential pair	I PCIE		
PCIE_SW_PORT5_TXP28_P3	E6	PLX8750 PCI Express port5 channel 28, Transmit Output positive differential pair	O PCIE		AC coupled 220nF on VPX6200
PCIE_SW_PORT5_TXN28_P3	F6	PLX8750 PCI Express port5 channel 28, Transmit Output negative differential pair	O PCIE		AC coupled 220nF on VPX6200
PCIE_SW_P5_R_TXP29	E8	PLX8750 PCI Express port5 channel 29, Transmit Output positive differential pair	O PCIE		AC coupled 220nF on VPX6200, KX4 no used, KR is P5 lane 29
PCIE_SW_P5_R_TXN29	F8	PLX8750 PCI Express port5 channel 29, Transmit Output negative differential pair	O PCIE		AC coupled 220nF on VPX6200, KX4 is NA_PLTRST-L, KR is P5 lane 29
PCIE_SW_PORT5_TXP30_P3	D11	PLX8750 PCI Express port5 channel 30, Transmit Output positive differential pair	O PCIE		AC coupled 220nF on VPX6200
PCIE_SW_PORT5_TXN30_P3	E11	PLX8750 PCI Express port5 channel 30, Transmit Output negative differential pair	O PCIE		AC coupled 220nF on VPX6200
PCIE_SW_PORT5_TXP31_P3	D13	PLX8750 PCI Express port5 channel 31, Transmit Output positive differential pair	O PCIE		AC coupled 220nF on VPX6200
PCIE_SW_PORT5_TXN31_P3	E13	PLX8750 PCI Express port5 channel 31, Transmit Output negative differential pair	O PCIE		AC coupled 220nF on VPX6200
NA_PCH_PCIE13_RX_P	A1	PCH PCI Express port13 channel 13, Receive Input positive differential pair	I PCIE		Node A
NA_PCH_PCIE13_RX_N	B1	PCH PCI Express port13 channel 13, Receive Input negative differential pair	I PCIE		Node A
NA_PCH_PCIE14_RX_P	B2	PCH PCI Express port13 channel 14, Receive Input positive differential pair	I PCIE		Node A
NA_PCH_PCIE14_RX_N	C2	PCH PCI Express port13 channel 14, Receive Input negative differential pair	I PCIE		Node A
NA_PCH_PCIE13_C_TX_P	D1	PCH PCI Express port13 channel 13, Transmit Output positive differential pair	O PCIE		Node A, AC coupled 220nF on VPX6200
NA_PCH_PCIE13_C_TX_N	E1	PCH PCI Express port13 channel 13, Transmit Output negative differential pair	O PCIE		Node A, AC coupled 220nF on VPX6200

Signal	Pin	Description	I/O	PU/PD	Comment
NA_PCH_PCIE14_C_TX_P	E2	PCH PCI Express port13 channel 14, Transmit Output positive differential pair	O PCIE		Node A, AC coupled 220nF on VPX6200
NA_PCH_PCIE14_C_TX_N	F2	PCH PCI Express port13 channel 14, Transmit Output negative differential pair	O PCIE		Node A, AC coupled 220nF on VPX6200
NA_PCIE_CLK_100M_P	B4	PCI Express Reference Positive Clock output for all PCI Express Lanes	O PCIE		Source Node A
NA_PCIE_CLK_100M_N	C4	PCI Express Reference Negative Clock output for all PCI Express Lanes	O PCIE		Source Node A
NA_SATA_3_C_RXP	B10	Serial ATA channel 3, Receive Input positive differential pair	I SATA		Node A, AC coupled 10nF on VPX6200
NA_SATA_3_C_RXN	C10	Serial ATA channel 3, Receive Input negative differential pair	I SATA		Node A, AC coupled 10nF on VPX6200
NA_SATA_3_C_TXP	E10	Serial ATA channel 3, Transmit Output positive differential pair	O SATA		Node A, AC coupled 10nF on VPX6200
NA_SATA_3_C_TXN	F10	Serial ATA channel 3, Transmit Output negative differential pair	O SATA		Node A, AC coupled 10nF on VPX6200
NA_USB3_1_RXP	A3	USB 3.2 Gen 1 Differential Receive channel 1, Receive Input positive differential pair	I USB		Node A, USB 1.1/ 2.0 / 3.2 Gen1 compliant
NA_USB3_1_RXN	B3	USB 3.2 Gen 1 Differential Receive channel 1, Receive Input negative differential pair	I USB		Node A, USB 1.1/ 2.0 / 3.2 Gen1 compliant
NA_USB3_1_TXP	D3	USB 3.2 Gen 1 Differential Receive channel 1, Transmit Output positive differential pair	O USB		Node A, USB 1.1/ 2.0 / 3.2 Gen1 compliant
NA_USB3_1_TXN	E3	USB 3.2 Gen 1 Differential Receive channel 1, Transmit Output negative differential pair	O USB		Node A, USB 1.1/ 2.0 / 3.2 Gen1 compliant
NA_USB3_2_RXP	A9	USB 3.2 Gen 1 Differential Receive channel 2, Receive Input positive differential pair	I USB		Node A, USB 1.1/ 2.0 / 3.2 Gen1 compliant
NA_USB3_2_RXN	B9	USB 3.2 Gen 1 Differential Receive channel 2, Receive Input negative differential pair	I USB		Node A, USB 1.1/ 2.0 / 3.2 Gen1 compliant
NA_USB3_2_TXP	D9	USB 3.2 Gen 1 Differential Receive channel 2, Transmit Output positive differential pair	O USB		Node A, USB 1.1/ 2.0 / 3.2 Gen1 compliant
NA_USB3_2_TXN	E9	USB 3.2 Gen 1 Differential Receive channel 2, Transmit Output negative differential pair	O USB		Node A, USB 1.1/ 2.0 / 3.2 Gen1 compliant
NA_SPI_CLK	E5	Clock from module to carrier board SPI BIOS flash	O 3.3VA		Source Node A
NA_SPI_CS2-L	B5	Chip select for Carrier Board SPI BIOS Flash	O 3.3VA		Source Node A

Signal	Pin	Description	I/O	PU/PD	Comment
NA_SPI_MISO	A5	Data in to module from carrier board SPI BIOS flash	I 3.3VA	PU 10k to P_+3V3_SPI_A	Source Node A
NA_SPI_MOSI	D5	Data out from module to carrier board SPI BIOS flash	O 3.3VA		Source Node A
NA_BIOS_SEL1-L	B14	Reserved for Node A BIOS selection from RTM	I 3.3VA	PU 10k to P_+3V3_EC_A	Node A
NB_BIOS_SEL1-L	C14	Reserved for Node B BIOS selection from RTM	I 3.3VA	PU 10k to NB_P_+3V3_EC_A	Node A, For KR SKU, KX4 SKU is not used
NA_PLTRST_R-L	G7	Node A PCH Platform Reset	O 3.3VA		Node B
NA_RTM_BOOT#	E4	Reserved for boot from RTM BIOS	I 3.3VA	PU 100k to P_+3V3_EC_A	Node A
NA_EXT_NODE_RST-L	F4	Receive Node A Extreanl Reset Button status	I 3.3VA	PU 10k to P_+3V3_AUX	Node A
NA_EC_GPIO0	B12	General Purpose Input/Output signal 0	I/O 3.3VA		Source Node A EC
NA_EC_GPIO1	G3	General Purpose Input/Output signal 1	I/O 3.3VA		Source Node A EC
NA_EC_GPIO2	G5	General Purpose Input/Output signal 2	I/O 3.3VA		Source Node A EC
NA_EC_GPIO3	G1	General Purpose Input/Output signal 3	I/O 3.3VA		Source Node A EC
NA_EC_GPIO4	G9	General Purpose Input/Output signal 4	I/O 3.3VA		Source Node A EC
NA_EC_GPIO5	G11	General Purpose Input/Output signal 5	I/O 3.3VA		Source Node A EC
NA_EC_GPIO6	G13	General Purpose Input/Output signal 6	I/O 3.3VA		Source Node A EC
NA_EC_GPIO7	G15	General Purpose Input/Output signal 7	I/O 3.3VA		Source Node A EC
GND	A2	Ground			
GND	A4	Ground			
GND	A6	Ground			
GND	A8	Ground			
GND	A10	Ground			
GND	A12	Ground			
GND	A14	Ground			
GND	A16	Ground			
GND	C1	Ground			
GND	C3	Ground			

Signal	Pin	Description	I/O	PU/PD	Comment
GND	C5	Ground			
GND	C7	Ground			
GND	C9	Ground			
GND	C11	Ground			
GND	C13	Ground			
GND	C15	Ground			
GND	D2	Ground			
GND	D4	Ground			
GND	D6	Ground			
GND	D8	Ground			
GND	D10	Ground			
GND	D12	Ground			
GND	D14	Ground			
GND	D16	Ground			
GND	F1	Ground			
GND	F3	Ground			
GND	F5	Ground			
GND	F7	Ground			
GND	F9	Ground			
GND	F11	Ground			
GND	F13	Ground			
GND	F115	Ground			
GND	G2	Ground			
GND	G4	Ground			
GND	G6	Ground			
GND	G8	Ground			
GND	G10	Ground			
GND	G12	Ground			
GND	G14	Ground			
GND	G16	Ground			
NC	A7	No Connection			
NC	A15	No Connection			
NC	B7	No Connection			
NC	B8	No Connection			
NC	B15	No Connection			
NC	C8	No Connection			
NC	C12	No Connection			

Signal	Pin	Description	I/O	PU/PD	Comment
NC	D7	No Connection			
NC	E7	No Connection			

P4 Connector Pin Assignment

	VPX6200 - P4 (Project 1 KX Sku by BOM option)						
	A	B	C	D	E	F	G
1	NB_PCH_PCIE13_RX_P	NB_PCH_PCIE13_RX_N	GND	NB_PCH_PCIE13_C_TX_P	NB_PCH_PCIE13_C_TX_N	GND	NB_EC_GPIO0
2	GND	NB_PCH_PCIE14_RX_P	NB_PCH_PCIE14_RX_N	GND	NB_PCH_PCIE14_C_TX_P	NB_PCH_PCIE14_C_TX_N	GND
3	NB_USB3_1_RXP	NB_USB3_1_RXN	GND	NB_USB3_1_TXP	NB_USB3_1_TXN	GND	NB_EC_GPIO1
4	GND	NB_PCIECLK4_100M_P	NB_PCIECLK4_100M_N	GND	NC	NB_EXT_NODE_RST-L	GND
5	NB_SPI_MISO	NB_SPI_CS2-L	GND	NB_SPI_MOSI	NB_SPI_CLK	GND	NB_EC_GPIO2
6	GND	PCIE_SW_Port1_RXP13_P4	PCIE_SW_Port1_RXN13_P4	GND	PCIE_SW_Port1_TXP14_P4	PCIE_SW_Port1_TXN14_P4	GND
7	NC	NC	GND	NC	NC	GND	NB_EC_GPIO3
8	GND	NC	NC	GND	NC	NB_PLTRST-L	GND
9	NB_USB3_2_RXP	NB_USB3_2_RXN	GND	NB_USB3_2_TXP	NB_USB3_2_TXN	GND	NB_EC_GPIO4
10	GND	NB_SATA_3_C_RXP	NB_SATA_3_C_RXN	GND	NB_SATA_3_C_TXP	NB_SATA_3_C_TXN	GND
11	NB_1GKX_RX_P3_P	NB_1GKX_RX_P3_N	GND	NB_1GKX_TX_P3_P	NB_1GKX_TX_P3_N	GND	NB_EC_GPIO5
12	GND	NA_1GKX_RX_P3_P	NA_1GKX_RX_P3_N	GND	NA_1GKX_TX_P3_P	NA_1GKX_TX_P3_N	GND
13	NB_1G_P1_MDI0P	NB_1G_P1_MDI0N	GND	NB_1G_P1_MDI1P	NB_1G_P1_MDI1N	GND	NB_EC_GPIO6
14	GND	NB_1G_P1_MDI2P	NB_1G_P1_MDI2N	GND	NB_1G_P1_MDI3P	NB_1G_P1_MDI3N	GND
15	NA_1G_P1_MDI0P	NA_1G_P1_MDI0N	GND	NA_1G_P1_MDI1P	NA_1G_P1_MDI1N	GND	NC
16	GND	NA_1G_P1_MDI2P	NA_1G_P1_MDI2N	GND	NA_1G_P1_MDI3P	NA_1G_P1_MDI3N	GND

	VPX6200 - P4 (Project 2 KR Sku by BOM option)						
	A	B	C	D	E	F	G
1	NB_PCH_PCIE13_RX_P	NB_PCH_PCIE13_RX_N	GND	NB_PCH_PCIE13_C_TX_P	NB_PCH_PCIE13_C_TX_N	GND	NB_EC_GPIO0
2	GND	NB_PCH_PCIE14_RX_P	NB_PCH_PCIE14_RX_N	GND	NB_PCH_PCIE14_C_TX_P	NB_PCH_PCIE14_C_TX_N	GND
3	NB_USB3_1_RXP	NB_USB3_1_RXN	GND	NB_USB3_1_TXP	NB_USB3_1_TXN	GND	NB_EC_GPIO1
4	GND	NB_PCIECLK4_100M_P	NB_PCIECLK4_100M_N	GND	PCIE_SW_Port1_TXP13	PCIE_SW_Port1_TXN13	GND
5	NB_SPI_MISO	NB_SPI_CS2-L	GND	NB_SPI_MOSI	NB_SPI_CLK	GND	NB_EC_GPIO2
6	GND	PCIE_SW_Port1_RXP13_P4	PCIE_SW_Port1_RXN13_P4	GND	PCIE_SW_Port1_TXP14_P4	PCIE_SW_Port1_TXN14_P4	GND
7	NC	NC	GND	NC	NC	GND	NB_EC_GPIO3
8	GND	NC	NC	GND	PCIE_SW_Port1_RXP14	PCIE_SW_Port1_RXN14	GND
9	NB_USB3_2_RXP	NB_USB3_2_RXN	GND	NB_USB3_2_TXP	NB_USB3_2_TXN	GND	NB_EC_GPIO4
10	GND	NB_SATA_3_C_RXP	NB_SATA_3_C_RXN	GND	NB_SATA_3_C_TXP	NB_SATA_3_C_TXN	GND
11	NB_1GKX_RX_P3_P	NB_1GKX_RX_P3_N	GND	NB_1GKX_TX_P3_P	NB_1GKX_TX_P3_N	GND	NB_EC_GPIO5
12	GND	NA_1GKX_RX_P3_P	NA_1GKX_RX_P3_N	GND	NA_1GKX_TX_P3_P	NA_1GKX_TX_P3_N	GND
13	NB_1G_P1_MDI0P	NB_1G_P1_MDI0N	GND	NB_1G_P1_MDI1P	NB_1G_P1_MDI1N	GND	NB_EXT_NODE_RST-L
14	GND	NB_1G_P1_MDI2P	NB_1G_P1_MDI2N	GND	NB_1G_P1_MDI3P	NB_1G_P1_MDI3N	GND
15	NA_1G_P1_MDI0P	NA_1G_P1_MDI0N	GND	NA_1G_P1_MDI1P	NA_1G_P1_MDI1N	GND	NB_PLTRST-L
16	GND	NA_1G_P1_MDI2P	NA_1G_P1_MDI2N	GND	NA_1G_P1_MDI3P	NA_1G_P1_MDI3N	GND

P4 Pinout Description

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_SW_PORT1_RXP13_P4	B6	PLX8750 PCI Express port1 channel 13, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT1_RXN13_P4	C6	PLX8750 PCI Express port1 channel 13, Receive Input negative differential pair	I PCIE		
PCIE_SW_P1_R_TXP13	E4	PLX8750 PCI Express port1 channel 13, Transmit Output positive differential pair	O PCIE		For KR SKU is AC coupled 220nF on VPX6200, KX4 SKU is not used
PCIE_SW_P1_R_TXN13	F4	PLX8750 PCI Express port1 channel 13, Transmit Output negative differential pair	O PCIE		For KR SKU is AC coupled 220nF on VPX6200, KX4 SKU is NB_EXT_NODE_RST-L
PCIE_SW_P1_R_RXP14	E8	PLX8750 PCI Express port1 channel 14, Receive Input positive differential pair	I PCIE		For KR SKU, KX4 SKU is not used
PCIE_SW_P1_R_RXN14	F8	PLX8750 PCI Express port1 channel 14, Receive Input negative differential pair	I PCIE		For KR SKU, KX4 SKU is NB_PLTRST-L
PCIE_SW_PORT1_TXP14_P4	E6	PLX8750 PCI Express port1 channel 14, Transmit Output positive differential pair	O PCIE		AC coupled 220nF on VPX6200
PCIE_SW_PORT1_TXN14_P4	F6	PLX8750 PCI Express port1 channel 14, Transmit Output negative differential pair	O PCIE		AC coupled 220nF on VPX6200
NA_1G_P1_MDI0N	B15	1000BASE-T Ethernet channel 1 signal 0 negative differential pair	I/O MDI		Control Plane, Node A, 10/100/1000BASE-T operation with external transformer
NA_1G_P1_MDI0P	A15	1000BASE-T Ethernet channel 1 signal 0 positive differential pair	I/O MDI		Control Plane, Node A, 10/100/1000BASE-T operation with external transformer
NA_1G_P1_MDI1N	E15	1000BASE-T Ethernet channel 1 signal 1 negative differential pair	I/O MDI		Control Plane, Node A, 10/100/1000BASE-T operation with external transformer
NA_1G_P1_MDI1P	D15	1000BASE-T Ethernet channel 1 signal 1 positive differential pair	I/O MDI		Control Plane, Node A, 10/100/1000BASE-T operation with external transformer
NA_1G_P1_MDI2N	C16	1000BASE-T Ethernet channel 1 signal 2 negative differential pair	I/O MDI		Control Plane, Node A, 10/100/1000BASE-T operation with external transformer

Signal	Pin	Description	I/O	PU/PD	Comment
NA_1G_P1_MDI2P	B16	1000BASE-T Ethernet channel 1 signal 2 positive differential pair	I/O MDI		Control Plane, Node A, 10/100/1000BASE-T operation with external transformer
NA_1G_P1_MDI3N	F16	1000BASE-T Ethernet channel 1 signal 3 negative differential pair	I/O MDI		Control Plane, Node A, 10/100/1000BASE-T operation with external transformer
NA_1G_P1_MDI3P	E16	1000BASE-T Ethernet channel 1 signal 3 positive differential pair	I/O MDI		Control Plane, Node A, 10/100/1000BASE-T operation with external transformer
NA_1GKX_RX_P3_N	C12	1000BASE-KX Ethernet channel 3 receive negative differential pairs	I KX		Node A, AC coupled 4.7nF on VPX6200
NA_1GKX_RX_P3_P	B12	1000BASE-KX Ethernet channel 3 receive positive differential pairs	I KX		Node A, AC coupled 4.7nF on VPX6200
NA_1GKX_TX_P3_N	F12	1000BASE-KX Ethernet channel 3 transmit negative differential pairs	O KX		Node A
NA_1GKX_TX_P3_P	E12	1000BASE-KX Ethernet channel 3 transmit positive differential pairs	O KX		Node A
NB_1G_P1_MDI0N	B13	1000BASE-T Ethernet channel 1 signal 0 negative differential pair	I/O MDI		Control Plane, Node B, 10/100/1000BASE-T operation with external transformer
NB_1G_P1_MDI0P	A13	1000BASE-T Ethernet channel 1 signal 0 positive differential pair	I/O MDI		Control Plane, Node B, 10/100/1000BASE-T operation with external transformer
NB_1G_P1_MDI1N	E13	1000BASE-T Ethernet channel 1 signal 1 negative differential pair	I/O MDI		Control Plane, Node B, 10/100/1000BASE-T operation with external transformer
NB_1G_P1_MDI1P	D13	1000BASE-T Ethernet channel 1 signal 1 positive differential pair	I/O MDI		Control Plane, Node B, 10/100/1000BASE-T operation with external transformer
NB_1G_P1_MDI2N	C14	1000BASE-T Ethernet channel 1 signal 2 negative differential pair	I/O MDI		Control Plane, Node B, 10/100/1000BASE-T operation with external transformer
NB_1G_P1_MDI2P	B14	1000BASE-T Ethernet channel 1 signal 2 positive differential pair	I/O MDI		Control Plane, Node B, 10/100/1000BASE-T operation with external transformer
NB_1G_P1_MDI3N	F14	1000BASE-T Ethernet channel 1 signal 3 negative differential pair	I/O MDI		Control Plane, Node B, 10/100/1000BASE-T operation with external transformer

Signal	Pin	Description	I/O	PU/PD	Comment
NB_1G_P1_MDI3P	E14	1000BASE-T Ethernet channel 1 signal 3 positive differential pair	I/O MDI		Control Plane, Node B, 10/100/1000BASE-T operation with external transformer
NB_1GKX_RX_P3_N	B11	1000BASE-KX Ethernet channel 3 receive negative differential pairs	I KX		Node B, AC coupled 4.7nF on VPX6200
NB_1GKX_RX_P3_P	A11	1000BASE-KX Ethernet channel 3 receive positive differential pairs	I KX		Node B, AC coupled 4.7nF on VPX6200
NB_1GKX_TX_P3_N	E11	1000BASE-KX Ethernet channel 3 transmit negative differential pairs	O KX		Node B
NB_1GKX_TX_P3_P	D11	1000BASE-KX Ethernet channel 3 transmit positive differential pairs	O KX		Node B
NB_PCH_PCIE13_RX_P	A1	PCH PCI Express port13 channel 13, Receive Input positive differential pair	I PCIE		Node B
NB_PCH_PCIE13_RX_N	B1	PCH PCI Express port13 channel 13, Receive Input negative differential pair	I PCIE		Node B
NB_PCH_PCIE14_RX_P	B2	PCH PCI Express port13 channel 14, Receive Input positive differential pair	I PCIE		Node B
NB_PCH_PCIE14_RX_N	C2	PCH PCI Express port13 channel 14, Receive Input negative differential pair	I PCIE		Node B
NB_PCH_PCIE13_C_TX_P	D1	PCH PCI Express port13 channel 13, Transmit Output positive differential pair	O PCIE		Node B, AC coupled 220nF on VPX6200
NB_PCH_PCIE13_C_TX_N	E1	PCH PCI Express port13 channel 13, Transmit Output negative differential pair	O PCIE		Node B, AC coupled 220nF on VPX6200
NB_PCH_PCIE14_C_TX_P	E2	PCH PCI Express port13 channel 14, Transmit Output positive differential pair	O PCIE		Node B, AC coupled 220nF on VPX6200
NB_PCH_PCIE14_C_TX_N	F2	PCH PCI Express port13 channel 14, Transmit Output negative differential pair	O PCIE		Node B, AC coupled 220nF on VPX6200
NB_PCIECLK4_100M_P	B4	PCI Express Reference Positive Clock output for all PCI Express Lanes	O PCIE		Source Node B
NB_PCIECLK4_100M_N	C4	PCI Express Reference Negative Clock output for all PCI Express Lanes	O PCIE		Source Node B
NB_SATA_3_C_RXP	B10	Serial ATA channel 3, Receive Input positive differential pair	I SATA		Node B, AC coupled 10nF on VPX6200
NB_SATA_3_C_RXN	C10	Serial ATA channel 3, Receive Input negative differential pair	I SATA		Node B, AC coupled 10nF on VPX6200

Signal	Pin	Description	I/O	PU/PD	Comment
NB_SATA_3_C_TXP	E10	Serial ATA channel 3, Transmit Output positive differential pair	O SATA		Node B, AC coupled 10nF on VPX6200
NB_SATA_3_C_TXN	F10	Serial ATA channel 3, Transmit Output negative differential pair	O SATA		Node B, AC coupled 10nF on VPX6200
NB_SPI_CLK	E5	Clock from module to carrier board SPI BIOS flash	O 3.3VA		Source Node B
NB_SPI_CS2-L	B5	Chip select for Carrier Board SPI BIOS Flash	O 3.3VA	PU 10k to P_+3V3_SPI_A	Source Node B
NB_SPI_MOSO	A5	Data in to module from carrier board SPI BIOS flash	I 3.3VA		Source Node B
NB_SPI_MOSI	D5	Data out from module to carrier board SPI BIOS flash	O 3.3VA		Source Node B
NB_USB3_1_RXP	A3	USB 3.2 Gen 1 Differential Receive channel 1, Receive Input positive differential pair	I USB		Node B, USB 1.1/ 2.0 / 3.2 Gen1 compliant
NB_USB3_1_RXN	B3	USB 3.2 Gen 1 Differential Receive channel 1, Receive Input negative differential pair	I USB		Node B, USB 1.1/ 2.0 / 3.2 Gen1 compliant
NB_USB3_1_TXP	D3	USB 3.2 Gen 1 Differential Receive channel 1, Transmit Output positive differential pair	O USB		Node B, USB 1.1/ 2.0 / 3.2 Gen1 compliant
NB_USB3_1_TXN	E3	USB 3.2 Gen 1 Differential Receive channel 1, Transmit Output negative differential pair	O USB		Node B, USB 1.1/ 2.0 / 3.2 Gen1 compliant
NB_USB3_2_RXP	A9	USB 3.2 Gen 1 Differential Receive channel 2, Receive Input positive differential pair	I USB		Node B, USB 1.1/ 2.0 / 3.2 Gen1 compliant
NB_USB3_2_RXN	B9	USB 3.2 Gen 1 Differential Receive channel 2, Receive Input negative differential pair	I USB		Node B, USB 1.1/ 2.0 / 3.2 Gen1 compliant
NB_USB3_2_TXP	D9	USB 3.2 Gen 1 Differential Receive channel 2, Transmit Output positive differential pair	O USB		Node B, USB 1.1/ 2.0 / 3.2 Gen1 compliant
NB_USB3_2_TXN	E9	USB 3.2 Gen 1 Differential Receive channel 2, Transmit Output negative differential pair	O USB		Node B, USB 1.1/ 2.0 / 3.2 Gen1 compliant
NB_PLTRST_R-L	G15	Node A PCH Platform Reset	O 3.3VA		Node B, For KR SKU, KX4 SKU is not used
NB_EC_GPIO0	G1	General Purpose Input/Output signal 0	I/O 3.3VA		Source Node B EC
NB_EC_GPIO1	G3	General Purpose Input/Output signal 1	I/O 3.3VA		Source Node B EC
NB_EC_GPIO2	G5	General Purpose Input/Output signal 2	I/O 3.3VA		Source Node B EC
NB_EC_GPIO3	G7	General Purpose Input/Output signal 3	I/O 3.3VA		Source Node B EC

Signal	Pin	Description	I/O	PU/PD	Comment
NB_EC_GPIO4	G9	General Purpose Input/Output signal 0	I/O 3.3VA		Source Node B EC
NB_EC_GPIO5	G11	General Purpose Input/Output signal 4	I/O 3.3VA		Source Node B EC
NB_EC_GPIO6_R	G13	General Purpose Input/Output signal 5	I/O 3.3VA		Source Node B EC, For KX4 SKU, KR SKU is NB_EXT_NODE_RST-L
GND	A10	Ground			
GND	A12	Ground			
GND	A14	Ground			
GND	A16	Ground			
GND	A2	Ground			
GND	A4	Ground			
GND	A6	Ground			
GND	A8	Ground			
GND	C1	Ground			
GND	C11	Ground			
GND	C13	Ground			
GND	C15	Ground			
GND	C3	Ground			
GND	C5	Ground			
GND	C7	Ground			
GND	C9	Ground			
GND	D10	Ground			
GND	D12	Ground			
GND	D14	Ground			
GND	D16	Ground			
GND	D2	Ground			
GND	D4	Ground			
GND	D6	Ground			
GND	D8	Ground			
GND	F1	Ground			
GND	F11	Ground			
GND	F13	Ground			
GND	F15	Ground			
GND	F3	Ground			
GND	F5	Ground			
GND	F7	Ground			

Signal	Pin	Description	I/O	PU/PD	Comment
GND	F9	Ground			
GND	G10	Ground			
GND	G12	Ground			
GND	G14	Ground			
GND	G16	Ground			
GND	G2	Ground			
GND	G4	Ground			
GND	G6	Ground			
GND	G8	Ground			
NC	A7	No Connection			
NC	B7	No Connection			
NC	B8	No Connection			
NC	C8	No Connection			
NC	D7	No Connection			
NC	E7	No Connection			

P5 Connector Pin Assignment

	A	B	C	D	E	F	G
1	NA_USB2P_1	NA_USB2N_1	GND	NA_USB2P_2	NA_USB2N_2	GND	P_+5V_NAUSBPWR1
2	GND	NA_USB2P_3	NA_USB2N_3	GND	NA_USB2P_4	NA_USB2N_4	GND
3	NA_COM1_RTS/TXP	NA_COM1_TXD/TXN	GND	NA_COM1_CTS/RXP	NA_COM1_RXD/RXN	GND	P_+5V_NAUSBPWR2
4	GND	NA_COM2_RTS/TXP	NA_COM2_TXD/TXN	GND	NA_COM2_CTS/RXP	NA_COM2_RXD/RXN	GND
5	NA_SATA_1_RXP_P5	NA_SATA_1_RXN_P5	GND	NA_SATA_1_TXP_P5	NA_SATA_1_TXN_P5	GND	P_+5V_NAUSBPWR3
6	GND	NA_SATA_2_RXP_P5	NA_SATA_2_RXN_P5	GND	NA_SATA_2_TXP_P5	NA_SATA_2_TXN_P5	GND
7	NA_1G_P2_MDI0P	NA_1G_P2_MDI0N	GND	NA_1G_P2_MDI1P	NA_1G_P2_MDI1N	GND	P_+5V_NAUSBPWR4
8	GND	NA_1G_P2_MDI2P	NA_1G_P2_MDI2N	GND	NA_1G_P2_MDI3P	NA_1G_P2_MDI3N	GND
9	PCIE_SW_Port1_RXP15_P5	PCIE_SW_Port1_RXN15_P5	GND	NA_BP_PWRBTN-L	NC	GND	NA_CN_HPD1
10	GND	NC	NC	GND	PCIE_SW_Port1_TXP15_P5	PCIE_SW_Port1_TXN15_P5	GND
11	NA_TMDS_DATA0_P	NA_TMDS_DATA0_N	GND	NA_TMDS_CLK_P	NA_TMDS_CLK_N	GND	NA_HDMI_SCL_P5
12	GND	NA_TMDS_DATA2_P	NA_TMDS_DATA2_N	GND	NA_TMDS_DATA1_P	NA_TMDS_DATA1_N	GND
13	IPMB_TDI	IPMB_TDO	GND	IPMB_TMS	IPMB_TCK	GND	NA_HDMI_SDA_P5
14	GND	IPMB_JTRST-L	NC	GND	NC	NC	GND
15	NC	NC	GND	NC	NC	GND	P_+5V_NAHDMI
16	GND	NA_1GKX_RX_P4_P	NA_1GKX_RX_P4_N	GND	NA_1GKX_TX_P4_P	NA_1GKX_TX_P4_N	GND

P5 Pinout Description

Signal	Pin	Description	I/O	PU/PD	Comment
P_+5V_NAHDMI	G15	HDMI power: +5V nominal	Power		Node A
P_+5V_NAUSBPWR1	G1	USB 3.2 port power for port1	Power		Node A
P_+5V_NAUSBPWR2	G3	USB 3.2 port power for port2	Power		Node A
P_+5V_NAUSBPWR3	G5	USB 3.2 port power for port3	Power		Node A
P_+5V_NAUSBPWR4	G7	USB 3.2 port power for port4	Power		Node A

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_SW_PORT1_RXP15_P5	A9	PLX8750 PCI Express port1 channel 15, Receive Input positive differential pair	I PCIE		
PCIE_SW_PORT1_RXN15_P5	B9	PLX8750 PCI Express port1 channel 15, Receive Input negative differential pair	I PCIE		
PCIE_SW_PORT1_TXP15_P5	E10	PLX8750 PCI Express port1 channel 15, Transmit Output positive differential pair	O PCIE		AC coupled 220nF on VPX6200
PCIE_SW_PORT1_TXN15_P5	F10	PLX8750 PCI Express port1 channel 15, Transmit Output negative differential pair	O PCIE		AC coupled 220nF on VPX6200
NA_1G_P2_MDI0N	B7	1000BASE-T Ethernet channel 2 signal 0 negative differential pair	I/O MDI		Node A, 10/100/ 1000BASE-T operation with external transformer
NA_1G_P2_MDI0P	A7	1000BASE-T Ethernet channel 2 signal 0 positive differential pair	I/O MDI		Node A, 10/100/ 1000BASE-T operation with external transformer
NA_1G_P2_MDI1N	E7	1000BASE-T Ethernet channel 2 signal 1 negative differential pair	I/O MDI		Node A, 10/100/ 1000BASE-T operation with external transformer
NA_1G_P2_MDI1P	D7	1000BASE-T Ethernet channel 2 signal 1 positive differential pair	I/O MDI		Node A, 10/100/ 1000BASE-T operation with external transformer
NA_1G_P2_MDI2N	C8	1000BASE-T Ethernet channel 2 signal 2 negative differential pair	I/O MDI		Node A, 10/100/ 1000BASE-T operation with external transformer
NA_1G_P2_MDI2P	B8	1000BASE-T Ethernet channel 2 signal 2 positive differential pair	I/O MDI		Node A, 10/100/ 1000BASE-T operation with external transformer
NA_1G_P2_MDI3N	F8	1000BASE-T Ethernet channel 2 signal 3 negative differential pair	I/O MDI		Node A, 10/100/ 1000BASE-T operation with external transformer
NA_1G_P2_MDI3P	E8	1000BASE-T Ethernet channel 2 signal 3 positive differential pair	I/O MDI		Node A, 10/100/ 1000BASE-T operation with external transformer
NA_1GKX_RX_P4_N	C16	1000BASE-KX Ethernet channel 4 receive negative differential pair	I KX		Node A, AC coupled 4.7nF on VPX6200
NA_1GKX_RX_P4_P	B16	1000BASE-KX Ethernet channel 4 receive positive differential pair	I KX		Node A, AC coupled 4.7nF on VPX6200
NA_1GKX_TX_P4_N	F16	1000BASE-KX Ethernet channel 4 transmit negative differential pair	O KX		Node A

Signal	Pin	Description	I/O	PU/PD	Comment
NA_1GKX_TX_P4_P	E16	1000BASE-KX Ethernet channel 4 transmit positive differential pair	O KX		Node A
NA_COM1_CTS/RXP	D3	Serial COM port 1 Clear to Send (RS-232 mode)/Receive Data positive signal (RS-422 mode)	I CMOS		Node A, Power rail tolerance ±3V to ±25V
NA_COM1_RTS/TXP	A3	Serial COM port 1 Request to Send (RS-232 mode)/Transmit Data positive signal (RS-422 mode)	O CMOS		Node A, Power rail tolerance ±3V to ±25V
NA_COM1_RXD/RXN	E3	Serial COM port 1 Receive Data (RS-232 mode)/Receive Data positive signal (RS-422 mode)	I CMOS		Node A, Power rail tolerance ±3V to ±25V
NA_COM1_TXD/TXN	B3	Serial COM port 1 Transmit Data (RS-232 mode)/Transmit Data negative signal (RS-422 mode)	O CMOS		Node A, Power rail tolerance ±3V to ±25V
NA_COM2_CTS/RXP	E4	Serial COM port 2 Clear to Send (RS-232 mode)/Receive Data positive signal (RS-422 mode)	I CMOS		Node A, Power rail tolerance ±3V to ±25V
NA_COM2_RTS/TXP	B4	Serial COM port 2 Request to Send (RS-232 mode)/Transmit Data positive signal (RS-422 mode)	O CMOS		Node A, Power rail tolerance ±3V to ±25V
NA_COM2_RXD/RXN	F4	Serial COM port 2 Receive Data (RS-232 mode)/Receive Data positive signal (RS-422 mode)	I CMOS		Node A, Power rail tolerance ±3V to ±25V
NA_COM2_TXD/TXN	C4	Serial COM port 2 Transmit Data (RS-232 mode)/Transmit Data negative signal (RS-422 mode)	O CMOS		Node A, Power rail tolerance ±3V to ±25V
NA_SATA_1_RXP_P5	A5	Serial ATA channel 1, Receive Input positive differential pair			Node A, AC coupled 10nF on VPX6200
NA_SATA_1_RXN_P5	B5	Serial ATA channel 1, Receive Input negative differential pair			Node A, AC coupled 10nF on VPX6200
NA_SATA_1_TXP_P5	D5	Serial ATA channel 1, Transmit Output positive differential pair			Node A, AC coupled 10nF on VPX6200
NA_SATA_1_TXN_P5	E5	Serial ATA channel 1, Transmit Output negative differential pair			Node A, AC coupled 10nF on VPX6200
NA_SATA_2_RXP_P5	B6	Serial ATA channel 2, Receive Input positive differential pair			Node A, AC coupled 10nF on VPX6200
NA_SATA_2_RXN_P5	C6	Serial ATA channel 2, Receive Input negative differential pair			Node A, AC coupled 10nF on VPX6200
NA_SATA_2_TXP_P5	E6	Serial ATA channel 2, Transmit Output positive differential pair			Node A, AC coupled 10nF on VPX6200
NA_SATA_2_TXN_P5	F6	Serial ATA channel 2, Transmit Output negative differential pair			Node A, AC coupled 10nF on VPX6200
NA_TMDS_DATA0_N	B11	TMDS Datal 0 negative differential pair			Node A
NA_TMDS_DATA0_P	A11	TMDS Datal 0 positive differential pair			Node A

Signal	Pin	Description	I/O	PU/PD	Comment
NA_TMDS_DATA1_N	F12	TMDS Datal 1 negative differential pair			Node A
NA_TMDS_DATA1_P	E12	TMDS Datal 1 positive differential pair			Node A
NA_TMDS_DATA2_N	C12	TMDS Datal 2 negative differential pair			Node A
NA_TMDS_DATA2_P	B12	TMDS Datal 2 positive differential pair			Node A
NA_TMDS_CLK_N	E11	TMDS clock negative differential pair			Node A
NA_TMDS_CLK_P	D11	TMDS clock positive differential pair			Node A
NA_HDMI_SCL_P5	G11	General purpose I²C port clock output/input of HDMI DDC			Node A
NA_HDMI_SDA_P5	G13	General purpose I²C port data I/O line of HDMI DDC			Node A
NA_CN_HPD1	G9	Hot plug detect of HDMI			Node A
NA_USB2P_1	A1	USB 2.0 differential positive data pairs for Port 1			Node A, USB 1.1/ 2.0 compliant
NA_USB2N_1	B1	USB 2.0 differential negative data pairs for Port 1			Node A, USB 1.1/ 2.0 compliant
NA_USB2P_2	D1	USB 2.0 differential positive data pairs for Port 2			Node A, USB 1.1/ 2.0 compliant
NA_USB2N_2	E1	USB 2.0 differential negative data pairs for Port 2			Node A, USB 1.1/ 2.0 compliant
NA_USB2P_3	B2	USB 2.0 differential positive data pairs for Port 3			Node A, USB 1.1/ 2.0 compliant
NA_USB2N_3	C2	USB 2.0 differential negative data pairs for Port 3			Node A, USB 1.1/ 2.0 compliant
NA_USB2P_4	E2	USB 2.0 differential positive data pairs for Port 4			Node A, USB 1.1/ 2.0 compliant
NA_USB2N_4	F2	USB 2.0 differential negative data pairs for Port 4			Node A, USB 1.1/ 2.0 compliant
IPMB_JTCK	E13	Test Clock signal of IPMC JTAG		PD 10k to GND	
IPMB_JTDI	A13	Test Data In signal of IPMC JTAG			
IPMB_JTDO	B13	Test Data Out signal of IPMC JTAG			
IPMB_JTMS	D13	Test Mode Select signal of IPMC JTAG			
IPMB_JTRST-L	B14	Target reset signal of IPMC JTAG		PD 10k to GND	
NA_BP_PWRBTN-L	D9	Power button to bring system out of S5 (soft off), active on falling edge		PU 4.7k to P_+3V3_AUX	
GND	A2	Ground			

Signal	Pin	Description	I/O	PU/PD	Comment
GND	A4	Ground			
GND	A6	Ground			
GND	A8	Ground			
GND	A10	Ground			
GND	A12	Ground			
GND	A14	Ground			
GND	A16	Ground			
GND	C1	Ground			
GND	C3	Ground			
GND	C5	Ground			
GND	C7	Ground			
GND	C9	Ground			
GND	C11	Ground			
GND	C13	Ground			
GND	C15	Ground			
GND	D2	Ground			
GND	D4	Ground			
GND	D6	Ground			
GND	D8	Ground			
GND	D10	Ground			
GND	D12	Ground			
GND	D14	Ground			
GND	D16	Ground			
GND	F1	Ground			
GND	F3	Ground			
GND	F5	Ground			
GND	F7	Ground			
GND	F9	Ground			
GND	F11	Ground			
GND	F13	Ground			
GND	F115	Ground			
GND	G2	Ground			
GND	G4	Ground			
GND	G6	Ground			
GND	G8	Ground			
GND	G10	Ground			
GND	G12	Ground			

Signal	Pin	Description	I/O	PU/PD	Comment
GND	G14	Ground			
GND	G16	Ground			
NC	A15	No connection			
NC	B10	No connection			
NC	B15	No connection			
NC	C10	No connection			
NC	C14	No connection			
NC	D15	No connection			
NC	E9	No connection			
NC	E14	No connection			
NC	E15	No connection			
NC	F14	No connection			

P6 Connector Pin Assignment

	A	B	C	D	E	F	G
1	NB_USB2P_1	NB_USB2N_1	GND	NB_USB2P_2	NB_USB2N_2	GND	P_+5V_NBUSB PWR1
2	GND	NB_USB2P_3	NB_USB2N_3	GND	NB_USB2P_4	NB_USB2N_4	GND
3	NB_COM1_RT S/TXP	NB_COM1_TX D/TXN	GND	NB_COM1_CT S/RXP	NB_COM1_RX D/RXN	GND	P_+5V_NBUSB PWR2
4	GND	NB_COM2_RT S/TXP	NB_COM2_TX D/TXN	GND	NB_COM2_CT S/RXP	NB_COM2_RX D/RXN	GND
5	NB_SATA_1_R XP_P6	NB_SATA_1_R XN_P6	GND	NB_SATA_1_T XP_P6	NB_SATA_1_T XN_P6	GND	P_+5V_NBUSB PWR3
6	GND	NB_SATA_2_R XP_P6	NB_SATA_2_R XN_P6	GND	NB_SATA_2_T XP_P6	NB_SATA_2_T XN_P6	GND
7	NB_1G_P2_M DI0P	NB_1G_P2_M DI0N	GND	NB_1G_P2_M DI1P	NB_1G_P2_M DI1N	GND	P_+5V_NBUSB PWR4
8	GND	NB_1G_P2_M DI2P	NB_1G_P2_M DI2N	GND	NB_1G_P2_M DI3P	NB_1G_P2_M DI3N	GND
9	NB_RTM_BOO T#	NC	GND	NB_BP_PWRB TN-L	NB_EC_GPIO7	GND	NB_CN_HPD1
10	GND	NC	NC	GND	NC	NC	GND
11	NB_TMDS_DA TA0_P	NB_TMDS_DA TA0_N	GND	NB_TMDS_CLK _P	NB_TMDS_CLK _N	GND	NB_HDMI_SCL _P6
12	GND	NB_TMDS_DA TA2_P	NB_TMDS_DA TA2_N	GND	NB_TMDS_DA TA1_P	NB_TMDS_DA TA1_N	GND
13	NC	NC	GND	NC	NC	GND	NB_HDMI_SD A_P6
14	GND	NC	NC	GND	NC	NC	GND
15	NC	NC	GND	NC	NC	GND	P_+5V_NBHD MI
16	GND	NB_1GKX_RX_ P4_P	NB_1GKX_RX_ P4_N	GND	NB_1GKX_TX_ P4_P	NB_1GKX_TX_ P4_N	GND

P6 Pinout Description

Signal	Pin	Description	I/O	PU/PD	Comment
P_+5V_NBHDMI	G15	HDMI power: +5V nominal	Power		Node B
P_+5V_NBUSBPW R1	G1	USB 3.2 port power for port1	Power		Node B
P_+5V_NBUSBPW R2	G3	USB 3.2 port power for port2	Power		Node B
P_+5V_NBUSBPW R13	G5	USB 3.2 port power for port3	Power		Node B
P_+5V_NBUSBPW R4	G7	USB 3.2 port power for port4	Power		Node B

Signal	Pin	Description	I/O	PU/PD	Comment
NB_1G_P2_MDI0N	B7	1000BASE-T Ethernet channel 2 signal 0 negative differential pair	I/O MDI		Node B, 10/100/ 1000BASE-T operation with external transformer
NB_1G_P2_MDI0P	A7	1000BASE-T Ethernet channel 2 signal 0 positive differential pair	I/O MDI		Node B, 10/100/ 1000BASE-T operation with external transformer
NB_1G_P2_MDI1N	E7	1000BASE-T Ethernet channel 2 signal 1 negative differential pair	I/O MDI		Node B, 10/100/ 1000BASE-T operation with external transformer
NB_1G_P2_MDI1P	D7	1000BASE-T Ethernet channel 2 signal 1 positive differential pair	I/O MDI		Node B, 10/100/ 1000BASE-T operation with external transformer
NB_1G_P2_MDI2N	C8	1000BASE-T Ethernet channel 2 signal 2 negative differential pair	I/O MDI		Node B, 10/100/ 1000BASE-T operation with external transformer
NB_1G_P2_MDI2P	B8	1000BASE-T Ethernet channel 2 signal 2 positive differential pair	I/O MDI		Node B, 10/100/ 1000BASE-T operation with external transformer
NB_1G_P2_MDI3N	F8	1000BASE-T Ethernet channel 2 signal 3 negative differential pair	I/O MDI		Node B, 10/100/ 1000BASE-T operation with external transformer
NB_1G_P2_MDI3P	E8	1000BASE-T Ethernet channel 2 signal 3 positive differential pair	I/O MDI		Node B, 10/100/ 1000BASE-T operation with external transformer
NB_1GKX_RX_P4_N	C16	1000BASE-KX Ethernet channel 4 receive negative differential pair	I KX		Node B, AC coupled 4.7nF on VPX6200
NB_1GKX_RX_P4_P	B16	1000BASE-KX Ethernet channel 4 receive positive differential pair	I KX		Node B, AC coupled 4.7nF on VPX6200
NB_1GKX_TX_P4_N	F16	1000BASE-KX Ethernet channel 4 transmit negative differential pair	O KX		Node B
NB_1GKX_TX_P4_P	E16	1000BASE-KX Ethernet channel 4 transmit positive differential pair	O KX		Node B
NB_COM1_CTS/ RXP	D3	Serial COM port 1 Clear to Send (RS-232 mode)/Receive Data positive signal (RS-422 mode)	I CMOS		Node B, Power rail tolerance ±3V to ±25V
NB_COM1_RTS/ TXP	A3	Serial COM port 1 Request to Send (RS-232 mode)/Transmit Data positive signal (RS-422 mode)	O CMOS		Node B, Power rail tolerance ±3V to ±25V
NB_COM1_RXD/ RXN	E3	Serial COM port 1 Receive Data (RS-232 mode)/Receive Data positive signal (RS-422 mode)	I CMOS		Node B, Power rail tolerance ±3V to ±25V

Signal	Pin	Description	I/O	PU/PD	Comment
NB_COM1_TXD/ TXN	B3	Serial COM port 1 Transmit Data (RS-232 mode)/Transmit Data negative signal (RS-422 mode)	O CMOS		Node B, Power rail tolerance ±3V to ±25V
NB_COM2_CTS/ RXP	E4	Serial COM port 2 Clear to Send (RS-232 mode)/Receive Data positive signal (RS-422 mode)	I CMOS		Node B, Power rail tolerance ±3V to ±25V
NB_COM2_RTS/ TXP	B4	Serial COM port 2 Request to Send (RS-232 mode)/Transmit Data positive signal (RS-422 mode)	O CMOS		Node B, Power rail tolerance ±3V to ±25V
NB_COM2_RXD/ RXN	F4	Serial COM port 2 Receive Data (RS-232 mode)/Receive Data positive signal (RS-422 mode)	I CMOS		Node B, Power rail tolerance ±3V to ±25V
NB_COM2_TXD/ TXN	C4	Serial COM port 2 Transmit Data (RS-232 mode)/Transmit Data negative signal (RS-422 mode)	O CMOS		Node B, Power rail tolerance ±3V to ±25V
NB_SATA_1_RXP_ P6	A5	Serial ATA channel 1, Receive Input positive differential pair	I SATA		Node B, AC coupled 10nF on VPX6200
NB_SATA_1_RXN_ P6	B5	Serial ATA channel 1, Receive Input negative differential pair	I SATA		Node B, AC coupled 10nF on VPX6200
NB_SATA_1_TXP_P 6	D5	Serial ATA channel 1, Transmit Output positive differential pair	O SATA		Node B, AC coupled 10nF on VPX6200
NB_SATA_1_TXN_ P6	E5	Serial ATA channel 1, Transmit Output negative differential pair	O SATA		Node B, AC coupled 10nF on VPX6200
NB_SATA_2_RXP_ P6	B6	Serial ATA channel 2, Receive Input positive differential pair	I SATA		Node B, AC coupled 10nF on VPX6200
NB_SATA_2_RXN_ P6	C6	Serial ATA channel 2, Receive Input negative differential pair	I SATA		Node B, AC coupled 10nF on VPX6200
NB_SATA_2_TXP_P 6	E6	Serial ATA channel 2, Transmit Output positive differential pair	O SATA		Node B, AC coupled 10nF on VPX6200
NB_SATA_2_TXN_ P6	F6	Serial ATA channel 2, Transmit Output negative differential pair	O SATA		Node B, AC coupled 10nF on VPX6200
NB_TMDS_DATA0_ N	B11	TMDS Datal 0 negative differential pair	I/O TMDS		Node B
NB_TMDS_DATA0_ P	A11	TMDS Datal 0 positive differential pair	I/O TMDS		Node B
NB_TMDS_DATA1_ N	F12	TMDS Datal 1 negative differential pair	I/O TMDS		Node B
NB_TMDS_DATA1_ P	E12	TMDS Datal 1 positive differential pair	I/O TMDS		Node B
NB_TMDS_DATA2_ N	C12	TMDS Datal 2 negative differential pair	I/O TMDS		Node B
NB_TMDS_DATA2_ P	B12	TMDS Datal 2 positive differential pair	I/O TMDS		Node B
NB_TMDS_CLK_N	E11	TMDS clock negative differential pair	I/O TMDS		Node B

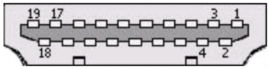
Signal	Pin	Description	I/O	PU/PD	Comment
NB_TMDS_CLK_P	D11	TMDS clock positive differential pair	I/O TMDS		Node B
NB_HDMI_SCL_P6	G11	General purpose I²C port clock output/input of HDMI DDC	I/O OD 5V	PU 2.2k o P_+5V	Node B
NB_HDMI_SDA_P6	G13	General purpose I²C port data I/O line of HDMI DDC	I/O OD 5V	PU 2.2k to P_+5V	Node B
NB_CN_HPD1	G9	Hot plug detect of HDMI	I CMOS 5V	Integrated PD 200k to GND	Node B
NB_USB2P_1	A1	USB 2.0 differential positive data pairs for Port 1	I/O USB		Node B, USB 1.1/ 2.0 compliant
NB_USB2N_1	B1	USB 2.0 differential negative data pairs for Port 1	I/O USB		Node B, USB 1.1/ 2.0 compliant
NB_USB2P_2	D1	USB 2.0 differential positive data pairs for Port 2	I/O USB		Node B, USB 1.1/ 2.0 compliant
NB_USB2N_2	E1	USB 2.0 differential negative data pairs for Port 2	I/O USB		Node B, USB 1.1/ 2.0 compliant
NB_USB2P_3	B2	USB 2.0 differential positive data pairs for Port 3	I/O USB		Node B, USB 1.1/ 2.0 compliant
NB_USB2N_3	C2	USB 2.0 differential negative data pairs for Port 3	I/O USB		Node B, USB 1.1/ 2.0 compliant
NB_USB2P_4	E2	USB 2.0 differential positive data pairs for Port 4	I/O USB		Node B, USB 1.1/ 2.0 compliant
NB_USB2N_4	F2	USB 2.0 differential negative data pairs for Port 4	I/O USB		Node B, USB 1.1/ 2.0 compliant
NB_BP_PWRBTN-L	D9	Power button to bring system out of S5 (soft off), active on falling edge.	I 3.3VA	PU 4.7k to P_+3V3_AUX	Node B
NB_RTM_BOOT#	A9	Reserved for boot from RTM BIOS	I 3.3VA	PU 100k to NB_P_+3V3_EC_A	Node B
NB_EC_GPIO7	E9	General Purpose Input/Output signal 0	I/O 3.3VA		Source Node B EC
GND	A2	Ground			
GND	A4	Ground			
GND	A6	Ground			
GND	A8	Ground			
GND	A10	Ground			
GND	A12	Ground			
GND	A14	Ground			
GND	A16	Ground			
GND	C1	Ground			
GND	C3	Ground			
GND	C5	Ground			

Signal	Pin	Description	I/O	PU/PD	Comment
GND	C7	Ground			
GND	C9	Ground			
GND	C11	Ground			
GND	C13	Ground			
GND	C15	Ground			
GND	D2	Ground			
GND	D4	Ground			
GND	D6	Ground			
GND	D8	Ground			
GND	D10	Ground			
GND	D12	Ground			
GND	D14	Ground			
GND	D16	Ground			
GND	F1	Ground			
GND	F3	Ground			
GND	F5	Ground			
GND	F7	Ground			
GND	F9	Ground			
GND	F11	Ground			
GND	F13	Ground			
GND	F115	Ground			
GND	G2	Ground			
GND	G4	Ground			
GND	G6	Ground			
GND	G8	Ground			
GND	G10	Ground			
GND	G12	Ground			
GND	G14	Ground			
GND	G16	Ground			
NC	A13	No connection			
NC	A15	No connection			
NC	B9	No connection			
NC	B10	No connection			
NC	B13	No connection			
NC	B14	No connection			
NC	B15	No connection			
NC	C10	No connection			

Signal	Pin	Description	I/O	PU/PD	Comment
NC	C14	No connection			
NC	D13	No connection			
NC	D15	No connection			
NC	E10	No connection			
NC	E13	No connection			
NC	E14	No connection			
NC	E15	No connection			
NC	F10	No connection			
NC	F14	No connection			

3.8 VPX6200-RL1 RTM Onboard Connector Pin Assignments

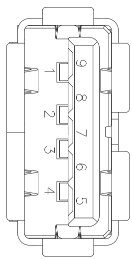
HDMI Connector



Pin #	Signal	Pin #	Signal
1	TMDS Data2+	2	TMDS Data2 Shield
3	TMDS Data2–	4	TMDS Data1+
5	TMDS Data1 Shield	6	TMDS Data1–
7	TMDS Data0+	8	TMDS Data0 Shield
9	TMDS Data0–	10	TMDS Clock+
11	TMDS Clock Shield	12	TMDS Clock–
13	CEC	14	Reserved
15	SCL	16	SDA
17	DDC/CEC Ground	18	+5 V Power
19	Hot Plug Detect		

USB 3.0 Connector

Pin #	Signal Name
1	+5V
2	Data-
3	Data+
4	GND
5	RX_N
6	RX_P
7	GND
8	TX_N
9	TX_P

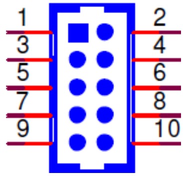


RJ-45 Gigabit Ethernet Connectors (CN9 and CN10)

Pin #	1000BASE-T
1	BI_DA+
2	BI_DA-
3	BI_DB+
4	BI_DC+
5	BI_DC-
6	BI_DB-
7	BI_DD+
8	BI_DD-

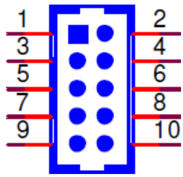
USB 2.0 Pin Header for Node A

Pin #	Signal Name	Pin #	Signal Name
1	P_+5V_NAUSBP WR3	2	P_+5V_NAUSBP WR4
3	NA_USB2_D3_N	4	NA_USB2_D4_N
5	NA_USB2_D3_P	6	NA_USB2_D4_P
7	GND	8	GND
9	GND	10	GND



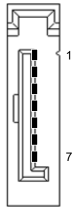
USB 2.0 Pin Header for Node B

Pin #	Signal Name	Pin #	Signal Name
1	P_+5V_NBUSBP WR3	2	P_+5V_NBUSBP WR4
3	NB_USB2_D3_N	4	NB_USB2_D4_N
5	NB_USB2_D3_P	6	NB_USB2_D4_P
7	GND	8	GND
9	GND	10	GND



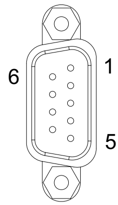
SATA 7-pin Connector

Pin #	Signal
1	GND
2	TXP
3	TXN
4	GND
5	RXN
6	RXP
7	GND



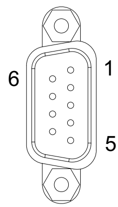
COM DB9 Connector for Node A

Pin	Signal	Pin	Signal
1	NA_COM1_PIN1	6	NA_COM1_PIN6
2	NA_COM1_RXD/RXN	7	NA_COM1_RTS/TXP
3	NA_COM1_TXD/TXN	8	NA_COM1_CTS/RXP
4	NA_COM1_PIN4	9	NA_COM1_PIN9
5	GND		



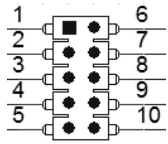
COM DB9 Connector for Node B

Pin	Signal	Pin	Signal
1	NB_COM1_PIN1	6	NB_COM1_PIN6
2	NB_COM1_RXD/RXN	7	NB_COM1_RTS/TXP
3	NB_COM1_TXD/TXN	8	NB_COM1_CTS/RXP
4	NB_COM1_PIN4	9	NB_COM1_PIN9
5	GND		



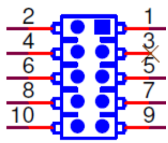
COM2 Pin Header for Node A & B

Pin	Signal	Pin	Signal
1	NA_COM2_RTS/TXP	6	NB_COM2_RTS/TXP
2	NA_COM2_TXD/TXN	7	NB_COM2_TXD/TXN
3	NA_COM2_RXD/RXN	8	NB_COM2_RXD/RXN
4	NA_COM2_CTS/RXP	9	NB_COM2_CTS/RXP
5	GND	10	COM1_CH_GND



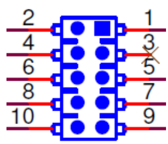
VPX IPMC JTAG Debug Port

Pin	Signal	Pin	Signal
1	GND	2	IPMB_JTCK
3	NC	4	IPMB_JTDO
5	P_+3V3_RTM	6	IPMB_JTMS
7	IPMB_JTRST-L	8	P_+3V3_RTM
9	GND	10	IPMB_JTDI



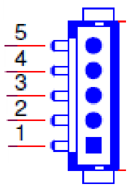
VPX PCIe Switch JTAG Debug Port

Pin	Signal	Pin	Signal
1	GND	2	PEX_TCK
3	NC	4	PEX_TDO
5	P_+3V3_RTM	6	PEX_TMS
7	PEX_TRST-L	8	P_+3V3_RTM
9	GND	10	PEX_TDI



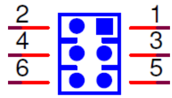
IPMB Connector

Pin	Signal
1	IPMB_SDA
2	GND
3	IPMB_SCL
4	P_+3V3_RTM
5	Pull High to P_+3V3_RTM



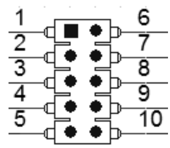
Debug 6-pin Connector

Pin	Signal	Pin	Signal
1	PEX_I2C_SCL0	2	IPMI_PRG_RX
3	GND	4	IPMI_PRG_TX
5	PEX_I2C_SDA0	6	GND



Debug 10-pin Connector

Pin	Signal	Pin	Signal
1	GND	6	S1_PWR_OK
2	NC	7	S1_PWR_EN
3	GND	8	S2_PWR_OK
4	S3_PWR_EN	9	S2_PWR_EN
5	GND	10	3_PWR_OK



M.2 2242 B-Key Connector for Node A & B

(Node A: NAM2_1; Node B: NBM2_1)

Pin	Signal Name	Pin	Signal Name
1	GND	2	P_+3V3
3	GND	4	P_+3V3
5	GND	6	N/C
7	N/C	8	N/C
9	N/C	10	N/C
11	GND		
		Key	
21	GND	20	N/C
23	N/C	22	N/C
25	N/C	24	N/C
27	GND	26	N/C
29	NA_PCH_PCIE14_RX_N	28	N/C
31	NA_PCH_PCIE14_RX_P	30	N/C
33	GND	32	N/C
35	NA_PCH_PCIE14_TX_N	34	N/C

Pin	Signal Name	Pin	Signal Name
37	NA_PCH_PCIE14_TX_P	36	N/C
39	GND	38	N/C
41	NA_PCH_PCIE13_RX_N	40	N/C
43	NA_PCH_PCIE13_RX_P	42	N/C
45	GND	44	N/C
47	NA_PCH_PCIE13_TX_N	46	N/C
49	NA_PCH_PCIE13_TX_P	48	N/C
51	GND	50	NA_PERST-L
53	N/C	52	N/C
55	N/C	54	N/C
57	GND	56	N/C
59	N/C	58	N/C
61	N/C	60	N/C
63	N/C	62	N/C
65	N/C	64	N/C
67	N/C	66	N/C
69	N/C	68	N/C
71	GND	70	P_+3V3_RTM
73	GND	72	P_+3V3_RTM
75	GND	74	P_+3V3_RTM

3.9 VPX6200-RL1 RTM VPX Connector Pin Assignments

RP0 Connector Pin Assignment

	VPX6200-RL1 - RP10 (Project 1 KX SKU by BOM option)						
	A	B	C	D	E	F	G
1	No Wafer						
2	P_+12V_PSU	P_+12V_PSU	P_+12V_PSU	NC	P_+12V_PSU	P_+12V_PSU	P_+12V_PSU
3	P_+5V_PSU	P_+5V_PSU	P_+5V_PSU	NC	P_+5V_PSU	P_+5V_PSU	P_+5V_PSU
4	NVMRO	SYSRESET#	GND	NC	GND	IPMBB_DAT	IPMBB_CLK
5	IPMBA_DAT	IPMBA_CLK	GND	P_+3V3_AUX	GND	GA4	GAP
6	GA0	GA1	GND	NC	GND	GA2	GA3
7	PEX_TRST-L	PEX_TMS	GND	PEX_TDI	PEX_TDO	GND	PEX_TCK
8	GND	NC	NC	GND	SBC_100M_REF_CLK_P	SBC_100M_REF_CLK_N	GND
9	NA_10G_RX0_L0_P	NA_10G_RX0_L0_N	GND	NA_10G_TX0_L0_P	NA_10G_TX0_L0_N	GND	GDISCRETE1-L
10	GND	NA_10G_RX0_L1_P	NA_10G_RX0_L1_N	GND	NA_10G_TX0_L1_P	NA_10G_TX0_L1_N	GND
11	NA_10G_RX0_L2_P	NA_10G_RX0_L2_N	GND	NA_10G_TX0_L2_P	NA_10G_TX0_L2_N	GND	P1_VBAT
12	GND	NA_10G_RX0_L3_P	NA_10G_RX0_L3_N	GND	NA_10G_TX0_L3_P	NA_10G_TX0_L3_N	GND
13	NB_10G_RX0_L0_P	NB_10G_RX0_L0_N	GND	NB_10G_TX0_L0_P	NB_10G_TX0_L0_N	GND	SYS_CON-L
14	GND	NB_10G_RX0_L1_P	NB_10G_RX0_L1_N	GND	NB_10G_TX0_L1_P	NB_10G_TX0_L1_N	GND
15	NB_10G_RX0_L2_P	NB_10G_RX0_L2_N	GND	NB_10G_TX0_L2_P	NB_10G_TX0_L2_N	GND	NC
16	GND	NB_10G_RX0_L3_P	NB_10G_RX0_L3_N	GND	NB_10G_TX0_L3_P	NB_10G_TX0_L3_N	GND
	VPX6200-RL1 - RP10 (Project 2 KR SKU by BOM option)						
	A	B	C	D	E	F	G
1	No Wafer						
2	P_+12V_PSU	P_+12V_PSU	P_+12V_PSU	NC	P_+12V_PSU	P_+12V_PSU	P_+12V_PSU
3	P_+5V_PSU	P_+5V_PSU	P_+5V_PSU	NC	P_+5V_PSU	P_+5V_PSU	P_+5V_PSU
4	NVMRO	SYSRESET#	GND	NC	GND	IPMBB_DAT	IPMBB_CLK
5	IPMBA_DAT	IPMBA_CLK	GND	P_+3V3_AUX	GND	GA4	GAP
6	GA0	GA1	GND	NC	GND	GA2	GA3
7	PEX_TRST-L	PEX_TMS	GND	PEX_TDI	PEX_TDO	GND	PEX_TCK
8	GND	NC	NC	GND	SBC_100M_REF_CLK_P	SBC_100M_REF_CLK_N	GND
9	NA_10G_RX0_L0_P	NA_10G_RX0_L0_N	GND	NA_10G_TX0_L0_P	NA_10G_TX0_L0_N	GND	GDISCRETE1-L
10	GND	NC	NC	GND	NC	NC	GND
11	NB_10G_RX0_L0_P	NB_10G_RX0_L0_N	GND	NB_10G_TX0_L0_P	NB_10G_TX0_L0_N	GND	P1_VBAT
12	GND	NC	NC	GND	NC	NC	GND
13	NC	NC	GND	NC	NC	GND	SYS_CON-L
14	GND	NC	NC	GND	NC	NC	GND
15	NC	NC	GND	NC	NC	GND	NC
16	GND	NC	NC	GND	NC	NC	GND

RP1 Connector Pin Assignment

	A	B	C	D	E	F	G
1	NA_10G_RX1_L0_P	NA_10G_RX1_L0_N	GND	NA_10G_TX1_L0_P	NA_10G_TX1_L0_N	GND	BP_PWRBTN-L
2	GND	NA_10G_RX1_L1_P	NA_10G_RX1_L1_N	GND	NA_10G_TX1_L1_P	NA_10G_TX1_L1_N	GND
3	NA_10G_RX1_L2_P	NA_10G_RX1_L2_N	GND	NA_10G_TX1_L2_P	NA_10G_TX1_L2_N	GND	S1_PWR_EN
4	GND	NA_10G_RX1_L3_P	NA_10G_RX1_L3_N	GND	NA_10G_TX1_L3_P	NA_10G_TX1_L3_N	GND
5	NB_10G_RX1_L0_P	NB_10G_RX1_L0_N	GND	NB_10G_TX1_L0_P	NB_10G_TX1_L0_N	GND	S1_PWR_OK
6	GND	NB_10G_RX1_L1_P	NB_10G_RX1_L1_N	GND	NB_10G_TX1_L1_P	NB_10G_TX1_L1_N	GND
7	NB_10G_RX1_L2_P	NB_10G_RX1_L2_N	GND	NB_10G_TX1_L2_P	NB_10G_TX1_L2_N	GND	MASK_RESET-L
8	GND	NB_10G_RX1_L3_P	NB_10G_RX1_L3_N	GND	NB_10G_TX1_L3_P	NB_10G_TX1_L3_N	GND
9	PCIE_SW_P4_RXP16	PCIE_SW_P4_RXN16	GND	PCIE_ SW_P4_TXP16	PCIE_SW_P4_TXN16	GND	S2_PWR_EN
10	GND	PCIE_SW_P4_RXP17	PCIE_SW_P4_RXN17	GND	PCIE_SW_P4_TXP17	PCIE_SW_P4_TXN17	GND
11	PCIE_SW_P4_RXP18	PCIE_SW_P4_RXN18	GND	PCIE_SW_P4_TXP18	PCIE_SW_P4_TXN18	GND	S2_PWR_OK
12	GND	PCIE_SW_P4_RXP19	PCIE_SW_P4_RXN19	GND	PCIE_SW_P4_TXP19	PCIE_SW_P4_TXN19	GND
13	PCIE_SW_P4_RXP20	PCIE_SW_P4_RXN20	GND	PCIE_SW_P4_TXP20	PCIE_SW_P4_TXN20	GND	PEX_I2C_SCL0
14	GND	PCIE_SW_P4_RXP21	PCIE_SW_P4_RXN21	GND	PCIE_SW_P4_TXP21	PCIE_SW_P4_TXN21	GND
15	PCIE_SW_P4_RXP22	PCIE_SW_P4_RXN22	GND	PCIE_SW_P4_TXP22	PCIE_SW_P4_TXN22	GND	PEX_I2C_SDA0
16	GND	PCIE_SW_P4_RXP23	PCIE_SW_P4_RXN23	GND	PCIE_SW_P4_TXP23	PCIE_SW_P4_TXN23	GND

RP2 Connector Pin Assignment

	A	B	C	D	E	F	G
1	PCIE_SW_P5_RXP24	PCIE_SW_P5_RXN24	GND	PCIE_SW_P5_TXP24	PCIE_SW_P5_TXN24	GND	IPMI_PRG_RX
2	GND	PCIE_SW_P5_RXP25	PCIE_SW_P5_RXN25	GND	PCIE_SW_P5_TXP25	PCIE_SW_P5_TXN25	GND
3	PCIE_SW_P5_RXP26	PCIE_SW_P5_RXN26	GND	PCIE_SW_P5_TXP26	PCIE_SW_P5_TXN26	GND	IPMI_PRG_TX
4	GND	PCIE_SW_P5_RXP27	PCIE_SW_P5_RXN27	GND	PCIE_SW_P5_TXP27	PCIE_SW_P5_TXN27	GND
5	PCIE_SW_P1_RXP8	PCIE_SW_P1_RXN8	GND	PCIE_SW_P1_TXP8	PCIE_SW_P1_TXN8	GND	S3_PWR_EN
6	GND	PCIE_SW_P1_RXP9	PCIE_SW_P1_RXN9	GND	PCIE_SW_P1_TXP9	PCIE_SW_P1_TXN9	GND
7	PCIE_SW_P1_RXP10	PCIE_SW_P1_RXN10	GND	PCIE_SW_P1_TXP10	PCIE_SW_P1_TXN10	GND	S3_PWR_OK
8	GND	PCIE_SW_P1_RXP11	PCIE_SW_P1_RXN11	GND	PCIE_SW_P1_TXP11	PCIE_SW_P1_TXN11	GND

RP3 Connector Pin Assignment

VPX6200-RL1 - RP13 (Project 1 KX SKU by BOM option)						
A	B	C	D	E	F	G
NA_PCH_PCIE13_RX_P	NA_PCH_PCIE13_RX_N	GND	NA_PCH_PCIE13_TX_P	NA_PCH_PCIE13_TX_N	GND	NA_EC_GPIO3
GND	NA_PCH_PCIE14_RX_P	NA_PCH_PCIE14_RX_N	GND	NA_PCH_PCIE14_TX_P	NA_PCH_PCIE14_TX_N	GND
NA_USB3_1_RXP	NA_USB3_1_RXN	GND	NA_USB3_1_TXP	NA_USB3_1_TXN	GND	NA_EC_GPIO1
GND	NA_PCIE_CLK_100M_P	NA_PCIE_CLK_100M_N	GND	NA_RTM_BOOT#	NA_EXT_NODE_RST#	GND
NA_SPI_MISO	NA_SPI_CS2-L	GND	NA_SPI_MOSI	NA_SPI_CLK	GND	NA_EC_GPIO2
GND	PCIE_SW_P5_RXP28	PCIE_SW_P5_RXN28	GND	PCIE_SW_P5_TXP28	PCIE_SW_P5_TXN28	GND
NC	NC	GND	NC	NC	GND	NC
GND	NC	NC	GND	NC	NA_PLTRST-L	GND
NA_USB3_2_RXP	NA_USB3_2_RXN	GND	NA_USB3_2_TXP	NA_USB3_2_TXN	GND	NA_EC_GPIO4
GND	NA_SATA_3_RXP	NA_SATA_3_RXN	GND	NA_SATA_3_TXP	NA_SATA_3_TXN	GND
PCIE_SW_P5_RXP29	PCIE_SW_P5_RXN29	GND	PCIE_SW_P5_TXP30	PCIE_SW_P5_TXN30	GND	NA_EC_GPIO5
GND	NA_EC_GPIO0	NC	GND	PCIE_SW_P5_RXP30	PCIE_SW_P5_RXN30	GND
PCIE_SW_P5_RXP31	PCIE_SW_P5_RXN31	GND	PCIE_SW_P5_TXP31	PCIE_SW_P5_TXN31	GND	NA_EC_GPIO6
GND	NA_BIOS_SEL1-L	NB_BIOS_SEL1-L	GND	PCIE_SW_P1_TXP12	PCIE_SW_P1_TXN12	GND
NC	NC	GND	PCIE_SW_P1_RXP12	PCIE_SW_P1_RXN12	GND	NA_EC_GPIO7
GND	P_+12V_PSU	P_+12V_PSU	GND	P_+5V_PSU	P_+5V_PSU	GND

VPX6200-RL1 - RP3 (Project 2 KR SKU by BOM option)						
A	B	C	D	E	F	G
NA_PCH_PCIE13_RX_P	NA_PCH_PCIE13_RX_N	GND	NA_PCH_PCIE13_TX_P	NA_PCH_PCIE13_TX_N	GND	NA_EC_GPIO3
GND	NA_PCH_PCIE14_RX_P	NA_PCH_PCIE14_RX_N	GND	NA_PCH_PCIE14_TX_P	NA_PCH_PCIE14_TX_N	GND
NA_USB3_1_RXP	NA_USB3_1_RXN	GND	NA_USB3_1_TXP	NA_USB3_1_TXN	GND	NA_EC_GPIO1
GND	NA_PCIE_CLK_100M_P	NA_PCIE_CLK_100M_N	GND	NA_RTM_BOOT#	NA_EXT_NODE_RST#	GND
NA_SPI_MISO	NA_SPI_CS2-L	GND	NA_SPI_MOSI	NA_SPI_CLK	GND	NA_EC_GPIO2
GND	PCIE_SW_P5_RXP28	PCIE_SW_P5_RXN28	GND	PCIE_SW_P5_TXP28	PCIE_SW_P5_TXN28	GND
NC	NC	GND	NC	NC	GND	NA_PLTRST-L
GND	NC	NC	GND	PCIE_SW_P5_TXP29	PCIE_SW_P5_TXN29	GND
NA_USB3_2_RXP	NA_USB3_2_RXN	GND	NA_USB3_2_TXP	NA_USB3_2_TXN	GND	NA_EC_GPIO4
GND	NA_SATA_3_RXP	NA_SATA_3_RXN	GND	NA_SATA_3_TXP	NA_SATA_3_TXN	GND
PCIE_SW_P5_RXP29	PCIE_SW_P5_RXN29	GND	PCIE_SW_P5_TXP30	PCIE_SW_P5_TXN30	GND	NA_EC_GPIO5
GND	NA_EC_GPIO0	NC	GND	PCIE_SW_P5_RXP30	PCIE_SW_P5_RXN30	GND
PCIE_SW_P5_RXP31	PCIE_SW_P5_RXN31	GND	PCIE_SW_P5_TXP31	PCIE_SW_P5_TXN31	GND	NA_EC_GPIO6
GND	NA_BIOS_SEL1-L	NB_BIOS_SEL1-L	GND	PCIE_SW_P1_TXP12	PCIE_SW_P1_TXN12	GND
NC	NC	GND	PCIE_SW_P1_RXP12	PCIE_SW_P1_RXN12	GND	NA_EC_GPIO7
GND	P_+12V_PSU	P_+12V_PSU	GND	P_+5V_PSU	P_+5V_PSU	GND

RP4 Connector Pin Assignment

	VPX6200-RL1 - RP14 (Project 1 KX SKU by BOM option)						
	A	B	C	D	E	F	G
1	NB_PCH_PCIE13_RX_P	NB_PCH_PCIE13_RX_N	GND	NB_PCH_PCIE13_TX_P	NB_PCH_PCIE13_TX_N	GND	NB_EC_GPIO0
2	GND	NB_PCH_PCIE14_RX_P	NB_PCH_PCIE14_RX_N	GND	NB_PCH_PCIE14_TX_P	NB_PCH_PCIE14_TX_N	GND
3	NB_USB3_1_RXP	NB_USB3_1_RXN	GND	NB_USB3_1_TXP	NB_USB3_1_TXN	GND	NB_EC_GPIO1
4	GND	NB_PCIE_CLK_100M_P	NB_PCIE_CLK_100M_N	GND	NC	NB_EXT_NODE_RST-L	GND
5	NB_SPI_MISO	NB_SPI_CS2-L	GND	NB_SPI_MOSI	NB_SPI_CLK	GND	NB_EC_GPIO2
6	GND	PCIE_SW_P1_RXP13	PCIE_SW_P1_RXN13	GND	PCIE_SW_P1_TXP14	PCIE_SW_P1_TXN14	GND
7	NC	NC	GND	NC	NC	GND	NB_EC_GPIO3
8	GND	NC	NC	GND	NC	NB_PLTRST-L	GND
9	NB_USB3_2_RXP	NB_USB3_2_RXN	GND	NB_USB3_2_TXP	NB_USB3_2_TXN	GND	NB_EC_GPIO4
10	GND	NB_SATA_3_RXP	NB_SATA_3_RXN	GND	NB_SATA_3_TXP	NB_SATA_3_TXN	GND
11	NB_1GKX_RX_P3_P	NB_1GKX_RX_P3_N	GND	NB_1GKX_TX_P3_P	NB_1GKX_TX_P3_N	GND	NB_EC_GPIO5
12	GND	NA_1GKX_RX_P3_P	NA_1GKX_RX_P3_N	GND	NA_1GKX_TX_P3_P	NA_1GKX_TX_P3_N	GND
13	NB_1G_P1_MDI0P	NB_1G_P1_MDI0N	GND	NB_1G_P1_MDI1P	NB_1G_P1_MDI1N	GND	NB_EC_GPIO6
14	GND	NB_1G_P1_MDI2P	NB_1G_P1_MDI2N	GND	NB_1G_P1_MDI3P	NB_1G_P1_MDI3N	GND
15	NA_1G_P1_MDI0P	NA_1G_P1_MDI0N	GND	NA_1G_P1_MDI1P	NA_1G_P1_MDI1N	GND	NC
16	GND	NA_1G_P1_MDI2P	NA_1G_P1_MDI2N	GND	NA_1G_P1_MDI3P	NA_1G_P1_MDI3N	GND

	VPX6200-RL1 - RP14 (Project 2 KR SKU by BOM option)						
	A	B	C	D	E	F	G
1	NB_PCH_PCIE13_RX_P	NB_PCH_PCIE13_RX_N	GND	NB_PCH_PCIE13_TX_P	NB_PCH_PCIE13_TX_N	GND	NB_EC_GPIO0
2	GND	NB_PCH_PCIE14_RX_P	NB_PCH_PCIE14_RX_N	GND	NB_PCH_PCIE14_TX_P	NB_PCH_PCIE14_TX_N	GND
3	NB_USB3_1_RXP	NB_USB3_1_RXN	GND	NB_USB3_1_TXP	NB_USB3_1_TXN	GND	NB_EC_GPIO1
4	GND	NB_PCIE_CLK_100M_P	NB_PCIE_CLK_100M_N	GND	PCIE_SW_P1_TXP13	PCIE_SW_P1_TXN13	GND
5	NB_SPI_MISO	NB_SPI_CS2-L	GND	NB_SPI_MOSI	NB_SPI_CLK	GND	NB_EC_GPIO2
6	GND	PCIE_SW_P1_RXP13	PCIE_SW_P1_RXN13	GND	PCIE_SW_P1_TXP14	PCIE_SW_P1_TXN14	GND
7	NC	NC	GND	NC	NC	GND	NB_EC_GPIO3
8	GND	NC	NC	GND	PCIE_SW_P1_RXP14	PCIE_SW_P1_RXN14	GND
9	NB_USB3_2_RXP	NB_USB3_2_RXN	GND	NB_USB3_2_TXP	NB_USB3_2_TXN	GND	NB_EC_GPIO4
10	GND	NB_SATA_3_RXP	NB_SATA_3_RXN	GND	NB_SATA_3_TXP	NB_SATA_3_TXN	GND
11	NB_1GKX_RX_P3_P	NB_1GKX_RX_P3_N	GND	NB_1GKX_TX_P3_P	NB_1GKX_TX_P3_N	GND	NB_EC_GPIO5
12	GND	NA_1GKX_RX_P3_P	NA_1GKX_RX_P3_N	GND	NA_1GKX_TX_P3_P	NA_1GKX_TX_P3_N	GND
13	NB_1G_P1_MDI0P	NB_1G_P1_MDI0N	GND	NB_1G_P1_MDI1P	NB_1G_P1_MDI1N	GND	NB_EXT_NODE_RST-L
14	GND	NB_1G_P1_MDI2P	NB_1G_P1_MDI2N	GND	NB_1G_P1_MDI3P	NB_1G_P1_MDI3N	GND
15	NA_1G_P1_MDI0P	NA_1G_P1_MDI0N	GND	NA_1G_P1_MDI1P	NA_1G_P1_MDI1N	GND	NB_PLTRST-L
16	GND	NA_1G_P1_MDI2P	NA_1G_P1_MDI2N	GND	NA_1G_P1_MDI3P	NA_1G_P1_MDI3N	GND

RP5 Connector Pin Assignment

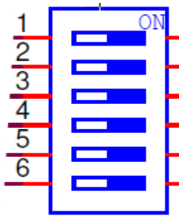
	A	B	C	D	E	F	G
1	NA_USB2P_1	NA_USB2N_1	GND	NA_USB2P_2	NA_USB2N_2	GND	P_+5V_NAUSBPWR1
2	GND	NA_USB2P_3	NA_USB2N_3	GND	NA_USB2P_4	NA_USB2N_4	GND
3	NA_COM1_RTS/TXP	NA_COM1_TXD/TXN	GND	NA_COM1_CTS/RXP	NA_COM1_RXD/RXN	GND	P_+5V_NAUSBPWR2
4	GND	NA_COM2_RTS/TXP	NA_COM2_TXD/TXN	GND	NA_COM2_CTS/RXP	NA_COM2_RXD/RXN	GND
5	NA_SATA_1_RXP	NA_SATA_1_RXN	GND	NA_SATA_1_TXP	NA_SATA_1_TXN	GND	P_+5V_NAUSBPWR3
6	GND	NA_SATA_2_RXP	NA_SATA_2_RXN	GND	NA_SATA_2_TXP	NA_SATA_2_TXN	GND
7	NA_1G_P2_MDI0	NA_1G_P2_MDI0	GND	NA_1G_P2_MDI1	NA_1G_P2_MDI1	GND	P_+5V_NAUSBPWR4
8	GND	NA_1G_P2_MDI2P	NA_1G_P2_MDI2N	GND	NA_1G_P2_MDI3	NA_1G_P2_MDI3N	GND
9	PCIE_SW_P1_RXP	PCIE_SW_P1_RXN	GND	NA_BP_PWRBTN-	NC	GND	NA_HDMI_HPD
10	GND	NC	NC	GND	PCIE_SW_P1_TXP	PCIE_SW_P1_TXN1	GND
11	NA_TMDS_DATA0_P_P5	NA_TMDS_DATA0_N_P5	GND	NA_TMDS_CLK_P_P5	NA_TMDS_CLK_N_P5	GND	NA_HDMI_SCL
12	GND	NA_TMDS_DATA2_P_P5	NA_TMDS_DATA2_N_P5	GND	NA_TMDS_DATA1_P_P5	NA_TMDS_DATA1_N_P5	GND
13	**IPMB_JTDI**	**IPMB_JTDO**	GND	**IPMB_JTMS**	**IPMB_JTCK**	GND	NA_HDMI_SDA
14	GND	**IPMB_JTRST-L**	NC	GND	NC	NC	GND
15	NC	NC	GND	NC	NC	GND	P_+5V_NAHDMI
16	GND	NA_1GKX_RX_P4	NA_1GKX_RX_P4_N	GND	NA_1GKX_TX_P4	NA_1GKX_TX_P4_N	GND

RP6 Connector Pin Assignment

	A	B	C	D	E	F	G
1	NB_USB2P_1	NB_USB2N_1	GND	NB_USB2P_2	NB_USB2N_2	GND	P_+5V_NBUSBPWR1
2	GND	NB_USB2P_3	NB_USB2N_3	GND	NB_USB2P_4	NB_USB2N_4	GND
3	NB_COM1_RTS/TXP	NB_COM1_TXD/TXN	GND	NB_COM1_CTS/RXP	NB_COM1_RXD/RXN	GND	P_+5V_NBUSBPWR2
4	GND	NB_COM2_RTS/TXP	NB_COM2_TXD/TXN	GND	NB_COM2_CTS/RXP	NB_COM2_RXD/RXN	GND
5	NB_SATA_1_RXP	NB_SATA_1_RXN	GND	NB_SATA_1_TXP	NB_SATA_1_TXN	GND	P_+5V_NBUSBPWR3
6	GND	NB_SATA_2_RXP	NB_SATA_2_RXN	GND	NB_SATA_2_TXP	NB_SATA_2_TXN	GND
7	NB_1G_P2_MDI0P	NB_1G_P2_MDI0N	GND	NB_1G_P2_MDI1P	NB_1G_P2_MDI1N	GND	P_+5V_NBUSBPWR4
8	GND	NB_1G_P2_MDI2P	NB_1G_P2_MDI2N	GND	NB_1G_P2_MDI3P	NB_1G_P2_MDI3N	GND
9	NB_RTM_BOOT#	NC	GND	NB_BP_PWRBTN-L	NB_EC_GPIO7	GND	NB_HDMI_HPD
10	GND	NC	NC	GND	NC	NC	GND
11	NB_TMDS_DATA0_P_P6	NB_TMDS_DATA0_N_P6	GND	NB_TMDS_CLK_P_P6	NB_TMDS_CLK_N_P6	GND	NB_HDMI_SCL_P6
12	GND	NB_TMDS_DATA2_P_P6	NB_TMDS_DATA2_N_P6	GND	NB_TMDS_DATA1_P_P6	NB_TMDS_DATA1_N_P6	GND
13	NC	NC	GND	NC	NC	GND	NB_HDMI_SDA_P6
14	GND	NC	NC	GND	NC	NC	GND
15	NC	NC	GND	NC	NC	GND	P_+5V_NBHDMI
16	GND	NB_1GKX_RX_P4_P	NB_1GKX_RX_P4_N	GND	NB_1GKX_TX_P4_P	NB_1GKX_TX_P4_N	GND

3.10 VPX6200-RL1 RTM Switches

Utility Signals Switch



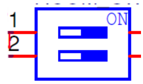
UT_SW1	GA Slot No.		
Pin	17	18	19
1	ON	OFF	ON
2	OFF	ON	ON
3	ON	ON	OFF

Pin	Direction	Mode
4	ON	NVMRO Write Enable
	OFF	NVMRO Write Protect
5	ON	System Controller
	OFF	Non System Controller
6	OFF	Reserved

RS232/RS422 Termination Switch

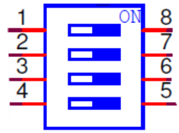
(Node A/B COM1/2)

Pin	Direction	Mode
1	ON	Add 120 ohm Termination Resistor
2		
1	OFF	No Termination Resistor
2		



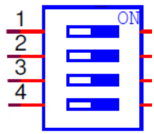
IPMB Source Selection Switch

Pin	Signal	Pin	Signal
1	IPMBA_CLK	8	IPMB_SCL
2	IPMBA_DAT	7	IPMB_SDA
3	IPMBB_CLK	6	IPMB_SCL
4	IPMBB_DAT	5	IPMB_SDA



BIOS Source Selection Switch

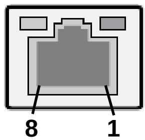
1 for Node A 3 for Node B	2 for Node A 4 for Node B	Mode
ON	ON	Main BIOS
ON	OFF	2nd BIOS
OFF	ON	RTM BIOS



3.11 VPX6200-RL2 Onboard Connectors

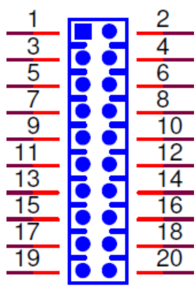
RJ-45 Gigabit Ethernet Connectors

Pin #	1000BASE-T
1	BI_DA+
2	BI_DA-
3	BI_DB+
4	BI_DC+
5	BI_DC-
6	BI_DB-
7	BI_DD+
8	BI_DD-



GPIO_CN1 Connector

Pin	Signal	Pin	Signal
1	NB_EC_GPIO7	2	NB_EC_GPIO6
3	NB_EC_GPIO5	4	NB_EC_GPIO4
5	NB_EC_GPIO3	6	NB_EC_GPIO2
7	NB_EC_GPIO1	8	NB_EC_GPIO0
9	GND	10	GND
11	NA_EC_GPIO7	12	NA_EC_GPIO6
13	NA_EC_GPIO5	14	NA_EC_GPIO4
15	NA_EC_GPIO3	16	NA_EC_GPIO2
17	NA_EC_GPIO1	18	NA_EC_GPIO0
19	GND	20	GND



4 Getting Started

This chapter describes the installation of the and VPX6200 blade and VPX6200-RL1 rear transition module.

4.1 Installing the VPX6200 to the Chassis

These instructions are for reference only. Refer to the user guide that comes with the chassis for more information.

1. Be sure to select the system slot to install the blade. The system power may be powered either on or off.
2. Align the module's top and bottom edges to the chassis card guides, and then carefully slide the module into the chassis. A slight resistance may be felt when inserting the module. If the resistance is too strong, check if there the wedge locks are tightened or if the board's connector pins are not properly aligned with connectors on the backplane. Then push the blade into the slot until it is completely flush with the chassis.
3. With the blade properly inserted, tighten the wedge locks to secure it to the chassis.

4.2 Installing the VPX6200-RL1 to the Chassis

The installation and removal procedures for a RTMs are the same as those for VPX blades. Because they are shorter than front boards, pay careful attention when inserting or removing RTMs.

Refer to previous sections for peripheral connectivity of all I/O ports on the RTM. When installing the VPX6200 and related RTMs, make sure the RTM is the correct matching model.

4.3 Driver Installation

The VPX6200 drivers are available from the ADLINK website (**www.adlinktech.com**). ADLINK provides validated chipset, graphics and LAN drivers for Windows 10.

Follow the steps below to install the drivers for Windows 10 64-bit.

1. Install the **Windows operating system** before installing any driver. Most standard I/O device drivers are installed during Windows installation.
2. Install the **chipset driver** by extracting and running the program in **01_Chipset-10.1.19199.8340-Public-MUP**
3. Install the **Graphics driver** by extracting and running the program in **02_Intel® Graphics Driver Production Version 101.4091 (PR12)**
4. Install the **CSME_TGL-H drivers** by extracting and running the program in **03_Intel CSME TGL-H 15.0.42.2268v3 B0 Corporate**
5. Install the **SerialIO drivers** by extracting and running the program in **04_SerialIO 30.100.2104.1 PV TGL PCH 20H2v2**
6. Install the **LAN Drivers** by extracting and running the program in **05_LAN-Driver-Release_27_6**
7. Install the **Trace_Hub driver** by extracting and running the program in **06_Intel(R)_Trace_Hub_10.0.19018.266**
8. Install the **PLX PCIe 8700 driver** by extracting and running the program in **07_PLX PCIe 8700 DMA Controller**

We recommend using the drivers provided on the ADLINK website to ensure compatibility. VxWorks BSPs can aldo be downloaded from the VPX6200 product page.

4.4 IPMC Firmware Update

Each IPMC firmware version can be used for multiple configurations. By default, the BIOS is set to fulfill 3x SBC and 1X SBC configurations. For 2x SBC configuration, please adjust the BIOS settings according to the BIOS manual.

Follow the steps below to update the IPMC firmware.

1. Connect RTM board and Motherboard to the backboard (ex. RTM board and Motherboard are connected to the 2nd slot of backboard in VPX6200). The Microsemi JTAG cable is connected to RTM board in VPX6200.
2. Launch **FlashPro** and click “New Project” to create a new project.
3. Click “Refresh/Rescan for Programmers” to check JTAG status (OK or failed).
4. Click “Browse…” and load IPMC_VPX6200_1_02.pdb file generated from Libero.
5. Click “PROGRAM” to start program and Click “Yes” to continue program.
6. After clicking “Yes”, **FlashPro** starts erasing.
7. Once erased, **FlashPro** proceeds to updating the firmware.

4.5 EC Firmware Update

The EC firmware can be updated either via UEFI or using an ITEDLB4-Board. See below for details.

Flashing EC Firmware using UEFI

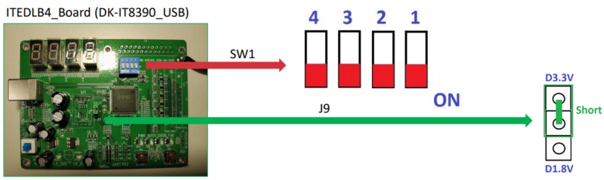
Follow the steps below to flash the EC firmware via UEFI.

1. Prepare a bootable USB flash drive by saving F.nsh, ifu.efi and VPX6200_ADLINK_XXX.bin into an empty USB drive using a flashing tool such as *Rufus*.
2. Insert the USB drive to the USB port of VPX6200.
3. Power on VPX6200.
4. Enter BIOS Setup Menu and check Secure Boot Control is set to “Disable”, if not, please change it and save changes.
5. In [Save & Exit] page, select [UEFI : Built-in EFI Shell] and press enter.
6. Enter UEFI mode and into USB flash by command fs0: (Maybe is fs1 that depending on VPX6200 detected.
7. Run F.nsh.
8. Once completed, the firmware has been successfully flashed.
9. Wait for the power cycle to complete to finish.
10. To check the version of the EC firmware, enter the BIOS menu and check the version shown next to SEMA Firmware Version.

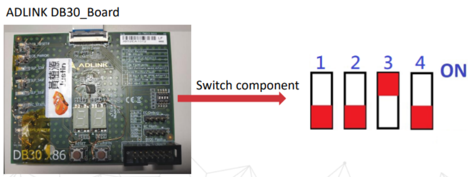
Flashing EC Firmware using ITEDLB4-Board

Follow the steps below to flash the EC firmware using ITEDLB4-Board.

1. Prepare the following:
   - ▷ an ITEDLB4 board
   - ▷ an ADLINK DB30 board
   - ▷ a USB A to B cable
   - ▷ a 30-pin x0.5_FFC cable
   - ▷ a 4-pin x2.54 cable
   - ▷ a host computer containing an "INI" folder and executable "ITEDLB4dll.dll" file
2. Configure the settings of the ITEDLB4 board as below.

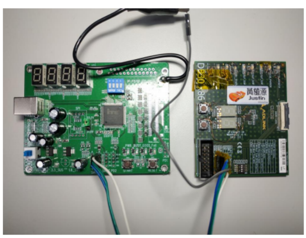


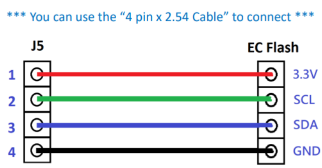
3. Configure the settings of the ADLINK DB30 board as below.



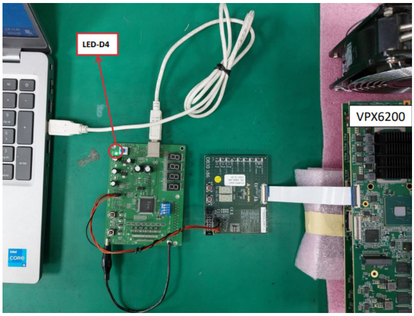
4. Connect the ITEDLB4 board and ADLINK DB30 board.

- ITEDLB4_Board (DK-IT8390_USB)
- ADLINK DB30_Board





5. Connect the ITEDLB4 board to a host PC, and connect the ADLINK DB30 board to the VPX6200 using an FFC cable.



6. Turn off the VPX6200, then press the DIP switch to power on the ITEDLB4 board. The host PC shall detect a “Download Board 4” device.
7. Execute “ITE_NewWinFlash.exe” as administrator.
8. Click Setup and enable “Dual-Flash”
9. If the EC in your project is not mounted with an external ROM, Please press the “Internal-Flash” button to target.
10. Press the “Load” button to load the EC-FW (ex.“XXXX.bin”).
11. Make sure theErase/Check/Program/Verify functions are allowed.
12. Press the green arrow icon to start flashing.
13. Once the flashing process is completed successfully, the information window is displayed in Blue. If failed, the information is displayed in red.
14. To check the version of the EC firmware, enter the BIOS menu and check the version shown next to SEMA Firmware Version.

5 Utilities

5.1 SEMA

Hardware monitoring and Watchdog Timer functionality are provided by ADLINK’s Smart Embedded Management Agent (SEMA), which operates via a Board Management Controller and communicates with the CPU through the SMBus. A graphical user interface program and command line interface are available to allow you to communicate with SEMA. Please refer to the SEMA user’s manual, available the SEMA GitHub page:
https://adlinktech.github.io/sema/index.html

5.2 Watchdog Timer

The VPX6200’s watchdog timer (WDT) is implemented by SEMA. For detailed information on how to program the WDT, refer to the SEMA user’s manual WDT section on the SEMA GitHub page:
https://adlinktech.github.io/sema/WatchDog.html#sysfs-In

This page intentionally left blank.

Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

A Lithium-type battery may be provided for uninterrupted, backup or emergency power.

WARNING:

Risk of explosion if battery is replaced with one of an incorrect type. Dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

Getting Service

Ask an Expert: https://www.adlinktech.com/en/Askanexpert.aspx

ADLINK Technology, Inc.
No. 66, Huaya 1st Rd., Guishan Dist.,
Taoyuan City 333411, Taiwan
Tel: +886-3-216-5088
Fax: +886-3-328-5706
Email: service@adlinktech.com

Ampro ADLINK Technology, Inc.
6450 Via Del Oro
San Jose, CA 95119-1208, USA
Tel: +1-408-360-0200
Toll Free: +1-800-966-5200 (USA only)
Fax: +1-408-600-1189
Email: info@adlinktech.com

ADLINK Technology (China) Co., Ltd.
300 Fang Chun Rd., Zhangjiang Hi-Tech Park
Pudong New Area, Shanghai, 201203 China
Tel: +86-21-5132-8988
Fax: +86-21-5132-3588
Email: market@adlinktech.com

ADLINK Technology GmbH
Hans-Thoma-Strasse 11
D-68163 Mannheim, Germany
Tel: +49-621-43214-0
Fax: +49-621 43214-30
Email: emea@adlinktech.com

Please visit the Contact page at **www.adlinktech.com** for information on how to contact the ADLINK regional office nearest you.